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A Silicon Photomultiplier Readout ASIC for the Mu3e Experiment

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Abstract

The Mu3e experiment is a proposed experiment to probe for new physics by searching for the charged lepton-flavour violating decay $\mu^+ \rightarrow e^+e^+e^-$ with a branching ratio sensitivity of 10^{-16}, improving the current limit by four orders of magnitude. To search for such rare events, extremely high muon decay rate, good background suppression and high detector efficiencies are required. This demands an excellent momentum, vertex and timing resolution from the detector systems. Furthermore, the experiment will be running at a muon stopping rate of more than 10^9 Hz in order to observe enough muon decays in a reasonable experiment running time. This poses another challenge to the detectors and readout electronics, which have to be designed to cope with the present event rate.
This thesis presents the development of a dedicated Silicon Photomultiplier (SiPM) readout Application-Specific Integrated Circuit (ASIC) for the Mu3e timing detectors. It provides the precise timing measurement while being capable of working with the high event rates. Fully differential analog front-end channel and 50 ps time binning TDC are utilized to achieve excellent timing resolution. The customized Low-Voltage Differential Signaling (LVDS) transmitter cell and double data rate serializer provides gigabit data rate to transfer data out of the chip. Detailed measurements have been preformed to characterize the timing performance and to verify the digital functionalities of the chip.

Zusammenfassung

Das Mu3E Experiment wurde vorgeschlagen um durch die Untersuchung des lepton-flavour verletzenden Zerfalls $\mu^+ \rightarrow e^+e^+e^-$ die Suche nach neuer Physik jenseits des Standardmodells weiter voranzutreiben. Um die bestehende Messung des Verzweigungsverhältnisses um vier Größenordnungen auf eine Empfindlichkeit von 10^{-16} zu verbessern, werden extrem hohe Myon-Zerfallsraten sowie exzellente Detektionseffizienzen und Unterdrückung des Untergrunds benötigt. Dies stellt hohe Anforderungen an die Impuls-, Vertex-, und Zeitauflösung des Detektors. Die für eine akzeptable Messzeit benötigte Zerfallsrate von 10^9 Hz stellt weitere Anforderungen an die Detektoren und deren Ausleseelektronik.
Diese Arbeit beschreibt die Entwicklung eines spezialisierten vollintegrierten Auslesechips für die Zeitmessung mit Silizium-Photomultipliern, der in beiden für diese Aufgabe vorgesehenen Detektoren in Mu3e zur Anwendung kommen wird. Eine voll-differenziell ausgelegte analoge Eingangsstufe ermöglicht auch bei hohen Ereignisraten eine exzellente Zeitauflösung. Die Zeitstempel werden von einem TDC mit einer Binbreite von 50 ps digitalisiert. Zur weiteren Verarbeitung der digitalen Daten wurden LVDS-Sender und -Empfängermodule entwickelt, die Mithilfe eines DDR-Serialisierungsblocks im Digitalteil des chips das Senden der Daten mit der notwendigen Rate von 1.25 Gbps ermöglichen. Detaillierte Messungen wurden durchgeführt, um die erreichbare Zeitauflösung und die digitalen Funktionen des chips zu verifizieren.

Contents

Chapter 1

Introduction

What makes up the universe? This is an ultimate question that physics as a scientific discipline is trying to answer. Particle physics answers this question in the way that the universe is made up by families of elementary building blocks, the particles. The Standard Model (SM) of elementary particle physics have been developed to describe the properties of the particle and their interaction. Amazingly, the Standard Model is able to describe the universe in most aspects and with a remarkable precision. With the discovery of Higgs boson at the Large Hadron Collider (LHC) in 2012 [1, 2], the last missing "building block" of the Standard Model has been found.

Although the Standard Model has been tested with great success in different scales and various circumstance, there are several theoretical arguments and experimental observation which strongly suggest that the Standard Model is not a complete model. For instance, lepton flavour is a conserved quantity in Standard Model. However, lepton flavour violation has been observed in neutrino oscillation experiment [3–5]. This also implies that the neutrinos have mass, which were long believed to be massless in the Standard Model. Another example is that only about 5 % of the energy in the universe can be explained by the matter described in Standard Model and the reset is believe to be dark matter (~25 %) and dark energy (~69 %), for which the Standard Model doesn't provide a good candidate particle. Furthermore, the Standard Model can not explain the matter-antimatter asymmetry observed in the universe. Thus, searching for new physics beyond the Standard Model has become the driving force in particle physics.

The Mu3e experiment [6] is a novel experiment to probe for new physics beyond the Standard Model by searching for the Charged Lepton Flavour Violating (cLFV) decay of $\mu^+ \longrightarrow e^+e^+e^-$ in an unprecedented sensitivity of 10^{-16}, which is a extremely suppressed process in the Standard Model with a branching ratio of $\mathcal{B}$ <10^{-54}. The main challenge for the Mu3e experiment is to run the experiment in a high muon decay rate of 10^8-10^9 Hz, to construct a detector system with high geometry acceptance and high efficiency, and to suppress the background below the signal level.

Good vertex, momentum and timing resolutions are required to separate decays from other processes showing a similar signature as a $\mu^+ \longrightarrow e^+e^+e^-$ signal, and thus for a successful experiment. The precise timing measurements are provided by the timing detectors, the fibre detector and the tile detector, in the Mu3e experiment. The timing information allows to further disentan-

gle uncorrelated decay products in order to reduce the accidental background which scales with the muon decay rate [7]. Both the fibre detector and the tile detector utilize the Silicon Photomultiplier (SiPM) as photon detector for its advantages of insensibility to the magnet, compactness, relative high Photon Detection Efficiency (PDE) and good timing performance.

In order to read out more than 9000 SiPM channels in an extremely dense experimental volume, Application Specific Integrated Circuits (ASICs) will be used for both timing detectors. The ASIC should exploit the timing potential of the detector system to achieve the required timing resolution, and to sustain the data rate in the fibre detector at the same time.

In this context the ASIC *Muon Timing Resolver with Gigabit link* (MuTRiG) has been designed and developed in Kirchhoff-Institute of Physics at Heidelberg University. The MuTRiG is a mixed mode ASIC consisting of 32 analog front-end channels, integrated TDCs and on-chip digital logic circuits. The low-jitter, fully-differential analog front-end circuit amplifies and discriminates the SiPM signals by leading edge discrimination method. The 50 ps timing binning TDC generates digital time stamps of the signals from the analog front-end for the time of arrival information and the time-of-flight information of the SiPM signals. The on-chip digital logic circuit generates the hit event data from the digitized time stamps. The digital logic circuit also buffers the hit event data and transfers the data in frames over a Gigabit serial data link to external Data Acquisition system (DAQ). In this thesis, the design, implementation and characterization of the MuTRiG chip will be presented.

Structure of the Thesis

This thesis is organized in seven chapters. It starts with the motivation for the development of the MuTRiG ASIC, which is presented in this chapter. In Chapter 2, the theoretical background and the setup of the Mu3e experiment will be introduced. An overview on working principle and and basic properties of the photon sensor used in the timing detectors of the Mu3e experiment, the SiPMs, will be presented in Chapter 3. An brief introduction to the basic building blocks of the analog circuits and digital circuits will be presented in Chapter 4. Chapter 5 will describe the design of the ASIC developed in this work, the MuTRiG ASIC. The characterization results of the MuTRiG ASIC will be presented in Chapter 6. And Chapter 7 will summarize this thesis.

Contributions from the Author

The development of an integrated circuit is a complex procedure which is usually a collaborative efforts from a group of people over a period of several years.

The development of the MuTRiG is based on the development of its predecessor, the STiCv3 chip [8–12]. The analog front-end channel utilized in the MuTRiG chip was developed and implemented in the STiCv3 chip. The author has participated in the development of the analog front-end by contributing the layout of several key building blocks, as well as by performing the

post-layout verification and the necessary modification to the analog front-end channel. The characterization of the analog front-end channel in the STiCv2 and STiCV3 ASIC was also carried out by the author. The integrated TDC module was developed by the designers at ZITI Heidelberg [13–15].

The development of the digital part of the MuTRiG chip was carried out by the author. The author has written most of the modules in the digital part and has adapted a few exiting modules developed by other members of the group into the digital part of the MuTRiG ASIC. Each module in the digital part, as well as the whole digital circuit were simulated and verified by the author before physical implementation of the chip. The author has also designed a Low Voltage Differential Signaling (LVDS) transmitter required to realize the gigabit serial data link. The schematic design, layout and simulation of the LVDS cell were all performed by the author. The author has also carried out the physical implementation of the MuTRiG chip.

The development of the the Printed Circuit Boards (PCBs) for the characterization of the ASIC was shared by the electronics department of KIP and the author. The author has developed the DAQ firmware and software for the MuTRiG ASIC based on a long-developing firmware and software framework in the group, to which the author has also been contributing. All the characterization measurements of the LVDS cell and the MuTRiG ASIC in the lab are performed by the author.

The construction of the MuTRiG setup for the test beam was shared by the members of the detector development group and the author. The measurement during the test beam is conducted by other members of the group.

The development of the MuTRiG chip leading to this thesis has been presented in several international conferences [16–19] and published in two proceeding papers [20, 21].

Chapter 2

The Mu3e Experiment

2.1 Theoretical Background

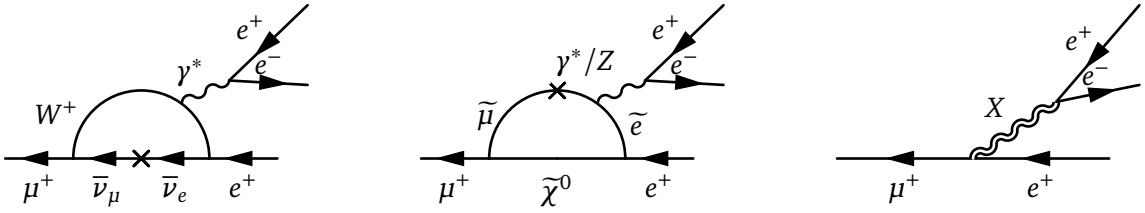
2.1.1 Lepton Flavour Violation

In the Standard Model, each lepton carries a quantum number called the lepton flavour L_e, L_μ and L_τ, where the e, μ, τ refer to the lepton generation. The lepton flavour is 1 and -1 for the corresponding lepton and its anti particle, and is 0 for other lepton generations (as shown in Table 2.1).

Table 2.1: Summary of the lepton flavour for the three lepton generation.

particle	L_e	L_μ	L_τ	particle	L_e	L_μ	L_τ	particle	L_e	L_μ	L_τ
e^-	1	0	0	μ^-	0	1	0	τ^-	0	0	1
ν_e	1	0	0	ν_μ	0	1	0	ν_τ	0	0	1
e^+	-1	0	0	μ^+	0	-1	0	τ^+	0	0	-1
$\overline{\nu}_e$	-1	0	0	$\overline{\nu}_\mu$	0	-1	0	$\overline{\nu}_\tau$	0	0	-1

The lepton flavour is a conserved quantity in the Standard Model of particle physics. However, lepton flavour violation (LFV) in the neutrino sector have been observed by several experiments such as the Super-Kamiokande [3], SNO [4] and KamLAND [5] in the form of neutrino mixing, which implies that neutrinos have non-zero mass. Consequently, lepton flavour is a broken symmetry and the Standard Model has to be extended to incorporate with massive neutrinos. The lepton flavour violation is also expected in the charged lepton sector, which will lead to $\mu \longrightarrow e$ and $\tau \longrightarrow \mu$ transitions without neutrinos in the final state. But charged lepton flavour violation (cLFV) haven't been observed even though the mixing angles in the neutrino matrix have been measured to be large. The reason is that cLFV reactions are forbidden at tree level in the extended Standard Model and can only be induced by lepton mixing through higher order processes described by loop or box diagram (see Figure 2.1a as an example). An example branching ratio in



(a) Standard Model **(b)** BSM penguin **(c)** BSM tree level

Figure 2.1: Fyenman diagram for the lepton violation decay $\mu \longrightarrow eee$. **(a)** The $\mu \longrightarrow eee$ decay via neutrino mixing in the Standard Model. **(b)** The $\mu \longrightarrow eee$ decay via penguin loop diagram involving new heavy particles in the super-symmetric models. **(c)** The $\mu \longrightarrow eee$ decay at tree level involving new particles in the models beyond Standard Model.

the $\mu \longrightarrow e\gamma$ channel is [22]

$$\mathcal{B}(\mu \longrightarrow e\gamma) = \frac{3\alpha}{32\pi} \left| \sum_{i=2,3} U^*_{\mu i} U_{ei} \frac{\Delta m^2_{i1}}{m^2_W} \right|^2 \tag{2.1}$$

where α is the fine structure constant, U_{li} are the elements of the neutrino mixing matrix, the Δm^2_{ij} are the neutrino mass-squared differences and m_W is the mass of W-boson. Due to the huge mass difference between the neutrinos and the W boson (m_ν<2 eV and m_W>80 MeV), such cFLV processes are extremely suppressed to a branching ratio of $\mathcal{B}(\mu \longrightarrow e\gamma)$<$10^{-54}$. If new heavy particles beyond the Standard Model are introduced, the situation changes completely. The cLFV effects are greatly enhanced and experimentally accessible in many extension of the Standard Model, such as grand unified model [23–25], left-right symmetric models [26–28], super-symmetric models [29] (see Figure 2.1b) and models with an extended Higgs sector [30]. Thus, the charge lepton flavour violation would be an ideal probe to search for the new physics beyond the Standard Model, possibly at energy scales far beyond the reach of the direct searches, such as the large hadron collider (LHC).

The cLFV muon decays have been investigation by several experiments, most prominent ones are the search for the radiative muon decay $\mu \longrightarrow e\gamma$ [31–34], the $\mu \longrightarrow eee$ decay [35] and the $\mu - e$ conversion in muonic atoms [36]. Table 2.2 lists the experimental upper limits for the lepton violating muon decays. The Mu3e experiment is aiming at searching for the LFV decay $\mu \longrightarrow eee$ with an unprecedented sensitivity of <10^{-16} and would provide an unique opportunity to explore physics beyond the Standard Model.

Table 2.2: Experimental upper limits on the LFV muon decays.

Decay Channel	Experiment	Branching Ratio Limit	Ref.
$\mu \longrightarrow e\gamma$	*MEGA*	$<1.2 \cdot 10^{-11}$	[31]
	MEG	$<5.7 \cdot 10^{-13}$	[33]
$\mu \longrightarrow eee$	*SINDRUM*	$<1.0 \cdot 10^{-12}$	[35]
$\mu Au \longrightarrow e Au$	*MEGA*	$<7.0 \cdot 10^{-13}$	[36]

2.1.2 The $\mu \longrightarrow eee$ Decay

The dominant muon decay mode is the lepton flavour conserving Michel decay $\mu^- \longrightarrow e^-\nu_\mu\overline{\nu}_e$, which has a branching ratio of $\mathcal{B}\approx$100 %. Other major decay modes are the radioactive decay $\mu^- \longrightarrow e^-\nu_\mu\overline{\nu}_e\gamma$ with a branching ratio of $\mathcal{B} = 6 \cdot 10^{-8}$ and the radioactive decay with internal conversion decay $\mu^- \longrightarrow e^-\nu_\mu\overline{\nu}_e e^+e^-$ with a branching ratio of $\mathcal{B} = 3.4 \cdot 10^{-5}$ [37].

The decay of $\mu^+ \longrightarrow e^+e^-e^+$ is charged lepton flavour violating decay. In the Standard Model, as discussed above, such decay is forbidden in the tree level and can only be occur via neutrino mixing through high order loop diagrams. However, the dominant neutrino mixing loop diagram (see Figure 2.1a) is strongly suppressed ($\mathcal{B}\ll10^{-50}$) in the Standard Model but has potentially high sensitivity in models beyond the Standard Model. Depending on the model, the $\mu^+ \longrightarrow e^+e^-e^+$ decay can be mediated via loop (Figure 2.1b) and box diagram or tree diagram (Figure 2.1c) by introducing new particles. The most general Lagrangian for this decay can be parameterized as [38]:

$$\begin{aligned} L_{\mu\to eee} = -\frac{4G_F}{\sqrt{2}} \cdot \Big[& m_\mu A_R \overline{\mu_R}\sigma^{\mu\nu} e_L F_{\mu\nu} \\ & + m_\mu A_L \overline{\mu_L}\sigma^{\mu\nu} e_L F_{\mu\nu} \\ & + g_1 (\overline{\mu_R} e_L)(\overline{e_R} e_L) \\ & + g_2 (\overline{\mu_L} e_R)(\overline{e_L} e_R) \\ & + g_3 (\overline{\mu_R}\gamma^\mu e_R)(\overline{e_R}\gamma_\mu e_R) \\ & + g_4 (\overline{\mu_L}\gamma^\mu e_L)(\overline{e_L}\gamma_\mu e_L) \\ & + g_5 (\overline{\mu_R}\gamma^\mu e_R)(\overline{e_L}\gamma_\mu e_L) \\ & + g_6 (\overline{\mu_L}\gamma^\mu e_L)(\overline{e_R}\gamma_\mu e_R) + H.c. \Big] \end{aligned} \tag{2.2}$$

where the first two terms are tensor type (dipole) couplings described by the form factor $A_{R,L}$ and are mostly contributed by the loop and box diagrams. The last six terms are four fermion contact interactions described with the scalar-type form factor $g_{1,2}$ and vector-type form factor $g_3 - g_6$, which are contributed by the tree diagram in leading order.

Neglecting higher orders terms in m_e, the total branching ratio of the $\mu \to eee$ decay can be given by [6]:

$$\begin{aligned}\mathcal{B}(\mu \to eee) =& \frac{g_1^2 + g_2^2}{8} + 2\,(g_3^2 + g_4^2) + g_5^2 + g_6^2 \\ &+ 32\,eA^2 \left(\ln \frac{m_\mu^2}{m_e^2} - 11/4\right) \\ &+ 16\,\eta\,eA \sqrt{g_3^2 + g_4^2} \\ &+ 16\,\eta'\,eA \sqrt{g_5^2 + g_6^2}\end{aligned} \tag{2.3}$$

where $A^2 = A_L^2 + A_R^2$. The term proportional to A^2 is logarithmically enhanced by the loop diagrams. The constant η and η' are T-violating mixing parameters. The different terms can be measured from the angular distribution of $\mu \to eee$ decay particles with a polarized muon beam.

The decay $\mu \to e\gamma$ is another lepton violating muon decay channel testing the physics beyond the Standard Model only by photon penguin diagrams (similar to Figure 2.1b), while the decay $\mu \to eee$ also includes Z-penguin, box and tree diagrams contributions. To compare the new physics mass scale reached by $\mu \to eee$ and $\mu \to e\gamma$ processes, a simplified Lagrangian with a common mass scale Λ can be formulated, assuming that the photon penguin diagram and the tree diagram are the only relevant contributions [6]:

$$\begin{aligned}L_{LFV} =& \left[\frac{m_\mu}{(\kappa+1)\Lambda^2}\overline{\mu_R}\,\sigma^{\mu\nu} e_L F_{\mu\nu}\right]_{\gamma-penguin} \\ &+ \left[\frac{\kappa}{(\kappa+1)\Lambda^2}\,(\overline{\mu_L}\gamma^\mu e_L)\,(\overline{e_L}\gamma_\mu e_L)\right]_{tree}\end{aligned} \tag{2.4}$$

where the parameter κ describes the ratio of the amplitudes of the tree (vector-type) term over the γ-penguin (tensor) term.

The limit on the common mass scale Λ as a function of the parameter κ is shown in Figure 2.2, with the input of the experimental upper limits on the branching ratio of $\mu \to e\gamma$ (MEG [33])and $\mu \to eee$ (SINDRUM [35]). Experimentally, the mass scale Λ is best constrained by the *MEG* experiment in the dipole coupling dominating region (small κ), and it is best constrained by the *SINDRUM* experiment in the four fermion contact interaction region ($\kappa \gtrsim 10$).

The mass scale Λ limit derived from the future *Mu3e* experiment with sensitivity of 10^{-15} (phase I) and 10^{-16} (phase II) is also shown in Figure 2.2. It can be seen that, with this simplified model the mass scale limit will be constrained by the *Mu3e* experiment for all κ range in phase I.

However, besides the γ-penguin and tree diagrams discussed above, the Z-penguin diagram can also contribute to the $\mu \to eee$ process significantly. Especially in the models where the new physics scale is higher than the electromagnetic scale [39–45], the Z-penguin enhances the LFV

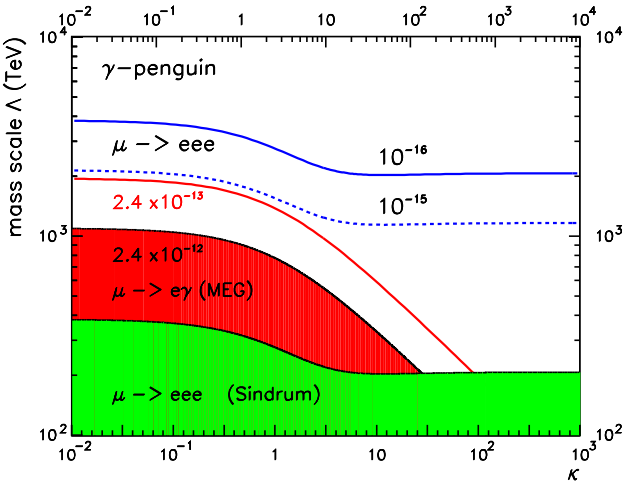


Figure 2.2: Limit on the common mass scale Λ as a function of the parameter κ [6].

decay $\mu \longrightarrow eee$ amplitude by order of magnetite over γ-penguin. With the Z-penguin diagram contributions, the mass scale limit constrained by the $\mu \longrightarrow eee$ process is significantly extended.

2.1.3 Event Signature and Backgrounds

As all the particles in the final state are detectable, the event structure in the $\mu \longrightarrow eee$ decay is kinematically well constructed. The following event signature could be used to discriminate the $\mu \longrightarrow eee$ signal and background:

- **Kinematics property:** The muon decay at rest will be used in *Mu3e* experiment. With the conservation of momentum and energy, the vectorial sum of the all decay particle momenta should vanish and the total energy should be equal to the muon mass:

$$\left|\overrightarrow{p}_{tot}\right| = \left|\sum \overrightarrow{p}_i\right| = 0 \tag{2.5}$$

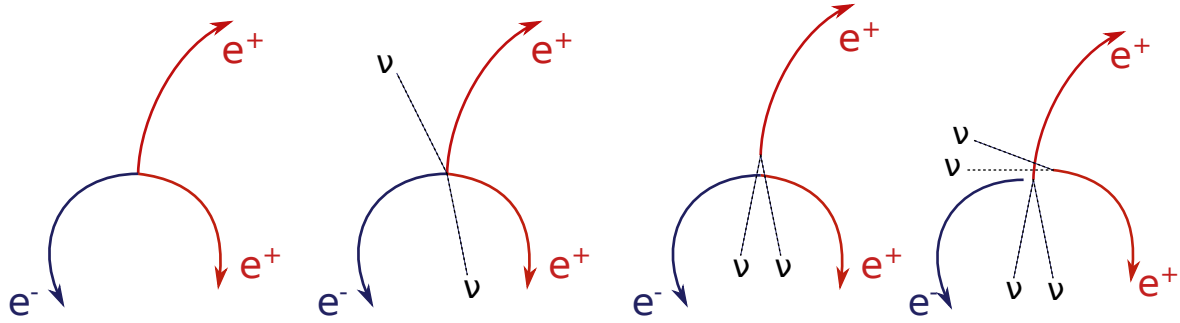
$$E_{tot} = \sum E_i = m_\mu \tag{2.6}$$

  where $\overrightarrow{p}_i$ and E_i $(i = 1, 2, 3)$ are the momenta and energy of the three decay particles. All decay particles should lie in a plane and should origin from the same vertex.

- **Timing property:** As the decay particles originally from the same decay event, they should coincide in time.

A typical signal topology is shown in Figure 2.3a.

There are two main physics background process for detecting the $\mu^+ \longrightarrow e^+e^+e^-$ decay. One is the allowed internal conversion decay $\mu^+ \longrightarrow e^+e^+e^-\nu_e\overline{\nu}_\mu$ with a branching ratio of $\mathcal{B} =$



(a) Signal Topology **(b)** Internal conversion **(c)** Combinatorial Background

Figure 2.3: Signal and background topology.

$3.4 \cdot 10^{-5}$ [37] (see Figure 2.3b). Due to the energy carried away by the undetected neutrinos, the $\mu \longrightarrow eee$ event and $\mu \longrightarrow eee\nu\nu$ event can be separated by making use of the momentum and energy conservation and the $\mu \longrightarrow eee\nu\nu$ background can be suppressed by requiring the total momentum of the event to be zero and the energy sum to be the muon mass. Precise momentum measurements are essential for the suppression of the internal conversion background to a level blow the target signal sensitivity level.

Another background is an accidental coincidence of two or three uncorrelated muon decays forming a similar signal topology to $\mu^+ \longrightarrow e^+e^+e^-$ decay, which is also referred as combinatorial background. As shown in Figure 2.3c, possible combinations are:

- One e^+ from Michel decay ($\mathcal{B} \approx 100\,\%$) and an additional e^+e^- pair. The e^+e^- pair could be produced either from the Bhabha scattering of the e^+ in the muon stopping target material or from the pair production of the photon, which could origin from Bremsstrahlung or the radiative muon decay $\mu^+ \longrightarrow e^+\gamma\nu_e\bar{\nu}_\mu$ ($\mathcal{B} = 6 \cdot 10^{-8}$).

- Two e^+ from Michel decays and an additional e^-. The e^- could come from the Bhabha scattering of the e^+ in the target region with a e^+ undetected.

The combinatorial background is highly correlated with the muon decay rate. The one Michel decay with e^+e^- pair component scales linear with rate and the two Michel decay with an additional e^- component scales quadratic with the rate. Simulations have shown that linear component is the dominating part for rate up to $2 \cdot 10^9$ muon stops per second [7]. A good momentum, vertex and timing resolution is crucial to suppress the combinatorial background by requiring the correct kinetic and timing properties of decay particles from the $\mu \longrightarrow eee$ event.

2.2 Experimental Concept

The momentum of the decay electrons[1] will be measured using silicon pixel detector in a solenoidal magnetic field. Four radial layer of the tracking detector around a fixed target would allow for precise momentum and vertex measurements.

In muon decays, the energies of all the production electrons are below 53 MeV. In such electron energy range, the multiple scattering in the detector material is the dominating effect on the momentum resolution. In the first order, the momentum resolution depends on the track deflection Ω and the multiple scattering angle Θ_{MS} (Figure 2.4a) [6]:

$$\frac{\sigma_p}{p} \propto \frac{\Theta_{MS}}{\Omega} \tag{2.7}$$

A large lever arm would help to improve the momentum measurement resolution. This can be realized by placing the outer tracker layers to large radii. However the acceptance of the low momentum electrons is compromised in this way and the phase region to test new physics is reduced. If the magnet field volume is large enough, all the electrons can recurl back towards the same axis of the decay point and then can be measured with large track deflection Ω and good momentum resolution. Further more, the effects of the multiple scattering in the first few detector material on the momentum resolution are cancelled out in the first order after travelling exactly half a circle (see Figure 2.4b). To exploit this feature for better momentum resolution, the design of the experiment leads to a narrow, long tube layout to measure the recurling tracks.

The tracking detector is complemented by two timing detectors, the scintillating fibre detector and scintillating tile detector, for precise timing measurements in order to suppress the accidental background.

2.3 Design of the Experiment

The Mu3e experiment follows the modular design concept. The experiment will be built up in three different phases and the physical data can be taken in any phase of the experiment. Shown in Figure 2.5a is the minimal detector configuration for the early commissioning of the experiment, where only four layers of the silicon tracking detector are installed around the double cone shaped target.

After successful commissioning of the center tracking detector, the two recurl stations can be added to the upstream and downstream of the center station. Each recurl station is build from a tile detector and two tracking detector layers which are a copy of the two outer silicon tracking detector layers in the center station. The scintillating fiber detector in the center station can be added at any stage. This configuration of a center station with two recurl stations is defined

[1] electrons here and after refer to both the negative charged electron e^- and positive charge positron e^+.

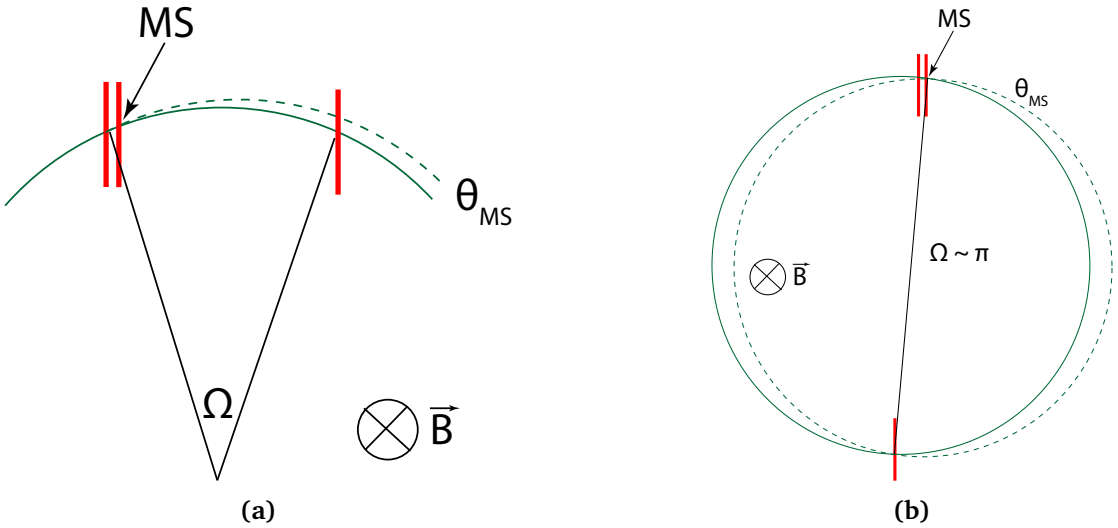


Figure 2.4: Multiple scattering seen at a plane transverse to the direction the magnetic field. **(a)** after a track deflection Ω and **(b)** for a semi-circle trajectory [6].

as the Phase I configuration of the experiment (Figure 2.5b). In phase I, precise momentum measurements for suppressing the $\mu \rightarrow eee\nu\nu$ background can be achieved with the help of the two recurl stations. Precise timing measurements with the two timing detectors will be necessary for track reconstruction and the suppression of the accidental background. The experiment will be running at a muon beam rate of $\sim 10^8$ Hz. The goal of this phase of the experiment is to reach a sensitivity of $\mathcal{O}(10^{-15})$, which is limited by the muon decay rate.

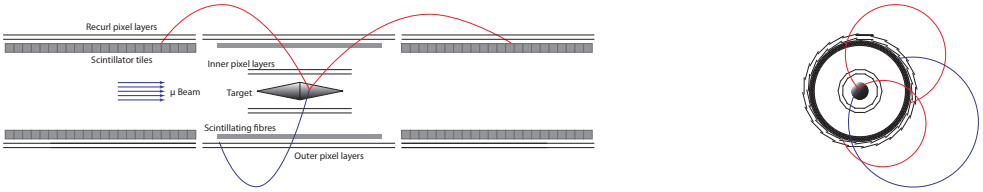
In the final phase of the experiment, phase II, two more recurl stations will be added to the upstream and downstream of the Phase I detector system and the Mu3e experiment will be running at a muon decay of 10^9 Hz. A sketch of the experiment in phase II configuration is shown in Figure 2.5c. The acceptance of the detector is further increased such that precise momentum measurements for all the recurl particles in the acceptance of the center tracking detectors can be performed. The additional tile detectors will help to fight with the increasing accidental background at higher muon decay rate with its high timing resolution and high granularity. In this phase, the Mu3e experiment will reach its ultimate goal of searching for $\mu^+ \rightarrow e^+e^+e^-$ with a branching ratio sensitivity $\mathcal{B}(\mu \rightarrow eee) \leq 10^{-16}$.

Background Suppression

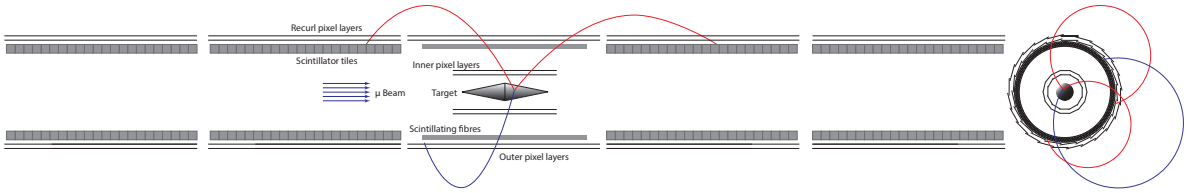
In order to achieve the branching ratio sensitivity goal, all the background have to be suppressed below the target signal level.

Figure 2.6 shows the internal conversion background suppression factor for differences momentum measurement resolutions. During phase I of the experiment, the momentum resolution has to achieve 0.8 MeV in order to get sufficient internal conversion background suppression and

(a) Minimal detector configuration



(b) Phase I



(c) Phase II

Figure 2.5: Schematic view of the Mu3e detector for early commissioning phase, Phase I and Phase II [6].

to reach a sensitivity of $2 \cdot 10^{-15}$ with a 2σ reconstructed momentum cut.

A suppression of at least two order of magnitude is necessary to reduce the accidental background below the target signal level for the phase I operation of the experiment. This requires the fibre detector and the tile detector to provide timing measurements with a resolution of below below 500 ps and 100 ps respectively.

2.4 Muon Beam and Muon Stopping Target

The Mu3e experiment will be located in the front area of the πE5 beam line at the Paul Scherrer Institute (PSI) in Villigen, Switzerland, where the most intense continues low energy muon beams in the world is provided. Figure 2.7 shows the layout of the πE5 area at PSI. The Muon production starts from the High Intensity Proton Accelerator (HIPA) facility in PSI which delivers a 590 MeV

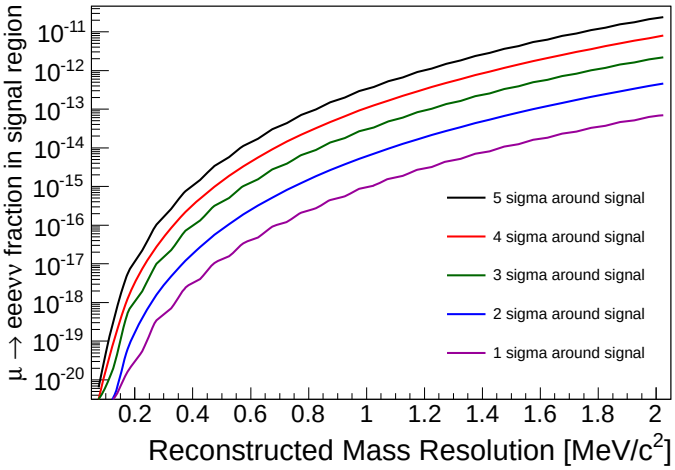


Figure 2.6: Internal conversion signal fraction as a function of the momentum resolution [6].

proton beam with a beam current up to 2.4 mA and a beam power of ~1.4 MW. The proton beam is brought to hit a target made by graphite, referred as *target E*, and the pions are produced via various proton-proton and proton-neutron interactions. Through the pion delays of $\pi^+ \longrightarrow \mu^+ + \nu_\mu$ and $\pi^- \longrightarrow \mu^- + \bar{\nu_\mu}$, the muons are produced. The surface muons, which are produced from the pions stopped by the production target and decay at the surface of the target, are extracted to the πE5 beam line for the Mu3e experiment. The surface muons are best suit for the Mu3e experiment for their low momentum of around 28 MeV/c and 100 % polarization.

The πE5 beam line will be shared with the upgrade of the MEG experiment - MEG II experiment [46], which will be located at the rear area of the πE5 beam line. A Compact Muon Beam Line (CMBL) has been developed to share the common elements between two experiments and to minimize the transition time and beam line modification to switch from one experiment to another. A Computer Aided Design (CAD) drawing of the CMBL is shown in Figure 2.8. A commissioning run of the CMBL in 2016 has shown a $\sim 8 \cdot 10^7\, \mu^+/s$ at the injection to the Mu3e solenoid at 2.2 mA proton current . The muon rate of $10^8\, \mu^+/s$ for the Phase I configuration of the Mu3e experiment is expected for running with 2.4 mA proton current and larger pion/muon production *target E* at the beginning of the πE5 beam line [47].

The muon beam is transport to the muon stopping target in a 60 mm diameter beam vacuum-pipe. The vacuum pipe also contains a 600 µm Mylar degrader to help with stopping muons on the stopping target. The design of the muon stopping target is a trade-off between the muon stopping power and background reduction. On one hand, the muon stopping target should have sufficient material to to stop most of the muons, which is assisted by the degrader in beam line. On the other hand, the muon stopping target should contain as less as possible material to reduce the contribution to the accidental background, such as the Bhabha scattering, photon conversion or Compton scattering, as well as to reduce the influence on the momentum measurement of the

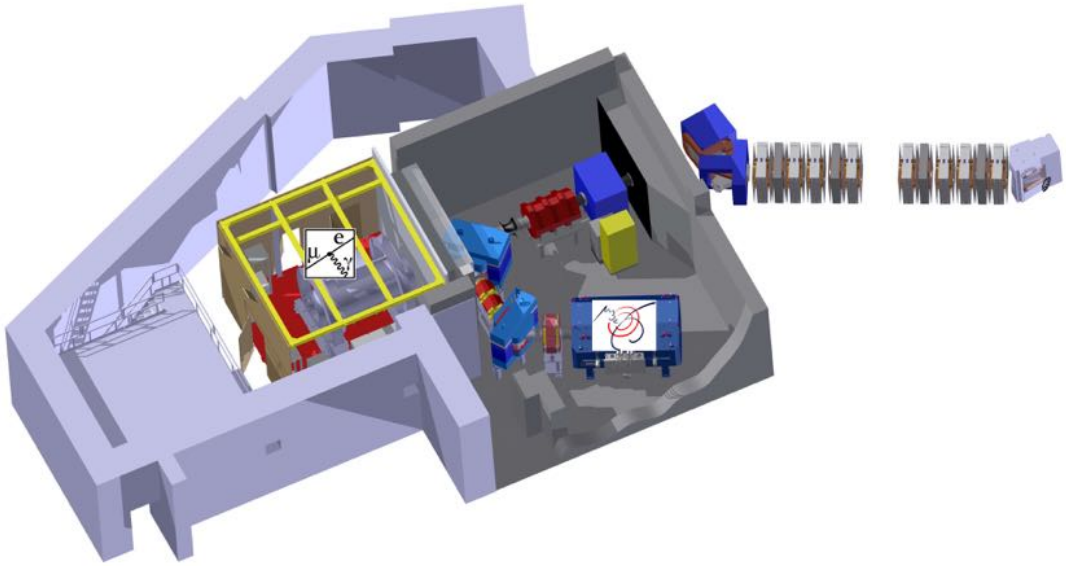


Figure 2.7: Layout of the πE5 area at PSI [48].

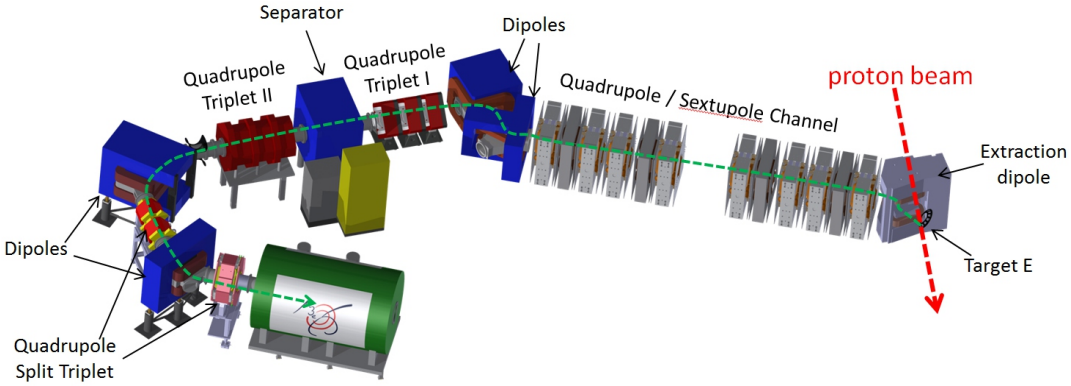


Figure 2.8: CAD drawing of the Compact Muon Beam Line at the πE5 channel [48].

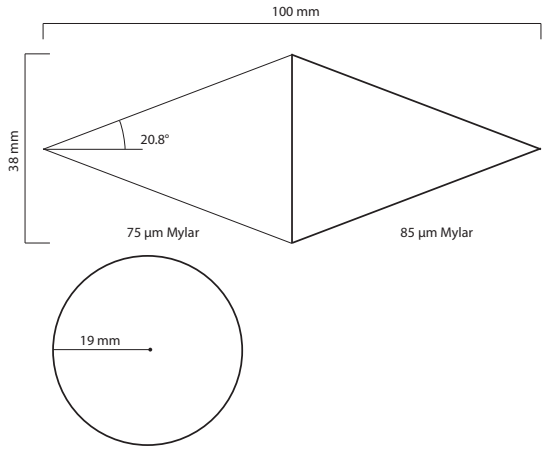


Figure 2.9: Muon stopping target design [7].

decay electrons due to multiple scattering. Thus low-Z material is preferred for the target design. Additionally, the vertices of muon decays should be evenly spread out on target to reduce the accidental coincidence of two uncorrelated track, as well as to distribute the tracks hits on the inner tracking detector. Figure 2.9 shows the baseline design of the muon stopping target. Similar to the approach of the SINDRUM experiment, it is a hollow double cone target with a length of 100 µm and a diameter of 38 µm. Mylar is used to produce the target with a thickness of 75 µm for the upstream part and 85 µm for the downstream part. The total projection thickness is then 425 µm, corresponding to 0.16 % radiation length X_0. The muon stopping target will be suspend by three thin nylon strings on both side of the target, which will be connected to the supporting structure of the pixel detectors.

2.5 Magnet

The Mu3e experiment requires a homogeneous solenoidal magnet field for the momentum measurement of the decay electrons. The nominal field strength of 1 T is chosen for the tradeoff between the acceptance of low energy electrons on one hand, where a weak magnet is preferred, and a good momentum resolution on the other hand, where a strong magnet field is preferred. Superconducting magnet technology will be applied to generate the magnet field with a warm bore dimension of 1 m in diameter and 2.6 m in length, and with a field homogeneity of $\Delta B/B \leq 10^{-4}$.

2.6 Detector System

The detector system of the Mu3e experiment consists of the pixel tracking detector for the precise momentum and vertex measurement, complemented by the scintillating fibre detector and the scintillator tile detector for precise timing measurement. The momentum resolution is crucial for the suppression of the irreducible internal conversion background. The vertex and timing resolution is essential for the suppression of the accidental combinatorial background.

2.6.1 Pixel Tracking Detector

As the momentum measurement resolution is dominated by the multiple scattering in the Mu3e experiment, it is essential to reduce the material in the detector area to achieve required momentum resolution. The Mu3e tracking detector is to be built from thin silicon pixel sensors, called MuPix, based on High-Voltage Monolithic Active Pixel Sensors (HV-MAPS) technology [49] for the minimization of the material in the active volume. The MuPix chip has featured the sensor with readout electronics on the same device, which helps to reduce the material in the detector area greatly with the absence of the additional interconnect and extra readout electronics. Due to its thin active depletion volume, MuPix can be thinned down to 50 µm or less, significantly reducing the material budget further down to an equivalent radiation length of X/X_0<0.1 %.

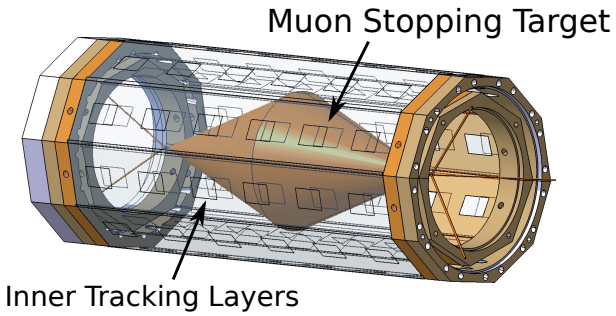


Figure 2.10: Mechanics of the inner tracking layers and the muon stopping target. Modified from [7].

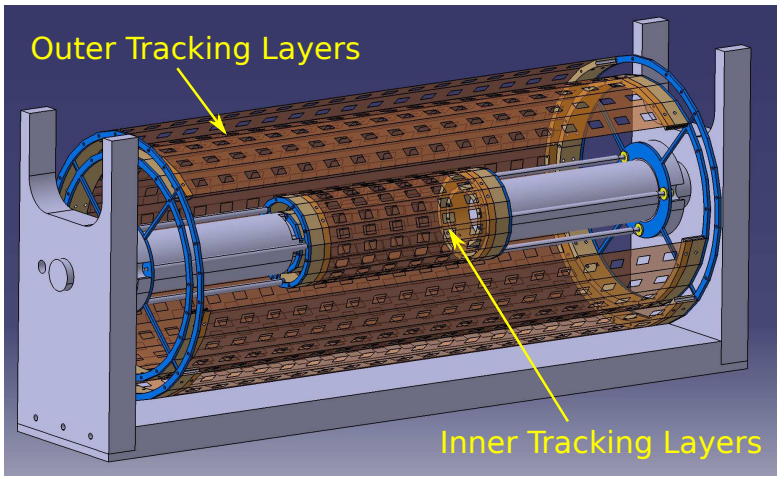


Figure 2.11: Mounting of the pixel tracking detectors. Modified from [6].

With a bias voltage higher than 50 V, the charges on MuPix chips are collected by drift other than diffusion, which will result in a much faster signal and a timing resolution in the order of $\mathcal{O}(10\text{ns})$.

The MuPix chip will have a active area of 20 mm × 20 mm filled with 80 µm × 80 µm pixels. Each pixel has its own processing and readout circuit for the sensor signals. Upon hit by a particle, time stamp information is generated on the corresponding pixel. The time stamp information, together with the address of the pixel, is then send out via a Low Voltage Differential Signaling (LVDS) serial data link with a bit rate of 1.25 Gbps[1].

The power and the signal connection of the MuPix chip are realized by by Single-point Tape Automated Bonding (SpTAB) to so called High Density Interconnects (HDI), which is made by thin aluminum traces on thin polyimide substrates. The support structure for the sensor are made from thin polyimide. The sensor-HDI-polyimide composite is self supporting and has a equivalent radiation length of $X/X_0 = 0.115\,\%$.

[1] Giga bit per second.

Three tracking detectors will be installed for the Phase I run of the Mu3e experiment - the center tracker and two trackers at the upstream and downstream recurl stations.

The center tracker detector will have four MuPix tracking layers consisting of several modules built from the senor-HDI-polyimide composites. As shown in Figure 2.10 is the CAD drawing of the two inner tracking layers and the muon stopping target. The inner tracking layers are 12 cm long to cover the muon stopping target with a length of 10 cm. They are at radius[1] of 23.31 mm and 29.80 mm respectively. The two outer tracking layers are at much large radius of 73.87 mm and 86.34 mm and have a length of 34 cm and 36 cm respectively to provide a large acceptance for the decay electrons. V-folds supporting structures made from polyimide are used for maintaining the mechanical stability of the two long outer pixel tracking layers. A drawing of the centering tracker station with the mounting structure is shown in Figure 2.11.

As mentioned in previous paragraph, the trackers at the recurl stations are copies of the two outer tracking layer of the center tracker for the momentum measurement of the recurling particles. The trackers will be immersed in dry helium and cooled by the helium gas flows. In total 2844 MuPix chips will be used to build the center tracker and the recurl trackers.

2.6.2 Fibre Detector

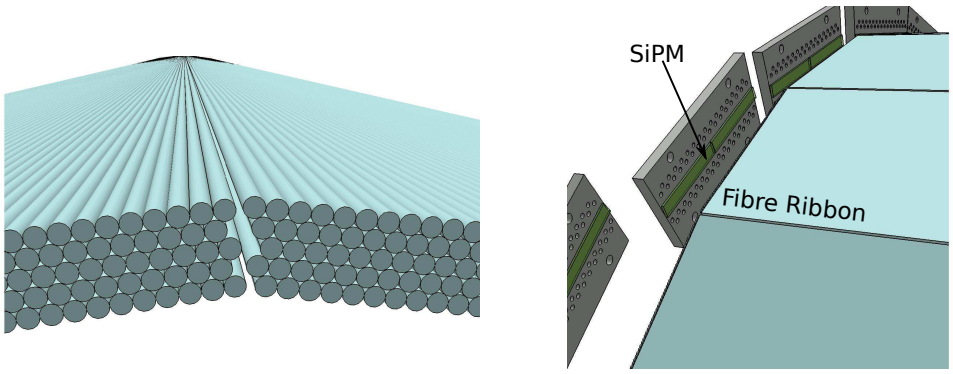
The Mu3e fibre detector is planed for the timing measurement in the center station, especially for the timing measurements of the particles which do not reach the recurl stations. The fibre detector is required to achieve a timing resolution of better than 500 ps and a detector efficiency close to 100 % for the suppression of the accidental background. Minimal amount of material should be used in the fibre detector to reduce the deterioration in the momentum measurement resolution. Furthermore, the fibre detector has to cope with the high rate environment and very tight space constraints.

The fibre detector is built from scintillating fibres coupled to the Silicon Photomultipliers (SiPMs). Shown in Figure 2.12a is a CAD drawing of the scintillating fibre ribbons, which will be made by three or four layer of 250 µm scintillating fibres glued together. The ribbons will be placed at a radius of 64 mm, right below the third pixel tracking layer. The ribbons will be longer than 28 cm, which is determined by the acceptance of the outer tracking layers.

Due to the tight space constraints, SiPMs are the only option for the photon sensors in fibre detector. SiPMs also have the advantages of insensibility to the magnet field, relatively high photon detection efficiency (PDE) and fast timing response. The fibre ribbons are coupled to the SiPM arrays at both sides, as shown in Figure 2.12b and Figure 2.13. Acquiring signals at both sides will help with improving the timing resolution and to remove noise event at later data processing stages in the Data Acquisition system (DAQ).

The SiPM will be readout by the dedicated Application Specific Integrated Circuit (ASIC), the MuTRiG chip, which sit on the front-end readout printed circuit board (PCB) connected to the

[1] Radius is defined as the minimum distance between the MuPix chip and the center axis.



(a) Fibre ribbons. **(b)** SiPM and fibre array.

Figure 2.12: CAD drawing of the scintillating fibre detector. Reprinted or modified from [6]. Please note that the optimal number of fibre layers is under investigation.

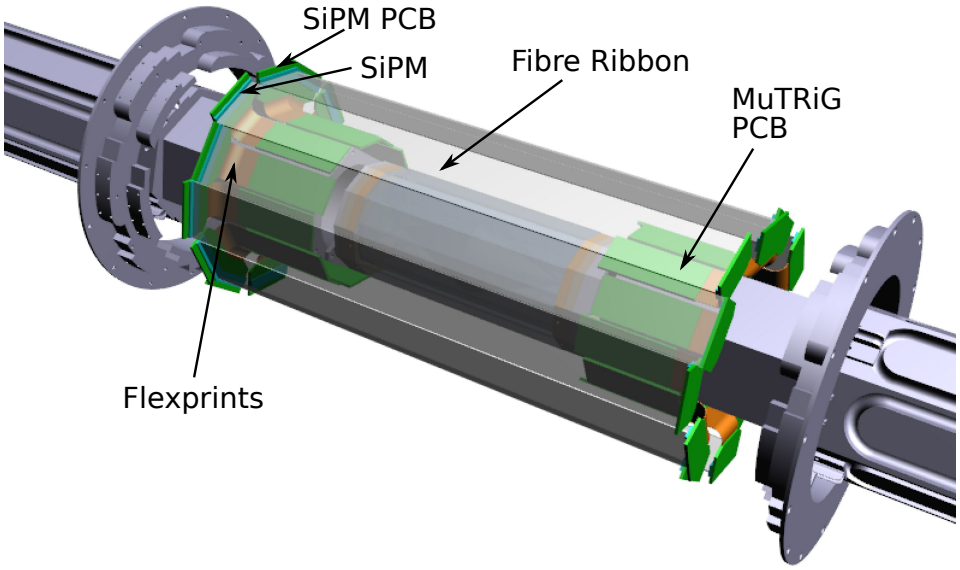


Figure 2.13: CAD drawing of the Mu3e fibre detector. Modified from [7].

SiPM PCB via flex print. The front-end readout PCBs will be fixed on the cooled support plates around the beam pipe.

Modular design is also applied for the fibre detector. The fibre detector consists of six modules, each of which is built from two fibre ribbons and their corresponding SiPMs, flex prints fixed to the mechanical support at both sides. The fibre modules can be mounted or unmounted radially.

2.6.3 Tile Detector

The timing resolution of the fibre detector alone is not sufficient for the desired accidental background suppression. It is complemented by the timing measurements from two identical tile

detectors sitting inside of the pixel tracking layers in the recurl stations. As there is no material budget requirements for the tile detector, much thicker scintillating material can be used compared to the fibre detector, yielding much larger signals and significant better timing resolution. Achieving a timing resolution of better than 100 ps and a detector efficiency close to 100 % is the main goals of the tile detectors. Very tight spatial constraints are also applied to the tile detectors.

The tile detectors follow the modular design concept. The basic unit of the tile detector, referred as submodule, is shown in the Figure 2.14. It consists 32 channels in two 4×4 scintillating tile matrices glued to SiPMs. The tiles will be made from Ej-228 [50] fast plastic scintillator with a size of $6.3\,\text{mm} \times 6.2\,\text{mm} \times 5.0\,\text{mm}$ for the two center rows of cubic shape tiles and $7.44\,\text{mm} \times 6.2\,\text{mm} \times 5.0\,\text{mm}$ for two edge rows of trapezoidal shape tiles. Each tile will be wrapped with reflecting foil individually to improve light collection and to avoid optical crosstalk between tiles. A outlet window with a size of the SiPM active area will be cut out on the reflecting foil for transferring the scintillating photons to the photon sensor. The SiPM with $3\,\text{mm} \times 3\,\text{mm}$ active area and $50\,\mu\text{m} \times 50\,\mu\text{m}$ pixel size is chosen to achieve sufficient signals and optimized timing resolution [51]. The SiPMs will be soldered on the flex print PCB and read out by the MuTRiG chip which sits on the center part of the PCB. Around 1000 photons are expected to be detected by the SiPM in the tile detector compared to a few photon in the fibre detector.

14 submodules will wrap around a metal supporting structure to form a 448 channels module, which will be cooled by water running through the structure. The tile detector at each recurl station is made from seven module on the end ring with a length of 368 mm and a outer radius of 62 mm. The two tile detector will comprise of 6722 detector channels in total. A CAD drawing of the tile detector station is shown in Figure 2.15.

2.7 Data Acquisition system

The DAQ system of the Mu3e experiment is a streaming system without a hardware trigger. The zero-suppressed hit information data from the detectors is sent to DAQ system continuously. The overall view of the Mu3e experiment DAQ system is shown in Figure 2.16.

The DAQ system consists of three layers: the front-end FPGAs, the switching boards and the filter farm. In the first layer, the hit information data are sent from both the tracking detectors and the timing detectors to the front-end FPGAs with 1.25 Gbps LVDS links. Depending on the occupancy of the detectors, a row data rate of ~105 Gbps between the detectors and the front-end FPGAs is appraised for the Phase I of the experiment. Using the time stamp information of each hit data, the front-end FPGAs also performed a sorting and grouping operation on the buffered hit data into different packets of 50 ns length. A preliminary clustering operation is also applied on the fibre detector data to reduce the data rate to the next layer.

The front-end FPGAs send the packets to the switching boards using optical links with 6 Gbps bandwidth per link. The switching boards merge the packets from different front-end FPGAs and

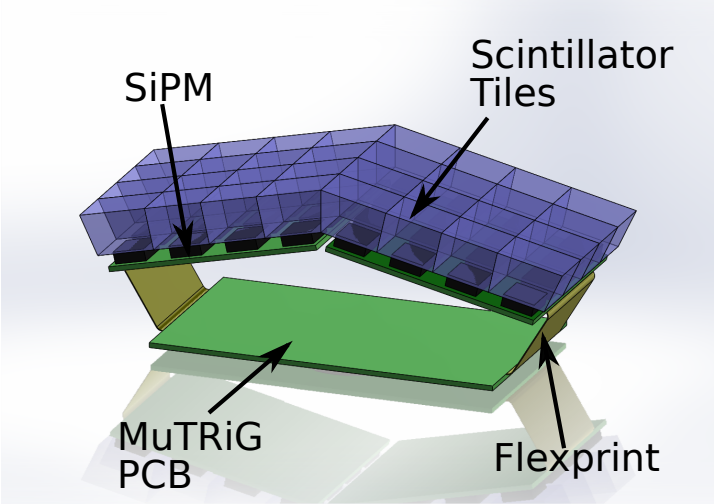


Figure 2.14: CAD drawing of a Mu3e Tile submodule. Modified from [51].

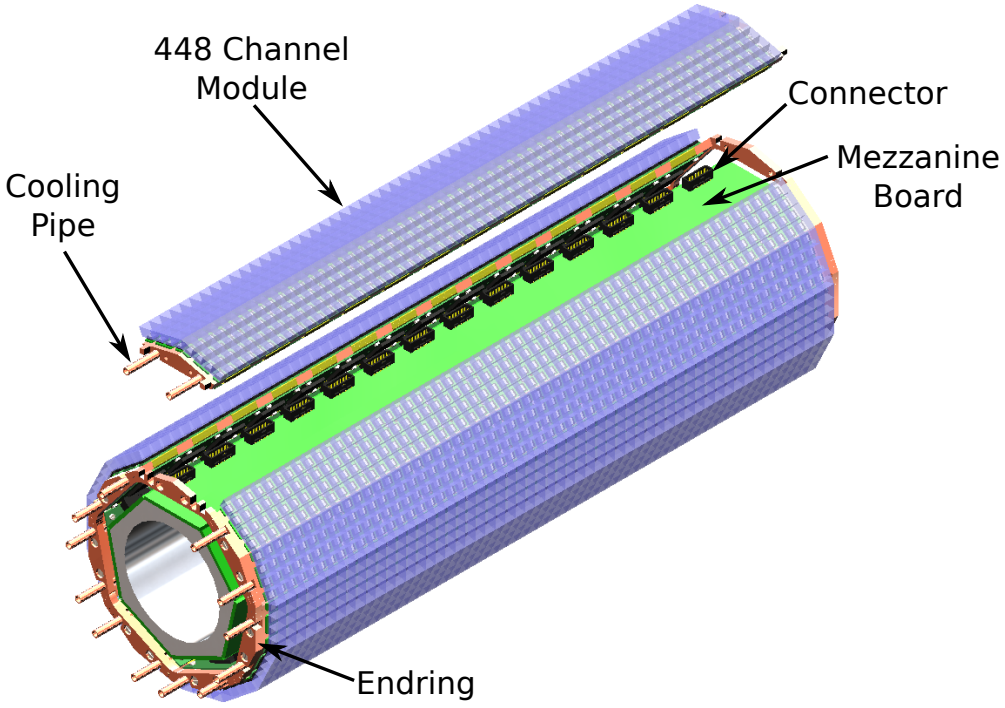


Figure 2.15: CAD drawing of a Mu3e Tile detector station [7].

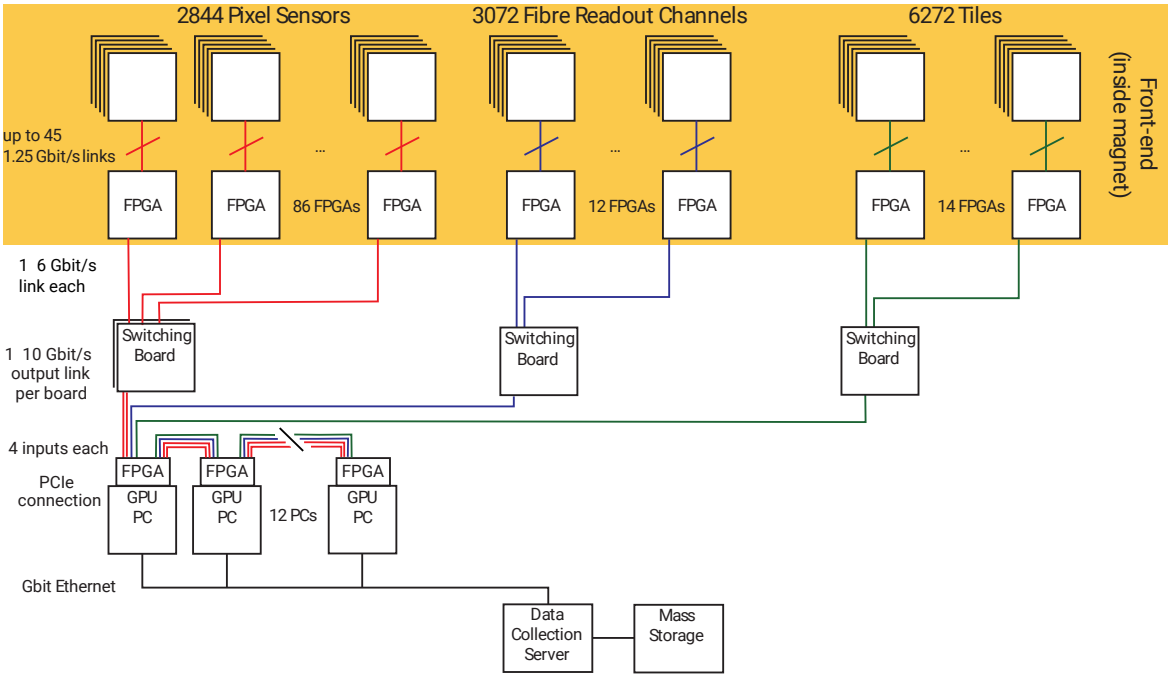


Figure 2.16: Schematic of the DAQ system [53].

deliver the merged packets to the FPGA PCIe boards in the event filter farm PCs, allowing every event filter farm PC to see the data from all the detectors for a certain time slice. The optical links with 10 Gbps bandwidth per link will be used between the switching boards and the event filter farm PCs.

The FPGAs in the event filter farm PCs will perform the event building, buffering and simple event clustering, sorting and selection. The event data are then transferred to the memory of the high-performance graphics processing units (GPU) through the main memory of the PC via Direct Memory Access (DMA). An online selection algorithm with track fitting and vertex reconstruction will be running on the GPUs to reduce the data rate by a factor of 100. The selected events are then delivered from the filter farm PCs to the center DAQ computer, where the well established Maximum Integrated Data Acquisition System (MIDAS) [52] software will be running. The final data rate from the filter farm PCs to the center DAQ computer is expected to be in the order of 50-100 MByte/s and a Giga bit Ethernet link will be used there.

Chapter 3

Silicon Photomultiplier

Silicon Photomultipliers (SiPMs) are solid-state photon sensor with the capability of detecting single photon. With the development in the last decade, SiPMs have become more and more popular for photon detection in the fields of high energy physics and medical imaging for their comparable performance to the conventional photomultiplier tubes (PMT) and their additional advantages of insensitivity to the magnet, compact sizes, low operation voltage and good timing performance. SiPMs are chosen as photon sensors for the Mu3e fibre and tile detectors.

In the first part of this chapter, the working principle of the SiPM will be outlined. Then will follow a description of the electronic module and the typical output signal of the device. In the last part, the basic property of SiPMs will be discussed.

3.1 Working Principle

Solid-state detectors use the small energy-gap between the valence band and conduction band in the semiconductor material, such as Silicon and Germanium, for radiation detection. Despite the solid-state detectors are of different types and various properties, they are all based on the properties of the *p-n junction*.

P-N Junction

The p-type semiconductor materials are generated by doping the intrinsic semiconductor material with the acceptor impurities and has larger concentration of the positive charge carriers (*holes*) than the negative charge carriers (*electrons*). Conversely, the n-type semiconductor is made from intrinsic semiconductor material doped with the donor materials and has larger concentration of electrons than holes. The p-doped and n-doped semiconductor materials are relative conductive due to their abundant majority charge carriers. In the p-n junction, the majority charge carriers of the p-type and n-type semiconductor materials diffuse towards and combined with each other, leaving net charge of fixed ions behind and forming the *space charge region*, or the *depletion region*. An electric field is created with the net charge distribution in the depletion region and opposes with the diffusion process. A equilibrium will be built up between the diffusion process and

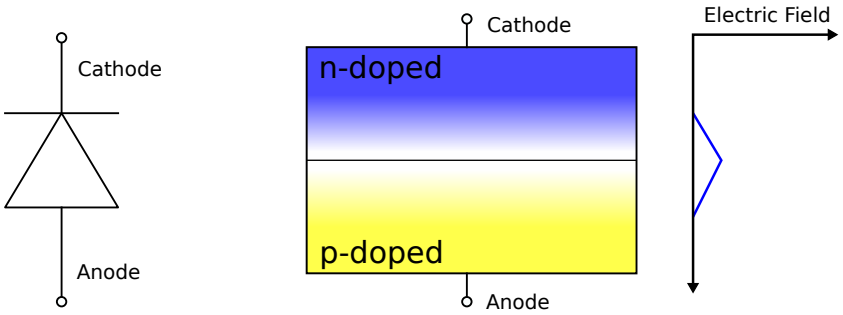


Figure 3.1: Circuit symbol, schematic structure and electronic field distribution of a p-n junction.

increasing of the electric field. The structure of a p-n junction and the electric field distribution in the depletion region are shown in Figure 3.1.

The depletion region has some attractive properties as a radiation detecting medium. By absorption of a photon in this volume, an electron can be excited from the valence band to the conduction band of the material through photoelectric effect, generating an electron-hole pair. Sensing the electric field existed in the depletion region, the generated electron drifts to the n-doped electrode and the hole drifts to the p-doped electrode. An electrical signal is created by the motion of the generated electron and hole [54].

The p-n junction can work as a photon detector but has very poor performance. The electric field in the depletion region is not strong enough such that the generated electrons and holes are not moving rapidly and can be easily lost by recombination or trapping. In addition, the depletion region, which is the sensitive detector volume, is very small.

The p-n junction can be biased in a reversed direction, where the n-doped part (cathode) is applied with higher potential than the p-doped part (anode). As the depletion region has much higher resistivity than the n-doped or p-doped materials, the applied voltage is virtually applied on the depletion region, strengthening the electrical field in the depletion region. The majority charge carriers in both parts are pushed to the electrodes, extending the width of the depletion region.

PIN Photodiodes

For photon detection, the *PIN photodiode* is a useful alternative for its advantages over the conventional p-n junction. The schematic structure of a PIN diode is shown in Figure 3.2. It has a sandwich structure of a thin high p-doped layer, a thick intrinsic semiconductor layer and a thin high n-doped layer. Only a small reversed voltage is required to fully deplete the intrinsic region. Due to the thick intrinsic layer, the depletion region is largely extended compared to the p-n junction, resulting in a much larger sensitive volume and much higher efficiency. Furthermore, the width of the depletion region and the detection properties of the p-n junction depend on the applied voltage and the temperature. The sensor response of the PIN photodiode is not influence

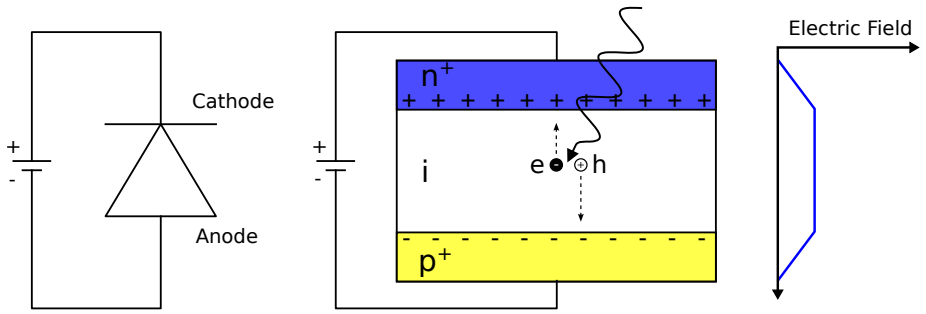


Figure 3.2: Circuit symbol, schematic structure and electronic field distribution of a PIN diode. Based on a figure from [51].

by the variations on the operation voltage and the temperature once the intrinsic region is fully depleted. However, the PIN photodiode is not able to detect small number of photons due to the lack of internal amplification mechanism.

Avalanche Photodiodes

Avalanche Photodiodes (APDs) follows the development and offers the possibility to measurement low light flux with a build-in amplification mechanism.

The structure of an APD is shown in Figure 3.3. Compared to the PIN photodiode, APD has an additional p-doped layer (p layer) between the intrinsic layer(i or p^- layer) and the high n-doped layer (n^+ layer) to generate a high doping gradient at the p-n junction region. With a high reversed bias voltage (100-200 V for silicon), a strong electrical field is generated around that area. The electron, which is generated from the absorption of a photon and drifts to the high electrical field region, is strongly accelerated and can gain enough energy to create secondary electron-hole pairs through *impact ionization*, yielding an avalanche multiplication.

The avalanche multiplication factor, or the *gain* of an APD, is governed by the number of created secondary electron-hole pairs per unit length, or the *ionization coefficient*, which is determined by the applied bias voltage.

The relationship between the gain of an APD and the applied bias voltage is sketched in Figure 3.4, which usually can be obtained with an "I-V" curve measurement.

There are three different working regions depends on different reversed bias on an APD. At low voltages, the electrons can not be accelerated to enough energy for impact ionization due to small electrical field present in the APD. In this mode, the APDs essentially work like a PIN photodiode.

In the second working region with higher applied bias voltage, the electrical field is strong enough to accelerate the electrons to enough energy for creating secondary electron-hole pairs and undergoing avalanche multiplication process. As holes have smaller ionization coefficient than electrons [55–57], the holes can not gain enough energy for impact ionization in this bias region. Thus the avalanche process stops when the electron avalanche reaches the boundary of

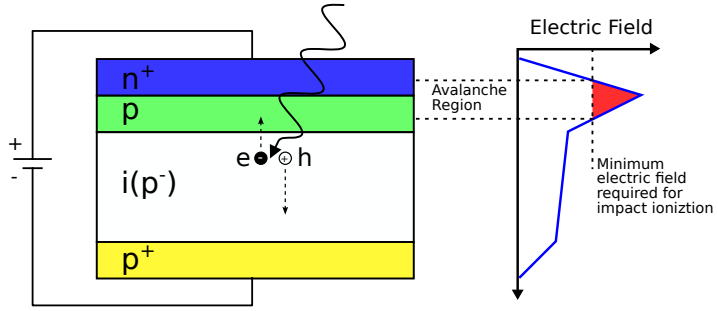


Figure 3.3: Structure and the electronic field distribution of an APD. Based on a figure from [51].

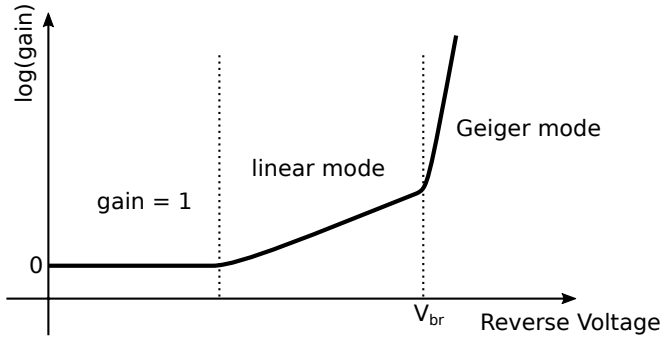


Figure 3.4: Gain of the APD in different reverse bias voltage.

the avalanche region. This is the *linear mode* for the operation of an APD. The logarithm of the gain increases linearly with the applied bias voltage and the gain can reach as high as 10^3.

For the third operation region, the bias voltage exceeds so called *breakdown voltage* V_{br}. In this region, the electrical field is so strong that not only the electrons, but also the secondary holes gain enough energy for impact ionization and undergoing avalanche process. The electron avalanches and hole avalanches propagate towards two different direction and initiate new avalanches for each other. This results in a self-sustaining multiplication process and a constant current through the APD device. This process is called *Geiger discharge* and an APD working in this region is referred as *Geiger mode Avalanche Photodiode* (G-APD) or *single-photon avalanche diode* (SPAD).

Once the G-APD is triggered, the avalanche current flowing through the device is constant and the G-APD is not sensitive to further incoming particles. In order to reset the device for the next photon detection, the bias voltage has to be reduced to the breakdown voltage V_{br} to stop the Geiger discharge current. This process is referred as *quenching*. A commonly used technique is *passive quenching*, which is to connect the G-APD in series with a resistor of $\mathcal{O}(100\,\mathrm{k}\Omega)$ to the bias voltage. Figure 3.5 shows the working principle of the passive quenching in a G-APD. When there is no avalanche process ongoing, there is no current flowing through the resistor and G-APD. Due to big resistance of G-APD device under the reverse bias, all the bias voltage are virtually applied on the G-APD. Upon triggered by the absorption of an photon, the G-APD undergoes Geiger discharge and the avalanche current builds up. This current also flows through

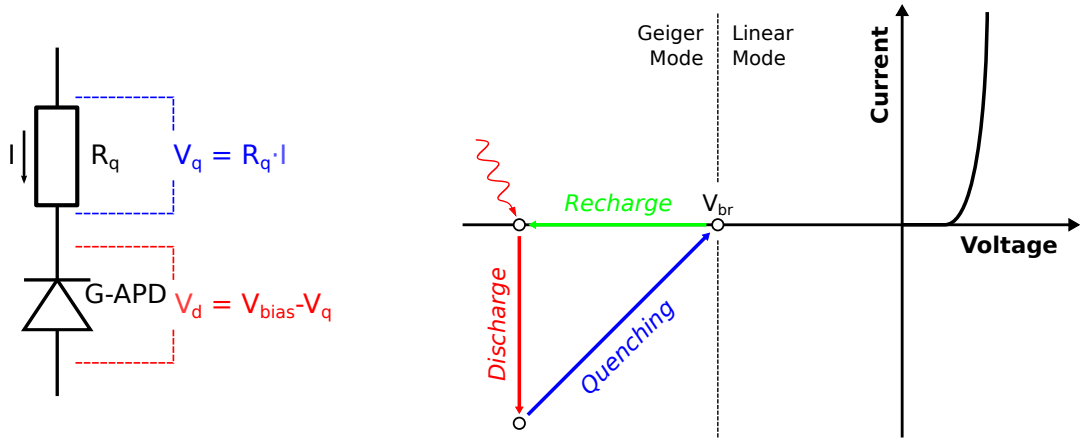


Figure 3.5: Working principle of passive quenching in a G-APD [51].

the quenching resistor, generating a voltage drop of $V_q = I \cdot R_q$ over the resistor and reducing the voltage over the G-APD $V_d = V_{bias} - V_q$. The electrical field in the depletion region falls with V_d and will become too week to allow self-sustaining avalanche process when the V_d drops to the breakdown voltage V_{br}. After quenching, the voltage over the G-APD slowly recharges to the applied bias voltage. The resulting output signal is a current pulse with a fast rising edge and a slow recovery tail and of a fixed charge Q. The output change comes from the difference of the charge stored on the diode capacitance C_{APD} with its bias voltage changed from V_{bias} to V_{br}, thus output charge Q can be obtained by:

$$Q = (V_{bias} - V_{br}) \cdot C_{APD} = V_{ov} \cdot C_{APD}. \tag{3.1}$$

where $V_{ov} = V_{bias} - V_{br}$ is the applied *over voltage* of the G-APD.

The gain of the G-APD can be as high as $\mathcal{O}(10^6)$, which is comparable to that of PMTs. The majority limitation of G-APD is that it is a binary device and can only count single photon, as its output signal does not depends on the number of incoming photon.

Silicon Photomultiplier

The photon counting limitation of G-APD is solved by the development of the *Silicon Photomultipliers* (SiPMs)[1].

SiPM is pixelated device. The pixels are identical and each of them is a Geiger-mode APD connected with a quenching resistor. A picture of a SiPM and a microscope view of its pixel can be seen in Figure 3.6a and the schematic of a SiPM is shown in Figure 3.6b. All the pixels are connected in parallel to a common bias input and a common output. The output signal of a SiPM is the sum of the current signals from all the pixel. As each pixel acts as a binary device and

[1] There are different names for this device, such as Multi Pixel Photon Counters (MPPCs), depending on the manufacture.

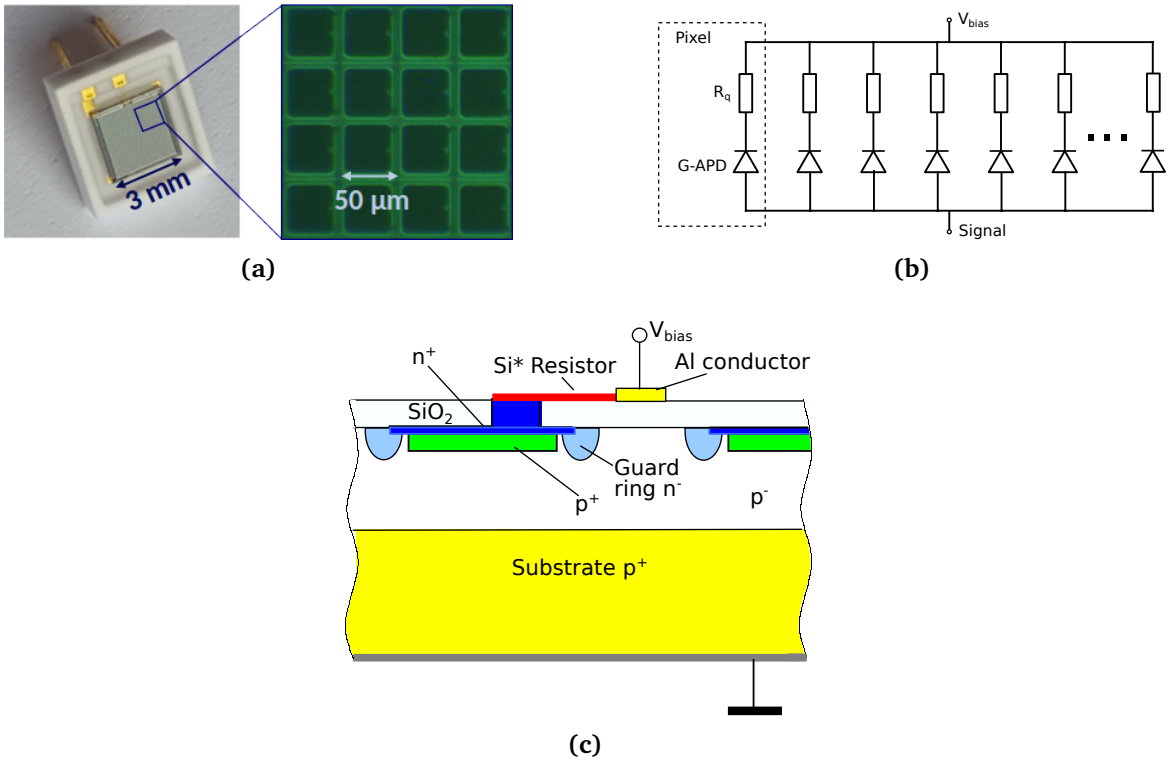


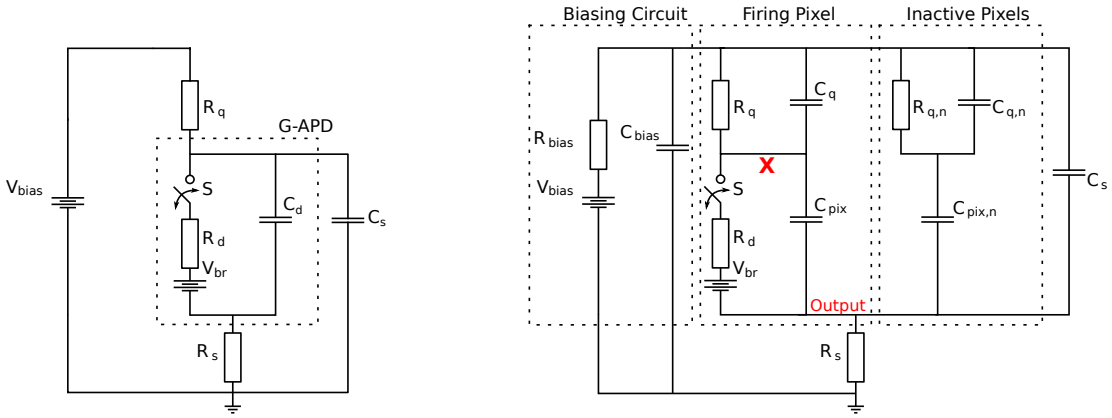
Figure 3.6: (a) A picture of a 3 mm × 3 mm SiPM and a microscope picture of the 50 µm × 50 µm pixels. **(b)** Schematic drawing of a SiPM. **(c)** Cross-section structure of a SiPM pixel [58].

outputs a defined charge Q_{pixel} once triggered by a photon, the total output charge Q is the sum of the charges from all the triggered pixel:

$$Q = \sum_{i}^{n_{triggered}} Q_{pixel,i} = n_{triggered} * Q_{pixel} \tag{3.2}$$

Thus the number of the triggered pixels can be extracted from the output charge of SiPMs and can be used to infer the number of incoming photons.

Figure 3.6c shows the structure of a single pixel. The diode part has similar structure to that of an APD. Guard ring structures are added around the p-n junction area of each pixel to suppress the undesired high electrical field at the pixel edges. The cathode of the diode (n^+-doped layer) in each pixel is connected to a metal contact for the common bias connection over a quenching resistor realized by polysilicon[1]. The transparent SiO_2 layer acts as the insulation between the metal contacts and the semiconductor materials.



(a) Equivalent circuit of a G-APD with quenching circuit, biasing circuit and readout resistor. Inspired by [59].

(b) Equivalent Circuit of a SiPM with biasing and readout circuit [8].

Figure 3.7: Electrical models of a G-APD and a SiPM.

3.2 Electrical Model

Figure 3.7a shows the electrical model of a G-APD with quenching circuit [59]. The G-APD is modeled as parallel connection between a junction capacitance C_d and a series connected components of a switch S, diode resistance R_d and voltage source V_{br}. R_q is the resistor for passive quenching of Geiger discharge. C_s presents the parasitic capacitance of the diode cathode terminal to ground. R_s is the readout resistor to convert the G-APD output current signals to voltage signals.

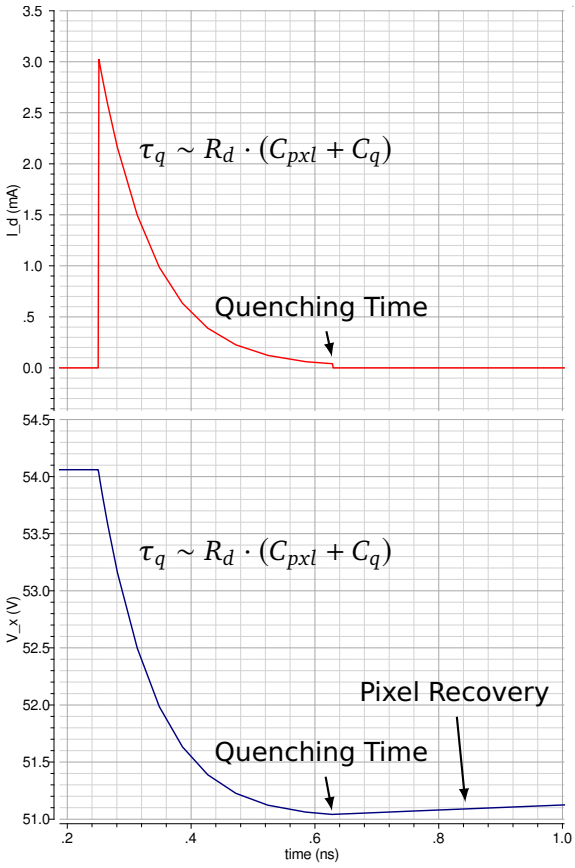
The electrical model of G-APD was later extended for SiPM by F. Corsi et al. [60]. As shown in Figure 3.7b, the SiPM is modeled by parallel connection of a firing pixel with the other inactive pixels. Each pixel is modeled similarly to G-APD with a quenching circuit. As the quenching resistors are manufacture close to the diodes inside the pixels of a SiPM, thus the parasitic capacitance between the quenching resistors and the diodes in the same pixel, C_q, can not be neglected and is added into the model. The inactive pixels are grouped and presented by the components $R_{q,n}$, $C_{q,n}$ and $C_{pxl,n}$. Assuming the total pixel number of the SiPM is N, then $R_{q,n} = R_q/(N-1)$, $C_{q,n} = (N-1)\cdot C_q$ and $C_{pxl,n} = (N-1)\cdot C_{pxl}$. C_s is presenting the parasitic capacitance between the bias distribution lines on the SiPM surface to the silicon substrate. R_{bias} and C_{bias} are part of the biasing circuit and have typical values of 10 kΩ and 100 nF.

Triggering a pixel is corresponding to closing the switch S in the firing pixel. At the moment of closing the switch, the voltage at node X V_x equals to V_{bias}, the voltage at the output node V_{output} equals to 0 and I_d, the current flowing through R_d, jumps to $(V_{bias} - V_{br})/R_d$. The charge stored in the pixel capacitance C_{pxl} starts to discharge with a time constant $\tau_q \sim R_d \cdot (C_{pxl} + C_q)$, causing V_x and in turn I_d to drop. Once I_d falls below a level of a few µA, the avalanche in the pixel is

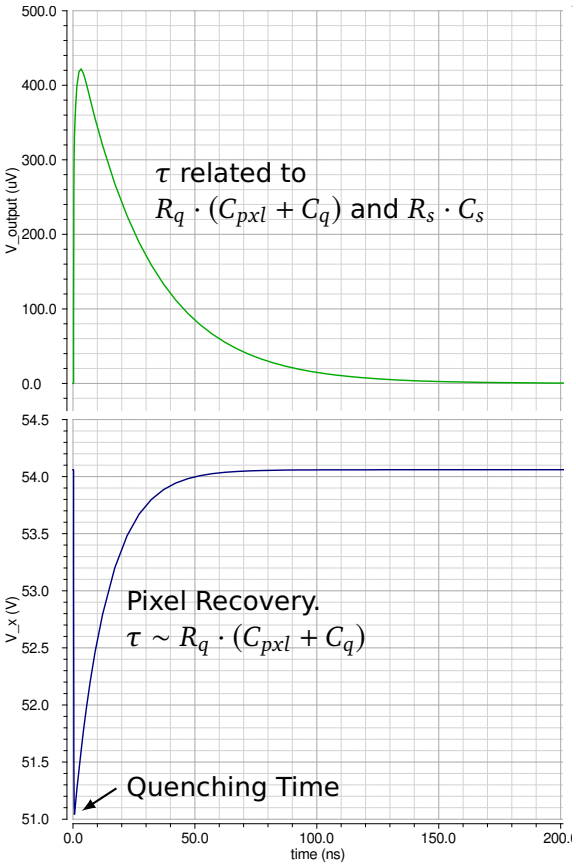
[1] The quenching resistors are realized by metal films in some device.

Table 3.1: Component parameter values for the SiPM electrical model in the simulation. Parameter values for SiPM are taken from [62].

C_{pxl}	C_q	C_s	C_{bias}	R_d	R_q	R_{bias}	R_s	N
83.88 fF	5 fF	35 pF	100 nF	1 kΩ	150 kΩ	10 kΩ	50 Ω	1600



(a) I_d(up) and V_x(down) waveforms around the quenching time.



(b) V_{output}(up) and V_x(down) waveforms.

Figure 3.8: SiPM response from simulation using the SiPM electrical model.

quenching and switch S is open. After quenching, V_x will recover to V_{bias} with a much larger time constant of $R_q \cdot (C_{pxl} + C_q)$ before C_{pxl} is recharged. The voltage at the output node V_{output} will have a tail with a time constant related to $R_q \cdot (C_{pxl} + C_q)$ and $R_s \cdot C_s$ [61]. An example SiPM repose simulated with the SiPM Model is shown in Figure 3.8. The parameter values used in the simulation are taken from [62] for S13360 3 mm × 3 mm sensor size, 50 µm pixel pitch MPPC. The values are listed in Table 3.1.

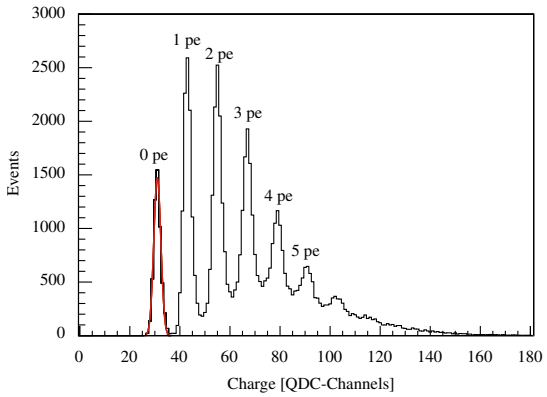


Figure 3.9: Single Photon Spectrum of a SiPM [63].

3.3 Basic Properties

3.3.1 Gain

Due to the quenching mechanism, the G-APD of the SiPM pixel will produce a fixed amount of charge in each avalanche multiplication process. The gain of SiPM is defined as the ratio of the generated charge Q_{pixel} in a SiPM pixel to the elementary charge e:

$$G = \frac{Q_{pixel}}{e} = \frac{V_{ov} \cdot C_{pxl}}{e} = \frac{(V_{bias} - V_{br}) \cdot C_{pxl}}{e} \tag{3.3}$$

where V_{ov} is the applied over voltage, V_{bias} is the bias voltage of the SiPM, V_{br} is the breakdown voltage of the SiPM and C_{pxl} is the pixel capacitance. The same as the G-APD, the gain of SiPM is in the order of $\mathcal{O}(10^6)$.

Figure 3.9 shows a typical charge spectrum of SiPM at low light intensity, which is also referred as Single Photon Spectrum (SPS). The peaks corresponding to different number of triggered pixels is clearly distinguishable. Due to the manufacture variance, the gain of each individual pixel is not uniform. This error source has contributed to the widening of individual peaks.

The gain of SiPM also fluctuates with the ambience temperature due to the temperature dependence of the breakdown voltage.

3.3.2 Photon Detection Efficiency

The *Photon Detection Efficiency* (PDE) is defined as the probability that an incoming photon triggers the SiPM to generate an output signal. It can be expressed as follows:

$$PDE = \varepsilon_{FF} \cdot (1 - P_R(\lambda)) \cdot QE(\lambda) \cdot P_G(\lambda, V, T) \tag{3.4}$$

ε_{FF} is the geometry fill factor describing the ration between the effective detection area to the

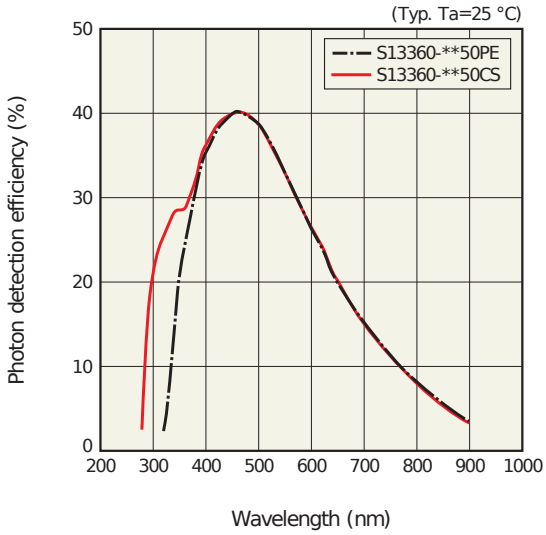


Figure 3.10: PDE vs. wavelength characteristic of the Hamamatsu S13360 series MPPC with 50 µm pixel pitch [64].

whole sensor area. Due to the dead area consumed by the quenching resistor[1], the guarding ring structure, as well as the metal bias connection, the fill factor is normally between 25 % to 80 % depending on the pixel sizes and the pixel layout scheme. For senor with larger pixel sizes, a larger fill factor usually is achieved. $P_R(\lambda)$ describes the reflection of the photon with a energy of hc/λ on the sensor surface and $(1 - P_R(\lambda))$ is the factor of the photon entrance transmittance. $QE(\lambda)$ is the wavelength dependent quantum efficiency of a pixel and describes the probability for a photon with given energy to generate an electron-hole pair in the pixel. The Geiger efficiency, P_G, describes the probability of an initial electron triggering a Geiger discharge in the pixel, which depends on the photon energy, temperature and the bias voltage.

The PDE of the sensor is wavelength, temperature, and bias voltage dependent and is significant different between different SiPM models. As shown in Figure 3.10 is an PDE characteristic of the Hamamatsu S13360 series MPPC with 50 µm pixel pitch at their recommended bias voltage and a temperature of 25 °C. At the peak sensitivity wavelength range $\lambda_p \sim 450$ nm, the PDE of these sensors reaches around 40 %. For sensors with different pixel sizes, the PDE of a sensor at peak sensitivity wavelength usually ranges from 20 % to 50 %.

3.3.3 Dark Noise

The dark noise event is an avalanche breakdown event without a photon reaching the sensor and the resulting signal is indistinguishable to the signal triggered by the absorption of a photon. The *Dark Count Rate* (DCR) is the characteristic to quantize the dark noise of a SiPM.

There are two known processed to generate the dark noise event, the thermal excitation and

[1] In some new sensor models, the quenching resistors are made from metal films which are transparent

quantum tunneling effect. The dark noise events induced by thermal excitation are triggered by the electrons which are excited from the valence band to conduction band via phonon interaction. The thermal excitation process is significant enhance by the intermediate energy levels introduced by the lattice defects and thus depends on the purity of the silicon material. This process also strongly depends on the temperature and DCR rises exponentially with the temperature of the sensor [65].

The dark noise events generated from quantum tunneling originate from the electrons in the valence band in the p-doped material tunneling across the band gap to the conduction band of the n-doped material in the avalanche region of the pixel, assisted by the strong electrical field presented in this region. The quantum tunneling process is determined by the bias voltage and independent of the temperature. It is the dominating process for dark noise events at high bias voltage.

With the development of SiPMs, the DCR has been largely reduced for the last few years. Currently, the Hamamatsu S13360 series MPPC achieve a typical DCR of ~55 kHz/mm^2 at room temperature [64]. Models with ultra low DCR of 30 kHz/mm^2 are also available [66].

3.3.4 Crosstalk

During the avalanche process in the pixel, photons in a energy range of of 0.8-2.5 eV can be generate [67]. If such photons have sufficient energy to create a electrons-hole pair, then they can be absorption in current pixel or in the neighboring pixel and initiate a new avalanche process there. A *Crosstalk* signal is generated by the avalanche process in the neighboring pixel with the absorption of an avalanche emitted photon. The creation and absorption process of such photons happens on a short time scale and the crosstalk signal can not be distinguished from the primary signal. The probability of avalanche photon emission with sufficient energy to create secondary electron-hole pair is around $1.2 \cdot 10^{-5}\ photon/e^-$ [67] and thus around 12 such photons can be generated in an avalanche process for sensors with a gain of 10^6.

The crosstalk probability increases with higher bias voltage and smaller pixel size. For higher bias voltage, more charge carriers are created in the avalanche process and the probability to initiate an avalanche breakdown is higher. Thus the number of the avalanche emitted photon with sufficient energy increases and the possibility of such a photon initiate a avalanche in the neighboring pixel increase, leading to a higher crosstalk probability. For SiPM with smaller pixel, the avalanche emitted photons are more likely to reach the neighboring pixel and initiate a avalanche process there. The crosstalk can be significantly suppressed to a few percent by adding optical trenches between pixels [62].

3.3.5 After-Pulse

After-pulsing describes the delayed secondary avalanche phenomenon. There are two known sources for the after-pulses. One source is the charge carriers trapped by the impurities of the

silicon lattice during the primary avalanche process. The trapped charge carriers is released after a certain time and could trigger a secondary avalanche. The trapping time, which is the delay of the secondary avalanche in this case, can be different for different impurities and different charge carriers. The second source is charge carriers generated by the absorption of avalanche emitted photons on the silicon substrate. These charge carriers could drift to the avalanche region and trigger a secondary avalanche there. The delay of the secondary avalanche is the drifting time of the charge carriers, which is in the order of $\mathcal{O}(10 - 100\,\text{ns})$.

If the after pulse happens during the recharging time of the pixel, the change of the after pulse is small then a full signal charge since the bias voltage of the pixel is not fully recovered.

3.3.6 Dynamic Range

After quenching of a Geiger discharge, the SiPM pixel has to recover to detect the next photon. The recovery time of the pixel is in the order of $\mathcal{O}(100\,\text{ns})$. If a second photon arrive in the pixel within a delay that is much shorter than the pixel recovery time, the pixel will be insensitivity to the second photon and the output signal is identical to the signal triggered by single photon.

Assume N_{photon} photons simultaneously and homogeneously arrive at the surface of a SiPM sensor with N_{pixel} pixels. If the N_{photon} is much smaller than N_{pixel}, the sensor output charge is proportional to the number of detected photons, as the probability of several photons hitting on the same pixel is small and the number of fired pixel N_{fired} is

$$N_{fired} = \varepsilon_{PDE} \cdot N_{photon} \tag{3.5}$$

where ε_{PDE} is the photon detection efficiency of the sensor.

With the increase of the N_{photon}, the sensor will not repose linearly with N_{photon} as the probability that two or several photons are absorbed in the same pixel goes higher. This leads to the saturation effect of the sensor and N_{fired} is given by:

$$N_{fired} = N_{pixel} \cdot (1 - e^{-\frac{N_{photon} \cdot \varepsilon_{PDE}}{N_{pixel}}}) \tag{3.6}$$

3.3.7 Timing Measurement

Due to the fast avalanche development during Geiger discharges, SiPMs has shown great potential in the timing measurement for particle detection. *Leading edge discrimination* (LED) are commonly used to mark the arrival time of the SiPM signals with the time stamps when the SiPM signals passes the threshold.

Shown in Figure 3.11 is the two timing error sources for the leading edge discrimination, *time walk* and *time jitter*. Time walk is the timing variation due to different signal amplitudes. The discrimination threshold is typical set above the baseline of the SiPM to avoid noise triggering.

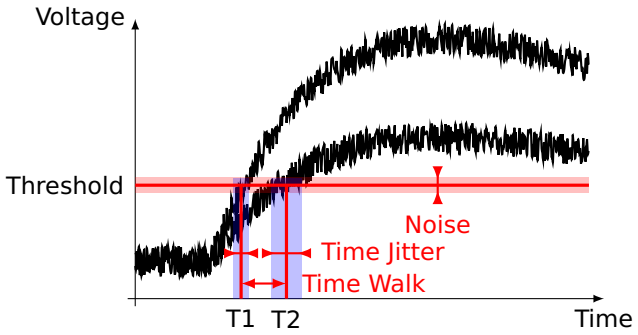


Figure 3.11: Timing errors with leading edge discrimination.

Thus the time intervals for SiPM signals to develop and to pass the threshold are different for signals with different amplitudes. The signals with larger amplitudes trigger earlier than the signals with smaller amplitudes. The time walk can be corrected with the signal amplitude information.

Time jitter is the statistic time stamp fluctuation due to noise in the system. The time jitter σ_t is determined by:

$$\sigma_t = \frac{\sigma_v}{\mathrm{d}(v(t))/\mathrm{d}t} \tag{3.7}$$

where σ_v is the total noise in the system and $\mathrm{d}(v(t))/\mathrm{d}t$ is the slop of the SiPM signal at the discrimination point.

There are different sources contribute to the total system noise σ_v, such as the statistic fluctuation of the charge carrier creation and initiation of the avalanche, the fluctuation of avalanche buildup process, as well as the noise on the quenching resistor and in the readout electrics. The baseline fluctuation due to the pipe-up effect of the dark count noise also contribute to the σ_v and degrades the time jitter at high bias voltages.

The slop $\mathrm{d}(v(t))/\mathrm{d}t$ is determined by the speed of the avalanche development, the detector parasitic, the bandwidth of the readout electronics, as well as the number of photons arrived at the sensor surface before the discrimination time. A more detailed discussion on the SiPM timing performance can be found in [61].

Chapter 4

Introduction to CMOS Technology and Digital Logic Circuit

Application Specific Integrated Circuits (ASICs) have been wildly used for the readout of the detectors in the high energy physics experiments and medical imaging system, especially for system with large number of signal channels. ASIC is able to accommodating a large number of readout channels in miniaturized sizes with low cost per channel and low power consumption compared to the readout circuit with discrete components. Moreover, the readout circuit can be put close to the detector due to the miniaturized size of the ASICs. This will minimize the parasitic capacitance on the connection of the detector and the readout electronics, which helps to improve the timing performance of the detector channel and to reduce the noise on the input of the readout electronics.

Complementary Mental Oxide Semiconductor (CMOS) is a commonly used technology to construct the readout ASICs for radiation detection detectors, due to its advantages of low cost, low complexity, relatively low power consumption, high integrated density as well as being capable of combining analog circuit and digital circuit on the same chip.

In this chapter, the basic component to build ASICs in CMOS technology will be described and the building blocks for the digital circuit will be introduced.

4.1 CMOS Technology

Metal oxide semiconductor field effect transistors (MOSFETs) are the basic components in CMOS technology. In analog circuit design, MOSFETs, together with other components like resistors and capacitors, are manually selected, parameterized and placed to build circuit with desired signal processing functionality and performance. In the digital logic circuit, the basic logic gates are also built up with MOSFETs.

4.1.1 MOSFET

CMOS technology provides both p-types and n-types MOSFET transistors. As shown in Figure 4.1 are the circuit symbol and the structure of n-type MOSFET transistor (NMOS). It has four con-

nection terminals: bulk (B), gate (G), source (S) and drain (D). The bulk connection provides the potential for the p-doped silicon substrate. It is realized by a high p-type doping region connected to a mental contact. The source and drain are made by high n-type doping regions contacted with metal interfaces. The gate terminal is constructed by a layer of polycrystalline silicon and a layer silicon dioxide on top of the silicon substrate.

MOSFET transistor controls its conductivity between source and drain by the voltage between gate and source V_{GS}. It can operate in three different mode depends on the voltages applied on the, gate, source and drain terminals. Bulk terminal is usually connected to ground potential for the functioning of the NMOS transistors.

When V_{GS} is less than threshold voltage of transistor V_{TH}, the transistor is turned off and there is no conductivity between the drain and the source. This operation mode is called *subthreshold Mode*.

When $V_{GS} > V_{TH}$ and $V_{DS} < (V_{GD} - V_{TH})$[1], the transistor is turned on and a conductive channel is created allowing current to flow between the source and the drain. Such operation mode is referred as *triod mode*.

In this working mode, the current between drain and source I_D is given by:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \tag{4.1}$$

where μ_n is the mobility of electrons, C_{ox} is the capacitance of the oxide layer per unit area, and W, L are the width and the length of the channel created between the drain and the source, respectively.

When $V_{GS} > V_{TH}$ and $V_{DS} > (V_{GD} - VTH)$, the transistor is turned on and a conductive channel is created. As V_{DS} is sufficiently high and V_{GD} is less then V_{TH} in this case, the conductive channel is pitched off at the drain terminal. Although the conductive channel is pitched off and does not extended to the full length between the source and the drain, the electrical field between the channel and the drain is high enough such that the electrons can still reach the drain terminal and the conduction continues. This operation mode is called *saturation mode*.

For transistor operated the saturation mode, the current between the drain and the source only weakly depends on the V_{DS} and is primarily determined by the V_{GS}:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \tag{4.2}$$

where λ is the channel length modulation coefficient to describe the modulation effect of V_{DS} on the length of the channel and in turn on the channel current. As λ represents the relative variation on the channel length, λ is small for long channels.

[1] This is equivalent to $V_{GD} > V_{TH}$

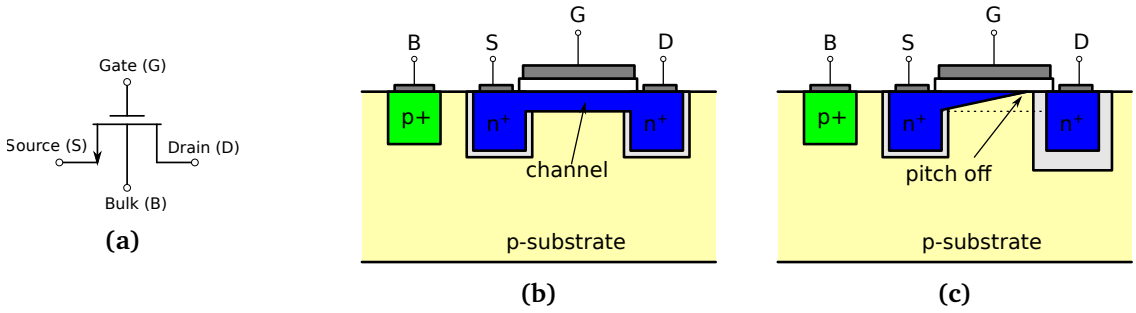


Figure 4.1: (a) Circuit symbol of a NMOS transistor. **(b)** Cross-section of a NMOS transistor operating in the triode mode. **(b)** Cross-section of a NMOS transistor operating in the saturation mode.

A key parameter of the transistor, the transconductance, can be obtained by:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{4.3}$$

Neglecting the channel length modulation for long transistors, we have

$$g_m \approx \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \tag{4.4}$$

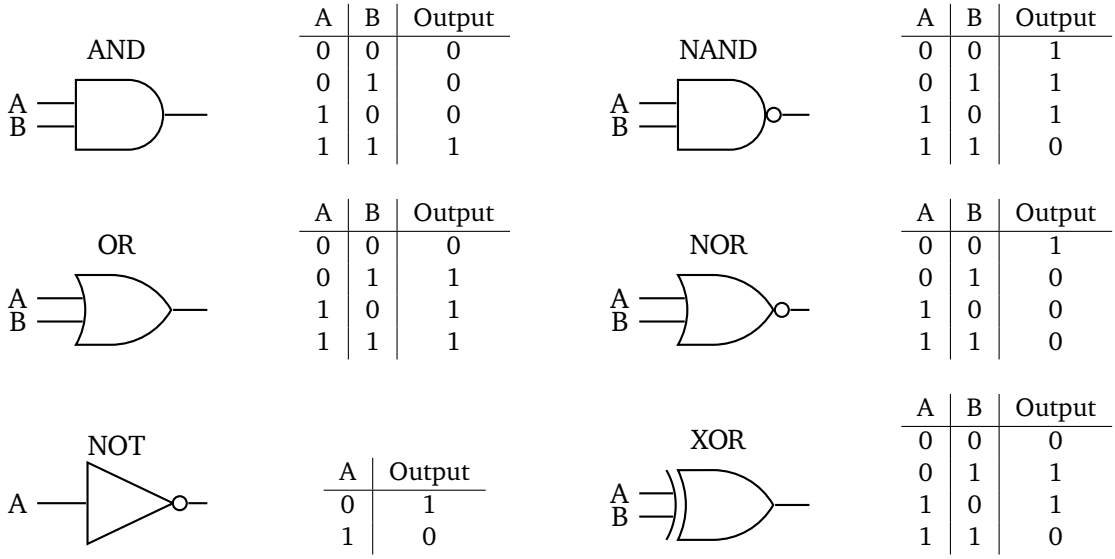
The saturation mode is usually the preferred mode in analog signal processing circuits. Various amplifiers are designed with the transistors working in the saturation mode. More details about CMOS technology and analog circuit design can be found in several textbooks, such as [68, 69].

4.2 Digital Logic Circuit

The analog circuits work with continues variable current or voltage signals. The digital logic circuits operate with on digital logic signals which have usually two levels and present the one binary bit data (`'0'` or `'1'`) at any given time.

In the detector readout ASIC, the digital logic circuit performs various tasks simultaneously. It processes the data signals from the digitization of the analog signals, provides signals to control the operating mode of the analog circuit modules, as well as buffers the data and provides interfaces to communicate with the external data acquisition system and control system.

The digital logic circuits are made from transistor fundamentally. However, the complexity of the digital logic design prevents manually placing of the transistors. Instead, in the digital design the circuit are described in the register-transfer level (RTL), which model the circuit by describing the digital signal flow between the register elements and logic operation on the digital signals.



A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

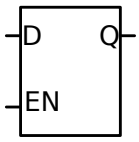
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

A	Output
0	1
1	0

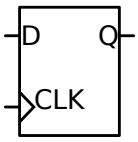
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

Figure 4.2: Circuit symbols and truth tables of commonly used logic gates.



EN	D	Q
0	X	No change
1	0	0
1	1	1

Figure 4.3: Electronic symbol and truth table of a D-latch.



Clock	D	Q
Rising edge	0	0
Rising edge	1	1
Non-Rising	X	No change

Figure 4.4: Circuit symbol and truth table of a flip-flop.

4.2.1 Logic Gates

Logic gates are the fundamental element in the digital circuits and perform boolean logic operation on the digital logic signals. The true tables describe the response of the logic gates. Figure 4.2 shows the electronic symbols and the true tables of six types of commonly used logic gates: AND, OR, NOT, NANT, NOR and XOR gate.

4.2.2 Latches and Flip-Flops

Latches and flip-flops are the register elements in the digital logic circuit and used for store information.

A latch is a level sensitive data storing device. Latches are of different types and implementations. A D-latch is based on the gated set-reset latch (SR latch) with a data (D) input and an enable (EN) input. Figure 4.3 shows the circuit symbol and the true table of a D-latch. Whenever enable line is high, the latch outputs what its input D is. When enable line is low, it outputs what the input D was when the enable line was high last time. D-latch is asynchronous device as its output doesn't aligned with the edges of a clock signal.

A flip-flop is a synchronous device and it is sensitive to the edges its clock input port. The

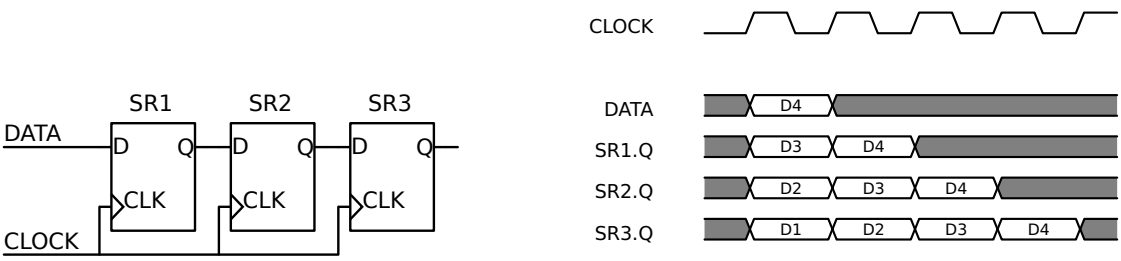


Figure 4.5: Schematic and timing diagram of a shift register with three flip-flops.

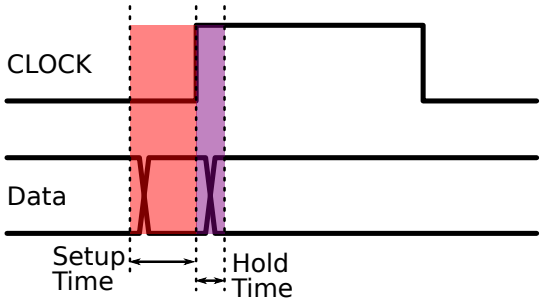


Figure 4.6: Setup time and hold time violation.

symbol and the true table of a flip-flop is shown in Figure 4.4. The flip-flop has two inputs, the data (D) input and clock (>) input. It will only change its output to what its D input is when a rising edge of `clock` signal arrives. Flip-flops are the essential part of the sequential digital logic circuits. For example, they can be used as memory devices to store the state information of the finite state machine. Flip-flops are also the basic elements of shift-registers, which are the essential part of many devices. Figure 4.5 shows a simple shift-register made up with three flip-flops connected in series. At each clock tick, the data stored in the flip-flops are shifted to the right one by one.

The input signal at the `data` input of a flip-flop must be hold steady within a time interval around the rising edge of the clock signal such that the input data is reliably sampled. The minimum length of time the data input signal should be held steady before the rising edge of the clock signal is called *setup time*. The minimum length of time the data input signal should be held steady after the rising edge of the clock signal is called *hold time*. Violation of the setup and hold time can result in unpredictable behaved output, called *metastable state* of the flip-flop. An example of setup and hold time violation is shown in Figure 4.6.

During the ASIC physical implementation, Static timing analysis (STA) is used to calculate the delay on each net of the circuit and validate the timing of the circuit.

Chapter 5

MuTRiG Chip Design

The MuTRiG (**Mu**on **T**iming **R**esolver **i**ncluding **G**igabit-link) ASIC is developed for the readout of Silicon Photomultipliers for applications in the High Energy Experiments (HEP) which require extremely high timing resolution and high event rate capability. It is dedicated to the readout of the timing detectors in the Mu3e experiment, where both high timing resolution and high event rate capability are required. The MuTRiG ASIC is the successor of STiCv3 chip [8, 9], the mixed-signal SiPM readout ASIC developed in the framework of EndoTOFPET-US project [70]. The timing resolution of the STiCv3 chip is good enough for the timing measurements in the Mu3e experiment. However, the chip is only capable of transferring ~40 kHz/channel through the 160 Mbit/s data link, which is too slow for the Mu3e timing detectors, especially for the fibre detector. The goal of the MuTRiG development is to provide high event rate capability and preserving the high timing resolution from STiCv3 at the same time.

The good timing resolution of STiCv3 benefits from its differential analog front-end and the 50 ps binning time-to-digital converter (TDC). The same analog front-end and TDC were implemented in the MuTRiG chip for the aim of preserving good timing resolution. A double data rate serializer and a customized low-voltage differential signaling (LVDS) transmitter were developed for establishing a gigabit data link with the Data Acquisition system (DAQ) for data transmission. The hit event data can also be switched to a short length to further increase the maximum output event rate of the chip. A few more new functionalities were implemented in the digital logic circuit of the MuTRiG chip for convenient and reliable operation of the chip. A MuTRiG prototype ASIC has been produced in spring 2017 and was characterized since then.

The development and the characterization of the STiCv3 ASIC was a collaborative effort of a group of people [8] and was also done as part of this thesis. However, the design of the MuTRiG ASIC was performed only by the author and it is the newest generation of the timing chips family. Therefore, this chapter will only present the design of the MuTRiG prototype chip.

The analog front-end and the TDC, which are the same modules from the STiCv3 chip, will be firstly briefly introduced. Then the digital logic circuit of the MuTRiG ASIC will be detailed explained. In the last section of this chapter, the physical implementation and the verification performed for this prototype ASIC is also presented.

5.1 Design Requirements

During phase I operation of the Mu3e experiment, the accidental background has to be suppressed below the level of $2 \cdot 10^{-15}$ in order to observe the $\mu^+ \longrightarrow e^+e^+e^-$ process with target sensitivity of $2 \cdot 10^{-15}$. This requires to suppress the background suppression by more than two orders of magnitude with the timing measurements from the fibre and the tile detectors. In oder to achieve required accidental background suppression factor and in the same time keep the signal acceptance close to 100 %, the fibre and tile detector are required to provide timing measurements with a resolution of 500 ps and 100 ps respectively. MuTRiG should provide low jitter and high precision measurements together with the fibre and tile detector to achieve the required timing resolution.

As ~1000 photons are expected to be detected for the hit events in the tile detector and the hit signals are much larger than DCR signals, the threshold of the readout electronics can be set above DCR signal level in order to avoid the triggering of the dark noise events without degrading the detection efficiency. The maximum hit rate on the tile SiPM detector channels are less than 60 kHz/channel [51], which will be the maximum event rate for the readout electronics of the tile detector. However, only a few photons are detected in the photon sensors of fibre detector. The threshold of the readout electronics has to be put below the DCR signal level to achieve a higher detection efficiency and a better timing resolution. The hit rate on the fibre SiPM channels are expected to be ~720 kHz/channel including the DCR of ~300 kHz from each SiPM channels before irradiation [71]. The DCR of SiPMs will increase after irradiation and MuTRiG is required to handle 1 MHz/channel event rate to achieve 100 % data acquisition efficiency for the readout of the fibre detector.

5.2 MuTRiG Channel

An excellent measurement of the arrival time of the electrons from the muon decays is crucial for both fibre and tile detectors in order to provide the required suppression of the accidental background. Although the energy information of the events is not used for event reconstruction of the signal event, it can be used to improve the timing resolution of the Mu3e tile detectors by applying a time-walk correction to the measured time stamps [51]. For the Mu3e fibre detector, the demand for sufficient output event rate and the difficulty to achieve enough energy resolution at the low signal level have surpassed the benefit of the time walk correction. Thus the energy information is omitted and will not be sent out for the Mu3e Fibre detector in order to save the bandwidth of the output data link.

The MuTRiG chip provide the time of arrival information with a fast discriminator for leading edge discrimination and a fine bin size TDC for generating the time stamps of the discrimination signal. The energy of the event is measured with a linearized Time-over-Threshold method [61], where the same TDC is used to generate the time stamp of the falling edge of the discriminator

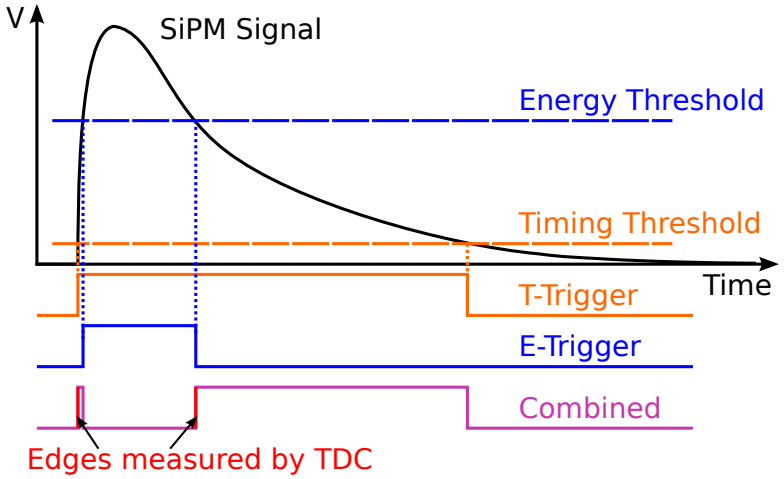


Figure 5.1: Trigger principle of the MuTRiG channel.

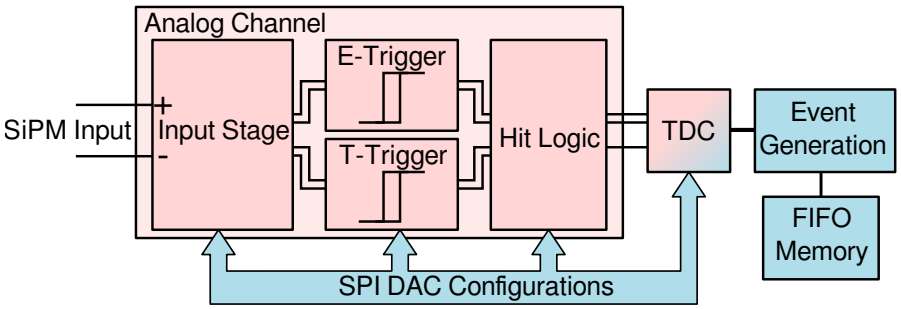


Figure 5.2: Diagram of a MuTRiG channel.

output signal. In this way, both the time of arrival information and energy information of the event can provided without additional analog to digital converter (ADC) circuit which otherwise would complicate the channel design and might take up a lot of chip area and increase the power consumption of the chip.

The readout principle of MuTRiG is shown in Figure 5.1. The SiPM signal is discriminated with two different thresholds, one threshold for time of arrival measurement and one for energy measurement. The two trigger signals from the discriminators are combined into one signal, encoding the rising edge of the timing trigger signal and the falling edge of the energy trigger signal into two rising edges of a combined signal which can be processed by the TDC. The time of arrival information can be obtained from the timing measurement of the first rising edge. The energy information of the event can be presented by the time difference between two rising edges of the combined signal.

Figure 5.2 shows the channel diagram of MuTRiG. The SiPM current signal is taken by the input stage of the analog front-end. After the input stage, two signals are provided to the timing branch and energy branch for time and energy discrimination. The discrimination signals from the timing and the energy branch are encoded in the hit logic module to generate the combined

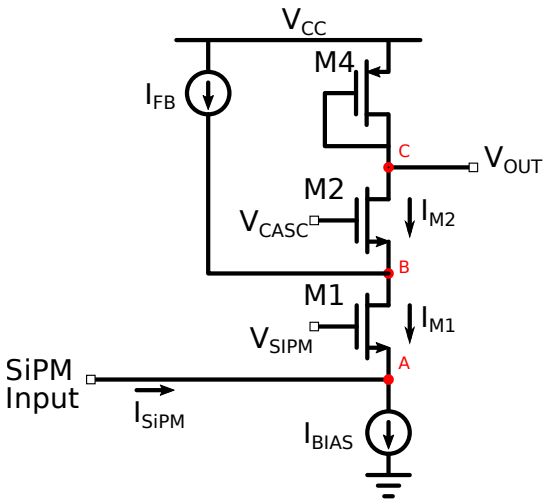


Figure 5.3: Schematics of one half of the MuTRiG input stage.

hit signal discussed in the previous paragraph. The TDC monitors the combined hit signal and generates the time stamps for each rising edge of the hit signals. The on-chip event generation logic then combines the digitized time stamps from the TDC module into full hit information data including the time and energy information, which will be buffered on the on-chip memories and later transfered out of the chip. The analog front-end, TDC and digital modules are configured using a Serial Peripheral Interface (SPI) interface.

5.3 Analog Front-End

The analog front-end is designed in a fully differential structure to suppress the common-mode noise from the external sources and the on-chip digital circuit. It consists of input stage, timing branch, energy branch and hit logic unit. Both timing branch and energy branch contain amplification stages and discriminators.

Input Stage

The input stage buffers the input current signal from the SiPMs for the following signal processing blocks. It provides a low input impedance to take in the SiPM signals, generates the output voltage signals for the timing branch, and permits to adjust the DC voltage at the input terminal in a range of 900 mV which allows to compensate for differences of the optimum SiPM bias voltage level on per channel bases.

The input stage is designed in a fully different manner, and Figure 5.3 shows one half of the differential circuit. It based on a common gate transistor $M1$ with low frequency current feedback.

Applying Kirchhoff's current law to the node A, B and C, we have

$$I_{BIAS} = I_{SiPM} + I_{M1} \tag{5.1}$$

$$I_{M1} = I_{FB} + I_{M2} \tag{5.2}$$

$$I_{M2} = I_{M4} \tag{5.3}$$

where I_{BIAS} is the tail bias current; I_{SiPM} is the current flow from the sensor to the input of the MuTRiG channel; I_{M1}, I_{M2} are the current flow though transistor $M1$ and $M2$ respectively; I_{FE} is the low frequency feedback current.

Combining above equations, the current through transistor $M4$ is given by

$$I_{M4} = I_{BIAS} - I_{FB} - I_{SiPM} \tag{5.4}$$

I_{BIAS} is constant and I_{FB} is also constant because of the low frequency response with respect to the signals discussed here. If we differentiating both side of Equation 5.4 with respect to ∂I_{SiPM}, we can get:

$$\partial I_{M4} = -\partial I_{SiPM} \tag{5.5}$$

The diode connection of M4 gives rise to a voltage swing at the output node V_{OUT} when a signal current is injected to the channel. At first order, the transconductance of the transistor M4 gives the inverse impedance at this node, and thus the voltage swing:

$$g_{M4} = \partial I_{M4} / \partial V_{GS,M4} \tag{5.6}$$

$$V_{GS,M4} = VCC - V_{OUT} \tag{5.7}$$

Then we have:

$$\partial I_{M4} = -g_{M4} \partial V_{OUT} \tag{5.8}$$

Thus the small signal output voltage swing is given by

$$v_{OUT} = \partial V_{OUT} = \frac{1}{g_{M4}} \partial I_{SiPM} = \frac{1}{g_{M4}} i_{SiPM} \tag{5.9}$$

A smaller input impedance will help with the jitter performance by increase the slop of the input signal [8, 61]. The MuTRiG input stage is designed such that the input impedance of the

input stage is stable over the full frequency range:

$$R_{IN} \sim \frac{1}{g_{m,M1}} = \frac{1}{\sqrt{2 \cdot \mu_n C_{ox} \frac{W}{L} I_{M1}}} \tag{5.10}$$

$$= \frac{1}{\sqrt{2 \cdot \mu_n C_{ox} \frac{W}{L} (I_{BIAS} - I_{SiPM})}} \tag{5.11}$$

where R_{IN} is the input impedance of the input stage, $g_{m,M1}$ is the transconductance of the transistor $M1$ and μ_n is the mobility of the electrons in the transistor. A large tail bias I_{BIAS} has been used in the input stage to achieve a low impedance.

In a large system, the bias voltage of the SiPMs are generated commonly for several sensors, prohibiting to set the optimum bias voltage for each SiPM individually. The input stage also provides the possibility to fine tune SiPM operation voltage individually to its optimum bias voltage by changing the V_{SiPM} at the gate of the transistor $M1$. It can be also used to compensate the SiPM breakdown voltage fluctuation due to temperature variation. The bias voltage V_{SiPM} is generated by a Digital-to-Analog Converter (DAC).

Note that

$$I_{M4} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (VCC - V_{OUT,OFFSET} - V_{TH})^2 \tag{5.12}$$

where μ_p is the mobility of the holes in the transistor, C_{ox} is the gate oxide per unit area and W, L are the width and the length of the transistor channel.

The operating point (i.e. the DC voltage at the output node) is defined by the constant tail bias current I_{BIAS} and the feedback current I_{FB}. Neglecting I_{SiPM} for the analysis of the operation point and putting Equation 5.12 with Equation 5.4, the output signal offset $V_{OUT,OFFSET}$ is given by

$$V_{OUT,OFFSET} = VCC - V_{TH} - \sqrt{\frac{2(I_{BIAS} - I_{FB})}{\mu_p C_{ox} \frac{W}{L}}} \tag{5.13}$$

In the previous discussion, only the half circuit of the input stage was considered. By introducing a current difference between the differential I_{FB} pair, also the output voltage offset difference for the differential input stage is set, which will define the threshold for the time discrimination branch connected to the input stage.

Timing Branch

The block diagram of the timing path is shown in Figure 5.4. It consists of a amplification block and a discrimination block. The threshold for the discriminator block, $V_{T\_threshold}$, is the offset

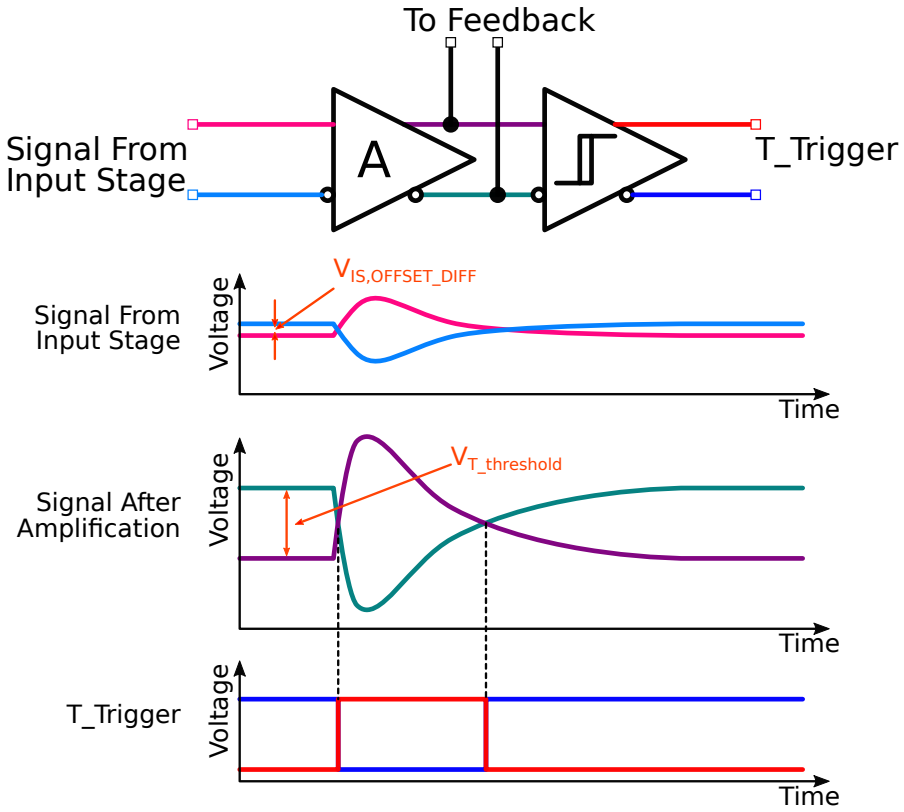


Figure 5.4: Diagram of a MuTRiG timing brach.

difference between its two inputs, which comes from the amplification of offset difference of the input stage output signals ($V_{IS,OFFSET\_DIFF}$). The threshold range is designed to be very low in order to trigger on the first or second photo electrons (p.e.). In fact, the threshold can be configured to both polarities and over a range of 0 to ~ 4 p.e. for Hamamatsu 3 mm × 3 mm area, 50 µm pitch MPPC under norminal operating voltages. When the input voltage difference of the discriminator is close to zero, small noise on the input signals might change its output rapidly and cause glitches on the discriminator output which need to be masked from the TDC. An internal hysteresis with positive feedback has been implemented in the discriminator such that the discriminator will not be sensitive to such noise [61].

Energy Branch

The block diagram of the energy branch is shown in Figure 5.5. It selects one of the differential amplified SiPM signal and uses a pulse shaper stage to shape the selected signal to a smooth triangle-like shaped signal. The shaped signal is then compared with a voltage threshold with a amplifier and a discriminator. The energy threshold is provided by a linear voltage DAC ranged from 0 V to *VCC* (1.8 V). Also in the case of the energy measurement discriminator, positive feedback is utilized to obtain a hysteresis to mask noise triggers on the energy discriminator

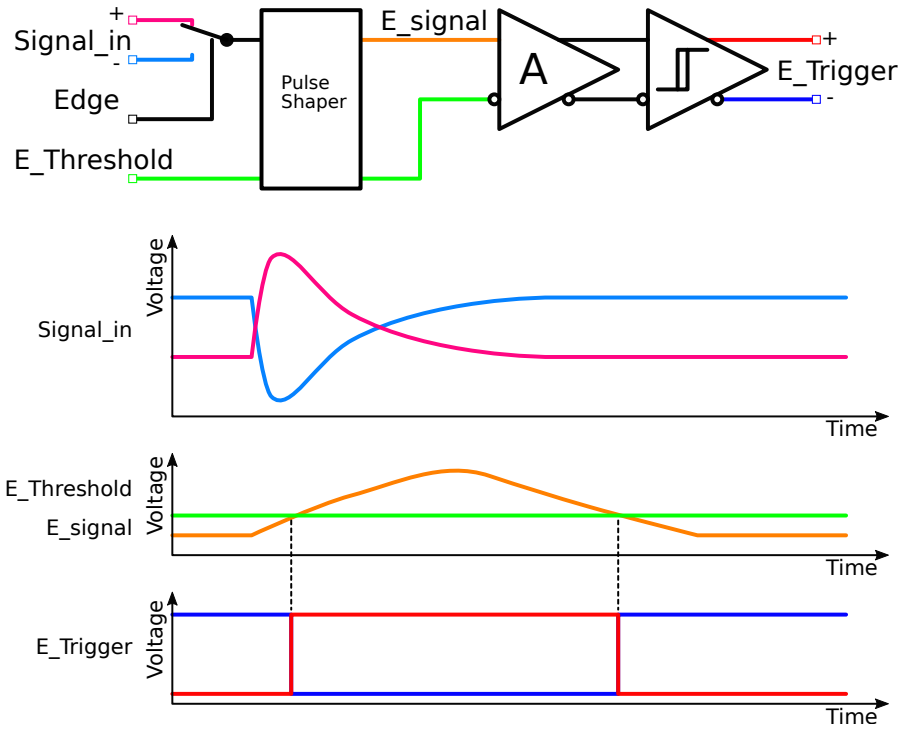


Figure 5.5: Diagram of a MuTRiG energy branch.

output.

A linearized Time-over-Threshold(ToT) method is implemented for the energy measurement [61]. The energy information of the hit particles can be referred from the charge of the SiPM signals. When the SiPM charge is large enough, the SiPM input signal will saturate the input stage and be cut off such that the charge of the SiPM signal will be discharged with a constant tail bias current of the input stage I_{BIAS}. Therefore, the width of the SiPM input signal, which is the discharging time of the change from the SiPM, is then linearized to the charge of the SiPM signal. The width of the SiPM signal seen by the readout channel is then measured by the ToT method. The linearization of the hit signal starts only when the SiPM signal charge is large enough. The pulse shaper stage stretches incoming signals to the same shape for both the linearization or before linearization cases in order to improve the overall linearity of the energy measurement. The pulse shaper stage can be turned off and the original incoming signals will be amplified and discriminated.

Hit Logic Unit

The Hit Logic unit combines the discrimination outputs from the timing and energy branch (called `T_Trigger` and `E_Trigger` signal respectively) into one signal (called `Hit_Signal`) such that only one TDC is required for the timing measurements for both time of arrival and energy information.

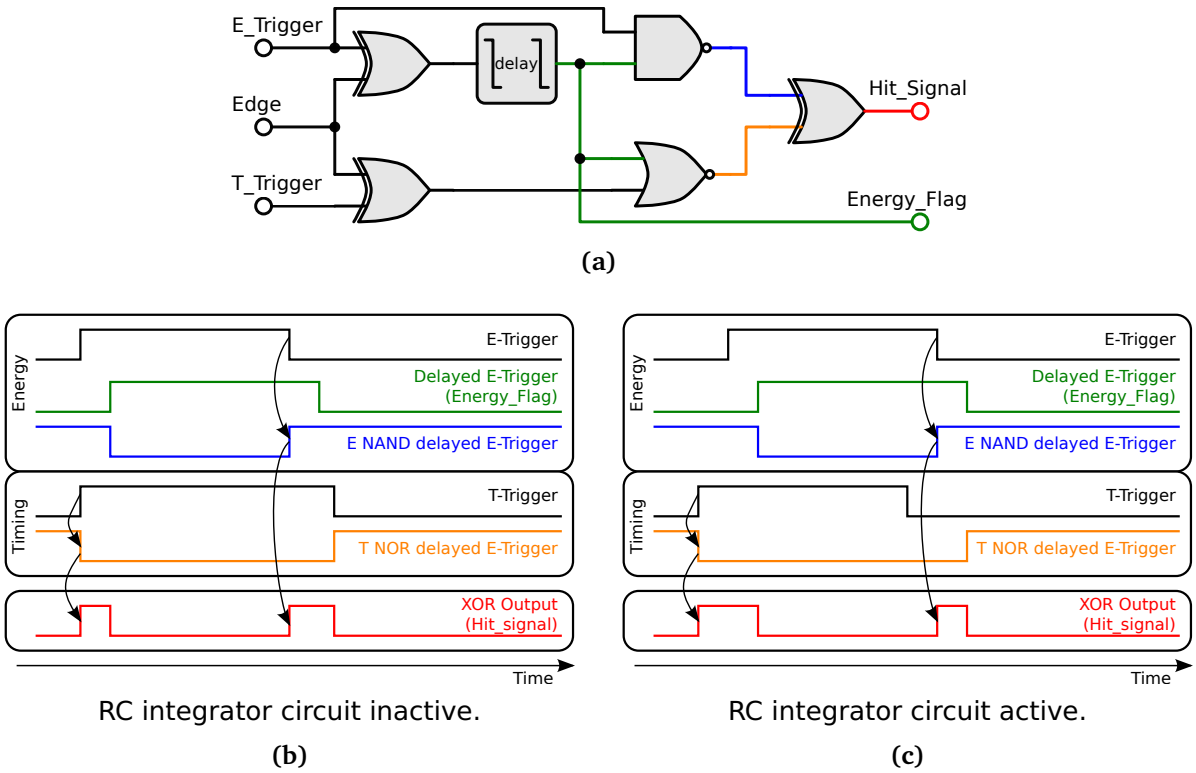


Figure 5.6: Signal processing in the MuTRiG hit logic unit.

While the TDC is sensitive only to the rising edges, the rising edge of the `T_Trigger` signal and the falling edge of the `E_Trigger` signal need to be sample to extract the arrival time and energy information. The hit logic unit generates a common `Hit_Signal` with the two rising edges and an energy flag signal asserted only while sampling the falling edge of the `E_Trigger` signal. The common `Hit_Signal` is generated by XOR combination of the discriminator output signals. Since the rising time of the SiPM signal is very short and the rising edges of the `T_Trigger` and `E_Trigger` signals are very close, the width of the first pulse is too short to trigger the operation in the TDC, in particular when the pulse shaper stage in the energy branch is disabled. On the other hand, when the pulse shaper stage is active, the `E_Trigger` signal might be longer than the `T_Trigger` signal and the resulting XOR combination signal would only preserve the rising edge and falling edges of the `T_Trigger` signal but not the falling edge of the `E_Trigger`.

Therefore, the signal processing unit as shown in Figure 5.6a is use, where a delay cell, a NAND gate and a NOR gate are used before the output XOR gate. Figure 5.6b and Figure 5.6c shows the signal logic processing in the hit log unit for both pulse shaper stage active and inactive cases. The NAND gate and NOR gate works together to make sure that the falling edge of the `E_Trigger` can be recorded correctly. The delay cell provides 15 ns to 20 ns delays to extend the width of the first and second pulse on the `Hit_Signal` for the two cases respectively. The delayed `E_Trigger` is used as the `Energy_Flag` to indicate the rising edge of the energy measurement.

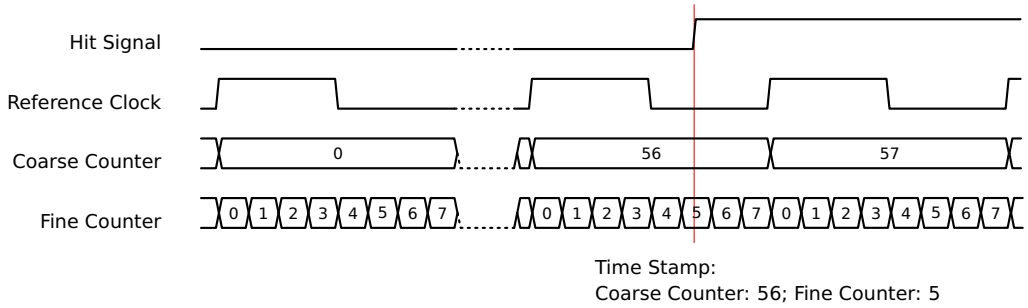


Figure 5.7: Working principle of the TDC.

The XOR gates connected to the Edge signal act as controllable inverters to to provide correctly `Hit_Signal` polarity for the case when the SiPM is negative biased.

All the cells in the hit logic unit are designed in differential Current Mode Logic (CML). This implementation has the benefit of a good rejection of noise on the digital power supply nets while minimized the injection of switching noise to the latter. A downside of the CML logic implementation is the increased static power consumption compared to CMOS logic, which is however not of major concern for this application. Compared to the PLL used for the TDC and the amplifiers in the timing branch of the front-end, the power consumed by the hit logic is still small.

5.4 Time to Digital Converter

The time of arrival information of the hit signals are digitized by the on-chip Time-to-Digital Converter (TDC) modules. The working principle of a TDC is shown in Figure 5.7, the TDC module samples the state of a counter incremented with a reference clock (coarse counter) at the arrival of a hit signal. Each reference clock interval can be sub-quantize for higher time digitization resolution. Fine counter values is then generated for measuring the time interval between the start time of a reference clock and the arrival time of the hit signal. The coarse counter values and the fine counter values are recorded as the time stamp of the hit signal.

The schematic of the TDC module is shown in Figure 5.8. It consists of a global TimeBase unit and latch units in each readout channel (TDC channel) . The global TimeBase unit provides the common coarse counter and fine counter values to all the channels for time stamping. And the latch units in the channels record the counter values from the TimeBase unit upon the arrival of a hit signal. The recorded counter values are then read as time stamps by the digital logic circuit of the chip, which also takes care of a proper reset of the latches after the digital time stamps has been sampled by the digital logic circuit of the chip.

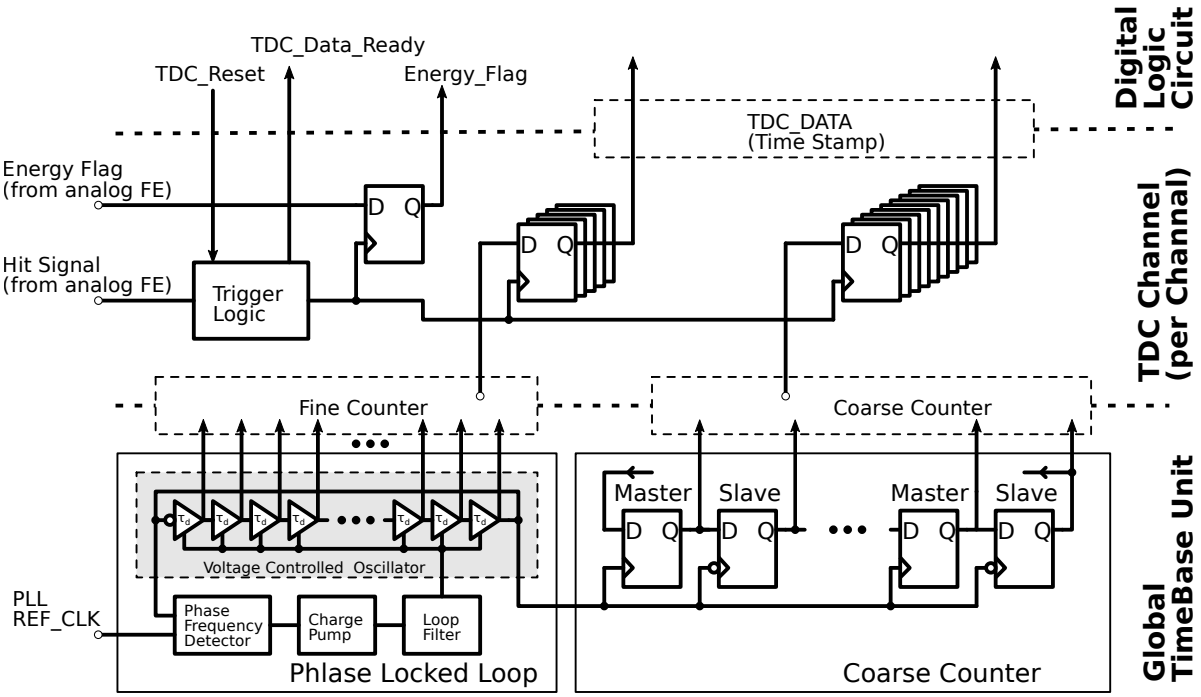


Figure 5.8: Schematic of the TDC in MuTRiG. Re-drawn from [8].

TimeBase Unit

The TimeBase unit is built from a phase-locked loop (PLL) driving two sets of coarse counters.

The PLL generates a stable clock signal for timing measurements It consists of a Voltage Controlled Oscillator (VCO) connected in a feedback loop. The output clock frequency of the VCO can vary and is controlled by a bias voltage and regulated by the feedback loop in the PLL. The feedback loop, which consists of a Phase Frequency Detector (PFD), a Charge Pump (CP) and a Loop Filter, compares the phase of the VCO output clock with an external reference clock at every clock cycle and generated the control bias voltage for VCO such that the VCO output clock is locked in-phase with the stable external reference clock. Furthermore, the VCO output clock frequency is also made unaffected from rapid disturbance on the clock as well as the power voltages or ground potential with the help of the feedback loop. In this way, a low-jitter clock which has the same frequency as the external clock is generated and its frequency is invariant under process, voltage and temperature variation.

As shown in Figure 5.9, VCO is built from 16 delay cells connected in a ring with the inversion of the output of the last cell connected to the input of the first cell to introduce the positive feedback loop necessary to create the oscillation behavior. The output of the 8th delay cell in the circuit is taken as the output clock signal. (In Figure 5.8 and Figure 5.9, the output of last cell is take as clock output for illustration.) With either logic `'0'` or logic `'1'` propagating through the delay cells, there are in total 32 VCO states in one clock cycle. The time interval of each VCO state lasts is given by the propagation delay of each delay cells, controlled by the control bias generated by

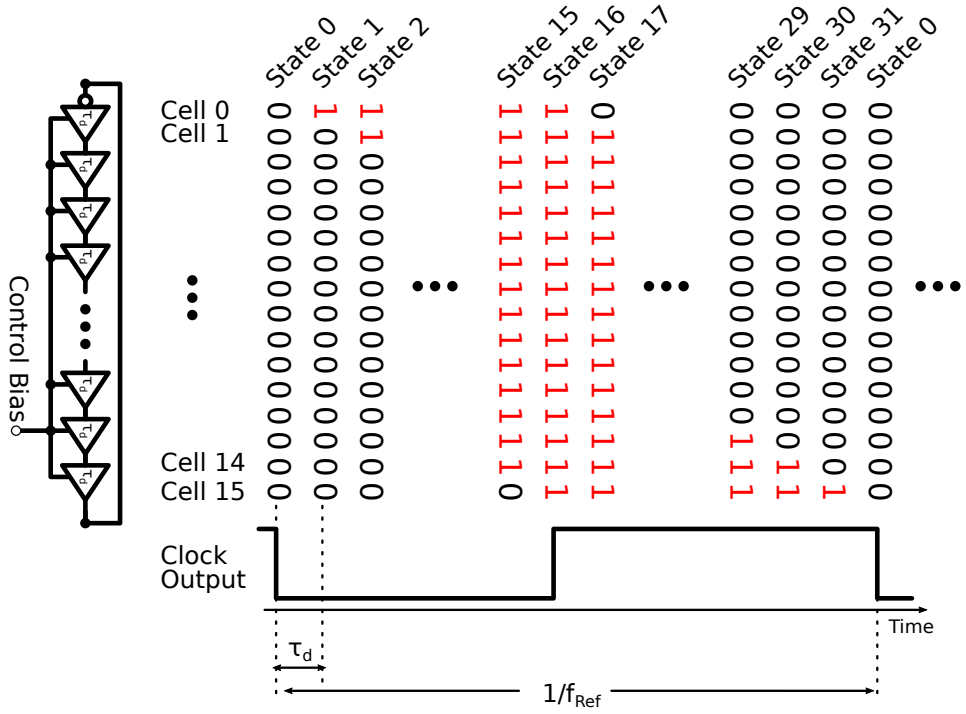


Figure 5.9: Working principle of the VCO cell.

the feedback loop. In the locked state of the PLL, the average propagation delay of the delay cells is controlled such that $< \tau_d >= 1/32 \times 1/f_{Ref}$. In this way, each period of the reference clock is subdivided into 32 fine bins by the VCO states. And the VCO states are used as fine counter values for timing measurements.

The coarse counters is driven by the VCO output clock and count the number of cycle of VCO clocks as coarse counter values. They are implemented by 15-stage Linear-Feedback shift register (LFSR) which is fast enough to work with 625 MHz VCO output clock. The LFSR is designed in a way that the LFSR runs though a deterministic order of $2^{15}-1$ states repetitively. The LFSR states will be decoded into successive counter values in the later data processing stage by mapping the LFSR states to its sequences number. The LSFR output is not stable at the time LSFR is changing from one state to the next state.

Two coarse counters have been implemented in the TimeBase Unit in order to provide valid timestamps at any moment. For a single counter, the output is invalid during the short period when the counter is changing from one state to the next state. One reason is that the output of the counter is not stable for a short time interval due to the fact that not all the flip-flips in the LSFR are switch at the same time. It takes certain time for all the flip-flops to be stable. The other reason is that the counter output should fulfill the setup- and hold-time constraints of the latch units in the TDC channel. The change of counter output within the setup- and hold-time of the latch units will not be registered correctly. Using two coarse counters, *master* coarse counter and *slave* coarse counter which change its state at the rising and falling edge of the VCO output clock

respectively, it is ensured that at least one counter has valid output at any moment. Both master and slave coarse counter values are latched by the latch unit in the TDC channel and the valid coarse counter value is selected according to the fine counter value in the digital logic circuit on the chip.

TDC Channel

There is a TDC channel at each SiPM readout channel. It records the fine counter and coarse counter values once there comes a hit signal from the analog front-end. As shown in Figure 5.8, a trigger logic monitors the hit signal from the analog front-end and generates a hit output, whose rising edge triggers the latching operation of the fine counter and coarse counter values from the TimeBase Unit. The energy flag from the analog front-end is also registered in the same time. The trigger logic generates a `TDC_Data_Ready` signal for data processing in the digital logic circuit. Once the digital logic circuit take over the time stamp and `Energy_Flag` information, a `TDC_Reset` signal will be asserted to clear the `TDC_Data_Ready` signal and also the latches in the TDC channel. After a recovery time of ~30 ns, the TDC channel is ready to take the next hit event.

DNL and INL

The PLL is designed to work in a frequency of 625 MHz. Then the average fine counter bin size, which is the average propagation delay of the delay cells in the VCO is

$$< \tau_d >= \frac{1}{32} \times \frac{1}{625\,\mathrm{MHz}} = 50\,\mathrm{ps} \tag{5.14}$$

Due to the mismatch during the semiconductor production process, not all the delay cells will have the same propagation delay, even though they are identically designed and have the same layout. Besides, the propagation delay for logic `'0'` and logic `'1'` are also not the same for the same delay cell. Therefore the sizes of the fine counter bins are not the same and this will result in errors in the timing measurements. The variance of the fine counter bin sizes can be described by differential nonlinearity (DNL) and integral nonlinearity (INL). The DNL of individual fine counter bin is defined as the relative deviation of its bin size to the average fine counter bin size:

$$DNL(i) = \frac{\tau_i}{< \tau_d >} - 1 \tag{5.15}$$

And the INL of a fine counter bin is defined as the deviation between the timing measurement to ideal correct fine time measurement. INL can be calculated by integrating the DNL of the fine

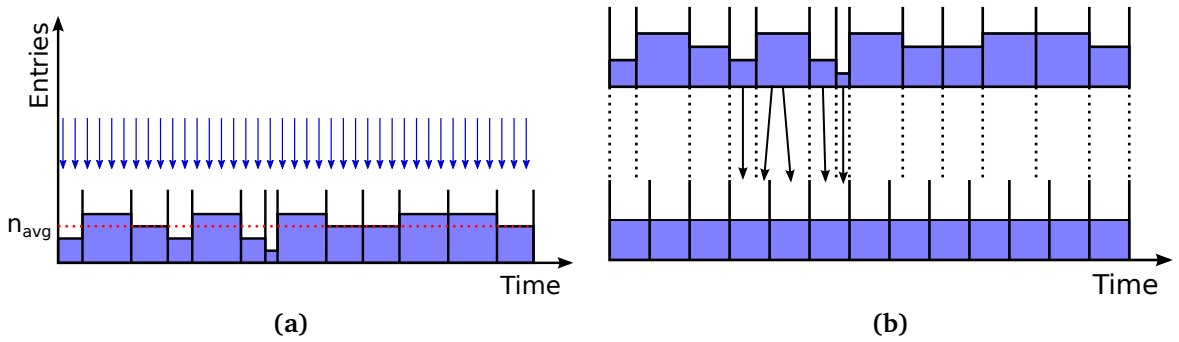


Figure 5.10: Measurement and correction of the TDC fine counter bins nonlinearity. Figures modified from [8].

counter bins up to the bin under investigation:

$$INL(i) = \sum_{j=0}^{i} DNL(j) \tag{5.16}$$

The nonlinearity of the TDC fine counter bins can be evaluated with a statistical code density test (CDT). A code density test for the TDC fine bins is demonstrated in Figure 5.10a. A large number of random events must be generated and measured by the TDC. The number of the events recorded in each single fine counter bins is a direct measurement of its relative bin size [72], whereas the average number of events in the fine counter bins n_{avg} is used as a reference for the expected ideal bin size. Thus, the differential nonlinearity of each fine counter bin can be calculated by the deviation of the number of events in each fine counter bin to the expected average number of events per bin:

$$DNL_i = \frac{n_i}{n_{avg}} - 1 \tag{5.17}$$

where n_i is the number of recorded event in fine counter bin i.

With the knowledge from the code density test, the nonlinearity of the TDC fine counter bins can be corrected by mapping the nonuniform fine counter bins to uniform bins [73]. As sketched in Figure 5.10b, the real binning of one VCO clock cycle can be built with the real bin size information of each bin from the code density test. This time interval can be ideally quantized into uniform bins. By overlapping these two binning of one VCO clock cycle, a mapping can be generated from the real fine counter bins to ideal uniform bins. A small real fine counter bin might be only mapped into one ideal bin. Others will mapped to multiple ideal bins. In such cases, a random dithering can be used to distribute the events in this real bin to its corresponding ideal bins.

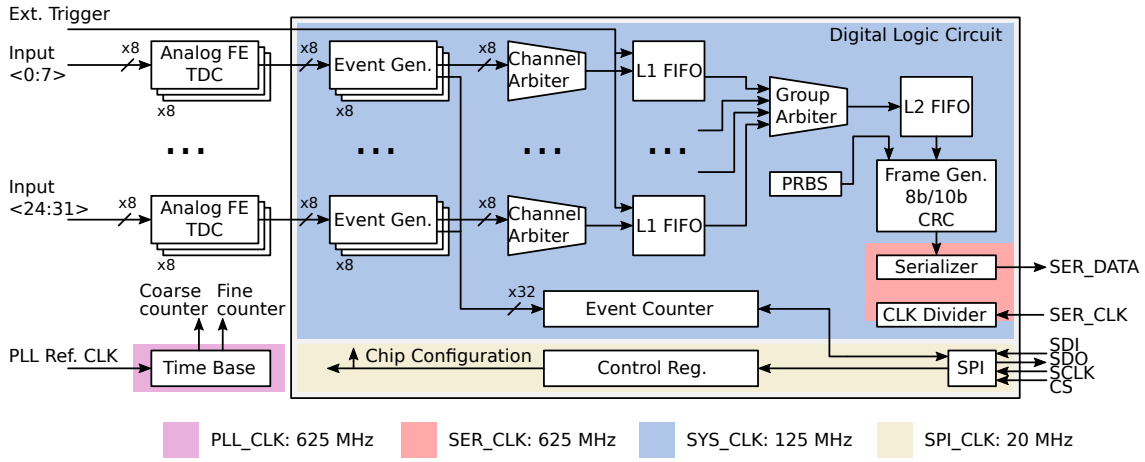


Figure 5.11: Block Diagram of the MuTRiG Chip.

5.5 MuTRiG Digital Part Design

The time stamps generated from the TDCs are processed, stored and transferred to external DAQ system by the on-chip digital logic circuity. Figure 5.11 shows the block diagram of the MuTRiG chip. The time stamps are received by the event generator modules at each channel to generate hit event data with time of arrival and time-over-threshold information. The channels are grouped into 4 groups and the hit event data from every 8 channels are stored in the L1 FIFO common for this group. The hit event data from all 4 group are then buffered in the L2 FIFO. The hit event data in the L2 FIFO is then transferred out in frames by the frame generator module and the double data rate serializer module.

There are four different clocks running on the MuTRiG chip:

- the 625 MHz PLL reference clock (`PLL_CLK`) used by the time base module for the time digitization
- the 625 MHz serial data link clock (`SER_CLK`) for data transmission on the serializer module
- the 125 MHz system clock (`SYS_CLK`) for the all the other modules besides the serializer in the digital logic circuitry. The system clock is generated from the serial data link clock by a clock divider on the chip.
- the 20 MHz SPI clock (`SPI_CLK`)for chip configuration and the readout of the channel event counter.

The digital logic circuit of the MuTRiG is an upgrade version of the STiC digital part [8]. New functionalities have been implemented for the readout of the Mu3e timing detectors. A customized LVDS transmitter and a double data rate serializer have been implemented to establish a gigabit serial data link for transferring the hit event data to the DAQ, which would allow for a much higher maximum event rate than the STiCv3 ASIC. A frame generator has been designed to provide the functionality of reducing the event length of the transmitted hit events, which

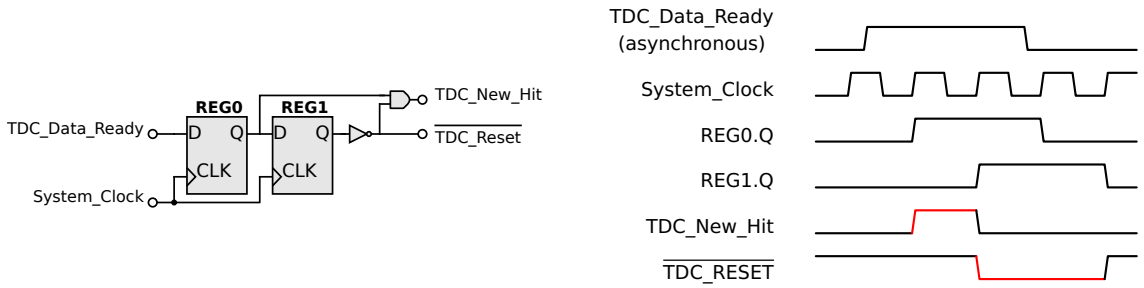


Figure 5.12: Schematic and the timing diagram of the circuit for generating the `TDC_New_Hit` and `TDC_Reset` signals. The red pulses indicates the assertion of the signals.

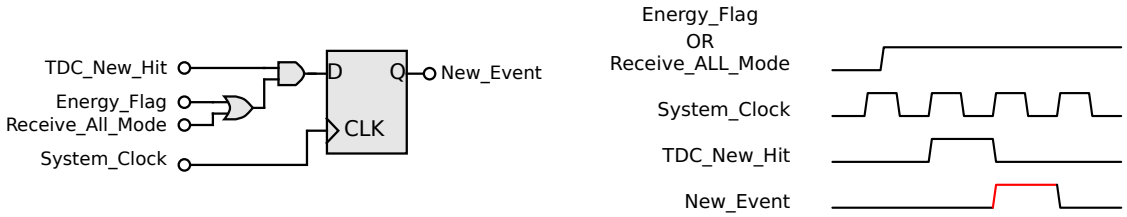


Figure 5.13: Schematic and timing diagram of the circuit for generating the `New_Event` signal. The red pulse indicates the assertion of the `New_Event` signal.

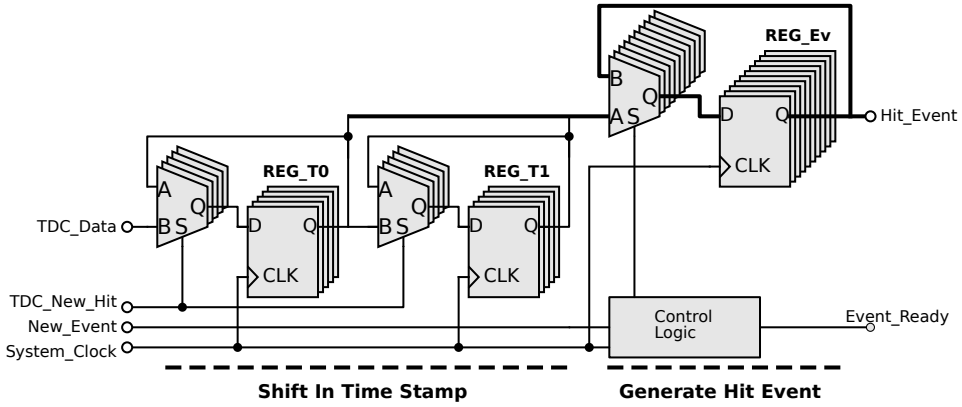
would further increases the bandwidth of the output data link. In order to monitor the serial data link quality and detect data transmission error at a gigabit link bit rate, Cyclic Redundancy Check (CRC) module is implemented to put check values at end of every data frame. The FIFO with external trigger functionality is also designed and implemented to provide the possibility of validating the hit event data with an external trigger signal, which can be of great help in the test beam or detector characterization scenarios. The channel event counter module is also implemented to facilitate channel calibration and monitoring for large number of channels.

In the following sections, the modules on the digital circuitry will be introduced.

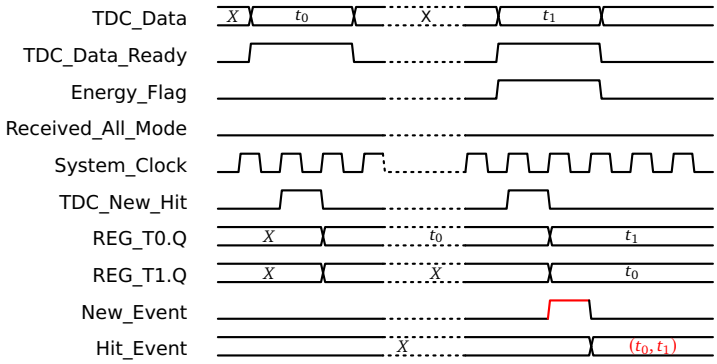
5.5.1 Event Generator

The event generator module is the first digital module in the digital part. It takes the time stamps from the TDC and generates the hit event data combining a time stamp for the time of arrival information and a second time stamp for the time over threshold information. The event generator uses two row of the registers to buffer the two most recent time stamp data from the TDC. Using the `TDC_Data_Ready` and `Energy_Flag` signals from the TDC, the module stores the digital time stamps from the TDC when the data is stable and issues the reset of the TDC latches.

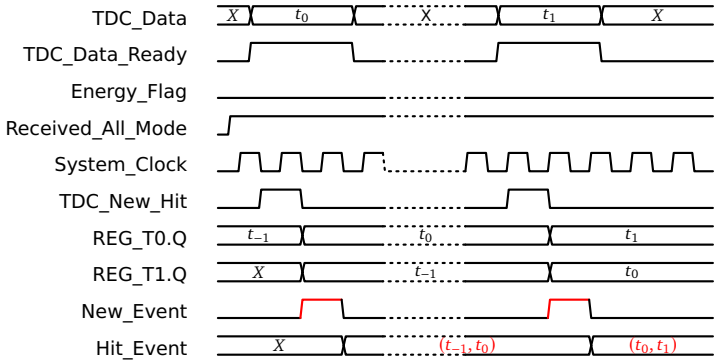
As the signals from the TDC are asynchronous signals, they need to be synchronized to the system clock for the further processing in the digital part and assure the data is stable when latched. The circuit shown in Figure 5.12 is used to generate a single clock cycle synchronous pulse signal, `TDC_New_Hit`, from the rising edge of the asynchronous `TDC_Data_Ready` signal. A



(a) Schematics of the Event generator module.



(b) Normal mode with event validation.



(c) Receive all mode.

Figure 5.14: Schematic and timing diagram of the event generation circuit.
(a) The circuit consists of two bands of registers: data register bands controlled by `TDC_New_Hit` signal to shift in the time stamps from the TDC module; and registers controlled by the `New_Event` signal to generate the new hit event data with both time stamps. It also contain an control logic to prevent the generation of new event data if current hit event data has not been taken by the following module.
(b) Timing diagram of generating hit event data in the normal mode. One new hit event data will be generated after storing both time stamps (T&E) with a `Energy_Flag` pulse.
(c) Timing diagram in the receive all mode. One new hit event data will be generated for every time stamps from TDC.

new TDC time stamp data is shifted in upon the assertion of the TDC_New_Hit signal. The active low TDC_Reset signal is also generated here.

The one clock cycle synchronous New_Event pulse is generated from the Energy_Flag signal from the TDC, or in the receive all mode, after every time time stamp created from TDC, as shown in Figure 5.13. Once the New_Event signal is asserted, the two time stamps will be saved into the event data registers as a new hit event to be sent to the downstream modules.

The event generator can work in two modes, the normal mode and the receive all mode, which is configured by the Receive_ALL_Mode signal. When the Receive_ALL_Mode signal is low, the event generator module works in normal mode and a new hit event data can only be generated once the Energy_Flag is asserted. When the Receive_ALL_Mode signal is high, the event generates module works in receive all mode. The New_Event pulse can be generated after each TDC_New_Hit pulse and new hit event data will be created for every new time stamps from the TDC.

The event generation module also contain a control logic for the hand-shaking with the following modules, which will prevent the generation of new event data if current hit event data has not been taken by the following module.

The circuit to buffer the time stamps and to generate event data is shown in Figure 5.14, as well as the timing diagram of the event generation in the normal mode and receive all mode. The timing diagram is drawn assuming hit event data is always read by the following module once generated.

5.5.2 Arbiter

Following the event generator module, the first level (L1) FIFOs, can only store one hit event data per clock cycle. The event generator modules in the same group are connected to L1 FIFO through the channel arbiter which decides the hit event data from which channel will be write to the FIFO at the next clock cycle. The hit event data which is not written will be kept in the channel event generator until it is written to the downstream L1 FIFO.

The event data stored in the L1 FIFOs are passed to L2 FIFO over the group arbiter.

5.5.3 FIFO

There are two levels of FIFO on the MuTRiG chip for buffering the hit event data. The two levels of buffers are used to minimize the dead time of the individual channels by assuring the event is transferred to the buffer as fast as possible. There are four first level (L1) FIFOs and each of them connects to 8 channels. The L2 FIFO merges the hit event data from all four L1 FIFOs and passes the hit event data to the downstream frame generator and serializer for sending the data out of the chip.

FIFOs are typically consist of storage, write/read pointer and the control logic which manipulates the write/read pointer and generates flag signals. The static random-access memories

(SRAM) are used as the storage elements for both the L1 FIFOs and L2 FIFO in the MuTRiG chip to save area and power as large amount of storage of 19968 bits and 12288 bits are required respectively.

The write/read pointers store the addresses on the SRAM for the next write/read operation. As the write and read operation are driven by the same clock, no additional measures need to be taken to synchronize the writing side and the reading side of the FIFO and a simple binary encoding is used for both write and read address. The control logic increase the address of the write/read pointer by 1 after each write/read operation. The flag signals, which indicates the state of the FIFO, are also generated as follows:

FIFO_Full When the write address is smaller than read address by 1. The FIFO is full of data and no more data can be written into the FIFO.

FIFO_Empty When the read address is equal to the write address. All the data in the FIFO has been read out.

External Trigger Functionality

Besides the data buffering function, a external trigger functionality is implemented on the L1 FIFOs in order to select and transfer only the data of hit events which are within the matching time window opened by an external trigger signal. This functionality is very helpful in the test beam scenarios where the interesting physical events happen in a short time period around trigger signals. By selecting and transferring only the valid events with the external trigger functionality, the bandwidth for data acquisition can be saved greatly and the data analysis can also be eased since the stored data contains less irrelevant events.

In many cases, the trigger signal validating the event will come with some delay with respect to the arrival time of the particle. In order to have the possibility to validate the hit events happens earlier than the external trigger signal, all the hit event data has to be buffered in the L1 FIFO before validation. And since the time stamps, of which the coarse counter are pseudo random bit pattern generated by LFSR, are not encoded in the binary encoding, it's not possible to get the time difference between the hit events and the trigger signal by simple comparison of the time stamps for the hit events and the trigger event. Instead, the system clock is used to estimate the time difference between the hit events and the external trigger event.

The working principle of the external trigger functionality is shown in Figure 5.15. As in the standard FIFO working case, the write and read operation are controlled in two independent process running in parallel. When the L1 FIFO is waiting for the external trigger signal, the `FIFO_Full` flag is set to `'0'` and the `FIFO_Empty` flag is set to `'1'`. In this state, the new hit event data is always written to the FIFO and no hit event data will be read from the FIFO and passed to downstream modules. The oldest data on the FIFO can be overwritten if the number of incoming hit events exceed the empty volume of the FIFO. Every 10 system clock cycle, the address of the

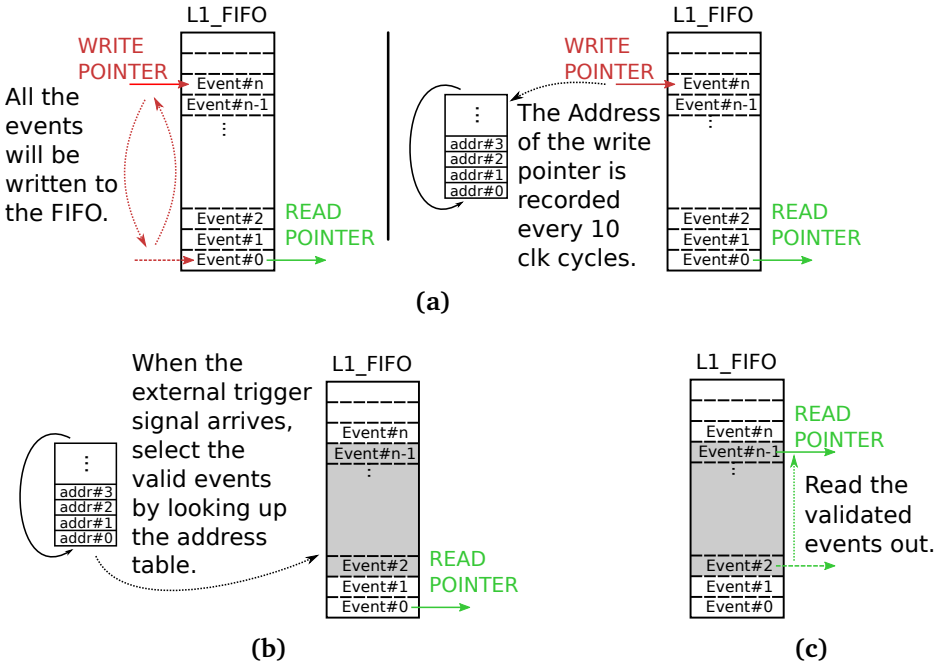


Figure 5.15: Implementation of the external trigger functionality on L1 FIFO.
(a) The write process of the FIFO when waiting for external trigger signal. The data are constantly written to the FIFO, and the oldest hit event data will be over-written if the FIFO is fully filled with data. The address of the write pointer is recorded to a address table every 10 clock cycles.
(b) When a external trigger signal arrives, the starting and ending address of the validated hit event data are looked up from the address table.
(c) The read precess of the FIFO. The hit event data within the valid region is read out.

write pointer is recorded in an address lookup table (Figure 5.15a). When an external trigger signal arrives, the valid hit events within the defined matching window are selected by looking up the starting address and the ending address of the valid data region (Figure 5.15b). The write pointer is then moved to the starting address of the valid data region. The selected hit event data within the valid data region can then be read out by the downstream module (Figure 5.15c). In the reading state, the `FIFO_Full` and `FIFO_Empty` flags are generated as standard FIFO such that the valid data will not be overwritten by the new data.

On the MuTRiG chip, the external trigger matching window can be adjusted in a step of 80 ns, 10 times of the system clock period. The maximum offset of the matching window can be set up to 1.28 µs before the external trigger and the the matching window can be configured to a width up to 2.48 µs, which is limited by the size of the address lookup table.

5.5.4 Frame generator

The hit event data of MuTRiG is transferred to the DAQ via a serial data link. Bitstrings are transmitted and a customized protocol is implemented for the communication between the MuTRiG

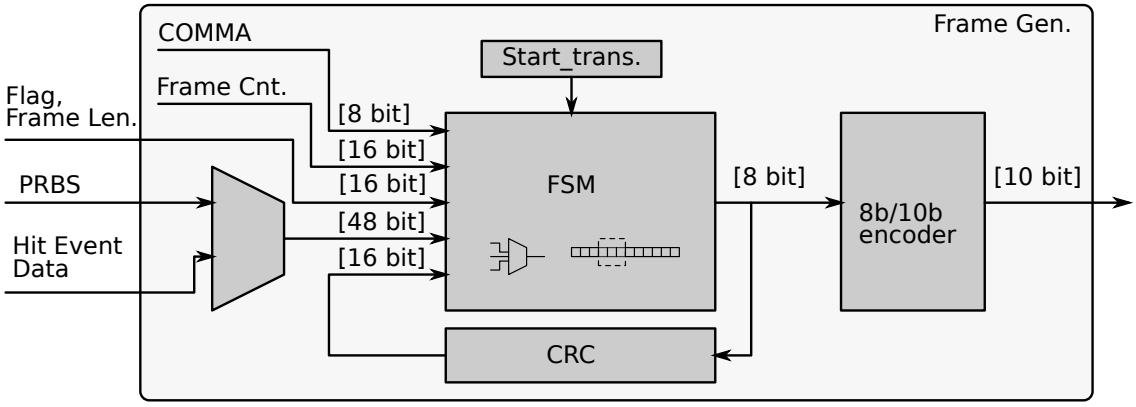


Figure 5.16: Block diagram of the frame generator unit.

chip and the DAQ system. The frame generator module collects the event data and generates the bitstrings, the data frames, in the formats defined by the protocol. In order to achieve higher output event rate for the Mu3e fibre detector at the same serial data link speed, the hit event data length can be reduced by discarding the energy time stamp information during the process when the frame generator module packs the hit event data into frames. This will reduce the length of single event from 48 bit to 27 bit.

The frame generator provides 8-bit bytes to the 8b/10b encoding module for achieving DC-balance and bounded disparity required by the LVDS serial data link, as well as for allowing clock recovery at the receiver side. The encoded 10-bit data from the 8b/10b encoding module is send to the downstream serializer module.

A block diagram of the frame generator block diagram is shown in Figure 5.16. The main body of the frame generator module is a Finite State Machine (FSM) which starts a data transmission at a fixed time intervals. The inputs of the FSM is as follows:

COMMA The control symbols of 8b/10b encoding, for data link synchronization or identification of the beginning and ending of the frame.

Frame Counter A 16-bit running counter for each frame, for merging data from different detectors by frame ID.

Frame Flag Flag bits indicates event data configuration and the running state of the chip.

Frame Length Number of the events in current frame.

Event Data The Event data can be either 48-bit PRBS data patterns for testing or the hit event data stored in L2 FIFO.

CRC The 16-bit Cyclic Redundancy Check value calculated for frame counter, frame flags, frame length and event data for transmission error detection.

As shown in Table 5.1, the data frame consists of four parts: header, payload, trailer and idle words. The header part is comprised of the header identifier, frame counter value, frame flags and the frame length. The header ID is a control symbol of 8b/10b encoding, `k28.0`, used to indicate

Table 5.1: Format of the data frame.

Field	Header				Payload	Trailer		Idel
	Header ID	Frame ID	Frame Flag	Frame Length	Hit Events	CRC	Trailer ID	Filler
Data	K28.0	Frame Counter Value	Flag Bits	Event Count	Event Data	CRC check value	K28.4	K28.5
Length [bit]	8	16	6	10	0-12240 or 0-7144	16	8	-

Table 5.2: The definition of the frame flags.

Bit Field	Definition
[5]	Generate Idle Signals
[4]	Short Hit Event Length Configuration
[3]	PRBS Debug mode
[2]	Sending 1 PRBS Pattern Per Frame
[1]	L2 FIFO Full
[0]	-

the beginning of the frame. The frame counter is a running counter value for each frame, used in the DAQ or analysis stage to merge data from different detectors by the frame counter value. The frame flags contains the flag bits to indicate the event structure and the chip status. The definition of the frame flag bits is shown in Table 5.2. The frame length part tells how many event are put into current frame. Depending on the configuration, the payload part is filled with either PRBS debugging bit sequences or all the hit event data stored in the L2 FIFO when the frame is started. The length of the payload part varies depending on the number of the hit events in the L2 FIFO. If there is no hit event to be transmitted, then the payload part will be omitted. The maximum length is 12240 and 7144 bits (1530 and 893 bytes) for the standard and short event length configurations respectively. The trailer part contains the Cyclic Redundancy Check (CRC) value and a trailer ID. The CRC value are the calculated check value for the bits starting from the frame counter part until the end of payload. The trailer ID is k28.4 control symbol of 8b/10b encoding, indicating the end of a frame. Between the end of a frame and the beginning of the next frame, the bitstrings is filled with the k28.5 control symbol of 8b/10b encoding, which can be used to recover the source-synchronous clock for the receiving module in the FPGA.

The hit event data structure in the standard event configuration is shown in Table 5.3. In this configuration, each hit event data contains the channel number information and two time stamps, one for time of arrival information and the other one for extract the energy information. The hit event data is 48 bits (6 bytes) long and the frame generator will put the data byte byte for 8b/10b encoding and for generating the frame to be sent out. The highest bits are always put

Table 5.3: Hit event structure in the standard event configuration (6 bytes).

Bit Field	Definition
[47:43]	Channel Number
[42]	T - BadHit
[41:27]	T - Coarse Counter
[26:22]	T - Fine Counter
[21]	E - BadHit
[20:6]	E - Coarse Counter
[5:1]	E - Fine Counter
[0]	E - Flag

Table 5.4: Hit event data structure in the short event configuration (3.5 bytes).

Bit Field	Definition
[27:23]	Channel Number
[22]	BadHit
[21:7]	Coarse Counter
[6:2]	Fine Counter
[1]	Energy_Flag
[0]	0

on the frame first.

As shown in Table 5.4, the hit event data is 27 bits long and contains only one time stamps for the time of arrival information for the short event configuration. Instead of the full energy information, a single bit `Energy_Flag` is used to indicate if the event had an energy sufficiently high to trigger the energy discriminator. A `'0'` is padded at end of the hit event data to become a 3.5 bytes long word. The frame generator packs the short hit event data to the frame by putting the highest byte into the frame first. The last 4 bits of the odd number of hit event data are packed with the first 4 bits of the next hit event to form a byte and then put into the frame. In case of an odd number of events in one frame, the last nibble is padded with zeros before transmission.

Cyclic Redundancy Check

Cyclic Redundancy Check (CRC) is commonly used for error detection in digital data communication and storage. The basic idea of the error detection is to calculate a short checksum value, which is calculated from the message, and to append the check value to the message. At the receiving side, the same calculation is applied to check if the calculated result of the received message is the same as the appended check value. With CRC, the check value is calculated by the polynomial division in modulo 2 arithmetic. Consider a message $M(x)$ (e.g. a message of `"1101"` can be represented by $M(x) = 1 \cdot x^3 + 1 \cdot x^2 + 0 \cdot x^1 + 1 \cdot x^0$) and a degree-n generator polynomial

$G(x)$, the check value is calculated by

$$M(x) \cdot x^n = Q(x) \cdot G(x) + R(x) \tag{5.18}$$

$$R(x) = M(x) \cdot x^n \bmod G(x) \tag{5.19}$$

The check value is appended to the message and sent out together with the message. Since the results of addition is equivalent to the results of subtraction in the modulo 2 arithmetic, the combined message called codeword which will be sent out is equivalent to $M(x) \cdot x^n - R(x)$. The receiver either apply the same calculation to the message $M(x)$ and check if the calculation result is the same as check value $R(x)$, or apply the same calculation to the whole received codeword $M(x) \cdot x^n - R(x)$ and check if the calculation result is 0:

$$(M(x) \cdot x^n - R(X)) \bmod G(x) = (Q(x) \cdot G(x)) \bmod G(x) = 0 \tag{5.20}$$

The error detection strength of a CRC depends on the generator polynomial $G(x)$. For MuTRiG chip, the CRC-16-ANSI ($G(x) = x^{16} + x^{15} + x^2 + 1$) polynomial is selected in order to detect the following errors [74, 75]:

- All single bit errors.
- All errors with odd number of bits.
- All two bit errors separated by a distance less than $2^{15} - 1 = 32767$, which is larger than the maximum MuTRiG frame length of 12400 bits.
- All burst errors of length less than 16.
- Most of the burst errors of length larger than 16. The asserted probability of failure error detection is 2^{-16}.

The CRC calculation is realized with linear-shift feedback register (LSFR) in hardware. Figure 5.17 shows the hardware implementation of bit-wise CRC-16-ANSI with LSFR which, take in signle new bit for calculation at each clock cycle. The registers store the interesting bits for subtraction in the polynomial division and the subtraction operation is realized by the XOR-gates. Two different operation are performed according to the MSB output of the LSFR:

MSB.Q = '0' The XOR-gate outputs are the same as the outputs of connected registers. At the next clock tick, a shift operation is performed to shift in a new bit of the message data to the interesting bit group. This is equivalent to the operation of bringing down a new term from dividend for the subtraction in the polynomial long division if the highest substation term is 0.

MSB.Q = '1' The XOR-gate outputs are the inverse of the outputs of the connected registers, equivalent to the subtraction to 1 operation results on the corresponding bit. Thus at the next clock tick, a subtraction operation with the generator polynomial $G(x) = x^{16} + x^{15} + x^2 + 1$ together with a shift operation are performed.

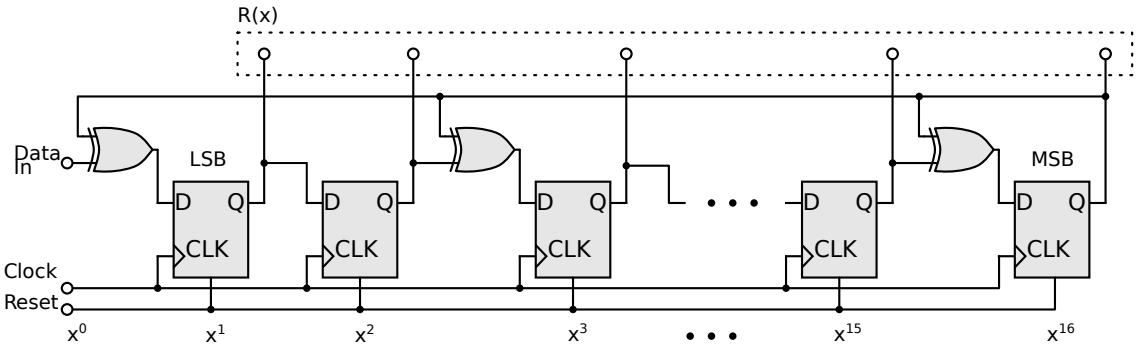


Figure 5.17: Hardware implementation of a single bit CRC-16-ANSI calculation circuit with a linear-shift feedback register.

Based on the hardware implementation of CRC calculation mentioned above, a few modification has been applied to cover more corner cases and more convenient integration to the MuTRiG chip:

- All the shift registers are initialized to '1' to detect the error of different numbers of leading zeros.
  The unmodified CRC calculator does not distinguish the message with different numbers of leading zeros simply for the reason that different numbers of leading zeros doesn't change the value of message $M(x)$. The operation of the initializing all the shift registers to '1' is equivalent to inverting the highest n bits of $M(x)$. The CRC calculation becomes:

$$\begin{aligned} R'(x) &= (M(x) + \sum_{i=m-n}^{m-1} x^i) \cdot x^n \bmod G(x) \\ &= M(x) \cdot x^n \bmod G(x) + \sum_{i=m}^{m+n-1} x^i \bmod G(x) \\ &= M(x) \cdot x^n - Q(x) \cdot G(x) + \sum_{i=m}^{m+n-1} x^i \bmod G(x) \end{aligned} \tag{5.21}$$

  where m is the length of the message $M(x)$ in bits. This modification makes $R'(x)$ as a function of the length of the message and thus enables the calculator to distinguish the messages with different number of the leading zeros.
  As long as the receiver side uses the same initial value for calculation, the codeword $M(x) \cdot$

$x^n - R'(x)$ will result in 0 if there is no error during transmission:

$$\begin{aligned}&(M(x) \cdot x^n - R'(x) + \sum_{i=m}^{m+n-1} x^i) \cdot x^n \bmod G(x)\\ &= Q(x) \cdot G(x) \cdot x^n \bmod G(x)\\ &= 0\end{aligned} \tag{5.22}$$

- The CRC calculation results are inverted before appended to the message to detect the error of appending trailing zeros after the CRC check value.
  The unmodified CRC calculator doesn't detect trailing zeros after the CRC check value because the codeword with trailing zeros is still a multiple of $G(x)$:

$$(M(x) \cdot x^n - R(x)) \bmod G(x) = 0 \tag{5.23}$$

$$(M(x) \cdot x^n - R(x)) \cdot x^k \bmod G(x) = 0 \tag{5.24}$$

  where k is the number of the trailing zeros of the error codeword.
  By inverting the CRC check value, the codeword sent to the receiver becomes $M(x) \cdot x^n - R(x) + \sum_{i=0}^{n-1} x^i$. At the receiver side, the CRC calculation result of the codeword is no longer 0, but a fixed "magic number":

$$\begin{aligned}C(x) &= (M(x) \cdot x^n - R(x) + \sum_{i=0}^{n-1} x^i) \cdot x^n \bmod G(x)\\ &= \sum_{i=n}^{2n-1} x^i \bmod G(x)\end{aligned} \tag{5.25}$$

  The trailing zeros after the CRC check value will be detected by giving a different calculation result at the receiver side:

$$\begin{aligned}C'(x) &= (M(x) \cdot x^n - R(x) + \sum_{i=0}^{n-1} x^i) \cdot x^m \cdot x^n \bmod G(x)\\ &= \sum_{i=n+m}^{2n+m-1} x^i \bmod G(x)\\ &\neq C(x)\end{aligned} \tag{5.26}$$

  The magic number of the implemented CRC-16-ANSI is `0x7FF2`.
- Byte-wise parallel operation.
  The hardware implementation of Figure 5.17 operates in bit-wise. It needs 8 clock cycles to produce the calculation results for each byte sent from frame generate FSM to 8b/10b

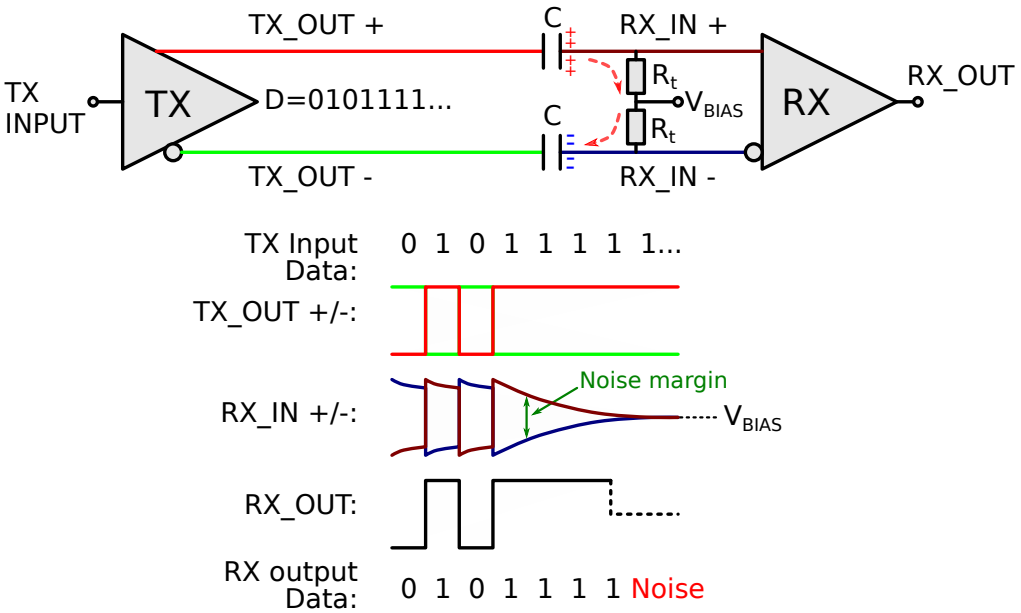


Figure 5.18: A example of DC unbalanced data over the AC-couples LVDS link. The red arrows indicate the current due to the flow of charge stored on the right conductor plan of capacitances C after the signal transition. Essentially the voltages of the these two node will result in the same potential as V_{BIAS}. The effect is exaggerated by using a small RC time constant.

encoder. A byte-wise parallelism is implemented by folding 8 times bit-wise CRC calculation and calculating the overall coefficients for each bit of the CRC registers. In this way, the byte-wise hardware implementation will generate a CRC results for 8 bits in one clock cycle and the calculation result is the same as bit-wise CRC calculator after 8 bits are shifted in [76].

8b/10b encoder

The term DC-balance describes the difference between the number of `'0'` and `'1'` in a set of consecutively transmitted bits. A DC-balanced datastream has equal number of `'0'` and `'1'` for a certain number of consecutive bit in the datastream. DC-balance is important for the AC-coupled LVDS links, which allows common mode level shifts between receiver and transmitter and has advantages on the performance and compatibility over the DC-coupled LVDS links. Figure 5.18 shows an example of a DC unbalance data transfered over a AC-coupled LVDS link. Due to the existence of the blocking capacitances C, the voltages at the input notes of the LVDS receiver (RX) will only change if there is a transition on the LVDS transmitter (TX) output signal, which originally from a `'0'` - `'1'` or `'1'` - `'0'` transition on the transferred data. After the transition, the voltages at the input terminals of the LVDS RX will decay towards a same value (V_{BIAS}) with a time constant defined predominately by the termination resistor R_t and the blocking capacitance C, reducing the noise margin of the RX inputs. For a long unbalanced data, the noise margin could get too small, causing the receiver cell to generate wrong outputs.

8b/10b encoding maps 8-bit words to 10-bit symbols to achieving DC-balance and bounded disparity. With the 8b/10b encoding, the number of '0' and '1' are difference no more than two in a string of data longer than 20 bits, and there are no more than five '0' or '1' in a row. The 8b/10b encoding used in the MuTRiG chip is using the IBM implementation described in [77, 78].

5.5.5 Serial Data Link

The 8b/10b encoded data is transfer out of the MuTRiG chip over a LVDS serial data link. On the MuTRiG chip side, a double data rate (DDR) serializer and a custom LVDS transmitter are implemented in order to achieve giga-bit link rate and to send out data for high input event rate cases.

Double Data Rate Serializer

As show in Figure 5.19, the serializer is implemented by two rows of shift registers which are shifting the odd and even bits of the encoded 10-bit data respectively. The odd and even bits of the 10-bit data are loaded into the shift registers every 5 clock cycles with the strobe BYTE_RD signal. The two rows of shift registers are then shifting out the data in a LSB first manner. The outputs of the odd and even bits shift registers are latched by two registers at rising and falling edges of the clock signal respectively. The output of the serializer is switched from the outputs of these two registers using a 2-to-1 multiplexer controlled by the voltage level of the clock signal. Thus the data is transferred on both the rising and falling edge of the clock signal. Since the even bits are always latched half clock cycles before its closest odd bits, thus the bits are in correct order at the output of the multiplexer, as shown in the timing diagram of Figure 5.19.

The worst timing path of this unit is from the output of the shift register SR_F0, which is shifting data at the rising edges of the clock SER_CLK, to the input of register REG_F which is triggered by the falling edges of the clock SER_CLK. The setup time constraint of the register REG_F should be fulfilled within half a clock period of the 625 MHz SER_CLK. For the other registers, one whole clock period of SER_CLK is available to fulfill their setup time constraints.

LVDS transmitter

The output data of the serializer is connected to an customized LVDS transmitter in order to drive the data over the large load of the pad of the chip, chip-board connection and the signal traces on the PCB to the receiver.

The schematic of the LVDS transmitter is shown in Figure 5.20. It consists of an LVDS driver to provide enough driving strength to drive the signal out, a pre-driver to convert the single-ended input signal to the input of the LVDS driver inputs with correct phase and common-mode feedback path to keep the common-mode voltage of the output signal to a desired value.

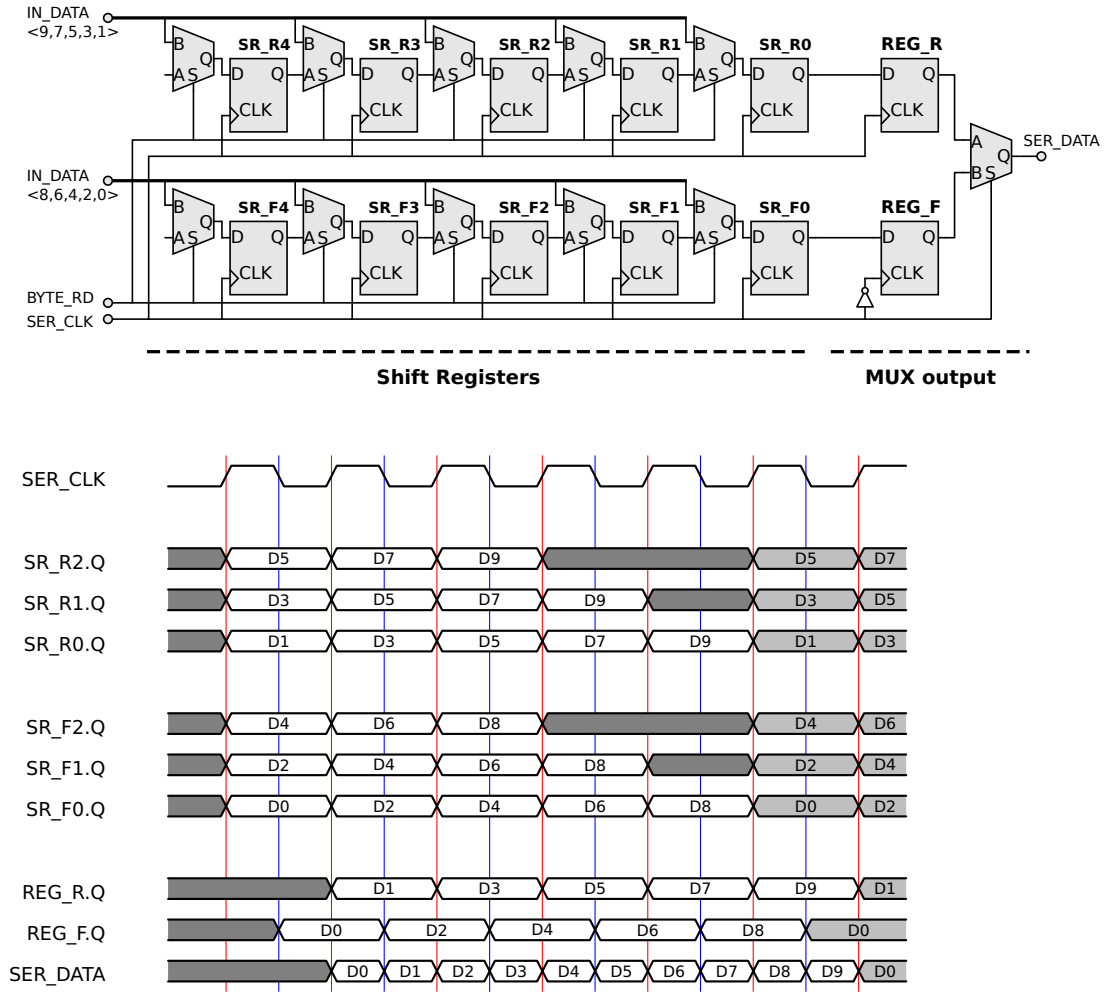


Figure 5.19: Schematics and timing diagram of the MuTRiG double data rate serializer.

The working principle of the LVDS driver is shown in the Figure 5.22. It's a Bridge-Switched Current Source LVDS driver architecture [79] which switches the current from the current sources with four switches. The switches are operated between two states:

- For driving logic '1', switch $S1$ and $S4$ are on. The current follows from top to bottom over the termination resister R_T, generating positive voltage across resister $V_{OUT} = I \times R_T$.
- For driving logic '0', switch $S2$ and $S3$ are on. The current follows from bottom to top over the termination resister R_T, generating negative voltage across resister $V_{OUT} = -I \times R_T$.

The circuit implementation of the LVDS driver and the Common-Mode Feedback (CMFB) is shown in Figure 5.22. The switches are implemented with transistors $M1$ - $M4$. $M1$ and $M2$ are PMOS transistors and will be turned on when the gate voltage is at low potential. $M3$ and $M4$ are NMOS transistors and will be turned on when the gate voltage is at high potential. By the swing of V_{IN}, the transistors $M1$ - $M4$ will act as switches between the two states mentioned

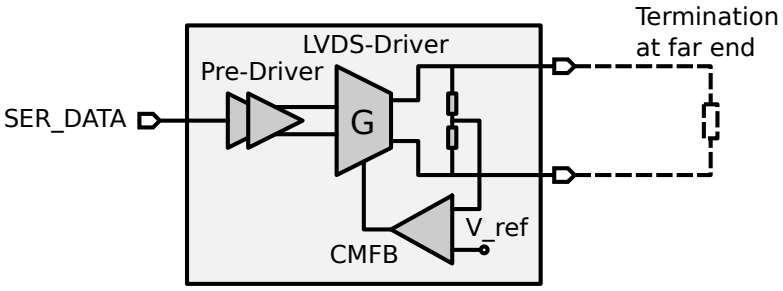


Figure 5.20: Diagram of the LVDS transmitter.

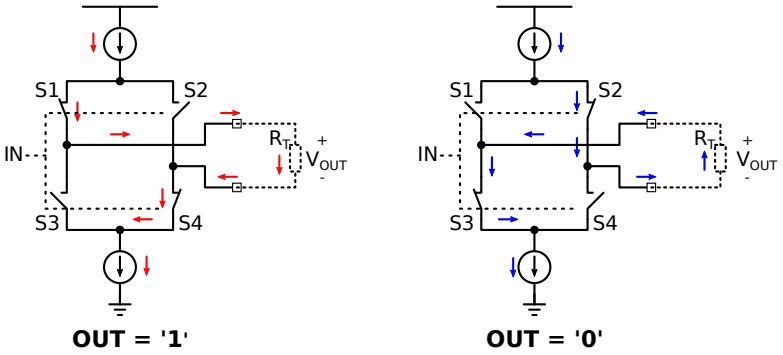


Figure 5.21: Working principle of the LVDS driver.

above. $M1$ - $M4$ typically are large transistors and have large W/L ratio to be able to deliver the current flowing through the driver. Taking into account the low 1.8 V VCC power voltage, a large W/L ratio also helps to reduce the voltage overhead of $M1$ - $M4$ during switched-on state.

Transistor M_P and M_N act as current sources shown in Figure 5.21. The gate voltage of the M_N are generated by a static stable bias generation circuit to generate a constant current of 4.5 mA for the LVDS driver. The current generated by the M_N and M_P can not perfectly be matched if both transistors were biased with a statically generated gate voltage. This would cause uncontrolled shifts of the output common mode voltage of the driver, potentially causing the driver to not function as intended. Instead, the gate voltage of the PMOS current source M_P is generated with an common mode feedback circuit. The common-mode voltage of the LVDS output signals (V_{CM}) is sensed by the a resister divider consisting of two 5 kΩ resistors. V_{CM} is then compared with reference voltage of desired potential (V_{REF}) with a differential amplifier. The output of the amplifier regulates the bias for M_P such that V_{CM} is the same as V_{REF}.

Figure 5.23 shows the schematic of the pre-driver stage. It is the interface between the on-chip digital circuit and the LVDS drivers. On one hand, the pre-driver converts the signal-ended CMOS signals to differential signals to the LVDS driver switches. On the other hand, it also ramps up the driving strength to keep a short signal transition time on the large load of the LVDS switch transistors. The pre-driver consists of a CMOS-to-differential converter stage, a control logic stage and a buffer stage. In the CMOS-to-differential stage, the single-ended CMOS signal is split into

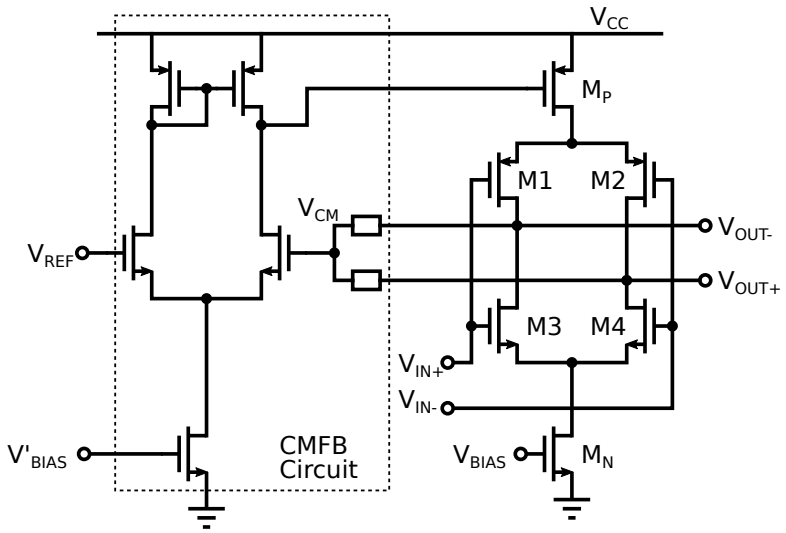


Figure 5.22: Schematics of the LVDS driver and the Common-Mode Feedback circuit.

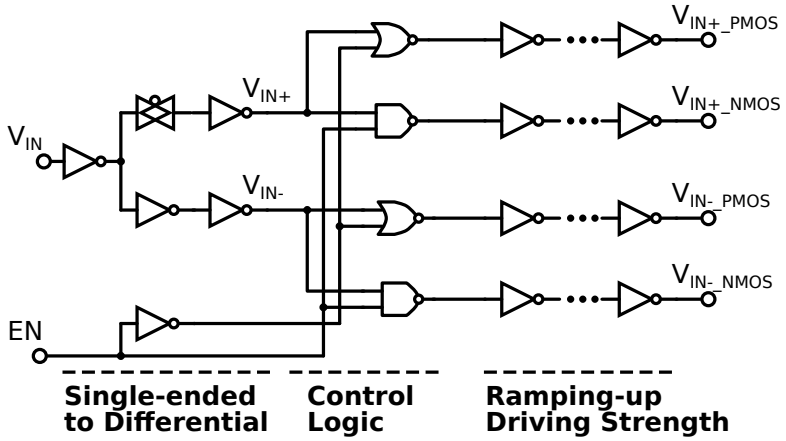


Figure 5.23: Schematics of the pre-driver block.

a inverter path and a transmission gate path to generate the differential signal. The delay of the inverter and the transmission gate need to be tuned individually such that the positive and negative signal of the output differential signal are in 180° phase different. This is one of the most different part of the LVDS transmitter cell, since different process corners yeild different delays in the gate driver cells, which needs to be compensated by custom CMOS cells. The control logic is designed implemented with NOR-gate and NAND-gate in order to switch off all the switches on the LVDS driver and cut off the LVDS driver current when the transmitter cell supposed to be disabled. Since the output of the LVDS driver is floating in the disable state, this control circuit provides the possibility of sharing outputs from multiple LVDS drivers if only one of them will be enable at the same time. In the buffer stage, a chain of the inverters with increasing W/L ratio (transistor width to length ratio) is used for every branch, in order to ramp up the driving strength and to drive the large gate capacitance on the LVDS switch transistors.

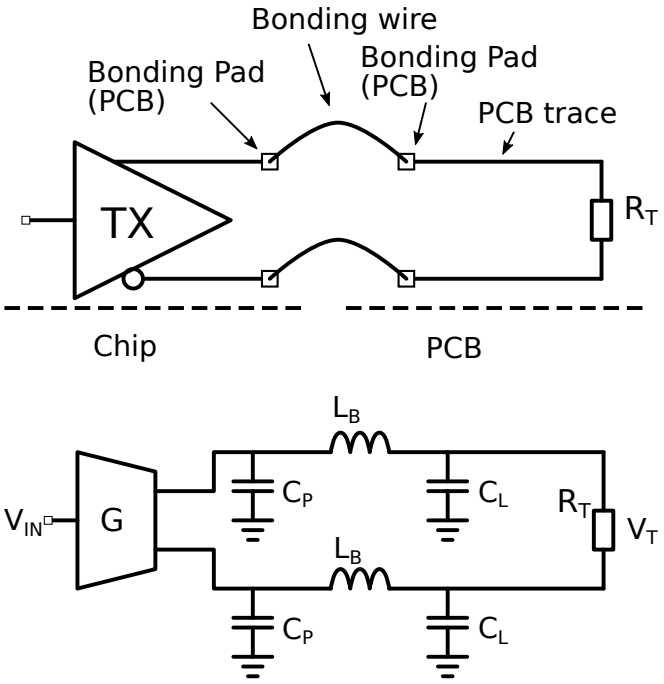


Figure 5.24: Distributed load model of the LVDS driver.

Table 5.5: LVDS driver load model parameter values.

Parameter	Value
C_P	3 pF
C_L	3 pF
L_B	5 nH
R_T	100 Ω

The bandwidth of the LVDS transmitter circuit, which determines the rising and falling time of the output signal as well as the maximum bit rate that can be driven by the driver, is highly affected by the load of the LVDS driver. As shown in Figure 5.24, a distributed line model is used to simulate the load of the LVDS driver, where C_P is the parasitic capacitance of the pad on the chip, L_B the inductance of the bond wire, C_L the load capacitance on the PCB and R_T the termination resistor at the receiver end.

A transfer function can be derived with this distributed line model as:

$$\begin{aligned}\frac{V_T(s)}{V_{IN}(s)} &= G(s) \cdot H_{Line\_Model}(s) \\ &= G(s) \cdot \frac{R_T}{s^3 C_P C_L L_B R_T + s^2 C_P L_B + s(C_L + C_P) R_T + 1}\end{aligned} \tag{5.27}$$

Where $G(s)$ is the transconductance of the LVDS driver.

The line model term of the transfer function Equation 5.27 has three poles, and two belong to a pair of complex conjugates. The normalized frequency response of the LVDS $G(s)$ with R_T

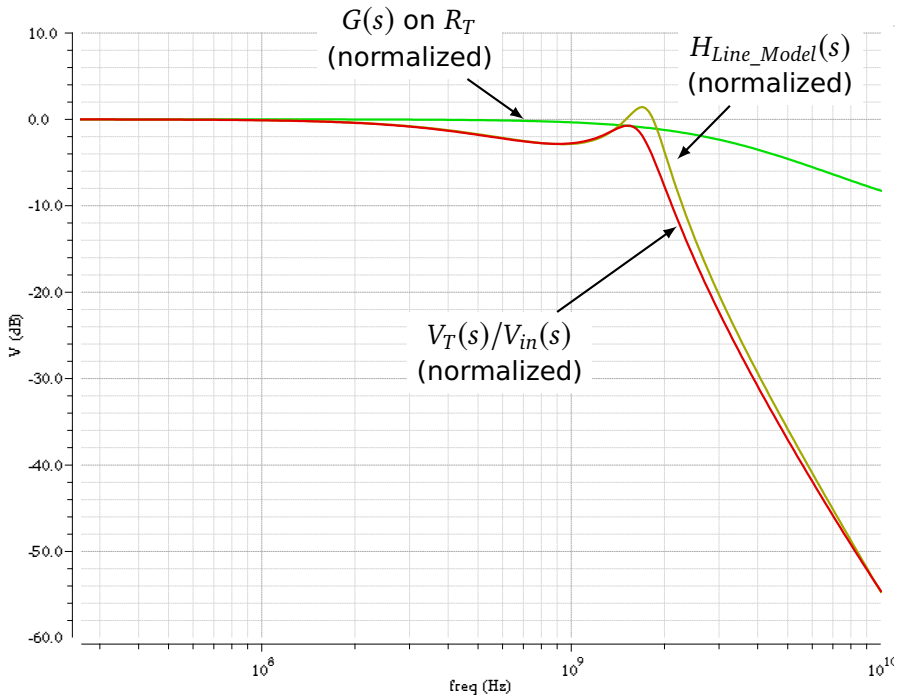


Figure 5.25: Frequency responses of the line load model and the LVDS transmitter with the load.

termination, the load line model $H_{Line\_Model}(s)$ and the whole circuit $V_T(s)/V_{IN}(s)$ from SPICE simulation is shown in Figure 5.25. The line model parameter value used in the simulation is listed in Table 5.5. $G(s)$ drops at high frequency region due to the gate-drain capacitance of the large switch transistors. This puts additional concern for optimizing the sizes of the switch transistors. For the frequency response of the load, a peaking is clearly visible due to the conjugated poles of its transfer function. This peaking also appears on $V_T(s)/V_{IN}(s)$ gain, which will help to improve its frequency response at peaking frequency region. The overall 3 dB bandwidth of the LVDS driver with this line model is at around ~2 GHz.

A simulated LVDS signal waveform on the termination resistor R_T for driving 625 MHz clock signal is shown in Figure 5.26. The overshoots visible on the waveform arises from the peaking on the frequency response of the LVDS transmitter, helping to improve the signal rise time and allow for high bit rate used in data link The rise time is ~260 ps from this simulation result. The signal swing amplitude of LVDS output waveform is around ±350 mV.

To allow an adjustment of the driving strength, an additional current DAC is connected in parallel to the bias generation circuit such that the M_N and M_P can be biased to provide higher current and to increase the amplitude of the LVDS output signals. The bias current for the LVDS driver can be as high as 9 mA in total.

The layout of the LVDS transmitter with the biasing and DAC blocks is shown in Figure 5.27. The whole LVDS transmitter, including pre-driver, LVDS driver, CMFB and DACs, is packed into an area of 135 µm × 145 µm surrounded by bulk connections to reduce the disturbance for the

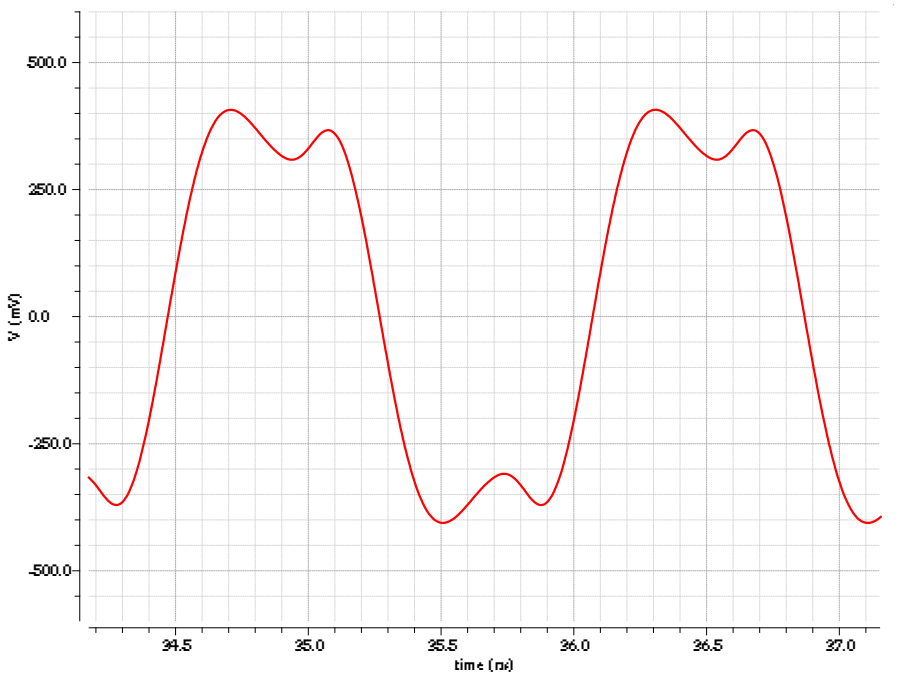


Figure 5.26: LVDS output waveform of 625 MHz clock signal from post-layout simulation.

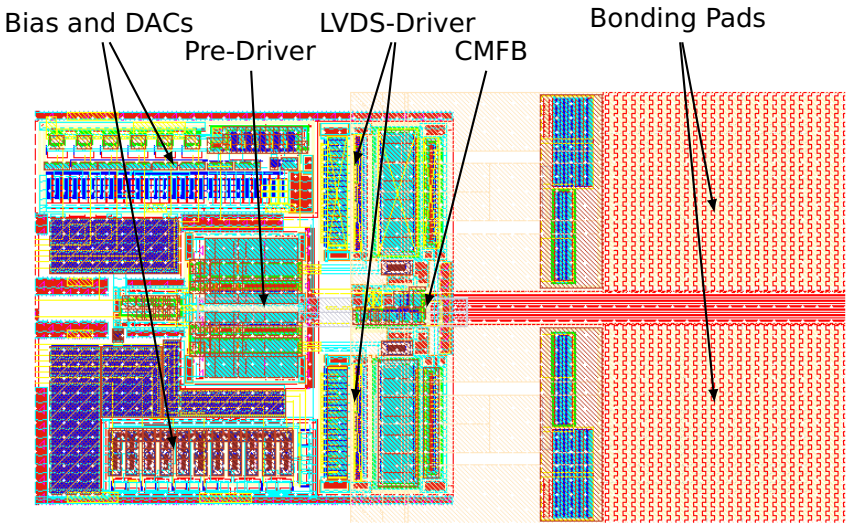


Figure 5.27: Layout of the LVDS transmitter.

other part of the chip. LVDS transmitter is also integrated with the bonding pads as an I/O cell which will be placed at the periphery of the chips.

5.5.6 Channel Event Counter

In order to monitor the event rate of each channel, channel event counter functionality has been implemented in the MuTRiG chip. A 12-bit binary counter for each channel is incremented for each new event recorded by the event generator module. The channel event counter values are read out using a separate SPI interface. At each read operation, the counter values are buffered by a row of registers and then transmitted. The counters are reset in the same time. Then the stored counter values is the number of new events between two read operations and the event rate of each channel can be calculated by the channel event counter values and the time interval between two read operation, which is controlled by the DAQ system. For a reading frequency of 1 MHz from the DAQ, the channel event counters are able to monitor the input event rate up to 4.095 GHz for each channel.

5.5.7 Chip Configuration and Chip Reset

An SPI interface is used to access the configuration in the ASIC. SPI operates in master-slave architecture with single master device (DAQ/control system) and single or multiple slave devices (chips) selected by the `CHIP_SELECT` (`CS`) signals. The SPI slave module in the chip is implemented with a chain of shift registers which shift in chip configuration data from an input port of the chip. The output of the last shift register is send off chip for shifting out the shift register value back to the master device. At the end of the chip configuration data transmission, the shift register value is latched to a row of D-latches which store the active configuration for the analog front-end, TDC and the digital logic modules.

There are two reset inputs on the MuTRiG chip. A channel reset input signal resets only the coarse counters in the TimeBase unit of TDC. It can be used for synchronizing different chips for timing measurement. The other reset input, chip reset, not only resets the coarse counters in the TDC, but also resets all the finite state machine in the digital part to their valid idle state.

5.6 Physical Design Implementation

The physical design, also called back-end design, include all steps to transport an abstract description of the digital part using a hardware description language as well as the custom analog blocks into the layout of the full chip which can be sent for production to the semiconductor fabrication plant for manufacturing.

The MuTRiG chip is implemented in the UMC 180 nm technology on a die area of 5 mm $\times$ 5 mm in a multi-project wafer (MPW) run, with which it is possible to produce low quantity prototype ASICs in a low price. The physical design flow of the MuTRiG chip is based on the design flow used for the Spikey [80] and STiC chips [8]. Chip specific configurations have to be taken care of to ensure the functionality and the performance of the chip.

5.6.1 Timing Constraints Specification

As described in section 5.5, there are four clocks running on the MuTRiG chip: PLL_CLK, SER_CLK, SYS_CLK and SPI_CLK. The SYS_CLK is generated by the SER_CLK and the other three clocks are coming from input pins. As PLL_CLK only runs on the TDC module for the timing measurements and it is not on any clock pin of the digital flip-flops on the digital part, thus the signals on this clock domain are considered as asynchronous signals and no specification is applied to PLL_CLK.

Table 5.6: Clock specification in the MuTRiG chip.

Clock Name	Period [ns]	Purpose
SER_CLK	1.25	serial data link clock and for generating SYS_CLK
SPI_CLK	20	SPI clock for chip configuration and for transferring channel event counter data

The specification for the SER_CLK and the SPI_CLK is listed in Table 5.6. Both SER_CLK and SPI_CLK are constrained to a higher frequency in order to improve the robustness of the digital part of the chip against the tough working environments. The SER_CLK is specified to 800 MHz and the SPI_CLK to 50 MHz. Other timing constraint specifications include:

- Specify the SPI_CLK as an asynchronous clock to SER_CLK and SYS_CLK.
- Disable the timing constraints for the signal paths from the TDC to the SER_CLK and SYS_CLK clock domain.
- Disable the timing constraints for the signal paths from the SPI_CLK domain to the analog front-end.
- Disable the timing constrains for the asynchronous reset signal and external trigger signal paths to the SER_CLK and SYS_CLK.

5.6.2 Floorplan of the MuTRiG Chip

As a mixed signal ASIC, the analog part, TDC and the digital part should be placed in a way that the signals can be easily routed, the timing constraints of all the part can be better met and that the influence of the digital activities on the timing performance of the analog front-end is minimized.

Figure 5.28 shows the top level floorplan of the MuTRiG chip. The following considerations have been taken for the floor-planning of the MuTRiG chip:

Power Pads In order to guarantee a stable power supply for the analog front-end channels and TDC, sufficient number of power pads have been assigned for the power of the analog front-end channels and TDC.

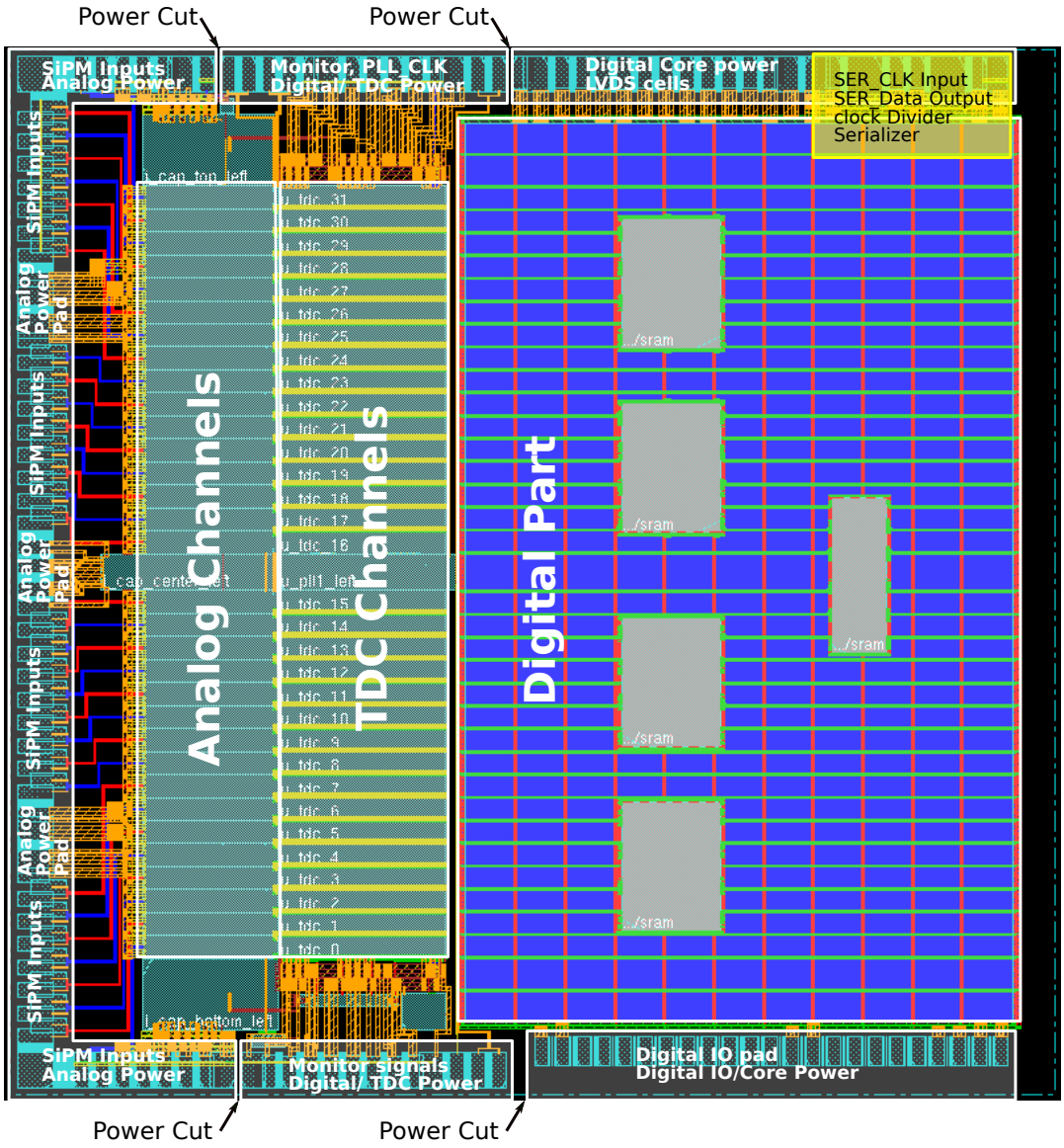


Figure 5.28: Floorplan of the MuTRiG Chip.

In total 11 pairs of power pads have been used for the analog power supply of the analog channels. The power pads are distributed along the top, left and bottom edges of the chip to ensure a homogeneous power distribution between channels. This also helps to reduce the noise on the power net in the way that the disturbance on the power net due to the activities of a certain channel can find a short path to go to the power pad without introducing noise to the power nets of other channels.

9 pairs of power pads are distributed for the power of the TDC channels on the top and bottom edge of the chip. The digital cells in the analog channels, like the discriminators and the hit log unit, are also connected to the same power nets as TDC.

Power Cut Power cuts are applied to divide the power ring into regions for the analog channels, TDC and the digital part. The power domain for the analog front-end, TDC and the digital part are physically separated on the MuTRiG chip to reduce the interference between parts, especially to avoid the direct coupling of the noise from the TDC activities and digital part activities into the analog channels.

High Frequency Clock Domain The serializer and the clock divider in the digital part, which work in the high frequency SER_CLK domain, are placed close to the LVDS receiver and transmitter cell, far from the analog channels to minimize the their coupling and influence to the analog part. The SER_CLK input pad and SER_DATA output pads are also placed to the same corner.

Event Generator The event generator modules has been placed to the left edge of the digital part and each of them are align with its corresponding TDC channel to ensure that each channel has the same connection between the TDC and digital part.

5.6.3 Timing Closure

In every optimization steps of the design flow, the design is verified if the timing constraints are met by RC-extraction, delay calculation and static timing analysis (STA) [80]. The generated timing reports in different optimization steps are monitored to determine if the design can meet the timing specification or not. For the paths which can not meet the timing constraints with all the optimization steps, digital part modifications, such as pipelining the path to reduce the depth of digital gates that data needs to propagate in one clock cycle, have been applied to the design without changing its functionality.

At the sign off stage of the design flow, a detailed timing analysis[1] with the final gate-level netlist and RC-extraction data is performed at different process corners and no timing constraints violation is found for the final design. Table 5.7 lists the worse setup time slack value for SER_CLK and SYS_CLK from the sign off stage STA. The expected maximum SER_CLK are calculated by subtracting the worst setup time slacks from the corresponding clock periods. As there is not negative slack for both clocks, SER_CLK frequency of the chip can be higher than the specified target value and the expected maximum SER_CLK frequency is 877 MHz, 1053 MHz and 1149 MHz respectively for the worst, typical and best case process corners.

SDF[2] files are also generated for different process corners with the interconnection delay and cell delay information. The SDF files are then used to perform back-annotated simulation with the gate-level netlist from the final design to check if the behavior of the final netlist matches the design behavior at different process corners.

[1] with Synopsys PrimeTime software
[2] Standard Delay Format

Table 5.7: Worst setup time slack value for SER_CLK and SYS_CLK in different process corners.

	$Slack_{ser\_clk}$ [ns]	$Slack_{sys\_clk}$ [ns]	Max. SER_CLK frequency [MHz]
Worst Corner	0.11	1.07	877
Typical Corner	0.30	1.66	1053
Best Corner	0.38	1.92	1149

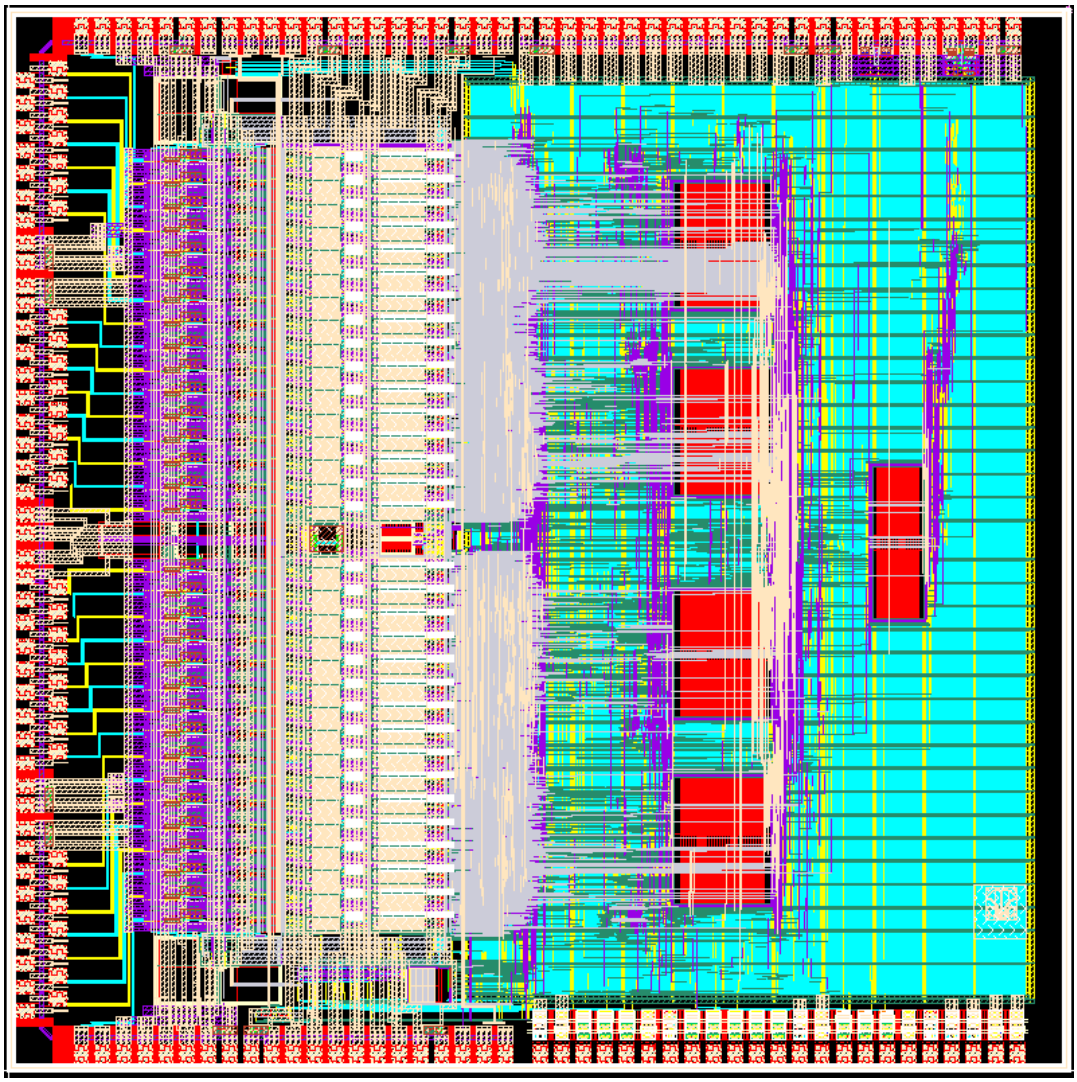


Figure 5.29: Layout of the MuTRiG Chip.

5.6.4 Physical Verification

Figure 5.29 shows the final layout of the MuTRIG chip. Before submitting the layout data file[1] for manufacturing, the layout of the chip has passed several physical verifications to make sure

[1]The layout file is in GDSII format, which an industrial standard format for integrated circuit layout data exchange.

the correctness of the layout, including:

DRC The design rule check (DRC) verifies the geometry of the layout fulfill the design rules of the fabrication process, such as minimal metal width, minimal spacing between metals etc.

LVS The layout versus schematic (LVS) checks if the implemented layout matches the schematic view of the chip. The SPICE netlist is extracted from the layout and then compared with the source schematic netlist.

Antenna The antenna check search for large metal structures which are connected to the gate of the transistors but not electrically connected to the silicon substrate. During the semiconductor manufacturing process, permanent physical damage can occur for these metal structures to the transistors due to the rapid discharging of the accumulated charge on the metal through the thin gate oxide.

ERC The electrical rule check looks for the dangerous electrical connection in the layout, such as wrong or floating connection for the transistor well or substrate which should be connected to power or ground for the functioning of the transistors.

Chapter 6

Characterization Measurement Results

A MuTRiG prototype chip was fabricated in the UMC 180 nm CMOS technology and arrived in early 2017. In order to verify the performance and the functionality of the MuTRiG chip, the MuTRiG prototype chip have been characterized in the lab since then. This chapter presents the characterization measurement results of the MuTRiG prototype chip. The MuTRiG characterization setup is described in the first section. The timing performance measurement results of the analog front-end and the full signal/data processing chain which includes analog front-end, TDC and the digital logic circuity are shown in the second section. Then follow the digital functionality validation results and serial data link characterization results.

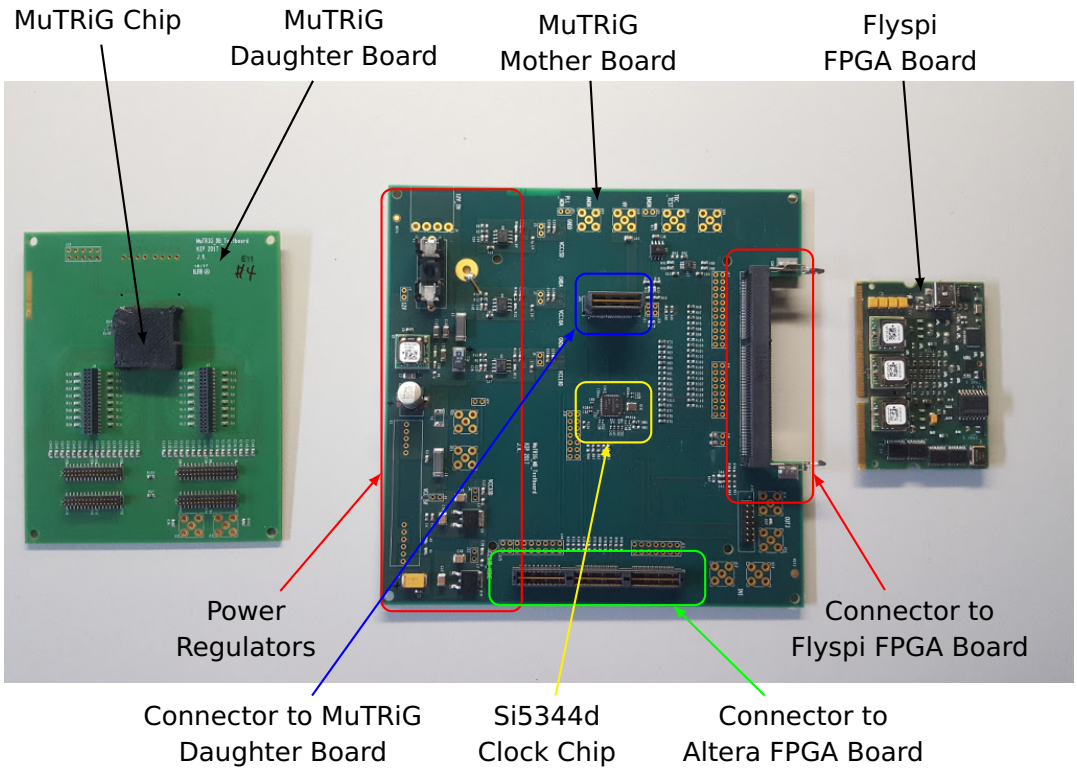
The MuTRiG has also been test with the Mu3e Tile detector module at DESY test beam to evaluate the performance of the ASIC with realistic inputs and under physical condition. The results from the DESY test beam will be shown in the last section.

6.1 MuTRiG Characterization Setup

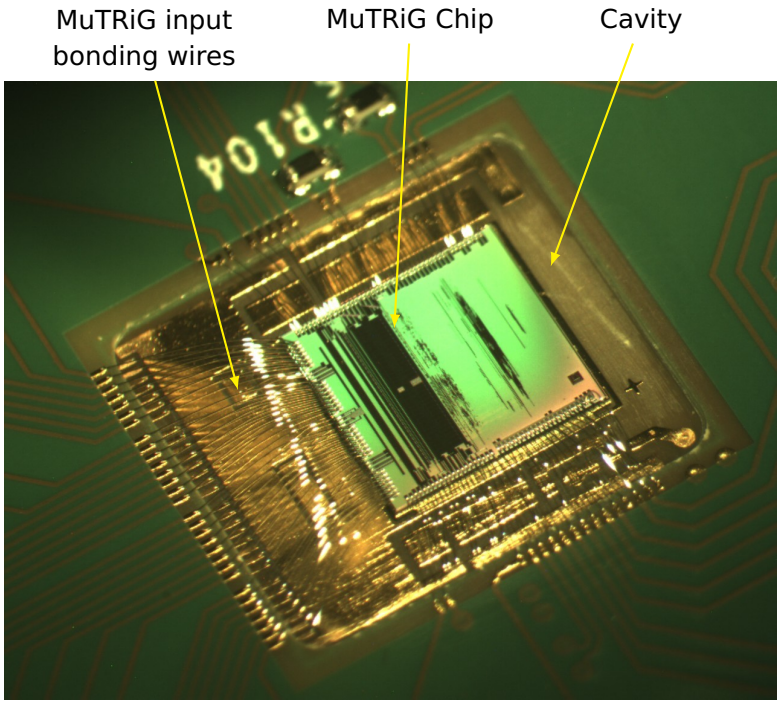
A set of Printed Circuit Boards (PCBs), consisting of a mother board and a daughter board, has been designed for the MuTRiG chip characterization. The MuTRiG mother board, daughter board as well as the field programmable gate array (FPGA) board is shown in Figure 6.1a.

The MuTRiG chip is wired bonded on the daughter board. As shown in Figure 6.1b, a cavity design has been implemented on the daughter board to overcome the bonding difficulty due to the dense bonding wires for the differential inputs of the MuTRiG channels, as well as to reduce the length of the bonding wires for channel input and power nets for reducing the inductance on the bonding wires and for better performance. As shown in Figure 6.2, a charge injection test input circuit is implemented parallelling to the SiPM detector input circuit. The test input circuit can be detached from the input of the chip by removing the 0 Ω resistors on the board in order to reduce the parasitic capacitance on the chip input nets.

The MuTRiG mother board provides a controlled working environment for MuTRiG characterization. Stable 3.3 V and 1.8 V power nets required by the MuTRiG chip is generated on the mother board with commercial DC-to-DC converters and Low-dropout regulators (LDOs). The 625 MHz PLL reference clock and 625 MHz serial data link clock for the MuTRiG chip is also



(a) MuTRiG characterization setup PCBs.



(b) MuTRiG chip bonded on the PCB.

Figure 6.1: The MuTRiG characterization setup.

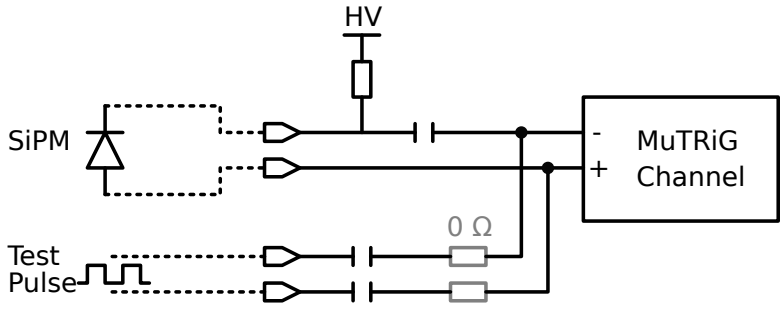


Figure 6.2: The input circuit on the MuTRiG test board. The grey 0 Ω resistors can be remove to detach the test pulse circuit from the MuTRiG input.

generated on the mother board with a high performance low jitter clock multiplier chip - Silcon lab Si5344d [81]. The mother board also allows the communication between the MuTRiG chip and the FPGA used in the DAQ system. Interfaces to two different DAQ system are provided on the MuTRiG mother board. One is based on Xilinx spartan-6 FPGA [82], which allows agile modification and debugging for single chip characterization. The other one is a bulkier but more scalable system based on Altera Stratix IV FPGA [83], which can be used in the Mu3e timing detector system integration, commissioning and later in the Mu3e experiment. It's possible to switch from one DAQ to the other by changing a few 0 Ω resistors on the mother board. The daughter board and the mother board are connected with high speed connectors [1].

The characterization measurements of single chip are carried out with the DAQ system based on Xilinx Spartan-6 FGPA. The overview of the DAQ system, including the hardware part and software part, is shown in Figure 6.3. The Xilinx Spartan-6 FPGA is sitting on a general purpose FPGA board called Flyspi board, which is developed in Kirchhoff-Institute for Physics at Heidelberg University and is also used in [84]. The FPGA sends the configuration data to the MuTRiG chip and to the Si5344 clock chip with SPI and I2C interfaces respectively. The serial data from the MuTRiG chip is de-serialized on the FPGA. The FPGA communicates with the PC through USB ports with a Cypress FX2LP USB2.0 micro-controller [85]. The power of the Flyspi board is provided from the MuTRiG mother board to make sure that the FPGA on the board gets sufficient and stable power supply.

On the software side, the data from/to the USB port is prepared with a libusb wrapper. The chip configuration data and the MuTRiG event data are processed in different way. The chip configuration bit pattern can be generated from a configuration file through Command Line Interface (CLI) or from a Graphic User Interface (GUI) with which we can easily change the configuration value for each chip configuration parameter. The chip configuration bit pattern is then transfered to the main DAQ software over message queue interface and later sent to the USB port to be send to FPGA. The configuration data read back from the chip is sent to the CLI or GUI for validation through message queue interface. While for the MuTRiG event data, it firstly decoded from the

[1] Samtec QTH/QSH series

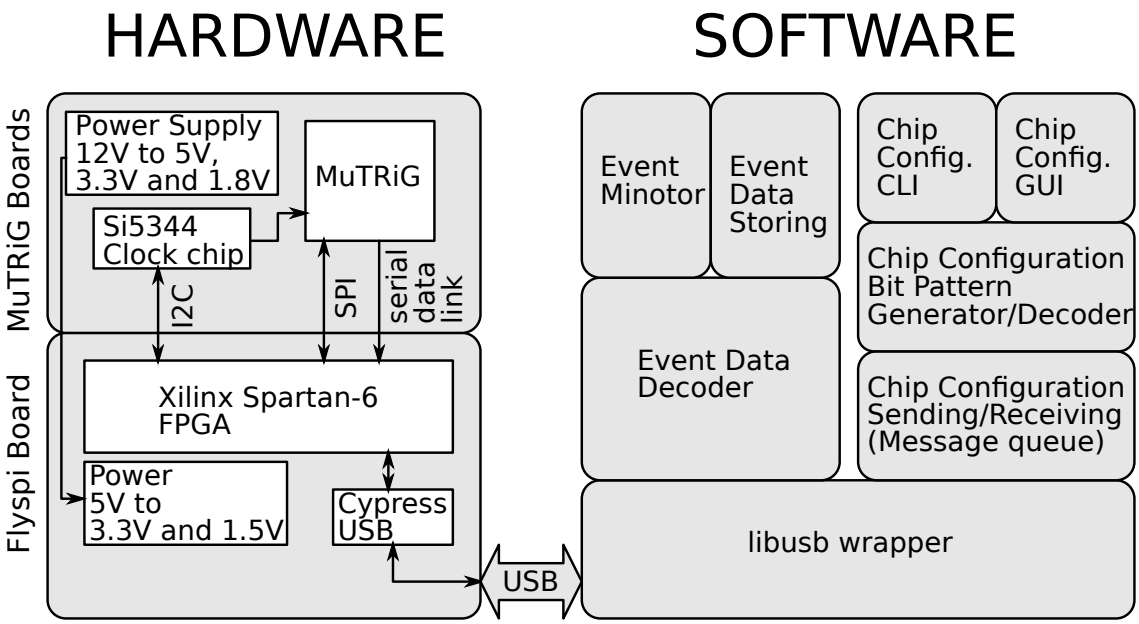


Figure 6.3: Overview of the MuTRiG characterization DAQ system.

USB chuck data to generate MuTRiG events. The decoded event fills the histograms for event monitoring and also write to a ROOT file to be saved in the hard disk. The different type of the data can be distinguished with a defined header field in the USB data.

Figure 6.4 is a detailed diagram of the DAQ firmware on the FPGA. The main part of the DAQ firmware is a finite state machine (FSM) controlling differential logic units for different tasks, which can be put into the following three categories:

1. Read the USB data sent from PC and prepare the data to be sent to PC.
2. Control and configure the components on the MuTRiG boards, such as MuTRiG chip and the Si5344 chip.
3. De-serialize and decode the serial data from the MuTRiG chip.

The communication between the FPGA and the PC is interfaced by the Cypress FX2LP chip on the Flyspi board. The Cypress FX2LP chip has an integrated FIFO buffer for the interface with the FPGA. The FPGA will read this FIFO buffer if there is new data sent from the DAQ software over USB link and will write the data to this FIFO if there is data to be sent to the DAQ software. The Cypress FX2LP chip handles the USB traffic with PC, puts the received data to this FIFO buffer and sends the data in the FIFO to PC.

The `DAQ control` FSM performs different functionalities depends on the command sent from the DAQ software. A reset signal of desired length will be generated on the signal line connected to the MuTRiG chip reset pin if there is a reset command sent from the software. The MuTRiG configuration bit pattern sent over USB will be put to an SPI master unit and sent to the MuTRiG chip over the SPI interface. The SPI read-back data will be put to the Cypress FX2LP FIFO to be

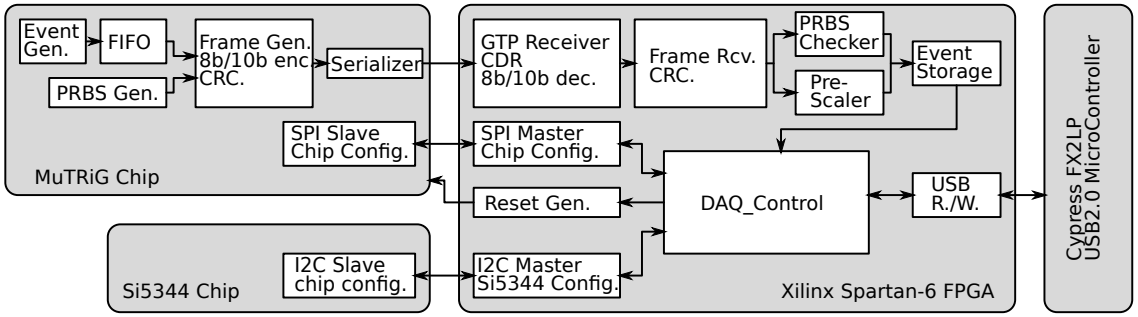


Figure 6.4: Logical Block of the DAQ firmware on FPGA. Related units in the MuTRiG and Si5344 chip is also shown.

sent back to DAQ software. A similar process happens for Si5344 chip configuration, where I2C master unit and I2C interface are used.

A simplified data path in the MuTRiG chip is also shown in Figure 6.4. Due to high bit rate of the serial data link, the 8b/10b encoded serial data from MuTRiG has to de-serialized by a special component on the FPGA, GTP receiver, which supports bit rate up to 3.125 gbps. Once configured correctly, the GTP receive will de-serialize the serial data stream at given bit rate. The GTP receiver will also perform clock data recovery (CDR), byte alignment, Loss-of-Sync (LOS) signal generation and 8b/10b decoding with the circuits in the GTP receiver block. The decoded 8 bit data is fed to downstream frame receiver unit to form 48 bit event words. The unused bit field are filled with zeros for short event structure. The frame counter value is prefixed to the event before sending to the downstream units. The event structure is shown in Table 6.1. The CRC information is checked for each frame in the frame receiver unit. A PRBS checker is implemented at the downstream of the frame receiver unit. If the MuTRiG data is PRBS debug data pattern, then the PRBS checker can be active to check if the PRBS pattern is correct, which is complement of the CRC check in the serial data link quality characterization. As the USB2.0 transmission is not fast enough for MuTRiG data, a pre-scaler unit is implement to store only a fraction of event data.

Besides the MuTRiG hit event data, the information of each received frame is also stored in the event storage unit implemented by a big FIFO buffer. The structure of the frame information data is shown in Table 6.2. The data in the event storage unit will be sent to the DAQ software when the `DAQ control` FSM received the command for fetching data.

6.2 Timing Performance Characterization Measurements

In order to characterize the timing performance of the MuTRiG chip, the timing jitter is firstly measured for the analog front-end and then for full signal/data processing chain the of the MuTRiG chip. The measurement of the timing jitter as a function of the input rate is also performed.

Table 6.1: Structure of the hit event sent from MuTRiG FPGA to PC

Bit	Standard Hit Event	Short Hit Event
[63]	0	0
[62:48]	Frame Number	Frame Number
[47:43]	Channel Number	Channel Number
[42]	T - BadHit	T - BadHit
[41:27]	T - Coarse Counter	T - Coarse Counter
[26:22]	T - Fine Counter	T - Find Counter
[21]	E - BadHit	0
[20:6]	E - Coarse Counter	0
[5:1]	E - Fine Counter	0
[0]	Energy Flag	Energy Flag

Table 6.2: Structure of the frame-info event sent from MuTRiG FPGA to PC

Bit	Frame-info Event
[63]	1
[62:48]	Frame Number
[47:42]	Frame Flag
[41:32]	Frame Length
[31:16]	RRBS Error Count
[15:1]	0
[0]	CRC Error

6.2.1 Analog Front-End Jitter Measurements

The analog front-end jitter is measured with charge injection. The setup to perform analog front-end jitter measurement is shown in Figure 6.5. The pulses from a 10 giga sample per second (GS/s) arbitrary waveform generator[1] is injected into the MuTRiG chip over a capacitor. A capacitance of 15 pF is chosen to emulate the loading of SiPM senors. The injected signals taken by the input stage of the chip and is amplified and discriminated with the fully-differential signal processing circuit in the analog front-end of the MuTRiG chip. The discriminated timing trigger signal is send out of chip by an on-chip LVDS driver to a 40 GS/s oscilloscope[2]. The time difference between the marker signal from the arbitrary waveform generator and the timing trigger from the MuTRiG chip is measured on the oscilloscope. As the output pulses of the arbitrary waveform generator has very low jitter referring to the marker signal. Therefore the jitter between the marker signal of the arbitrary waveform generator and the timing jitter signal from the MuTRiG chip can be measured as the jitter of the MuTRiG analog front-end.

The MuTRiG analog front-end jitter is evaluated for different input charges. In order to investigate the influence of on-board digital activities and the on-chip activities, the analog front-end

[1] Tektronix AWG7102
[2] Lecroy SDA 813Zi

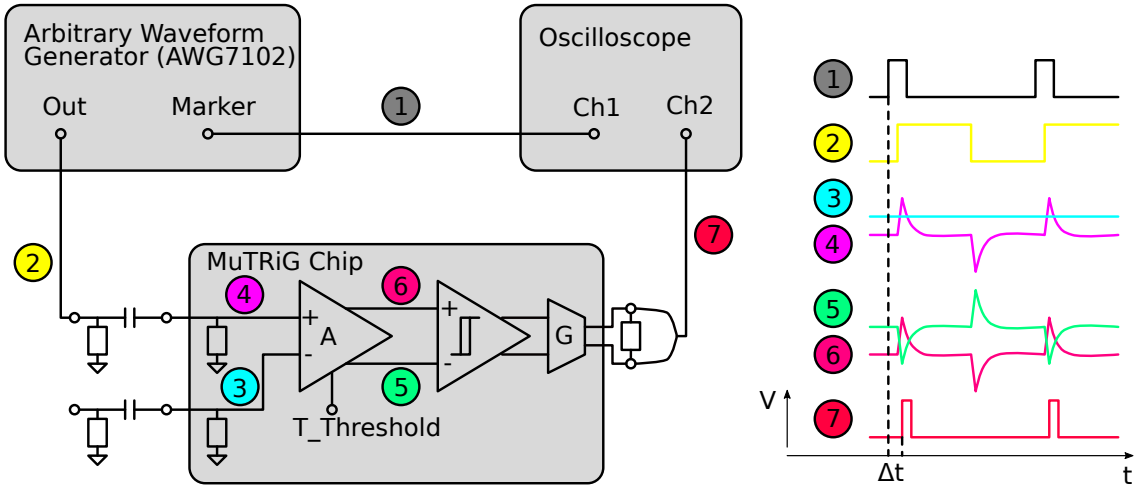


Figure 6.5: Front-end jitter measurement setup.

jitter measurement is carried out in different working environments where the following condition are applied one by one:

1. Only front-end part of the chip is active;
2. FPGA is connected but no clock is generated for the MuTRiG chip;
3. PLL reference clock (PLL_CLK) for TDCs is generated, but the PLL is powered off;
4. The on chip PLL is powered on;
5. The serial data clock (SER_CLK) is generated.

The analog front-end jitter measurement results for all the condition are shown in Figure 6.6. For each working environment, the MuTRiG analog front-end jitter decreases as the increase of input charges. This is due to a faster signal slope for a higher input signal amplitude. In a first order approximation, the jitter for the timing trigger signal σ_t, which is generated by a leading edge discriminator, is smaller for faster signal slope:

$$\sigma_t = \frac{\sigma_v}{k} \tag{6.1}$$

$$k \sim \frac{A * Amp_{signal}}{t_{rise}} \tag{6.2}$$

where σ_v and k are the noise level and the slope of the signal at the input of the discriminator, A is the gain of the amplifier in the channel, Amp_{signal} is the amplitude and the rise time of the input signal and t_{rise} is the rise time of the signal.

In the case when only analog front-end is active, the jitter is less than 11 ps for charges larger than 480 fC, the same charge of 1 photon event from a $3 \cdot 10^6$ gain SiPM device. As more on-board or on-chip parts are activated, the measured analog front-end jitter degrades. Big changes on the analog front-end jitter performance are observed for the generation of PLL reference clock

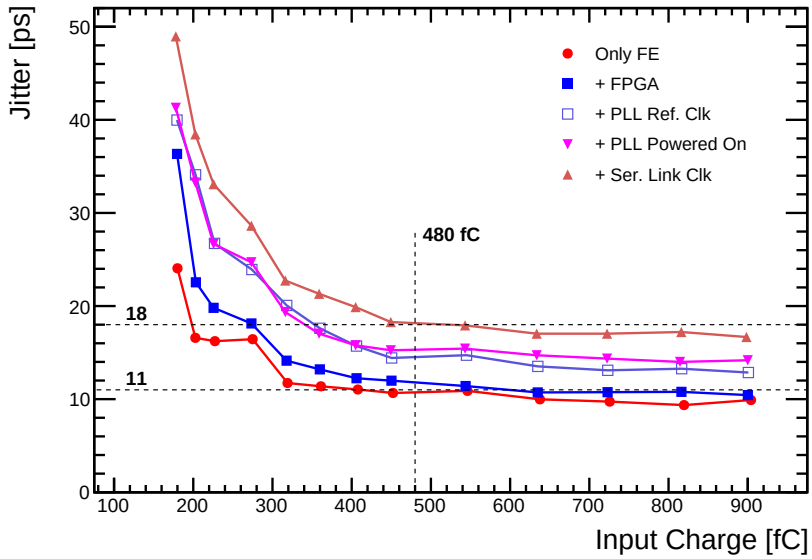


Figure 6.6: Front-end jitter measurement results.

and the serial data link clock. While the powering on the on-chip PLL have little influence on the jitter performance of the analog front-end, which indicate that the on-chip activity has little contribution to the degradation of the analog front-end timing performance and the dominating factors come on the board. For the cases where all the on-board and on-chip part are working, the jitter of the analog front-end is below 18 ps for charges larger than 480 fC.

6.2.2 Full Chain Jitter Measurements

In order to evaluate the timing performance of the chip when using the full signal and data processing chain on the chip, MuTRiG full chain jitter is characterized by measuring the period jitter of the input pulses with front-end, TDC and the digital part of the chip. The test setup for the full chain jitter measurement is shown in Figure 6.7. As similar to the front-end jitter measurement setup, the periodic input pulses are injected to a channel of the chip over a 15 pF capacitor. Instead of monitoring the timing trigger signal in the oscilloscope, the time of arrival information of each pulses is digitized with on-chip TDC and the hit event data is send to DAQ. The period of input pulses is calculated by the time difference between two consecutive events with the time of arrival information of the hit event data. The full chain jitter, which is the timing measurement resolution for the hit events on that channel, equals to the period jitter divided by $\sqrt{2}$:

$$\begin{aligned} t_{period} &= T1 - T2 \\ \sigma_{T1,T2} &= \sigma_{t_{period}}/\sqrt{2} \end{aligned} \tag{6.3}$$

As discussed in section 5.4, the TDC has nonlinearity effect which will result in errors in the

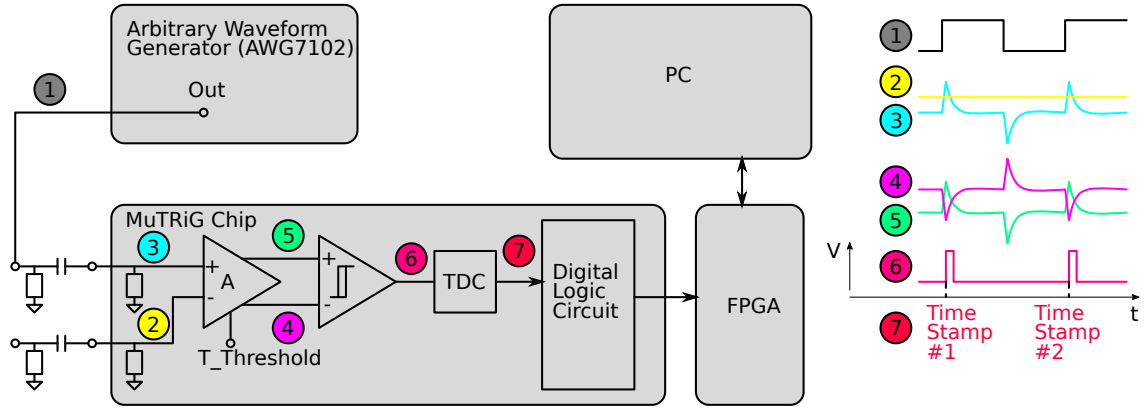


Figure 6.7: Full chain jitter measurement setup.

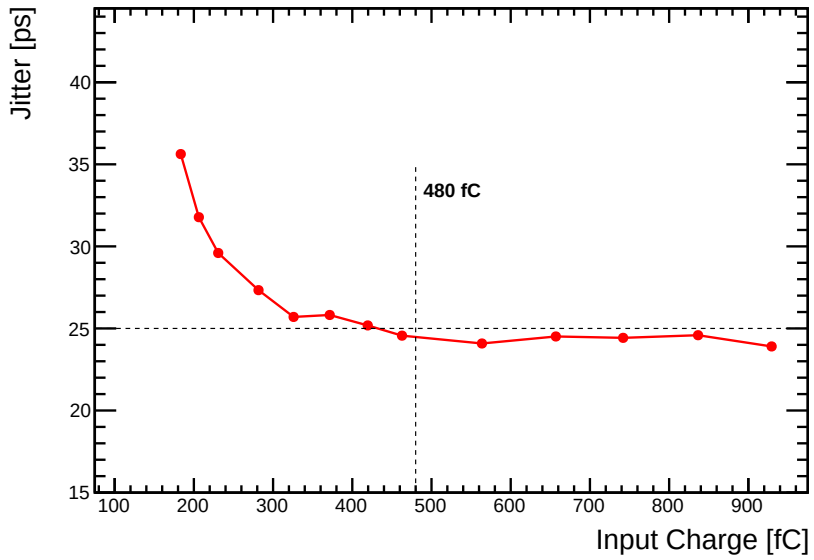


Figure 6.8: Full chain jitter as a function of input charge.

timing measurement. The bin dithering method described in section 5.4 has been applied in this analysis.

Figure 6.8 shows the full chain jitter measurement result. The MuTRiG full chain jitter is lower than 25 ps for charges larger than 480 fC.

6.2.3 Jitter vs Rate

In order to study the influence of rate related analog and digital activities to the timing performance of the chip, MuTRiG full chain jitter is measured with a input charge of 460 fC at different frequencies. The analog front-end jitter is also measured with the same inputs and the same channel settings for comparison.

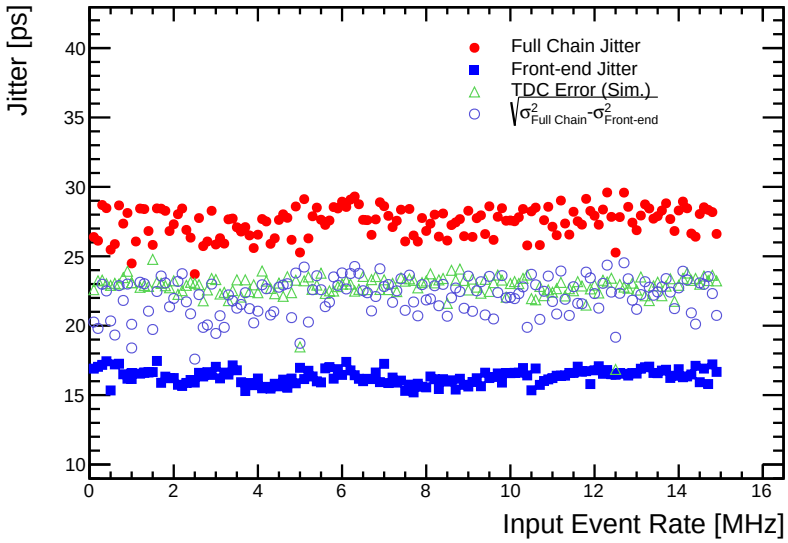


Figure 6.9: Measurement and simulation results of jitter vs rate relationship.

The full chain jitter and analog front-end jitter measurement results are shown in Figure 6.9. The full chain jitter stays between 24 ps to 31 ps for the input frequency up to 15 MHz. And the analog front-end jitter stays within 15 ps and 17 ps for the same input frequency range. No visible correlation between the timing performance of the chip and the input signal frequency is observed.

The timing measurement error from the TDC contributes to the full chain jitter performance. A Monte Carlo simulation has been performed to estimated the error of the TDC. The code density test results from the measurement data are fed into the simulation to emulate the nonlinearity of the TDC. The ideal hit events are generated with fixed periods and zero jitter. These events are digitized by the TDC emulator in the simulation to produce data for extracting the timing measurement error of the TDC. The timing measurement data from simulation is analyzed in the same way as the measurement data and the same DNL correction method is applied in the analysis.

The jitter component of the full chain jitter additional to the front-end jitter is calculated by the following equation for the comparison with the simulated TDC timing measurement error:

$$\sigma_{add} = \sqrt{\sigma^2_{Full\,Chain} - \sigma^2_{Front-end}} \tag{6.4}$$

The TDC measurement error from simulation and the calculated additional jitter component between the front-end jitter and the full chain jitter are both plotted on Figure 6.9. These two sets of data lay on top of each other, indicating that the TDC measurement error is primary part of the additional jitter contribution to the full chain jitter besides the front-end jitter, which is ~23 ps.

6.3 Digital Functionality Validation Measurements

A few new digital functionalities have been implemented on the MuTRiG chip. The validation results of the external trigger functionality and the functionality of the frame generator will be shown here. The characterization of the LVDS transmitter cell, the measurement results of the serial data line quality and the maximum event rate capability will be also presented.

6.3.1 Validation of the External Trigger Functionality

The external trigger functionality allows users to validate the hit events which happen within a matching time window around a external trigger signal. This functionality is very useful for test beam cases, where a trigger signal is available and the relevant events happen is close in time to the trigger signal. With this functionality, The bandwidth of the serial data link can be saved since the irrelevant noise data will not be sent off chip and occupy the bandwidth of the data link. The data analysis can also be benefit from this as the saved data are mostly the relevant hit events and less effort is required to filter the data.

The external trigger functionality is tested with 16 MHz input test signal and 250 kHz trigger signal. Using the time of arrival information of the hit events, the event distribution within a data frame is plotted in Figure 6.10a for three different configurations:

1. The external trigger functionality is turned off.
2. The external trigger functionality is turned on for matching window size of 15 units (One units is 10 clock cycle, 80 ns).
3. The external trigger functionality is turned on for matching window size of 31 units.

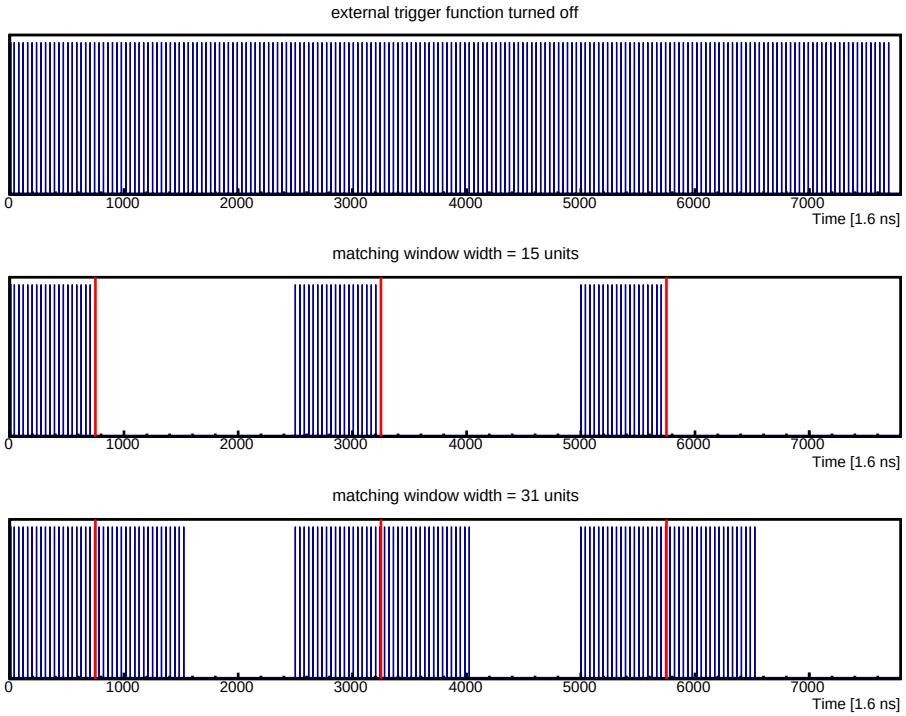
The first hit event in every frame is aligned as time zero for comparison. The red lines indicate the moment when the external trigger signals come. As illustrated in Figure 6.10a, the external trigger functionality works as expected. When the external trigger functionality is tuned off (the top plot), the frame is filled with 16 MHz hit events. When the external trigger functionality is turned on (the second and third plots), only the event within the matching window is saved in the data file.

Figure 6.10b shows the output event rate for different matching window size. The output event rate is expected to be

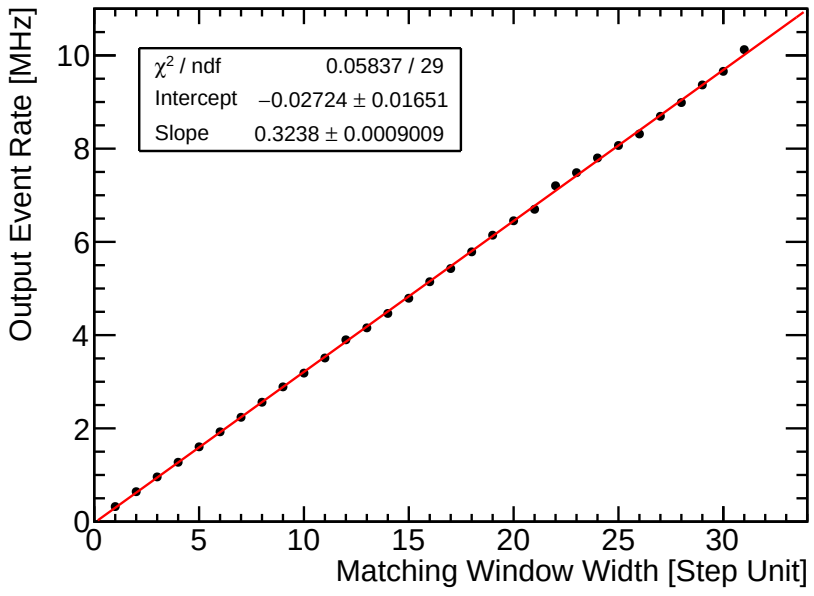
$$Rate_{data} = freq_{input\_signal} \cdot (freq_{external\_trigger} \cdot t_{matching\_windown\_unit} \cdot N) \tag{6.5}$$

By fitting with a linear function, the matching window size unit can be extracted from the slope of the linear function:

$$t_{matching\_windown\_unit} = \frac{Slop}{freq_{input\_signal} \cdot freq_{external\_trigger}} \tag{6.6}$$

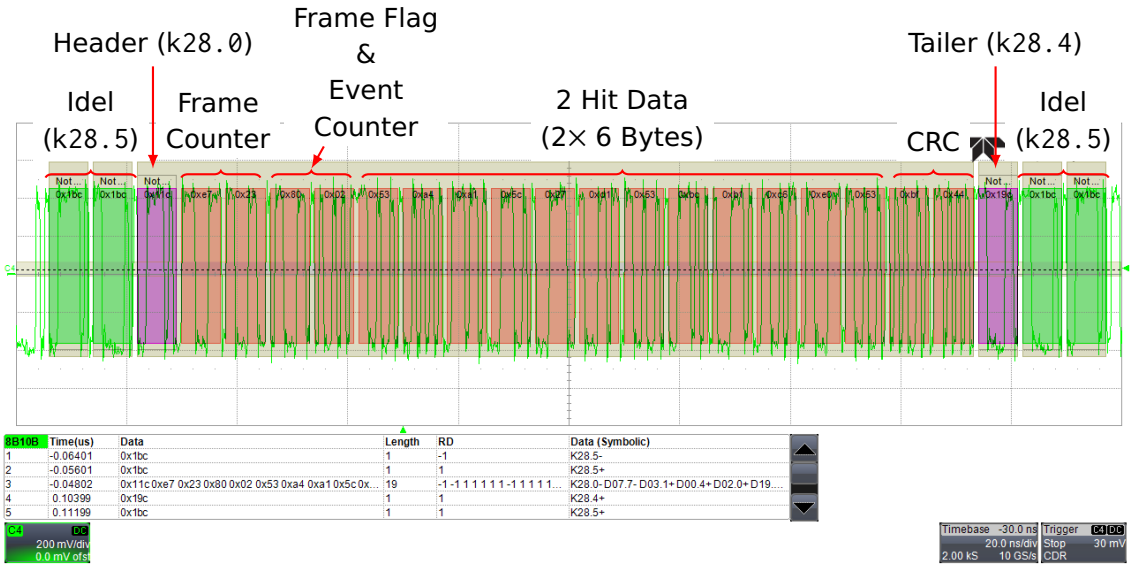


(a) Event distribution in one frame. Top: the external trigger functionality is turned off. Middle and bottom: the external trigger functionality is turned on, and the matching window widths are 15 units and 31 units respectively. The red lines indicate when the external trigger signal come.

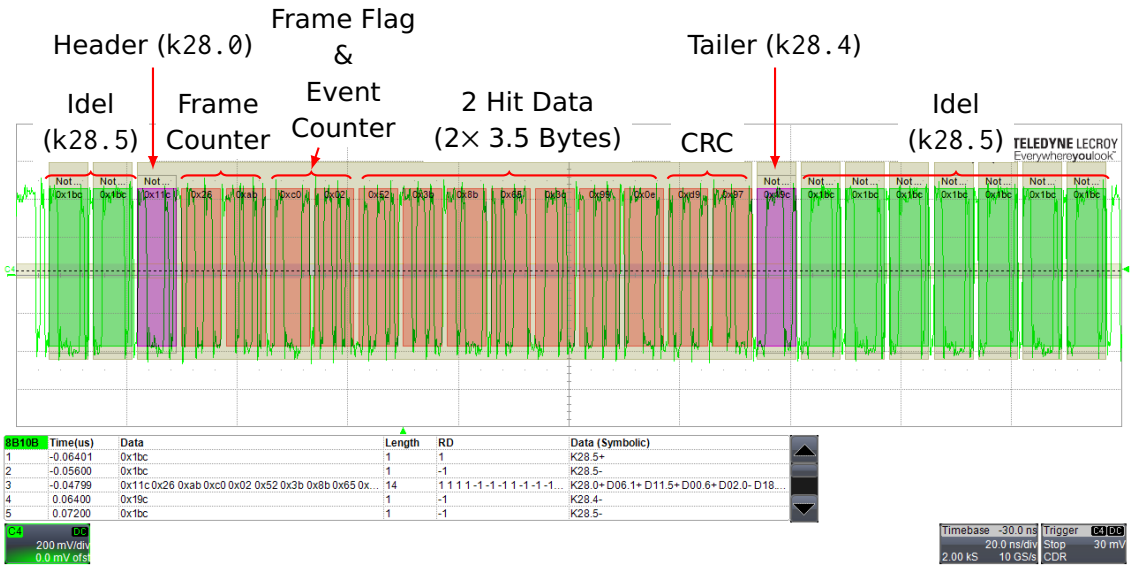


(b) Recorded(output) event rate as a function of matching window width.

Figure 6.10: Validation results of the external trigger functionality.



(a) Standard Event Configuration.



(b) Short Event Configuration.

Figure 6.11: Serial data waveform from the MuTRiG chip decoded by the 8b/10b decoder on the oscilloscope.

As expected, the matching window size is 80 ns, which is exactly 10 times of system clock period.

6.3.2 Validation of the Frame generator module

As discussed in subsection 5.5.4, the frame generator packs the hit events into data frames with a customized protocol. The hit event in the data frame to be sent out can be configured in standard

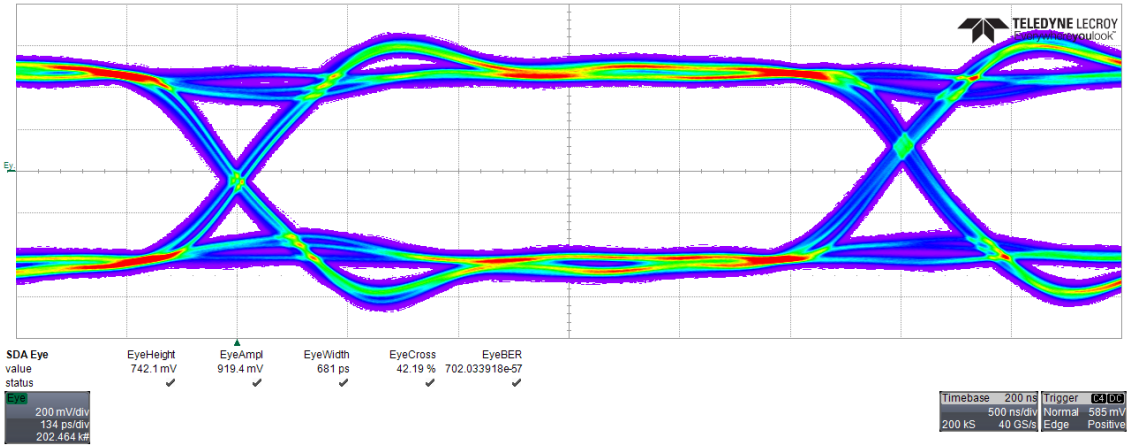
or short event lengths. The validation of the functionality of the frame generator is performed by monitoring the serial data waveforms on the oscilloscope. Two serial data waveforms are shown in Figure 6.11. The color blocks indicate the symbols recognized by the 8b/10b decoder on the oscilloscope, each of which presents ten 8b/10b encoded data on the serial data stream. As shown in Figure 6.11, all the part of the frame, including idle, header, tailer and payload, are correctly decoded by the 8b/10b decoder on the oscilloscope. And these parts of the data frame are packed in a correct order. There are two events in both cases shown in Figure 6.11, which are in the standard and the short hit event structure configuration respectively. The event lengths are 6 bytes and 3.5 bytes respectively, also the same as designed.

6.3.3 LVDS Transmitter Performance

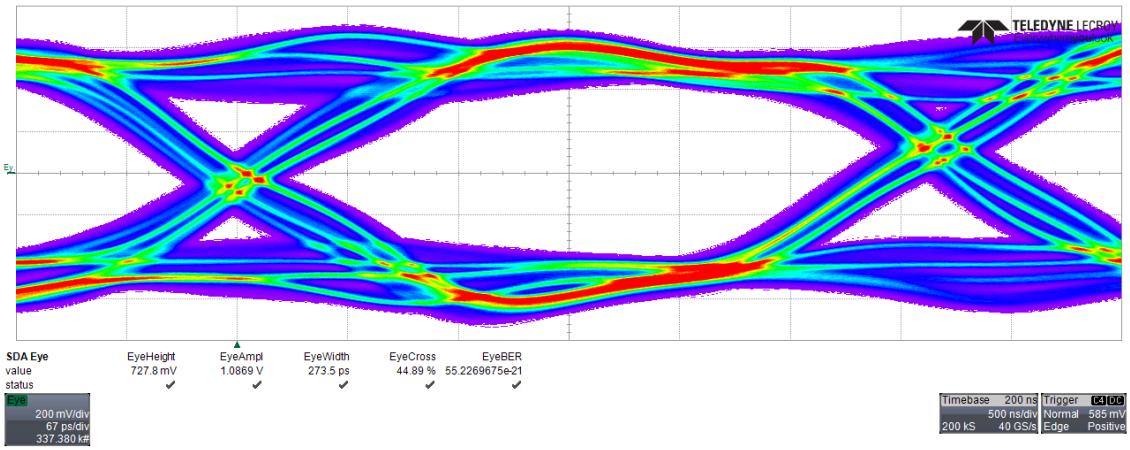
The customized LVDS transmitter is an crucial part for the LVDS serial data link. It is designed to drive the data link at a bit rate of at least 1.25 Gbps. The LVDS transmitter cell is characterized with a test chip submitted in 2015. A demo digital circuit is implemented on the LVDS test chip, including only the RPBS sequence generator, frame generator, 8b/10b encoder and double data rate serializer. A data stream with 8b/10b encoded PRBS patterns is driven by the LVDS transmitter off the chip. The signal waveforms are probed on an external 100 Ω termination resistor and the eye diagram is generated on the oscilloscope. As shown in Figure 6.12a, a widely opened eye diagram has been obtained at a bit rate of 1.25 Gbps. The eye height is 741.1 mV and the eye width is 681 ps. The bit error rate (BER) is at a level of $702 \cdot 10^{-54}$ given by the waveform analysis of the scope. The open eye diagram obtained for 8b/10b encoded PRBS data pattern at a bit rate of 2.5 Gbps is shown in Figure 6.12b. The BER estimated by the scope is at a level of $55 \cdot 10^{-21}$. The low level of estimated BER in both cases shows a good performance of the LVDS transmitter cell.

6.3.4 Serial Data Link Quality

The quality of the serial data link is measured by the bit error rate (BER) measurements on the MuTRiG characterization setup. The MuTRiG chip is configured in the PRBS debugging mode, when the RPBS patterns fill the payload part of the data frames and are sent to the DAQ system. On the DAQ side, both the RPBS pattern sequence and the CRC information are checked on the FPGA to detect bit errors. Data is transfered and taken for more than 37 hours to accumulate enough statistics. The BER is measured for serial data link bit rate up to 1.90 Gbps and no bit error is detected during the data taken, given a upper limit of BER. The BER measurement results are shown in Table 6.3. The BER is $< 5.90 \cdot 10^{-15}$ for serial data link speed of 1.25 Gbps and is $< 3.65 \cdot 10^{-15}$ for serial data link speed of 1.90 Gbps, showing a good link quality of the MuTRiG serial data link.



(a) Bit rate = 1.25 Gbps.



(b) Bit rate = 2.5 Gbps.

Figure 6.12: Eye diagram for the 8b/10b encoded PRBS bit patterns from the LVDS transmitter at bit rates of 1.25 Gbps and 2.5 Gbps.

Table 6.3: Bit error rate measurement results for MuTRiG serial data link.

Serial Data Link Bit Rate	Bit Error Rate
1.25 Gbps	$< 5.90 \cdot 10^{-15}$
1.50 Gbps	$< 4.34 \cdot 10^{-15}$
1.60 Gbps	$< 4.63 \cdot 10^{-15}$
1.90 Gbps	$< 3.65 \cdot 10^{-15}$

6.3.5 Event Rate Measurements

Handling the high rate events from the Mu3e fibre detector is one of the challenges for the MuTRiG ASIC.

The maximum event rate of the chip is characterized by injecting high rate test pulses to several

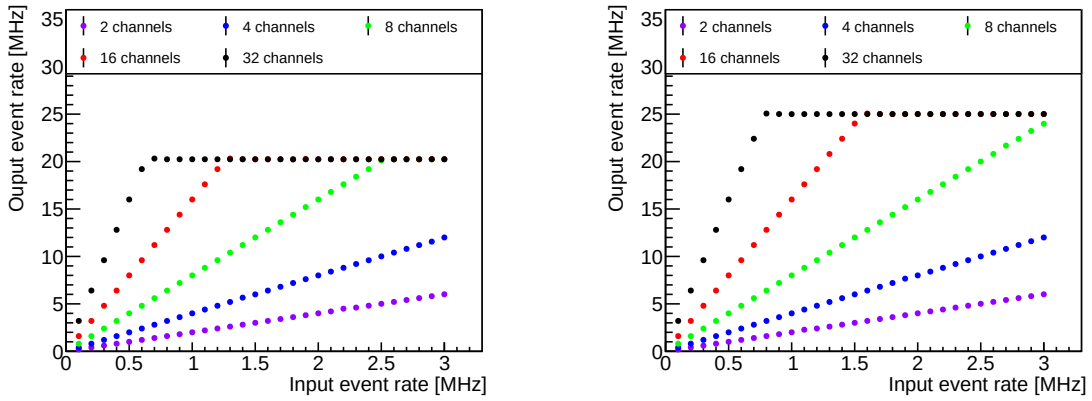


Figure 6.13: Output Event rate as a function of the input event rate. The test pulse is injected into 2, 4, 8, 16, 32 channels respectively. Left: standard event length configuration, where the hit event data has 48 bit. Right: short event length configuration, where the hit event data has 27 bit.

channels of the chip and measuring the output event rate. The input signal rate and the number of channels are gradually increased to search for the limit of the output event rate. The test setup is similar to that of full chain jitter measurement in Figure 6.7. The thresholds of each channel has been tuned such that all the channel will be triggered by the test pulses but not by noise. As described in subsection 5.5.4, the structure of the hit event to be send to DAQ can be switched from a standard event structure configuration of 48 bits to a short event structure configuration of 27 bits, to achieve higher event rate capability.

Figure 6.13 shows the maximum event rate measurement results for both the standard and short hit event configuration at the data link bit rate of 1.25 Gbps. For both configurations, the output event rate increase linearly with the input event rate before reaching the maximum value. For the standard hit event configuration, the event rate is limited at 20.24 MHz (on average 632 kHz/channel). At the maximum event rate cases, the serial data frames are filled fully with the event data, showing that this maximum event rate is limited by the bit rate of serial data link.

For the short hit event configuration, the maximum event rate is 25 MHz (on average 781 kHz/channel), which is exactly 1/5 of the system clock frequency and does not scaled with the change of the event length if compared with that of the standard hit event configurations case. This limit doesn't come from the bit rate of the serial data link, but come from the digital circuit on the chip. The L2 arbiter has been is identified to be the bottle neck of the digital logic circuit, which processes hit event data in a sequential way and each hit event takes five system clocks cycles. A new L2 arbiter, which process the event data in a pipelined way, will be implemented in the next version of the ASIC to remove this bottleneck. By this modification, the maximum event rate at the short hit event configuration will be limited by the bit rate of the serial data link, which is expected to be $\sim$ 35 MHz ($\sim$ 1.1 MHz/channel).

The maximum event rate of the chip is also measured for different serial data link rate. Fig-

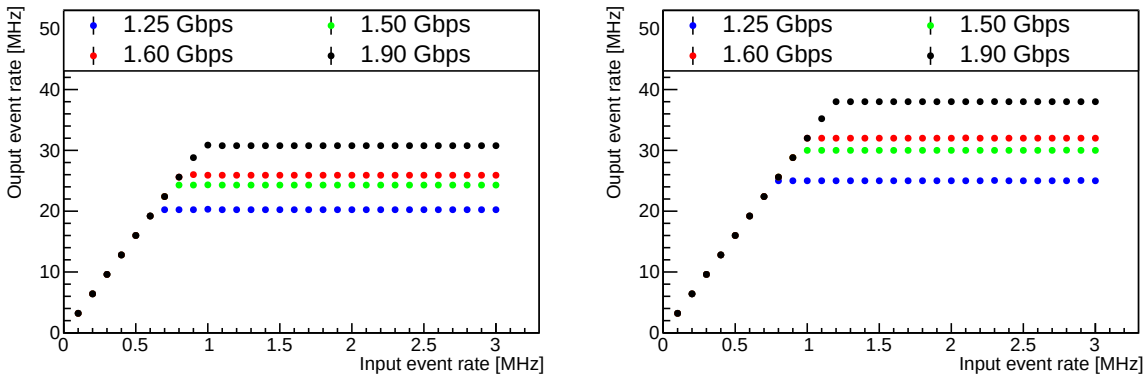


Figure 6.14: Event rate measurement result for different serial data link bit rate with the standard (left) and the short (right) event configurations.

Table 6.4: Summary of event rate measurement results for different serial link clock frequencies.

Serial Data Link Bit Rate	Serial Link Clock Frequency	Max. Event Rate (Standard Event Length)	Max. Event Rate (Short Event Length)
1.25 Gbps	625 MHz	20.24 MHz (632 kHz/ch)	25 MHz (781 kHz/ch)
1.50 Gbps	750 MHz	24.29 MHz (759 kHz/ch)	30 MHz (781 kHz/ch)
1.60 Gbps	800 MHz	25.91 MHz (810 kHz/ch)	32 MHz (1 MHz/ch)
1.90 Gbps	950 MHz	30.77 MHz (962 kHz/ch)	38 MHz (1.19 MHz/ch)

ure 6.14 shows the event rate measurement results for serial data link rate up to 1.9 Gbps for both the standard and short hit event structure configurations. The maximum event rate of the chip is scaled with the serial data link bit rate. And for the 1.9 GHz serial clock frequency, the maximum event rates of the chip are 961 kHz/channel and 1.19 MHz/channel respectively for the standard and short hit event structure configuration. A summary of the maximum event rate measurement results for different serial data link clocks are listed in Table 6.4.

6.4 Test Beam With Mu3e Tile Detector Prototype

In order to verify the functionality and the timing performance of the MuTRiG chip at the realistic condition, the MuTRiG chip has been tested with the Mu3e Tile detector prototype in a test beam campaign at DESY.

Figure 6.15 shows test beam setup for the MuTRiG and Mu3e Tile detector module. The Mu3e tile detector test module is designed and assembled by the Mu3e Tile detector group at Kirchhoff Institute for Physics, especially for the test beam with MuTRiG and detector performance study

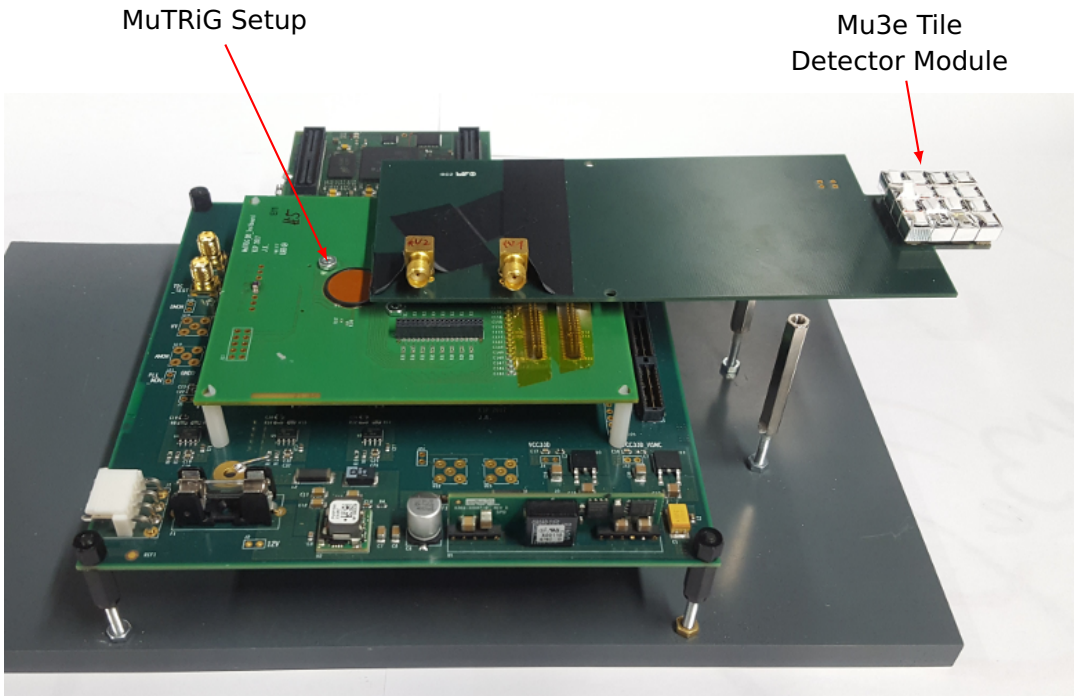


Figure 6.15: The MuTRiG and Mu3e Tile Detector test beam setup.

with oscilloscope. It consists of 16 scintillator tiles readout by SiPM photon detectors arranged in a 4 by 4 matrix, which is the same as in the Mu3e tile detector submodule.

The scintillator tiles are built from *Ej-228* plastic scintillator material [50] which has a fast rise and decay time constant for fast timing applications and will be used as the scintillating material for the Mu3e Tile detectors. As the tile detector module designed for the Mu3e experiment, the scintillating tiles has two different dimensions: $6.3\,\text{mm} \times 6.2\,\text{mm} \times 5.0\,\text{mm}$ for the center tiles and $7.44\,\text{mm} \times 6.2\,\text{mm} \times 5.0\,\text{mm}$ for the edge tiles. Each tile is wrapped with ESR reflector foil [86] to increase the photon collection efficiency. A small window with the size of the SiPM active area is cut out to let the scintillating light reach the photon sensor.

14 of the 16 photon sensor are Hamamatsu S13360-3050PE MPPCs, which are of the same type as the photon sensors in the baseline design of the Mu3e tile experiment. The breakdown voltages of these photon sensors are ~51.66 V. In the other two channels, two new type of MPPCs are used to evaluate their performance for the Mu3e tile detector design. The scintillating tiles are glued to the SiPM to ensure a well-controlled and good light transmission between the tiles and the SiPMs. The SiPMs are directly soldered on long PCB which distributes the SiPM signals to the mate connectors of SiPM input connector on the MuTRiG boards. As shown in the Figure 6.15, the detectors sits out side of the MuTRiG boards on the setup such that beam will not directly hit the DAQ FPGA and cause operation errors due to single event upset in the FPGA. The whole setup is placed in a light tight dark box during the test.

The setup was tested in the test beam 24 area at Deutsches Elektronen-Synchrotron (DESY).

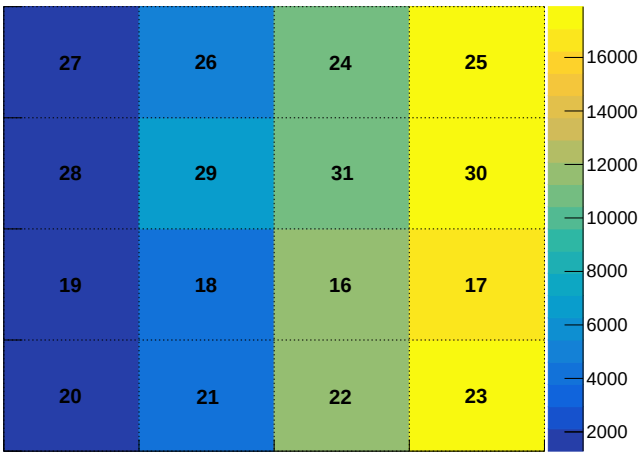


Figure 6.16: The hit map of a run in test beam. The numbers on the hit map are the channel number in the data for the detector at corresponding position.

The electron beam with an energy of ~2.4 GeV was sent to the experiment area. At this energy, the electrons are minimum ionization particles (MIPs) as in the Mu3e experiment. During the test, the SiPMs of the same types were operated in the same High Voltages (HVs). And the MuTRiG chip was configured in a way that the same settings were applied to all the channels. Several sets of data was acquired with 2-dimensions parameter scan for different SiPM operation voltage and MuTRiG timing threshold. The performance of the setup are evaluate with off-line analysis.

As the hit map shown in Figure 6.16, the electron beam was mainly going through the channels in the same column and these channels can be used for coincidence timing analysis. The channels in the last column (channel 25, 30, 17 and 23) have highest statistics and the SiPMs in these four channels are of the same type as the baseline design for the Mu3e tile detector. Thus these four channels are chosen to evaluate the timing performance of the MuTRiG for the readout of the Mu3e tile detector.

The energy spectrum of the electrons on these four investigated channels under the same test condition is shown in Figure 6.17. Most of the recorded events fall into the Landau peak on the spectrum. Those are the events when the electrons enter and leave the tile on two parallel surfaces. Those electrons travelled in the traces with similar lengths and deposited similar amount of energy in the tiles. On the tail of the Landau peaks, one or two additional peak are visible. These peaks come from the events when two or three such electrons are travel though the tile in the same time and deposit double or triple amount of energy in the tiles. As the detector module edge is not perfectly parallel to the beam direction, some electrons enter the tile on the front surface of the tile and leave the tile at the side surface. The travelling trace lengths of these electrons in the tiles are shorter than the above cases, thus the deposited energy are smaller.

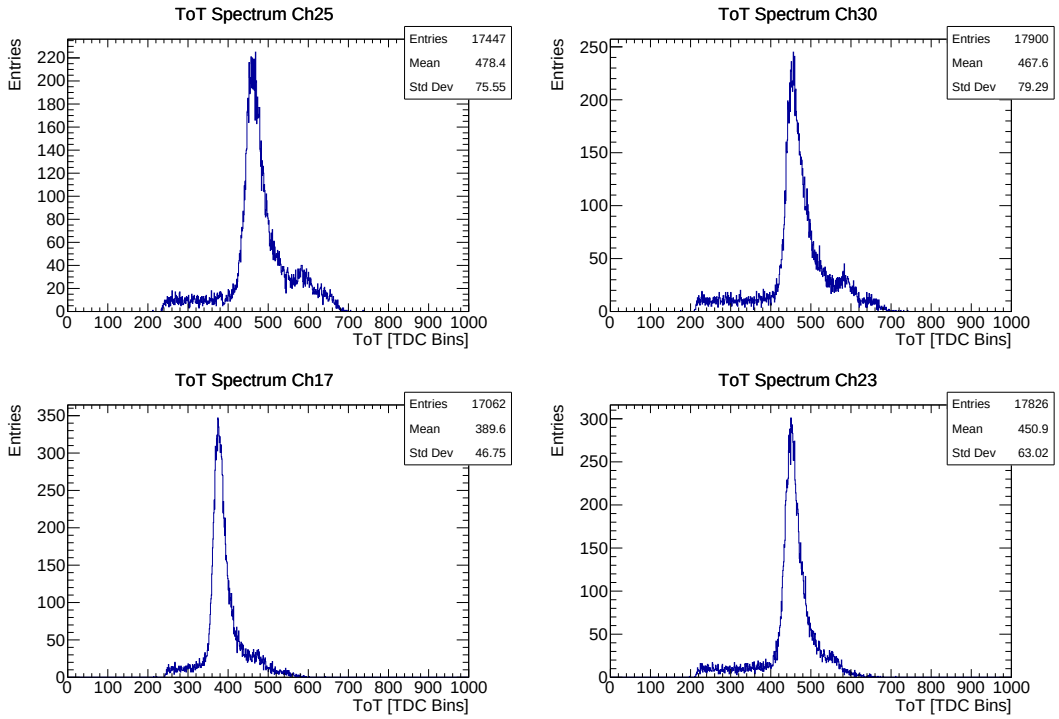


Figure 6.17: The energy spectrum of the MIP electrons recorded on channel 25, 39, 17 and 23.

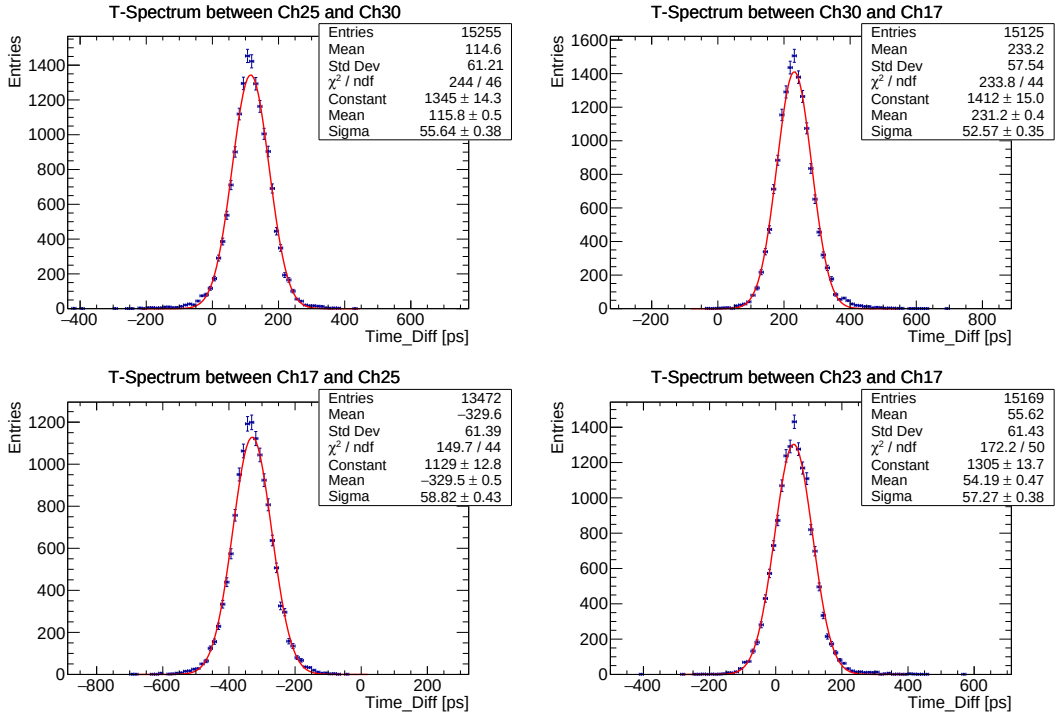


Figure 6.18: Coincidence timing spectrum between channel 25 and 30, 30 and 17, 17 and 25, and between channel 23 and 17.

Depends on the entering position of the electron and its entering angle, the trace length of the electron has a range from zero to the full length as that of the event in the Landau peak. And the deposited energy of these electrons range from zero to the same deposited energy as the energy in the Landau peak. These events contribute to the part of the energy spectrum which is on the left side of the Landau peak.

No energy cut is applied in the data analysis in order to assess the timing performance of the MuTRiG chip with the tile detector.

The timing performance of each channel can be deduced from the coincidence timing measurements between channels. Let T_{ch_i}, T_{ch_j} and T_{ch_k} be the timing measurement on channel i, j and k, and $t_{ch\_i\_j}$, $t_{ch\_i\_k}$ and $t_{ch\_j\_k}$ be the time difference of the coincidence events between these two channels. Then we have

$$t_{ch\_i\_j} = T_{ch\_i} - T_{ch\_j} \tag{6.7}$$
$$t_{ch\_i\_k} = T_{ch\_i} - T_{ch\_k} \tag{6.8}$$
$$t_{ch\_j\_k} = T_{ch\_j} - T_{ch\_k} \tag{6.9}$$
$$\tag{6.10}$$

And the coincidence resolution between every two channels are

$$\sigma^2_{t_{ch\_i\_j}} = \sigma^2_{T_{ch\_i}} + \sigma^2_{T_{ch\_j}} \tag{6.11}$$
$$\sigma^2_{t_{ch\_i\_k}} = \sigma^2_{T_{ch\_i}} + \sigma^2_{T_{ch\_k}} \tag{6.12}$$
$$\sigma^2_{t_{ch\_j\_k}} = \sigma^2_{T_{ch\_j}} + \sigma^2_{T_{ch\_k}} \tag{6.13}$$
$$\tag{6.14}$$

Thus we can extract the timing resolution of each channel:

$$\sigma_{T_{ch\_i}} = \sqrt{\frac{\sigma^2_{t_{ch\_i\_j}} + \sigma^2_{t_{ch\_i\_k}} - \sigma^2_{t_{ch\_j\_k}}}{2}} \tag{6.15}$$
$$\sigma_{T_{ch\_j}} = \sqrt{\frac{\sigma^2_{t_{ch\_i\_j}} + \sigma^2_{t_{ch\_j\_k}} - \sigma^2_{t_{ch\_i\_k}}}{2}} \tag{6.16}$$
$$\sigma_{T_{ch\_k}} = \sqrt{\frac{\sigma^2_{t_{ch\_i\_k}} + \sigma^2_{t_{ch\_j\_k}} - \sigma^2_{t_{ch\_i\_j}}}{2}} \tag{6.17}$$
$$\tag{6.18}$$

As shown in Figure 6.18 are the spectrum of t_{ch25_30}, t_{ch30_17}, t_{ch17_25} and t_{ch17_25} under one of the test configuration. The Gaussian function is fitted to the data over a range of $\pm 6\ \sigma$ to exact the coincidence timing resolutions between those four pairs of channels.

With Equation 6.18, timing performance of the four channels are exacted from the data taken under different applied SiPM bias voltages and different MuTRiG timing threshold settings.

The timing resolution of channel 25, 30, 17 and 23 at all the test configurations during the 2 dimension parameters scan are shown in Figure 6.20 and Figure 6.22. The MuTRiG and the Mu3e tile detector module have shown an excellent timing performance in the beam test. Channel 33 shows the best timing performance among them. It achieves ~35 ps over a large parameter space. And the timing jitter values obtained for channel 25 and channel 17 are lower than 45 ps for most of the configurations. Channel 23 shows worst performance among them, which results from the bubbles between the scintillating tile and the SiPMs during the assembly. Even though, channel 23 still achieve a timing resolution of lower than 50 ps for 1/3 of the parameter space. Overall, the timing resolution of the four channels are all below 50 ps in a large parameter space of:

$$\begin{aligned} 54.0 < \text{HV} < 56.4 \\ 0 < \text{timing threshold} < 26 \end{aligned} \tag{6.19}$$

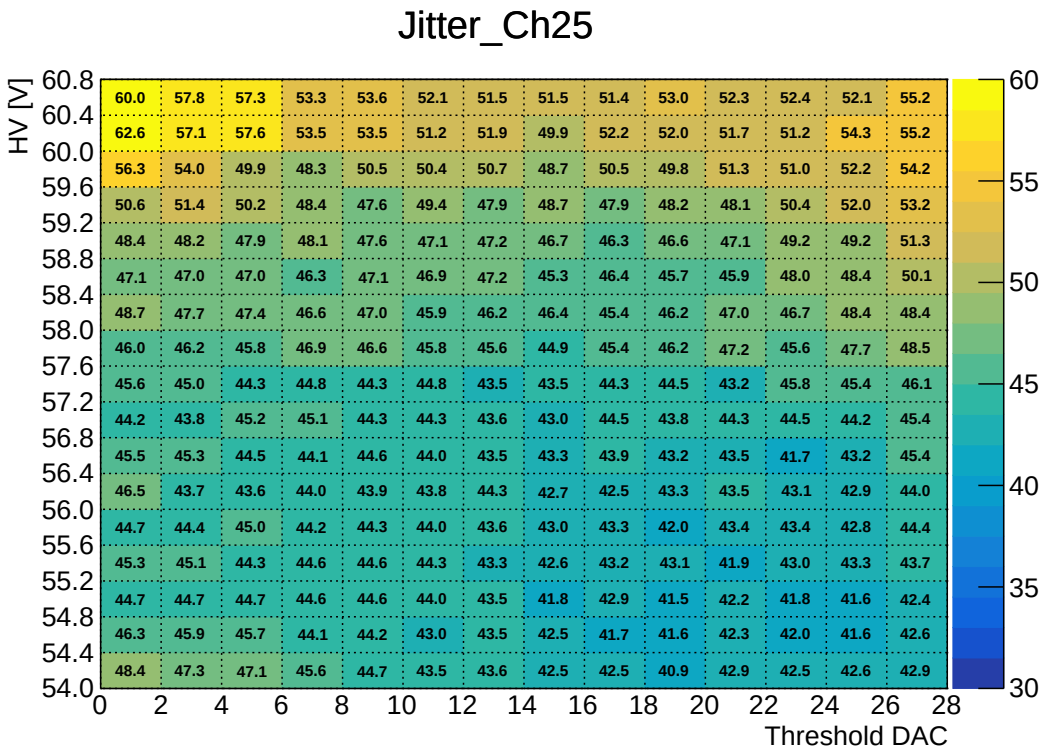


Figure 6.19: Timing resolution of channel 25 at all the tested configurations.

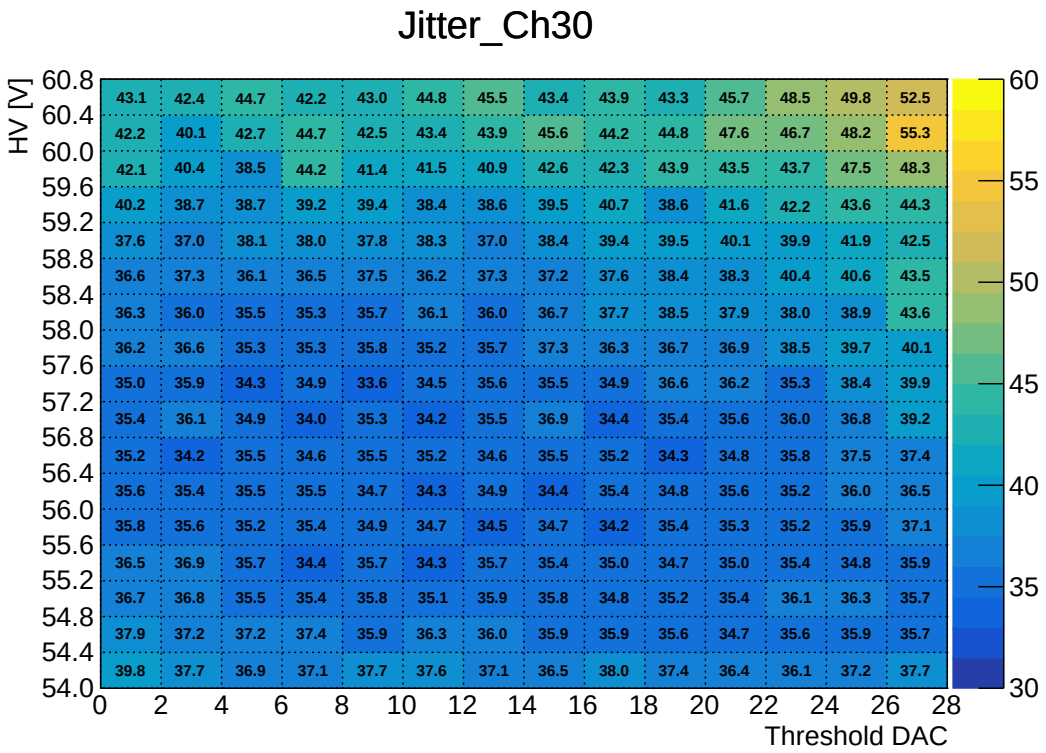


Figure 6.20: Timing resolutionof channel 30 at all the tested configurations.

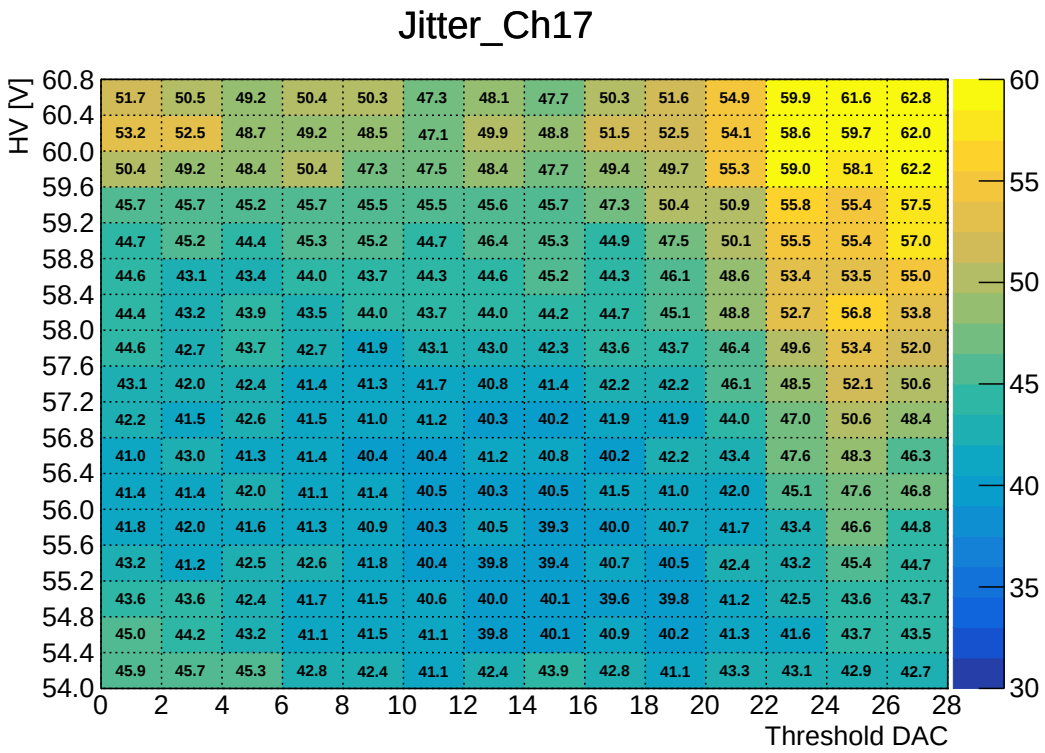


Figure 6.21: Timing resolution of channel 17 at all the test configurations.

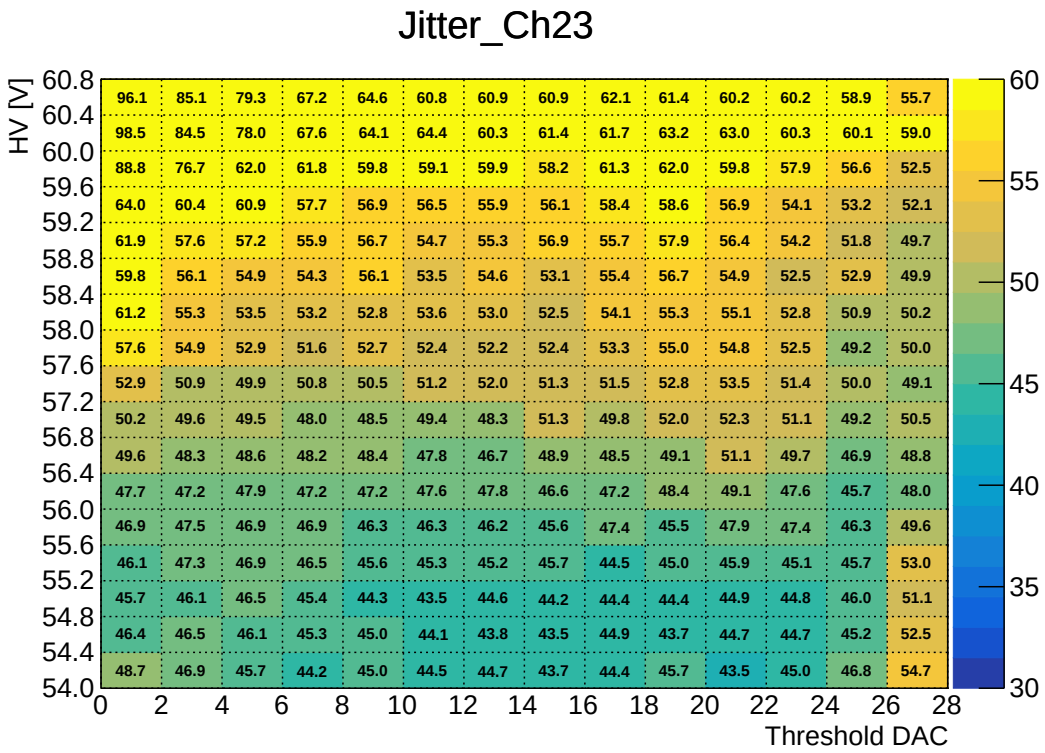


Figure 6.22: Timing resolution of channel 23 at all the test configuration.

Chapter 7

Summary

The Mu3e experiment is aiming at probing for new physics by searching for the charged lepton violating decay $\mu^+ \to e^+e^+e^-$. This process is extremely suppressed in the Standard Model with a branching ratio $\mathcal{B} < 10^{-54}$. While in a wide range of models for physics beyond the Standard Model, this process is significantly enhanced such that it might be in reach of being detected experimentally.

The ultimate goal of the Mu3e experiment is to search for the $\mu^+ \to e^+e^+e^-$ decay process with a branching ratio sensitivity of 10^{-16} at 90 % CL, improving the current best limit by four orders of magnitude. During the phase I operation of the experiment, a single event sensitivity of $2 \cdot 10^{-15}$ is targeted, which would require observing at least $2.5 \cdot 10^{15}$ muon decays and suppressing any background process to a level below $2 \cdot 10^{-15}$. In order to observe enough muon decays in a reasonable measurement time of around one year, the experiment will be running at a muon stopping rate as high as 10^8 Hz, requiring high rate capability from the detectors and readout electronics. There are two main background sources for the experiment: the internal conversion decay $\mu^+ \to e^+e^+e^-\nu_e\overline{\nu}_\mu$ and the accidental background of two or three uncorrelated muon decays forming a signature similar to the target signal. The internal conversion background can be suppressed by precise momentum measurements. The suppression of the accidental background relies on an excellent momentum, vertex and timing resolution provided by different detector systems.

The Mu3e fibre detector and the Mu3e tile detector will provide precise timing measurements. They are built from organic scintillating fibres and tiles read out by Silicon Photomultipliers. A good timing resolution of 500 ps is required for the fibre detector and 100 ps for the tile detector in order to suppress the accidental background by more than two orders of magnitude. In addition, the readout electronics of the fibre detector need to provide an event rate capability up to 1 MHz/channel. The total number of more than 9000 detector channels and these high specifications require development of a dedicated readout ASIC.

This thesis presents the development of the MuTRiG ASIC, which is designed for the readout of SiPMs with precise timing resolution and high event rate capability. MuTRiG is dedicated to the readout of the Mu3e fibre and tile detectors. The timing performance characterization

results of the chip show a jitter of less than 18 ps from the analog channel for charges larger than 480 fC. The full chain jitter of the MuTRiG, when the on-chip TDC channels are used for timing measurements, is lower than 25 ps for 480 fC charge, with the addition ~23 ps jitter contributed from the TDC. This clearly shows that the chip is capable of performing timing measurements with resolution less than 100 ps. Furthermore, the influence of the input event rate to the jitter of the chip is tested up to 15 MHz and no apparent change is observed for the rates studied.

A customized LVDS transmitter cell and a double data rate serializer have been developed to provide a 1.25 Gbps serial data link to transfer the hit event data to the DAQ. The transmitted digital hit event data can be switched to a structure with shorter length to further increase the bandwidth of the output data link. In the characterization measurements, the LVDS transmitter has produced an opened eye diagram at bit rate up to 2.50 Gbps, showing its good performance for driving the serial data link. The measured maximum event rate at the bit rate of 1.25 Gbps is 632 kHz/channel for the standard event structure configuration and 781 kHz/channel for short event structure configuration. The maximum event rate does not scale with the changed hit event length due to a bottleneck in the digital data path of the chip. The bottleneck will be removed in the final version of the chip. The chip is capable of working at higher serial data link bit rate of 1.9 Gbps, giving a maximum event rate of 962 kHz/channel and 1.1 MHz/channel respectively for the standard and short event structure configurations, which would be sufficient for the readout of fibre detector prototype.

New digital functionalities, such as the external trigger and the CRC check, are implemented for convenient and reliable operation of the chip. The upper limit of bit error rate of the MuTRiG serial data link is tested to be in a order of $\mathcal{O}(10^{-15})$ up to a bit rate of 1.9 Gbps.

The MuTRiG chip has been tested with the Mu3e Tile detector prototype during a test beam campaign at DESY. An excellent channel timing resolution of <50 ps has been obtained over a large chip configuration parameter range, confirming the performance and functionality of the chip. This also suggests a broad parameter space can be used without significant worsening the resolution and no fine tuning for individual channel is required a proper timing resolution.

Based on the obtained characterization results, it can be concluded that the current version of the MuTRiG chip provides excellent performance and utile functionalities for the development and prototyping of the Mu3e timing detector prototypes. The final version of the MuTRiG chip with minor changes in the digital part is expected to be submitted soon. After characterization of that chip, mass production and packaging of the final version of the MuTRiG chip is foreseen for the construction of the Mu3e timing detectors.

Appendix

Appendix A

Lists

A.1 List of Figures

A.2 List of Tables

Appendix B

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