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Trajectory Sensor and Readout Electronics of a Cosmic Dust Telescope

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Abstract

An Application Specific Integrated Circuit (ASIC) is developed for the processing of electrostatic signals from a trajectory sensor for cosmic dust. The detector is assembled of multiple wire electrodes which allow the determination of direction, speed and charge of cosmic dust. The circuit consists of two units, a low noise charge sensitive amplifier optimized for a specified detector capacitance and a multi-channel digital transient recorder. The last converts analog signals on 32 channels and buffers the data in a static memory. A controller coordinates the recording of the data and the serial readout on a trigger event. The two units are operated in a mixed-signal network performing a transient recording of a multi-channel low noise charge measurement. Physical separation of the individual front-end amplifiers allows the optimization of the detector capacitances. Circuit design and simulation, as well as successful system tests are presented.

Zusammenfassung

Trajektoriensensor und Ausleseelektronik eines kosmischen Staubteleskops:
Im Rahmen der vorliegenden Arbeit wurde ein ASIC (Application Integrated Specific Circuit) für die Verarbeitung von elektrostatischen Signalen eines Trajektoriensensors für kosmischen Staub entwickelt. Der Detektor besteht aus mehreren Drahtelektroden, die es erlauben, Richtung, Geschwindigkeit und Ladung von kosmischen Staubteilchen zu bestimmen. Der Schaltkreis besteht aus zwei Einheiten, einem Ladungsverstärker mit geringem Rauschpegel, optimiert für eine definierte Detektorkapazität, sowie einem digitalen Transientenrekorder. Dieser wandelt analoge Signale auf 32 Kanälen und speichert die Daten in einem statischen Memory zwischen. Eine Steuereinheit koordiniert die Aufnahme der Daten und das serielle Auslesen nach einem Triggersignal. Die zwei Einheiten werden in einem Mixed-Signal-Netzwerk betrieben, um eine Transientenaufnahme einer rauscharmen Ladungsmessung auf mehreren Kanälen zu machen. Die räumliche Trennung der einzelnen Vorverstärker erlaubt eine Optimierung der Detektorkapazitäten. Schaltungsdesign und Simulation, sowie erfolgreiche Systemtests werden präsentiert.

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Chapter 1

Introduction

1.1 Dust in Space

The study of dust in space started already in the 17^{th} century with the observation of the zodiacal light. The importance of cosmic dust for the planet formation process was realized and the first theoretical models were developed by Laplace in 1796 [1]. In the local universe, half of the stellar radiative energy in ultraviolet and optical wavelengths is absorbed by dust grains and re-radiated thermally in far infrared [2]. Therefore, dust is important for the shape of spectral energy distributions of galaxies from ultraviolet to far infrared.

Cosmic dust is a general term for the smallest solid bodies in space. They can be defined as grains with sizes of 0.02 μm .. 200 μm. The steps from condensation of single particles, the agglomeration to fluffy dust particles and the final accretion to planets are still not reliably understood [3]. Comets count as residuals of the formation of our own solar system [4]. Cometary dust should give hints on the formation and development of our solar system.

Many sources of dust are known by now. From the stellar winds of evolved stars, new dust is formed and is ejected into interstellar space. Dust is also produced by asteroid collisions, cometary activity and collisions in the inner solar system and in the Kuiper Belt [5]. Lately, the Sub-Millimeter Common User Bolometer Array (SCUBA) discovered the immense potential of dust generation of supernovae observing the Cassiopeia A supernova remnant.

With the beginning of space age, the in-situ analysis of cosmic dust in the interplanetary space became possible. So, the requirement for new measurement techniques arose. The first in-situ measurements comprised impact ionization experiments onboard Pioneer 8 and 9. With Helios, Galileo and Ulysses the dust environment between 0.3 AU and 5 AU in the ecliptic plane was reliably explored with instruments based on impact plasma detection. After its fly-by at Jupiter, the dust detector on board the Ulysses spacecraft detected the interstellar dust (ISD) flow, predominantly from a direction that was opposite to the expected impact direction of interplanetary dust grains [6]. The identification of ISD is

based on geometrical and dynamical arguments. It has been known that interstellar gas flows through the planetary system with a speed of 26 km/s in the direction of 73° ecliptic longitude and -5° ecliptic latitude [7, 8]. Before and after the Ulysses fly-by at Jupiter this direction was opposite to the prograde direction of Jupiter. The fact that the orbits of dust particles are predominantly retrograde at the Jupiter distance is very hard to explain without the assumption that the dust is from an interstellar source, since most of the heliospheric dust is moving on prograde orbits. Figure 1.1 shows a compilation of sources and formations of cosmic dust.

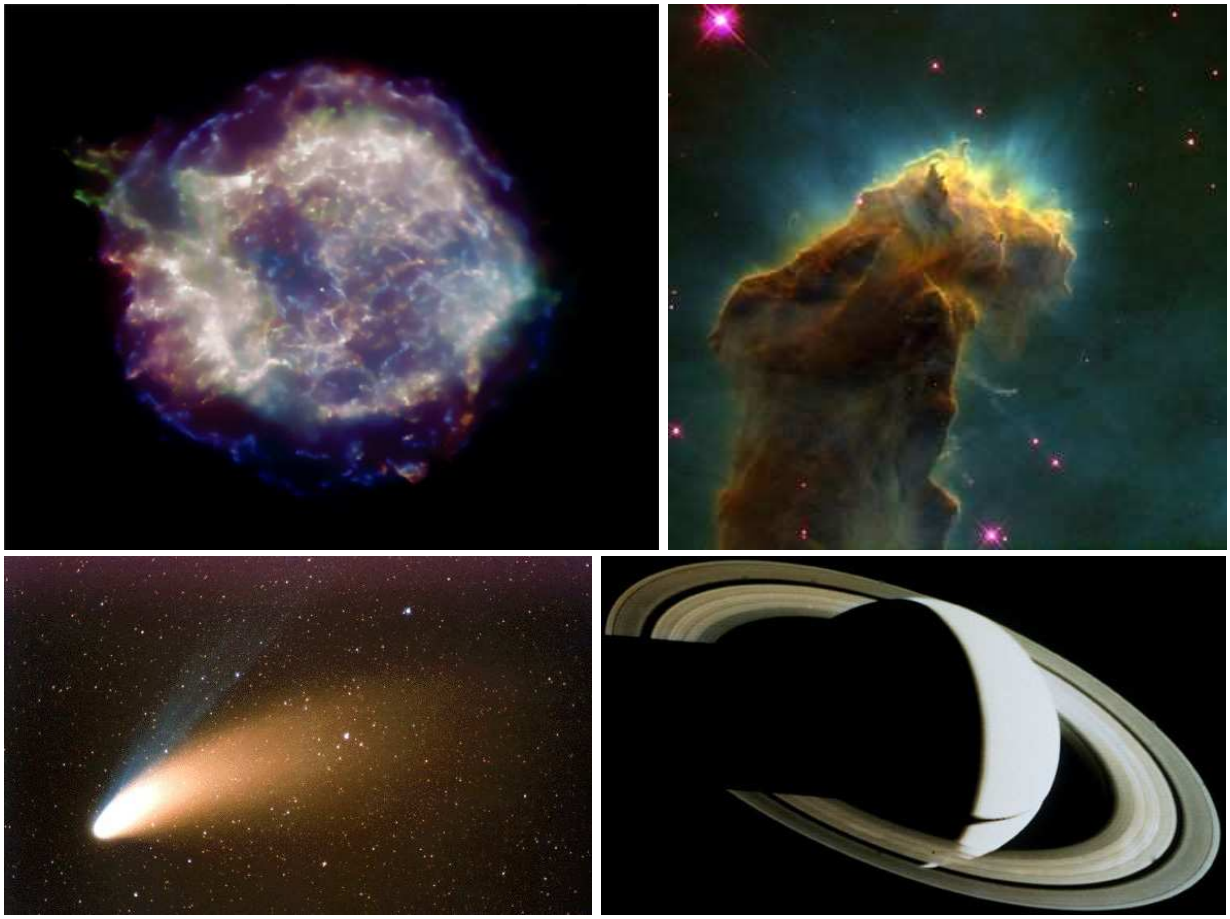

Figure 1.1: Sources and formations of cosmic dust. Top left: Cassiopeia A supernova remnant. Courtesy of the Chandra X Ray Observatory. Top right: Eagle Nebula. Courtesy of the Hubble Image Gallery showing vast clouds of dust and gas. Bottom left: Comet C/1995 Hale-Bopp. Bottom right: Saturn and its dusty rings. This image was taken by Voyager 1 in 1980. Courtesy of NASA.

The most obvious sources of interplanetary dust are comets which move on highly excentric orbits through the solar system [9]. Gas pressure from the sublimation of volatile ices in the nucleus emits dust grains into space. Dusty tails of particularly bright comets

can sometimes be observed with the naked eye (e.g. comet C/1995 Hale-Bopp, figure 1.1). The larger particles obtain heliocentric orbits that are similar to the parent comet, thus forming cometary trails [10]. If the earth crosses such a trail, large dust grains with sizes of 10 mm and bigger generate spectacular meteor storms, such as the Leonid meteor storm caused by debris from comet Temple-Tuttle. Although dust is concentrated along cometary trails, most of the dust gets contiguously distributed in interplanetary space by planetary perturbations, collisions and by the Pointing-Robertson effect. Millimeter to micron-sized particles populate the zodiacal dust cloud, which is concentrated along the ecliptic plane.

Galileo and Ulysses spacecraft discovered a high concentration of small dust impacts in the vicinity of Jupiter, the Jupiter dust streams. The strongest evidence that these particles originate from Jupiter is given by the change in impact direction between the pre- and the post-fly-by streams. Analysis by Zook et al. [11] showed that the Ulysses measurements can be explained as nanometer sized particles that are strongly deflected by the interplanetary magnetic field. Currently, Cassini spacecraft is orbiting Saturn exploring the composition of its dusty rings.

During the extensive in-situ analysis of cosmic dust, the interest of determining the impact direction of single dust grains with a high angular resolution has grown. The following section presents some existing detector designs and will give an outlook to new detector concepts.

1.2 Dust Detectors

Due to the photoelectric effect, dust in the interplanetary space is charged to a potential of approximately 5 V. The existence of the particle's charge is the key to in-situ trajectory measurements. By electrostatic induction, the particle causes displacement currents in sensing electrodes, which are attached to charge sensitive amplifiers. Depending on the electrode geometry, speed, charge and direction of an intersecting particle can be extracted from the resulting detector signals. In general, a particle is neither destroyed nor deflected by a charge sensing detector. The most sensitive in-situ charge measurements so far are delivered by the Cassini Cosmic Dust Analyzer (CDA), which records charge signals from a single sensing electrode with a sensitivity of 10^{-15} C (4 μm particle size). Figure 1.2 shows the Cassini spacecraft and its detector equipment. Figure 1.3 depicts the electrode configuration of the CDA.

State-of-the-art chemical analyzers are time-of-flight spectrometers, which are based on impact ionization. Ions are accelerated by an electric field, reflected and focused onto a multiplier by a special electrode configuration (reflectron). By adjusting the geometrical parameters of the reflectron, energy focusing can be achieved. The flight time from impact target to the multiplier is then independent of the ions' kinetic energy and directly proportional to their mass. Thus, the transient signal at the multiplier reflects the atomic mass distribution of the dust particle's and target's constituents. Relative mass resolutions of $m/\Delta m \geq 150$ have been achieved with the Cometary and Interstellar Dust Analyzer (CIDA) onboard the Stardust mission (see figure 1.4).

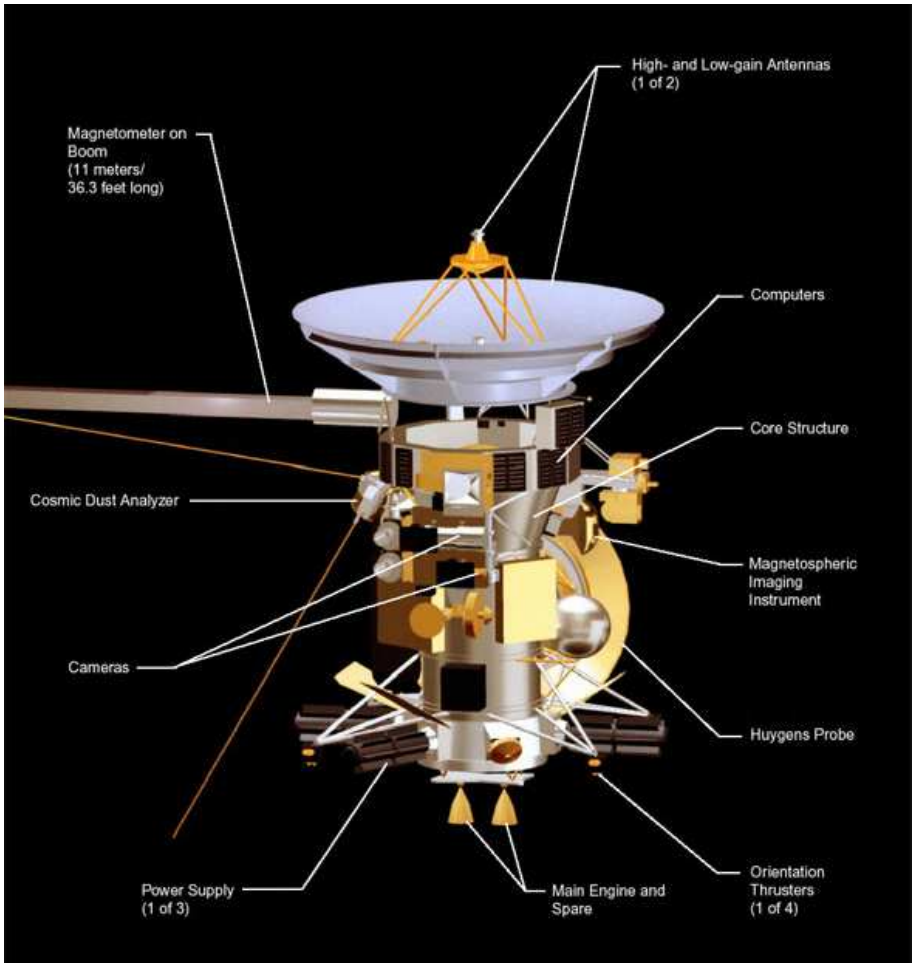

Figure 1.2: Cassini spacecraft. Launched from Kennedy Space Center on October 15, 1997, the Cassini-Huygens spacecraft reached the Saturnian region in July 2004. The mission is composed of two elements: The Cassini orbiter that will orbit Saturn and its moons for four years, and the Huygens probe that will dive into the atmosphere of Titan and land on its surface.

Generally, results from in-situ dust detectors suffer from the relatively small number of recorded impacts and hence from limited statistical accuracy. Therefore, methods have to be employed that allow us to get the most meaningful results out of these measurements [6]. For the detailed in-situ analysis of cosmic dust an advanced dust telescope is developed. This telescope will be assembled by two parts, a trajectory sensor for the detection of the particle's charge, speed and direction, and a Large-Area Mass Analyzer (LAMA) for the examination of its chemical composition. The electric field distribution of the LAMA configuration presented in figure 1.5 is simulated and optimized with SIMION, a software package by the Idaho National Engineering & Environmental Laboratory. LAMA has a cylindrical symmetry with a ring-shaped impact target, which is charged to a potential

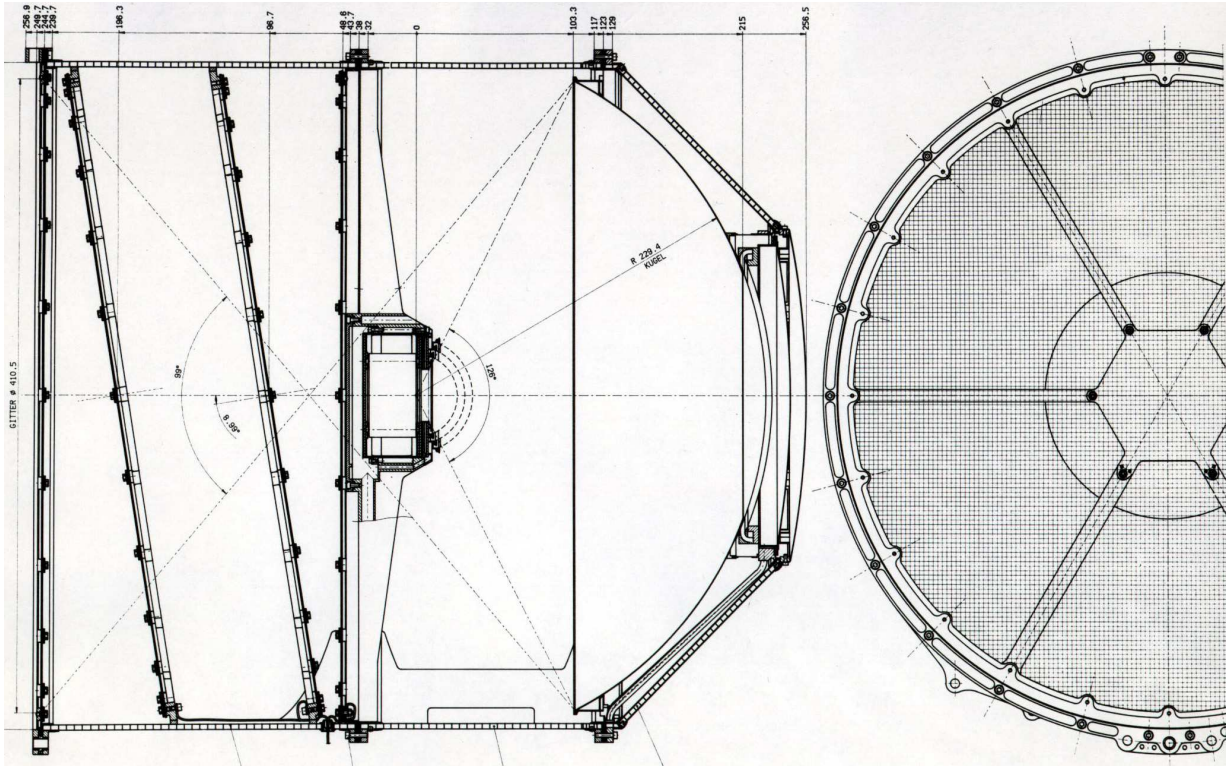

Figure 1.3: Cassini Cosmic Dust Analyzer (CDA). The charge sensor consists of two shielding grids and two tilted sensor grids. Both sensor electrodes are connected to one charge sensitive amplifier. From the signal shape of a particle measurement a rough estimate of the trajectory can be gained.

of 5 kV. A grounded acceleration grid is mounted 50 mm in front of the target. The accelerated ions fly into a reflectron consisting of two parabolic grids at 0 and 6000 V, respectively. Potential rings provide a smooth electric field close to the side wall. Ion trajectories are spatially and timely focused. By an ion detector (microchannel plate) of about 120 mm radius highly resolved spectra are measured. In front of the impact detector, a field-free drift region allows the integration of a trajectory sensor.

In order to improve trajectory measurement techniques, careful considerations about the detector geometry have to be combined with the development of custom design electronics. Major enhancements compared to existing devices would be an increased charge sensitivity and a higher angular resolution for dust measurements. The geometry of the sensing electrodes and shields determines the detector capacitance, which has a direct impact on the noise level of the measurement. Former detector designs like the Cassini CDA consist of one large electrode covering the whole sensitive area. The design presented in this thesis utilizes wires as sensing electrodes achieving a much lower detector capacitance. Therefore, dust particles are traced on multiple channels while data is processed with a mixed-signal ASIC chip.

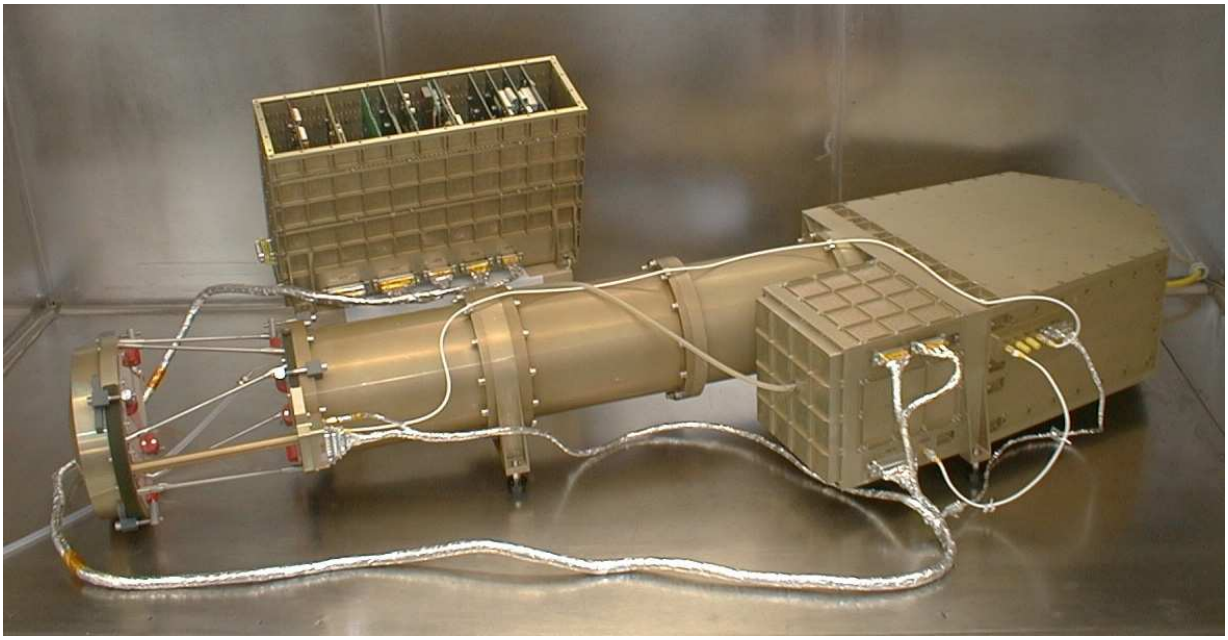

Figure 1.4: Cometary and Interstellar Dust Analyzer (CIDA). Time-of-flight mass spectrometer with high mass resolutions ($m/\Delta m \geq 150$)

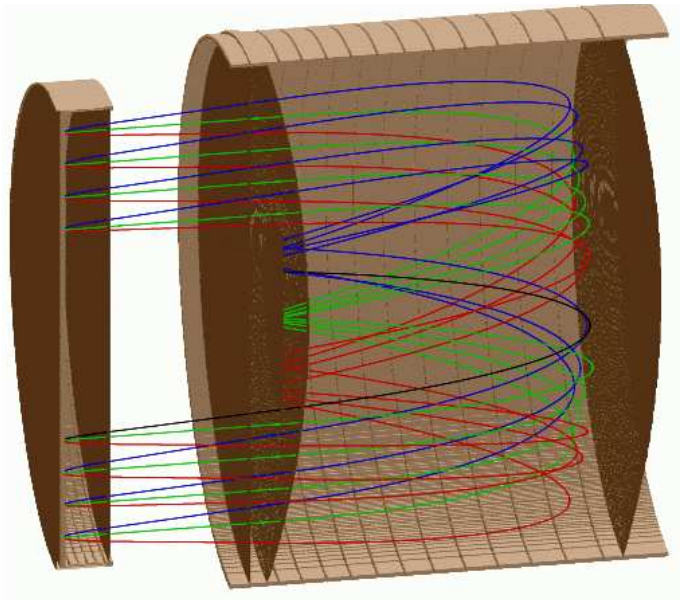

Figure 1.5: Large-Area Mass Analyzer (LAMA). Left: Impact target and acceleration grid. Right: Reflectron with two parabolic grids and potential rings at the side wall. In between the two units, a field-free region allows the integration of the trajectory sensor module. The colored lines represent ion trajectories for different initial conditions.

This thesis is organized as follows: Chapter 2 explains the architecture of the trajectory sensor developed for the advanced dust telescope in detail. An electromagnetic (EM) simulation of the detector is presented, as well as an ASIC solution for the processing of the detector signals. In Chapter 3, circuit details of DUNE 1.1, the current version of the electronics, are discussed. Chapter 4 comprises the measurements of the system from experimental setup to dust measurements at the Heidelberg dust accelerator facility. A conclusion is given in Chapter 5. Finally, the scenario of a future space mission is outlined.

Chapter 2

DUNE Trajectory Sensor and Readout Electronics

In this chapter the trajectory sensor unit of the advanced dust telescope will be introduced. The main focus is directed to the electronics of the detector, which poses the major challenges. After technical specifications are presented, the electrostatic behavior of the detector is simulated and detector signals are studied. The last section leads into ASIC design by illuminating the problems and achievements of the first integrated CMOS implementation of the readout electronics.

2.1 Specifications

The motivation for the design of an advanced dust telescope is to combine a highly resolved trajectory measurement of dust with a subsequent analysis of its chemical composition. In order to maximize the viewing angle and active area, a configuration is under investigation, where the trajectory sensor is placed inside the chemical analyzer in a field-free region.

Dust particles to be measured with the DUNE trajectory sensor are charged in the range of 10^{-16} C to 10^{-13} C and travel with 5 km/s to 100 km/s. The sensitive area of the detector is 0.1 m^2. Besides charge and velocity, the direction of incoming dust is measured with an angular resolution of about 1° and over a viewing angle of ± 50°.

The sensitivity of a charge detector is strongly dependent on the detector capacitance, which is connected to the charge sensitive amplifier. Thus, to be sensitive to dust particle charges of 10^{-16} C, a special detector geometry is required. Covering the desired active area and angular resolution while providing this sensitivity, necessarily leads to a multi-electrode configuration. Each electrode then has a sufficiently small capacitance to assure the desired noise level, but one has to deal with a large amount of data that has to be handled in realtime.

Another effect linked to the multi-channel approach is, that measured charges are in general only fractions of the particle charge, since the induced charge is distributed on multiple electrodes. A finite element simulation of the proposed detector shows that in the

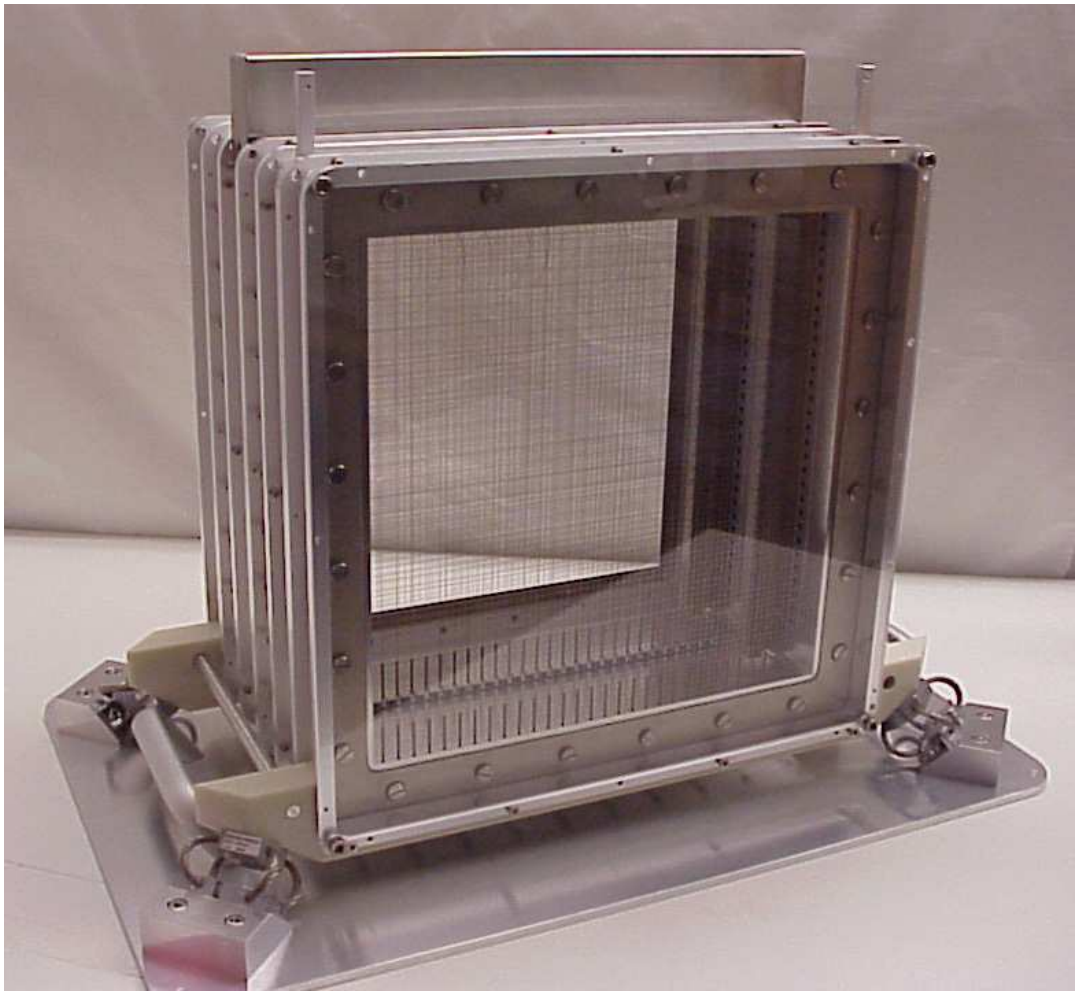

Figure 2.1: DUNE trajectory sensor. The detector consists of six stacked frames. The outer frames are shielding grids, the inner four are equipped with sensor wires. Wires of adjacent sensor planes have a perpendicular orientation with respect to each other. The spacing of the frames is 40 mm.

worst case, the induced charge on the dominating channel is approximately 30%. Nevertheless, the improvement in sensitivity due to the reduced detector capacitance is by far stronger. Figure 2.1 shows the trajectory sensor lab model.

The readout electronics has to handle the resulting transient signals, which cover a bandwidth of 10 kHz to 10 MHz. The targeted sensitivity requires an amplifier noise level of about 100 electrons which turns out to be the most critical requirement. In order to avoid aliasing, the sampling frequency is chosen to be 25 MHz. Due to the high data rate caused by the multiple sensing wires, CMOS ASIC design is a desired technology for this device. It offers a high integration density, as well as excellent analog properties.

2.2 Architecture

2.2.1 Detector Geometry

The trajectory sensor consists of a stack of four sensing and two shielding planes. The aperture of the planes is 300 mm × 300 mm and their spacing is 40 mm. The shielding planes are located on the top and bottom of the stack and consist of 4 mm mashed grids with a transparency of 95%. Their task is to keep radiated signals out of the sensitive detector volume. Figure 2.2 depicts the geometry of a sensor plane.

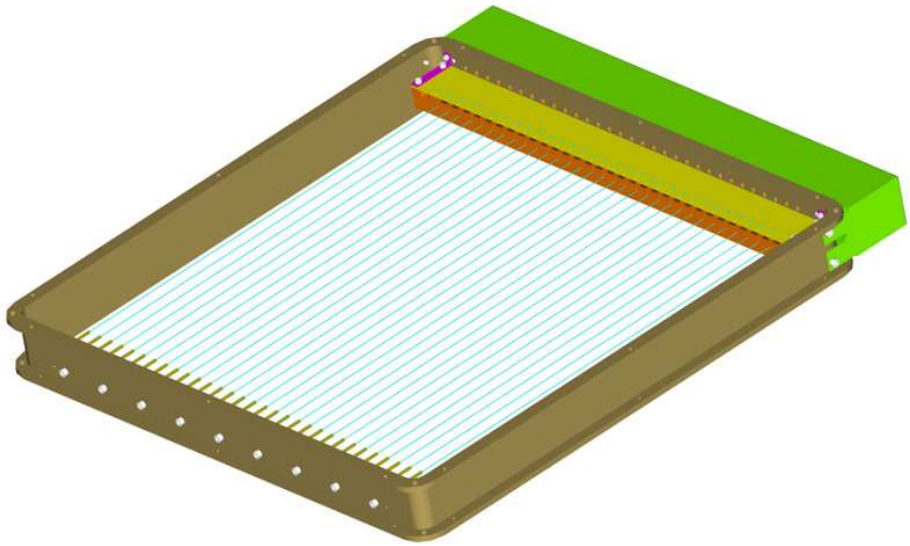

Figure 2.2: Sensor plane. Active area is 300 mm × 300 mm. Up to 31 wires can be mounted with a spacing of 10 mm. The nominal configuration consists of 16 wires (20 mm spacing). Mounts have been provided for the circuit boards carrying the readout electronics.

Wires of adjacent sensor planes have an orientation of 90° with respect to each other. The side wall of the detector consists of an aluminum frame, which forms the major part of the shield. The sensor planes can be equipped with up to 31 parallel wires of 0.2 mm diameter and 10 mm spacing. Their length of 300 mm is covering the whole aperture. For the lab version of the detector only 16 wires with 20 mm spacing are installed. Thus, smaller wire capacitances are achieved. The wires have a specially developed insulated mount with spring mechanism to guarantee sufficient tension on the wire under the influence of temperature variation and vibration. This effort has been made with regard to the requirements of a flight version. Also, the mount has to provide a maximum separation of the sensing wires to adjacent shields and other metal parts in order to keep the detector capacitances as small as possible.

2.2.2 EM-Simulation

The electrostatic behavior of the proposed detector geometry can be simulated with finite element simulation tools. Although, a solution of the Poisson equation can be expressed for given boundary conditions with the Green's function, the analytic solution of the Green's function for such in sections defined boundary conditions is not possible. Thus, EM-Studio by CST Inc. was used to study the induced charge signals for this specific electrode geometry. The simulation software solves the Maxwell equations for the electrostatic case. Figure 2.3 demonstrates the choice of the coordinate system and the simulation results for a typical trajectory. The signals of more distant wires show local minima at the intersection points. This can be explained by electric shielding of the closer wires, which are then between the particle and the considered channel.

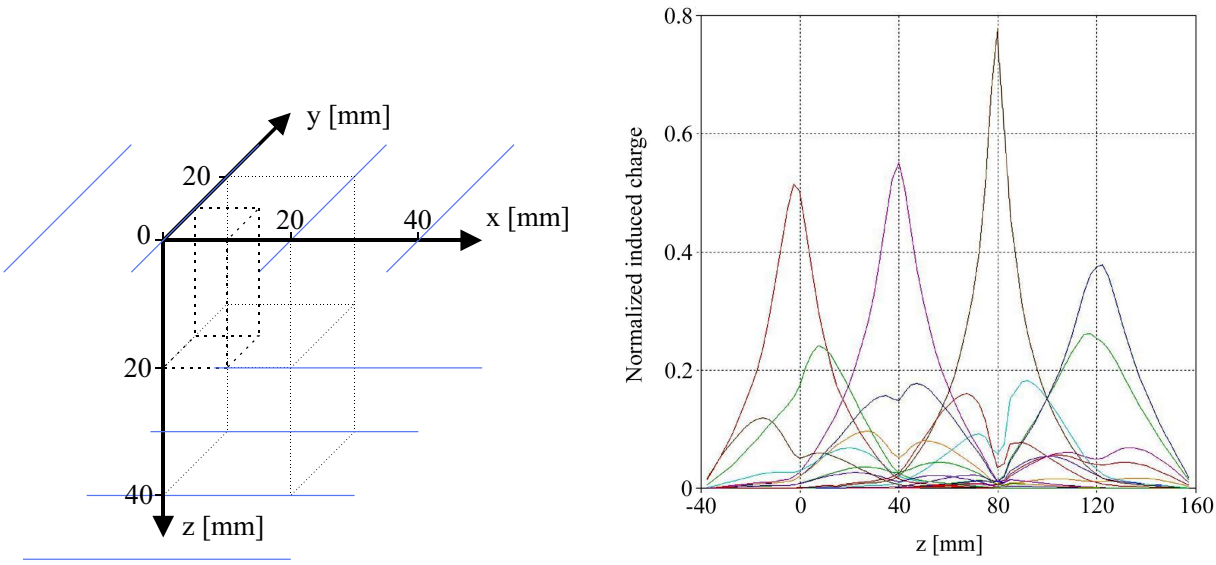

Figure 2.3: EM simulation of the detector signals for a typical trajectory. Left: Choice of the coordinate system. The sensor planes are located at z = 0, 40 mm, 80 mm and 120 mm (80 mm and 120 mm not shown). Right: Transient signals of a typical particle trajectory. Amplitudes are plotted as fractions of the particle charge.

Due to the periodicity and symmetry of the electrode configuration, it is sufficient to examine the amplitude distributions for particle positions within the dashed box (x = 0 .. 10 mm, y = 0 .. 10 mm, z = 0 .. 20 mm). Signals within this volume can be mapped to signals of any other part of the detection volume. Figure 2.4 explains this procedure. The red curve shows the signal of the closest wire as a function of distance to the dust particle. At x = 10 mm, The particle is located exactly between two wires of the sensor plane. Hence, the two strongest signals show the same amplitude. This is reflected by the green curve, which displays the signal of the second closest wire. At x = 10 mm, the two curves intersect at 30% of the particle charge. This also represents the worst case signal

amplitude for a dust measurement, what has to be considered for the sensitivity of the electronics. The blue, pink, yellow and purple curves represent the signals of the 3^{rd}, 4^{th}, 5^{th} and 6^{th} closest wires respectively.

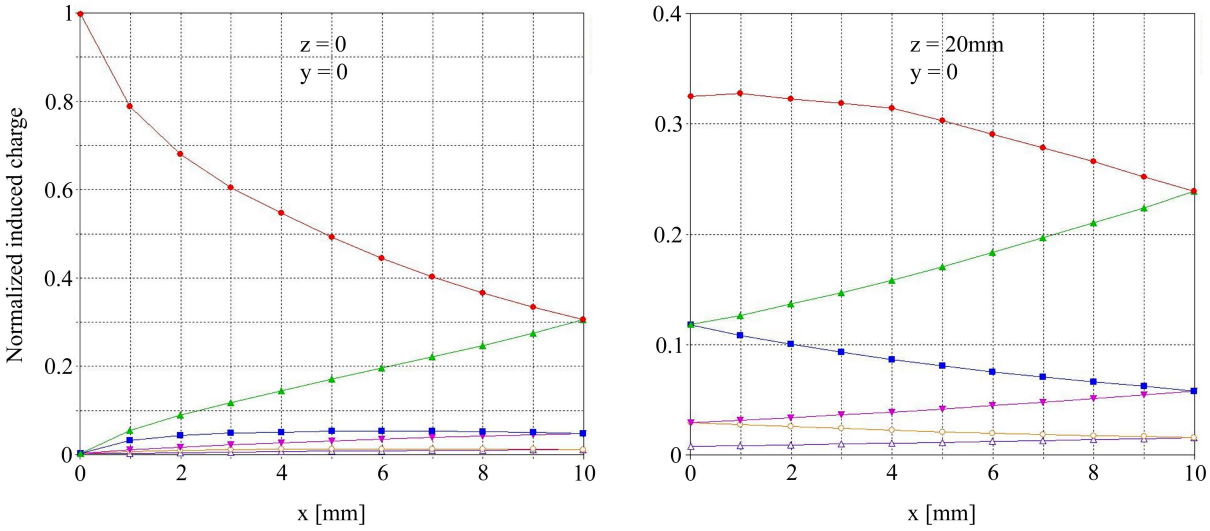

Figure 2.4: Distance function of induced charge signals for characteristic particle locations. Left: Particle position in the first sensor plane (z = 0). Amplitudes are plotted as functions of x, the distance to the closest wire. Right: Particle position between first and second sensor plane (z = 20 mm).

Since low-noise performance is the major goal of DUNE, every sensing wire is connected to an individual front-end amplifier close to the mount of the wire inside the sensitive volume. This guaranties the minimum length of the wire and the maximum spacing to its neighboring wires. Of course, CMOS technology would offer the total integration of multiple amplifiers plus data processing unit on one piece of silicon, but that would cause a dramatic increase of the detector capacitances, since all wires had to be connected to the electronics within a few millimeters.

2.2.3 Readout Electronics

The idea of using CMOS ASIC technology for the proposed trajectory sensor is triggered by the large number of detector signals and the associated data load. A fully equipped detector with 64 electrodes causes a data rate of 16 Gbit/s at a 25 MHz operation. It is convenient to handle this data with integrated circuits. Regarding the advanced performance characteristics of state-of-the-art deep sub-micron CMOS processes, such high data rates can be handled using massive parallel signal processing methods. Furthermore, excellent mixed-signal performance and detailed simulation models are given for these technologies.

DUNE is a mixed-signal ASIC design. Its tasks are to pre-amplify weak induced charge signals and to perform multi-channel analog data acquisition and digitization. This is realized by two independent units, a front-end amplifier with logarithmic compression and a digital transient recorder. Figure 2.5 shows the block diagram of the DUNE readout electronics. Table 2.1 summarizes the design specifications.

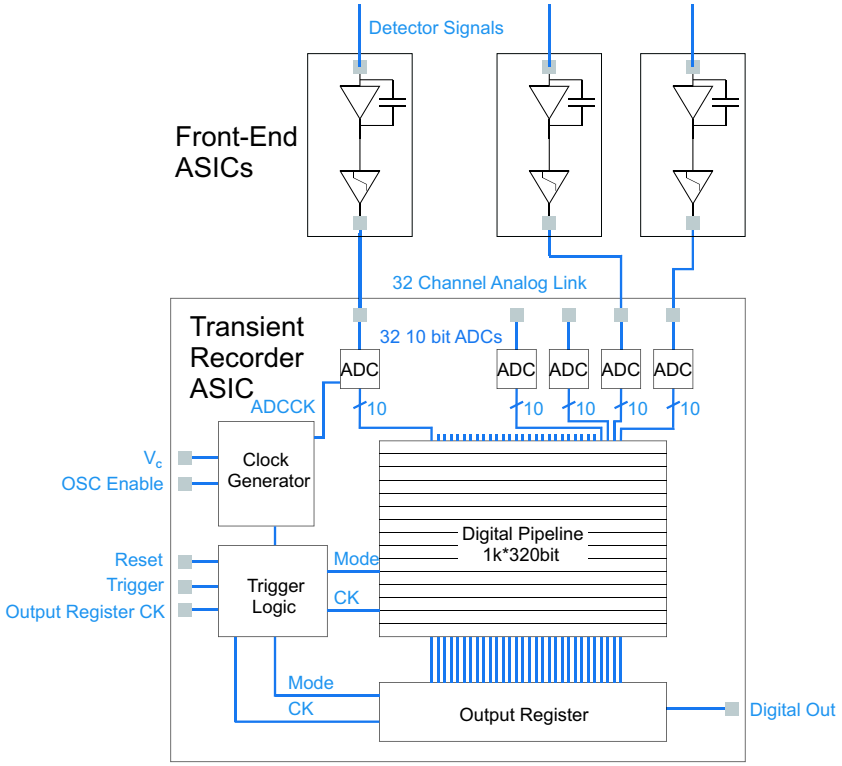

Figure 2.5: DUNE readout electronics block diagram. Individual front-end ASICs are connected to a 32 channel transient recorder ASIC. The analog signals are converted by ADCs at a conversion rate of 25 MS/s. The digital data is stored in a pipeline for 40 μs and can be read out on a trigger event.

Up to 32 front-end amplifiers can be connected via an analog link to a common multi-channel transient recorder, which is located outside of the detector shield. This part of the circuit digitizes incoming analog signals at a rate of 25 MHz and 10 bit resolution on 32 channels. Here, a low-power Analog-to-Digital Converter (ADC) is required in order to keep the on-chip power supply voltage stable and so avoid cross-talk. The digitized data is buffered in a pipeline, which is implemented as an SRAM (Static Random Access Memory) of 320 bit width and 1024 bit length. The pipeline is essential, since the trigger event signaling the electronics that a dust particle has been detected is issued by an impact detector mounted behind the trajectory sensor. Thus, when a trigger is issued, the trajectory of the corresponding dust particle has already been recorded. After a trigger event is received, data is serialized and read out. This action is controlled by an external

clock sent, e.g. from a computer or the main electronics of a spacecraft. When completed, this unit sends a reset signal, and the recording starts over.

Since particle detection rates are expected to be small in the interplanetary space, the readout of trajectory information can be processed slowly. Nevertheless, data has to be recorded continuously, since trigger signals are initiated by the impact of the particle, which occurs after the interaction with the trajectory sensor.

Property	Value
Detector capacitance	5 pF
Bandwidth	10 kHz .. 10 MHz
Dynamic range	10^{-16} C .. 10^{-13} C
Front-end power consumption (per channel)	50 mW
Noise	100 electrons
Sampling rate	25 MHz
Digital resolution	10 bit
Buffer depth	1024 samples
Number of channels	32
Power supply (core)	1.8 V
Power supply (digital I/O)	3.3 V
Process	UMC 0.18 μm CMOS

Table 2.1: Specifications of DUNE readout electronics.

2.3 Prototype - DUNE 1.0 Readout Chip

2.3.1 Design Concept

DUNE 1.0 is the prototype version of the ASIC designed to meet the specifications of the proposed trajectory sensor. The two units, analog front-end amplifier and a multi-channel transient recorder, are placed on one die in this version to reduce production costs. Nevertheless, they are intended to be operated exclusively. Thus, a chip can either be mounted as single front-end amplifier or as common transient recorder. This design is the foundation for the succeeding version DUNE 1.1, which is described in detail in the following chapter. Here, only fundamental aspects of the circuit as well as basic setup issues will be described.

Although, only a few connections are required to control the DUNE readout chain, the prototype is equipped with 208 pads, which enable external access to all sub-components of the circuit. Figure 2.6 presents the top level schematic and pad assignment of the prototype. The implementation of the prototype DUNE 1.0 can be seen in figure 2.7.

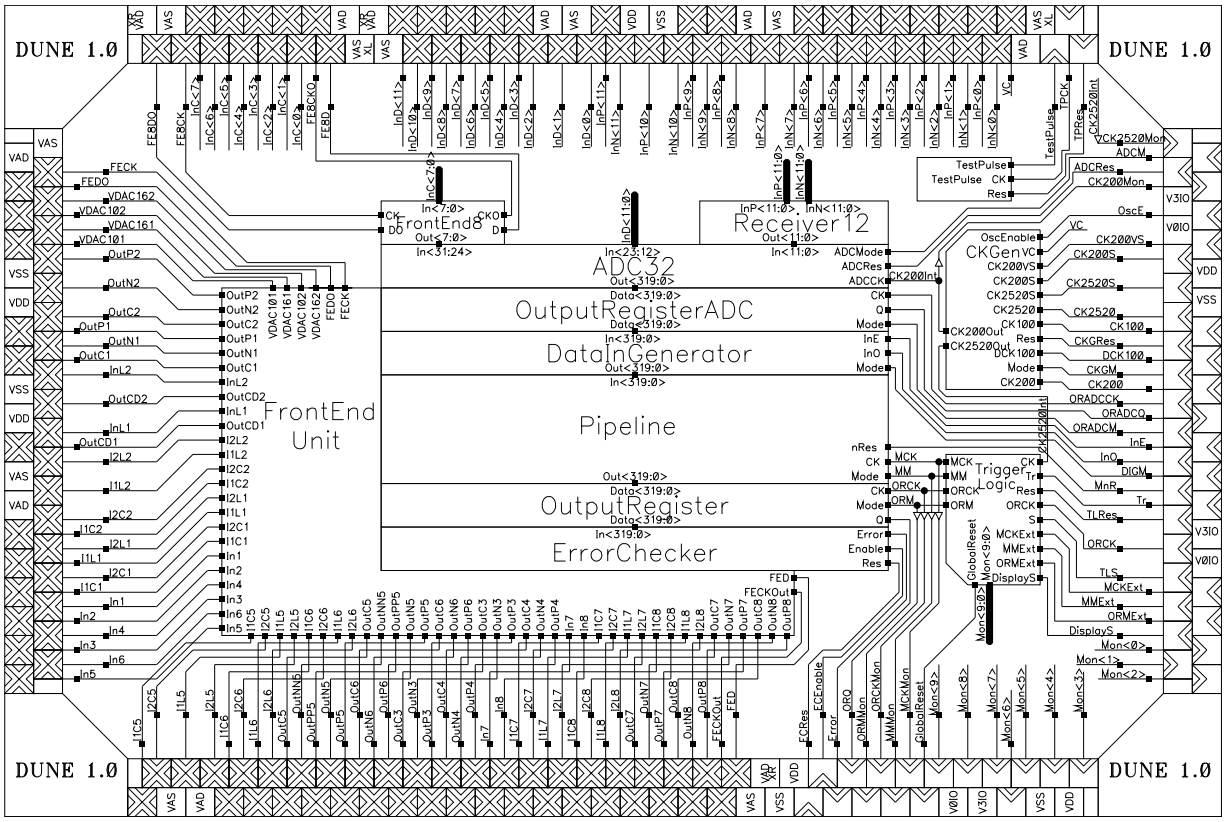

Figure 2.6: DUNE 1.0 top-level schematic and pad assignment. The prototype versions of the front-end unit and the transient recorder are implemented on the same chip. 208 pads enable flexible access to all sub-circuits.

2.3.2 Functionality

Various debug features were implemented in the design to assure a maximum of experience from the first silicon. Basically, all internal control signals between the sub-circuits can be selectively provided externally. Indeed, some of the connections turned out to be absolutely useful, since an error in the memory precharging scheme caused malfunction of the readout chain in the nominal configuration. Luckily, the memory readout control sequence, which is usually generated on-chip, can also be supplied from an external pattern generator. So, a special pipeline operation could be established and functionality of the pipeline achieved.

Considering the workaround for the memory bug, functionality is given for the complete DUNE 1.0 readout chain. A 250 MHz on-chip clock for the ADCs and a synchronized 25 MHz clock for pipeline and control logic can be generated on-chip. The control logic is sensitive to the trigger signal and coordinates the memory and output register during readout as expected.

Also, the ADCs show a convincing result. Two slightly different versions have been implemented and tested, one with transparent comparator and one with a clocked version.

The second was implemented as preparation for version 1.1 where the comparator receives a reset function for faster operation. Both operate even at much higher clock speeds than nominal (35 MS/s conversion rate, 350 MHz clock).

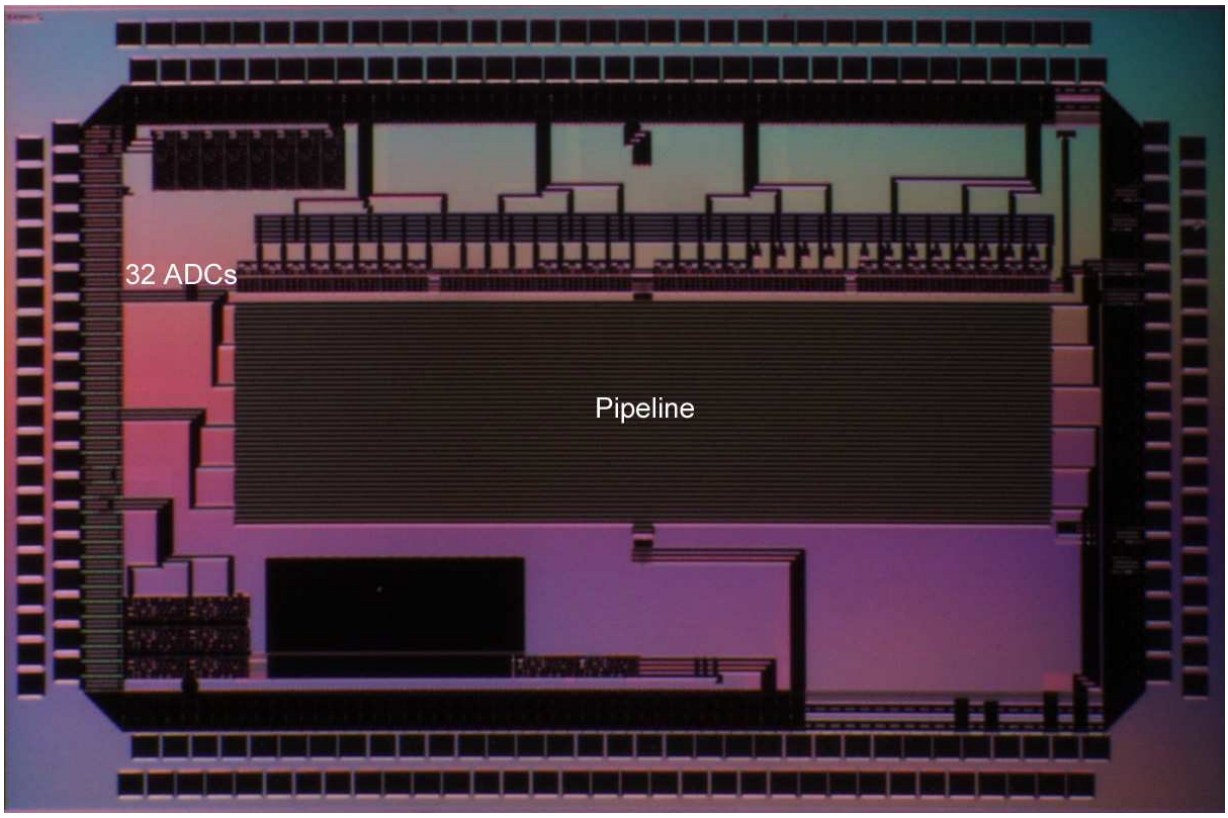

Figure 2.7: DUNE 1.0 chip photograph. Front-end amplifier unit (bottom left) and 32-channel transient recorder (center) with 10 bit resolution. Chip size: 5 mm × 3.3 mm. The two units can be powered and operated independently.

2.3.3 Front-End Noise

The analog performance of the front-end of version 1.0 is less convincing than the digital part of the circuit. The measured noise level is about ten times higher than predicted by the simulation and shows a clear 1/f behavior. Thus, the main goal of achieving a sensitivity of 10^{-16} Coulombs has been missed. On the other side, the operating conditions (baseline, bias voltage levels) are predicted quite accurate. A closer look at the front-end noise simulation results indicated, that the 1/f noise (flicker noise) contributions of the circuit were not included. The study of CMOS noise behavior in the targeted frequency range of 10 kHz to 10 MHz makes clear, that these contributions should rather dominate the total output noise. This gives rise to the conclusion, that the noise model used for the simulation

was incomplete. Just in time for the redesign, a new design kit including a special low noise transistor layout with flicker noise model was released by Virtual Silicon Technology Inc., which delivers the design kit for the UMC 0.18μm CMOS process. Thus, accurate noise predictions can be made since then, and the noise level could be dramatically decreased with the succeeding circuit.

2.3.4 Memory Bug

As mentioned, a design error occurred in the pipeline controller prototype. Initially, the pipeline didn't show the expected behavior. Not only was data at the output different from what was read in, but the memory content was altered by the readout procedure. By systematically changing the weight of states in the input pattern it was found out, that the memory cells belonging to the smaller weight were flipped when addressed. The stored pattern so converged in a state of identical entries within one column. Ideally, there should be no communication between memory cells within a column. Therefore, the bit lines are only connected to one cell at a time and potential differences on the bit lines are balanced by the prechargers before every readout. If the time between precharging and readout becomes too large, leakage currents can severely affect the potential of the bit lines which are floating in this phase. Leakage currents through the pass transistors are then causing the bit lines to drift towards the dominant memory entry. The succeeding readout of a memory cell ends up in a bit flip. This is what happened in the prototype.

In order to match the pipeline geometry to the channel spacing on the analog side of the circuit, memory columns are divided into four sub-columns, each of 256 bit length. The pipeline decoder iterates the addressing through the sub-columns on every readout cycle. Thus, one sub-column is addressed only every 4^{th} cycle. The error in the prototype timing is, that in the intermediate three cycles the prechargers are turned off so the bit lines were floating. If the memory clock is sufficiently high (in the order of 1 MHz), the floating time of three clock cycles becomes uncritical and data can be read out successfully. Hence, a pattern generator was used to operate the pipeline in read mode at a high frequency. After latching the pipeline output in the output register, the memory was clocked further until the address had passed through the memory once. At the same time, the output register was cleared, and the next data set could be latched. The effective pipeline clock frequency could so be increased while keeping the output data rate low. With this work around, the complete pipeline content could be accessed reliably.

In the succeeding version, the precharge timing has been corrected to avoid floating of the bit lines. Thus, readout at any clock frequency from 0 to 25 MHz is possible with DUNE 1.1!

Chapter 3

Design and Simulation of DUNE 1.1

Circuit details of the DUNE readout electronics are discussed in this chapter and simulation results are presented. The first section focuses on the front-end unit which is implemented on an individual ASIC chip. The second section describes the transient recorder unit and its basic operation procedure.

3.1 DUNE 1.1FE - Front-End Amplifier

As was learned from DUNE 1.0, the reduction of flicker noise becomes the most important task for the redesign of the front-end. The influence of external filter components such as inductances and capacitors is studied in the circuit simulation, while high-tech transistor layouts with corresponding noise model are utilized in order to keep parasitic layout effects small. Figure 3.1 shows the layout of the low noise RF transistor array implemented throughout the whole front-end design.

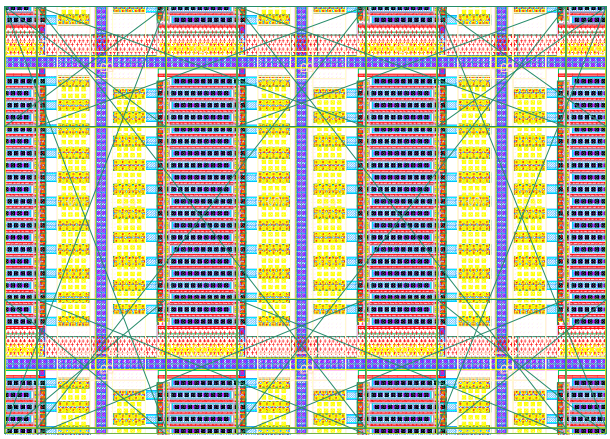

Figure 3.1: Low noise RF transistor array. Multi-finger layout assures a small gate resistance. Guard rings keep the substrate ground stable.

This is a multi-finger layout with minimum length gates (0.18 μm) of 5 μm width, which are contacted to metal on both ends for minimum gate resistance. The whole transistor is packed with the maximum number of contacts and all six metal layers are used to provide low ohmic connections to all ports. Each transistor is surrounded with a guard ring, a local connection to the substrate.

Insufficient contacts or too long gate strips result in a high gate resistance of a transistor, which can easily become the main noise contributor. Usually, these layout specific parasitic effects are not accounted for in the simulation. It is up to the designer to add parasitics (parasitic capacitances, resistances and inductances) into the simulation by considering the related layout. A reason, why design simulation and circuit layout can not be separated completely, but in case of critical designs should rather be done simultaneously.

DUNE 1.1FE consists of two consecutive amplifier stages, a charge sensitive amplifier and a logarithmic amplifier. Other than DUNE 1.0, the front-end unit of version 1.1 is placed on an individual piece of silicon. This provides more space for on-chip blocking and power and signal routing. The chip area is dominated by decouple capacitances. Figure 3.2 shows the layout of DUNE 1.1FE. For optimum low noise performance the power nets of the two amplifiers stages (charge sensitive amplifier and logarithmic amplifier) are separated and ground connections called clean ground (GNDCL, GNDCLL, one for each amplifier stage) are provided, which exclusively serve as decoupling reference. Figure 3.3 depicts the corresponding top-level schematic.

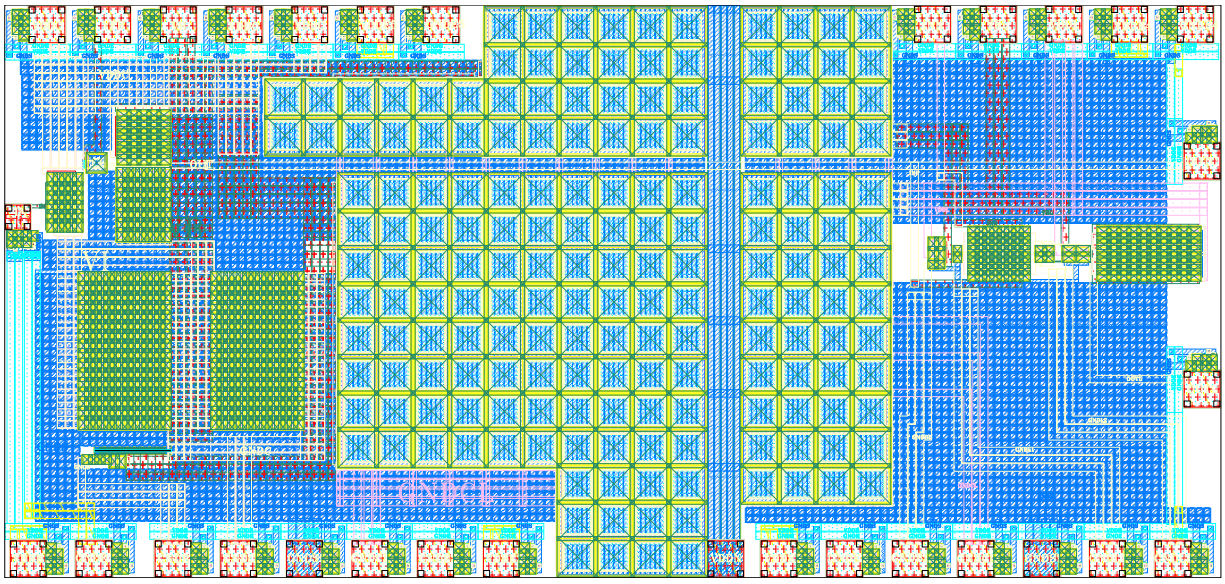

Figure 3.2: Layout of DUNE 1.1FE. The die size is 3.3 mm $\times$ 1.6 mm. Left: Charge sensitive amplifier. Center: Decoupling capacitances, Right: Logarithmic amplifier.

In order to avoid substrate coupling, current return paths through the substrate have to be avoided. Therefore, all current paths to ground (GNDB, GNDC, GNDBL, GNDL1,

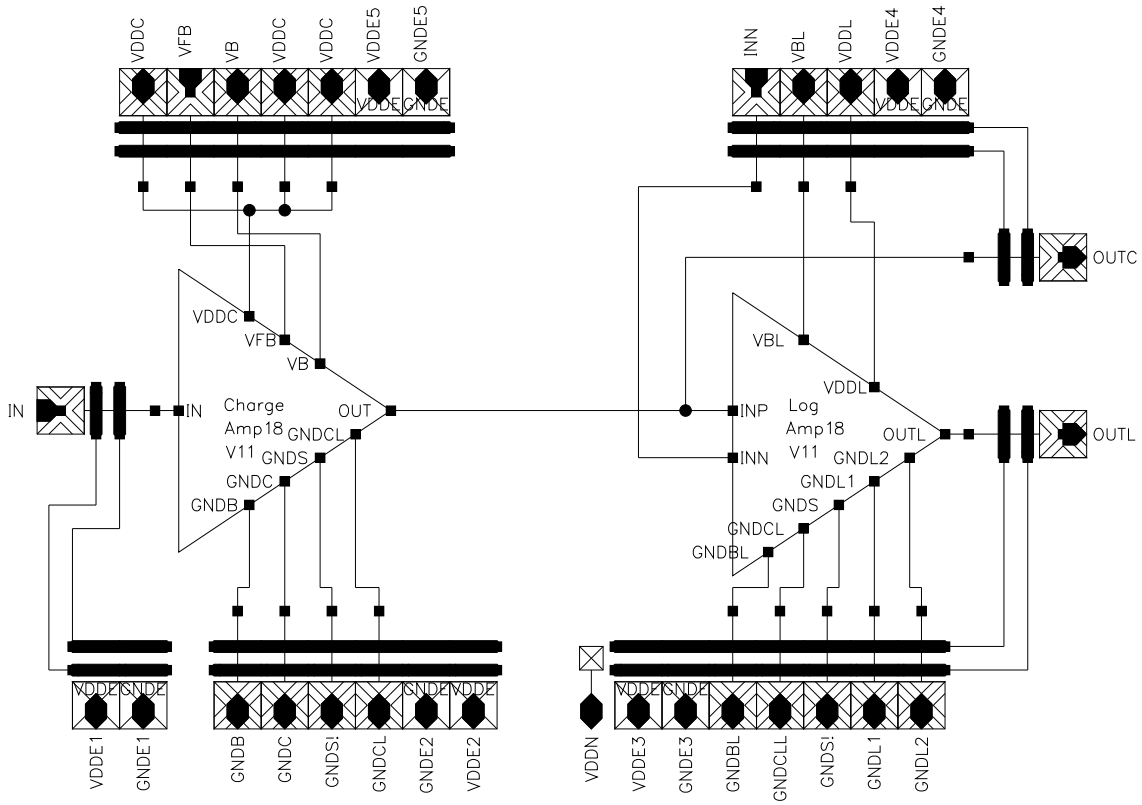

Figure 3.3: DUNE 1.1FE top-level schematic and pad assignment. The noninverting input (INP) of the logarithmic amplifier is connected to the charge sensitive amplifier, while the inverting input (INN) is provided by an external feedback circuit.

GNDL2) are separated from the substrate and are connected to individual bond pads. On the other side, one substrate ground net (GNDS!) for each amplifier stage is provided on-chip. In order to achieve a low ohmic connection to the substrate, substrate contacts are distributed over the whole chip area. On board level, all ground nets are connected. The substrate areas of the two amplifier stages are decoupled by a 100 μm wide n-well tied to VDD.

Last but not least, the whole charge amplifier unit is reversed with respect to DUNE 1.0 from n-MOS to p-MOS input. The reason for this is, that the p-MOS flicker noise density is about ten times smaller than the one of n-MOS transistors. Since the dominating noise contributor in a charge sensitive amplifier is the input transistor, this results in a major enhancement in the noise characteristics.

3.1.1 Charge Sensitive Amplifier

The charge sensitive amplifier is the first stage of the amplifier chain. Directly connected to the sensor electrodes, it is most critical concerning noise. Its task is to amplify extremely

weak charge signals without exceeding a noise level of about 100 electrons. This is only possible, if the detector capacitance is sufficiently small. The multi-channel detector geometry is chosen exactly for this reason. The simulated detector capacitance per channel is 4.7 pF. This is about two orders of magnitude smaller than the Cassini CDA detector capacitance and therefore enables much more sensitive measurements. Nevertheless, if the amplifier is not completely matched to the characteristic detector capacitance, optimum performance cannot be achieved. Figure 3.4 shows the schematic diagram of the charge sensitive amplifier. It is a folded cascode with capacitive feedback (C_F = 270 fF). The capacitance integrates the displacement current at the input caused by electrostatic interaction with the dust particle. The resulting signal is so proportional to the induced charge.

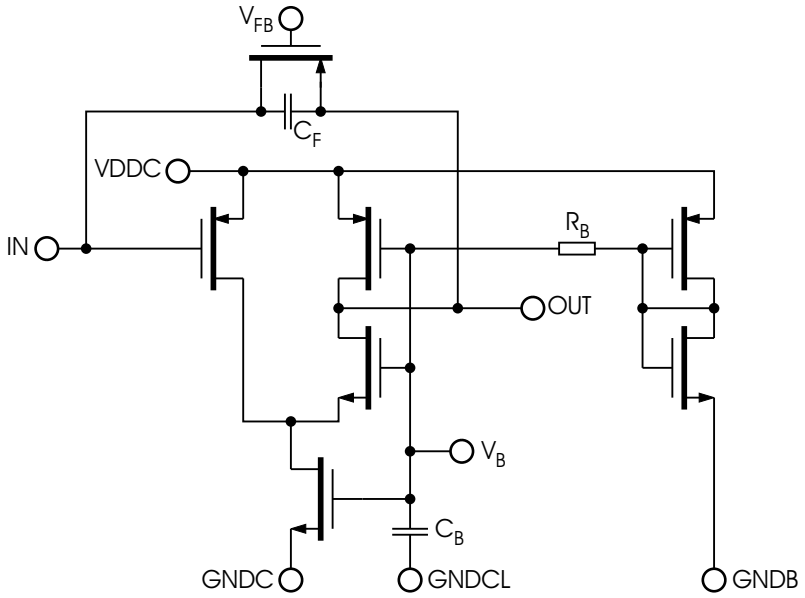

Figure 3.4: Charge sensitive amplifier. Folded cascode amplifier with capacitive feedback and on-chip biasing.

The bias voltage V_B for the cascode transistors and the current source is generated on-chip. The bias circuitry is also critical in terms of noise. In order to reduce the noise contribution of the bias transistors to a negligible amount, the generated bias voltage is connected to the cascode via a low-pass filter, which is supplemented by an external filter capacitance. For this reason, the size of the bias transistors and their related power consumption can be kept small. The on-chip resistor (R_B = 216 kΩ) of the low-pass is implemented by high resistive poly-silicon. Part of the low-pass filter capacitance (C_B = 142 fF) is located on-chip to assure proper filtering of high frequencies.

A different bias voltage V_FB is supplied externally to control the feedback resistance and so the shaping time of the amplifier. The ideal detector signal is a bipolar current signal. This means, that the net charge after the measurement is zero. For this reason,

the feedback resistance can be chosen rather high (e.g. 3 GΩ), in which case it doesn't reasonably influence the signal shape and noise. Experience with the Cassini CDA has shown, that plasma currents can cause serious baseline shifts. In the worst case, the baseline sticks to one rail of the amplifier stage and no useful data can be taken. In order to avoid this problem, the resistance of the feedback can be adapted to the needs of the experiment, so low-frequent disturbances are suppressed sufficiently. An even more powerful mechanism of suppressing baseline shifts with the feedback mechanism of the logarithmic amplifier and will be described below.

The schematic diagram in figure 3.4 is strongly simplified. The layout of the current source for example is actually an array of many multi-finger transistors (l = 0.18 μm, w = 100 μm), connected in series and in parallel. This way, the layout of a transistor optimized for low noise RF applications with known noise characteristics can be utilized. Also, a flicker noise model exists for this specific layout. Since the large discrepancy between simulation and measurement of DUNE 1.0 occurred due to the disregard of flicker noise, this is an important advantage.

3.1.2 Logarithmic Amplifier

The pre-amplified signals range over three orders of magnitude and are finally digitized with 10 bit resolution. A logarithmic post-amplifier increases the resolution of weak signals while covering this dynamic range. The logarithmic amplifier is implemented as a series of two differential amplifiers (see figure 3.5).

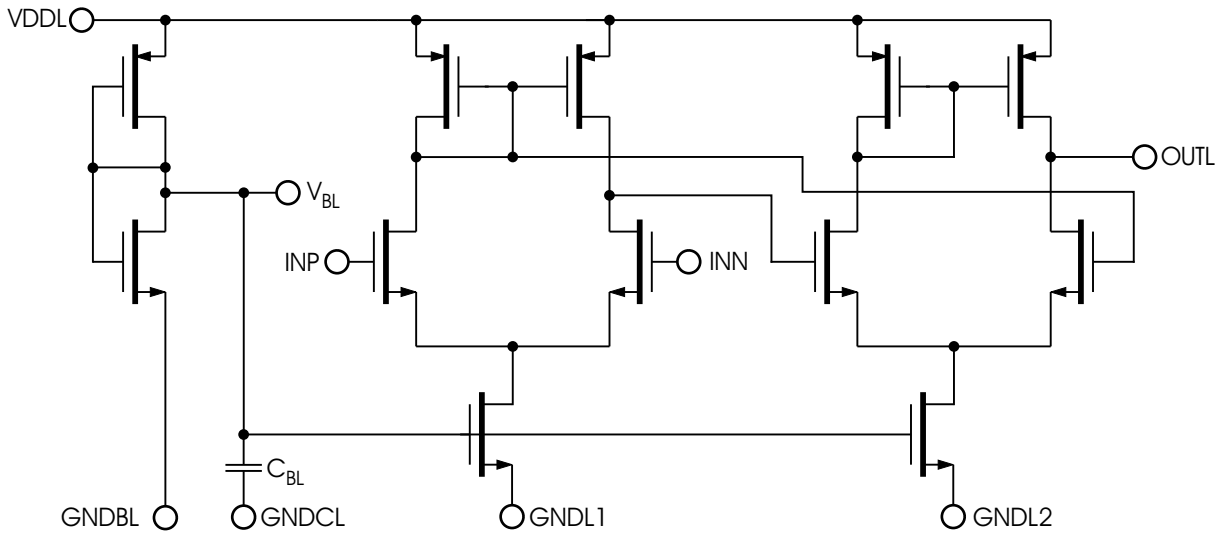

Figure 3.5: Logarithmic amplifier. Series of two differential amplifiers with on-chip biasing. The charge sensitive amplifier is connected to INP. External access to the inverting input (INN) enables the implementation of a feedback circuit for control of the operating point and stabilization of the baseline.

The first stage is connected to the charge amplifier and an external inverting input that serves as feedback connection. The logarithmic amplifier has a total amplification of 100 in the linear range (for small signals). Larger signals drive the stages into saturation and the total amplification drops. The transistor sizes are chosen, so the maximum signal of 10^{-13} C causes the amplifier to reach the rail. Also, a suitable driving capability has to be assured, so the signal can be linked to the transient recorder.

3.1.3 Simulation and External Setup

Figure 3.6 shows the external connections (simulation environment and board-level circuitry) of DUNE 1.1FE. The optimum performance of the amplifier is achieved in conjunction with external filter components. DC voltage nodes (bias voltages and power supplies) receive external capacitive blocking. The current path from the cascode current source to ground is completed by an inductance, whose parasitic series resistance has been accounted for in the optimization. This component reduces the flicker noise contribution of the n-MOS current source dramatically.

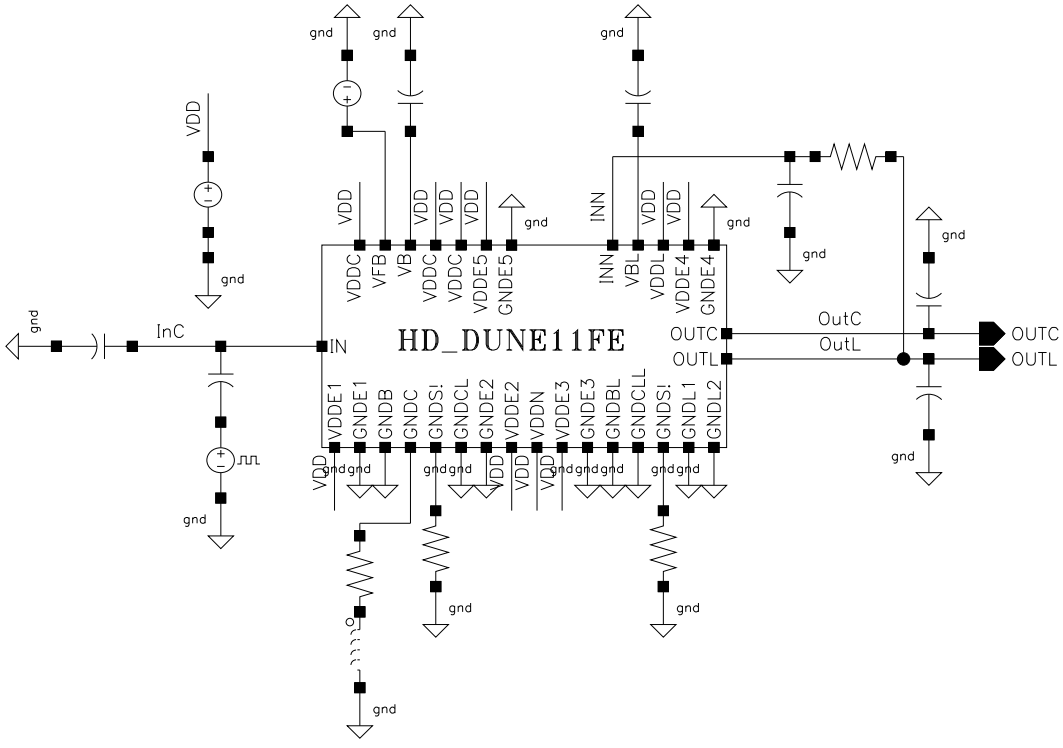

Figure 3.6: Simulation environment and external setup. The current source of the folded cascode is connected to ground via a 100 μH inductance (GNDC) in order to reduce flicker noise of the cascode current source. Its series resistance of 5 Ω has been considered in the optimization. The low-pass feedback from OUTL to INN forms the baseline stabilization circuit.

The logarithmic amplifier is controlled by a feedback circuit that is assembled off-chip. Therefore, direct access is provided to the inverting input (INN) of the logarithmic amplifier. By integrating a low-pass filter in the feedback path, it is possible to cut the signal bandwidth at low frequencies. Other than filtering low frequencies by decreasing the feedback resistance of the charge amplifier, this feedback does not introduce extra noise in the signal band, which makes it a powerful tool to decrease the system's sensitivity to low frequent disturbing signals. High frequencies can be filtered out with a low-pass filter in the output signal path. An appropriate choice of the upper and lower band limit optimizes the noise performance of the amplifier which is designed for the range of 10 kHz to 10 MHz. Figure 3.7 summarizes the simulation results of the front-end.

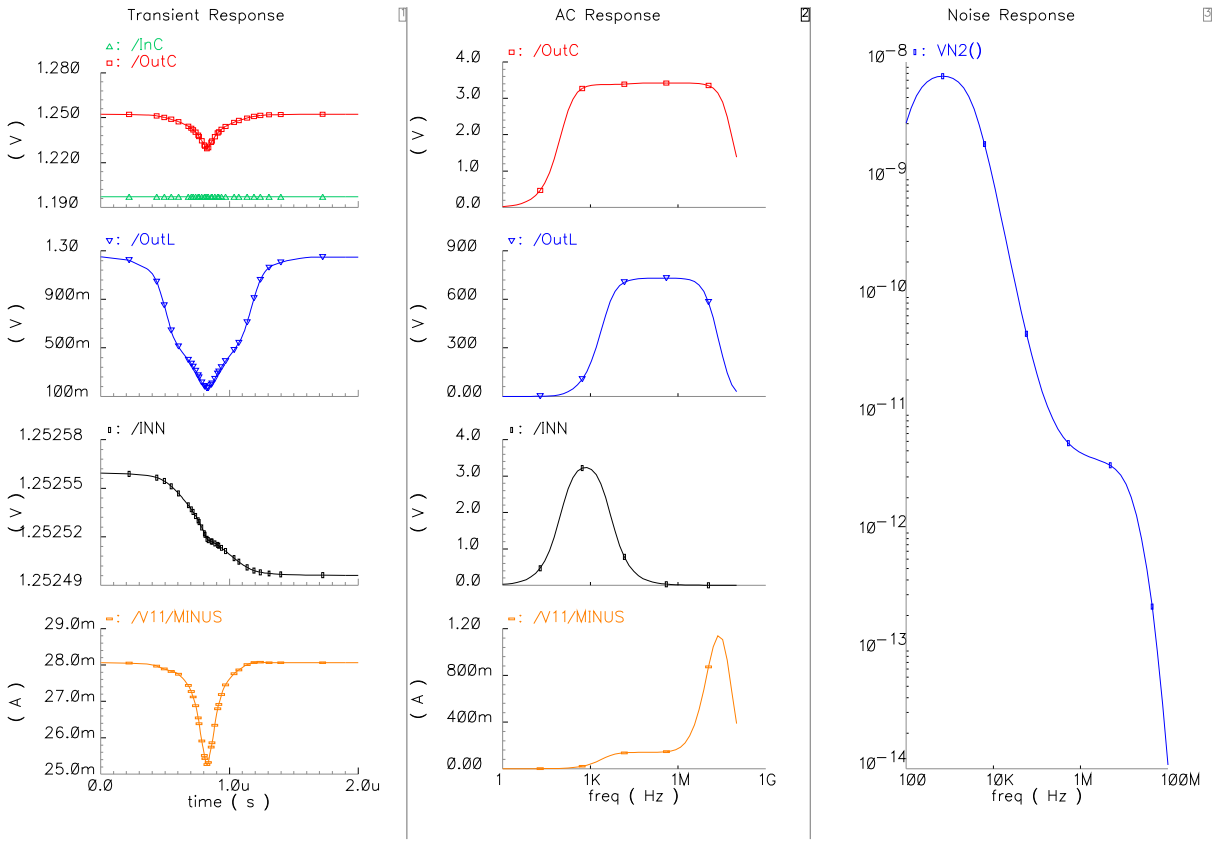

Figure 3.7: Simulation of the frond-end unit. Left: Transient response for a typical charge signal. From top to bottom: Input and output of the charge sensitive amplifier (InC, OutC), output of logarithmic amplifier (OutL), feedback voltage of logarithmic amplifier (INN), overall current drain (V11/MINUS). Middle: AC response of the corresponding signals. The spectrum of INN represents the frequencies filtered out by the external feedback circuit. Right: Noise spectral density. Flicker noise is dominant at lower frequencies up to 1 MHz. Above this range the spectral density flattens and white noise becomes dominant. The simulated total noise in the range of 10 kHz to 10 MHz is 65 electrons.

3.2 DUNE 1.1TR - Digital Transient Recorder

This unit is designed to digitize and record 32 analog signals with a resolution of 10 bit and a sampling rate of 25 MHz. The maximum buffer time is 40 μs. After that time, old data is replaced by new. Figure 3.8 shows the top level schematic of the transient recorder.

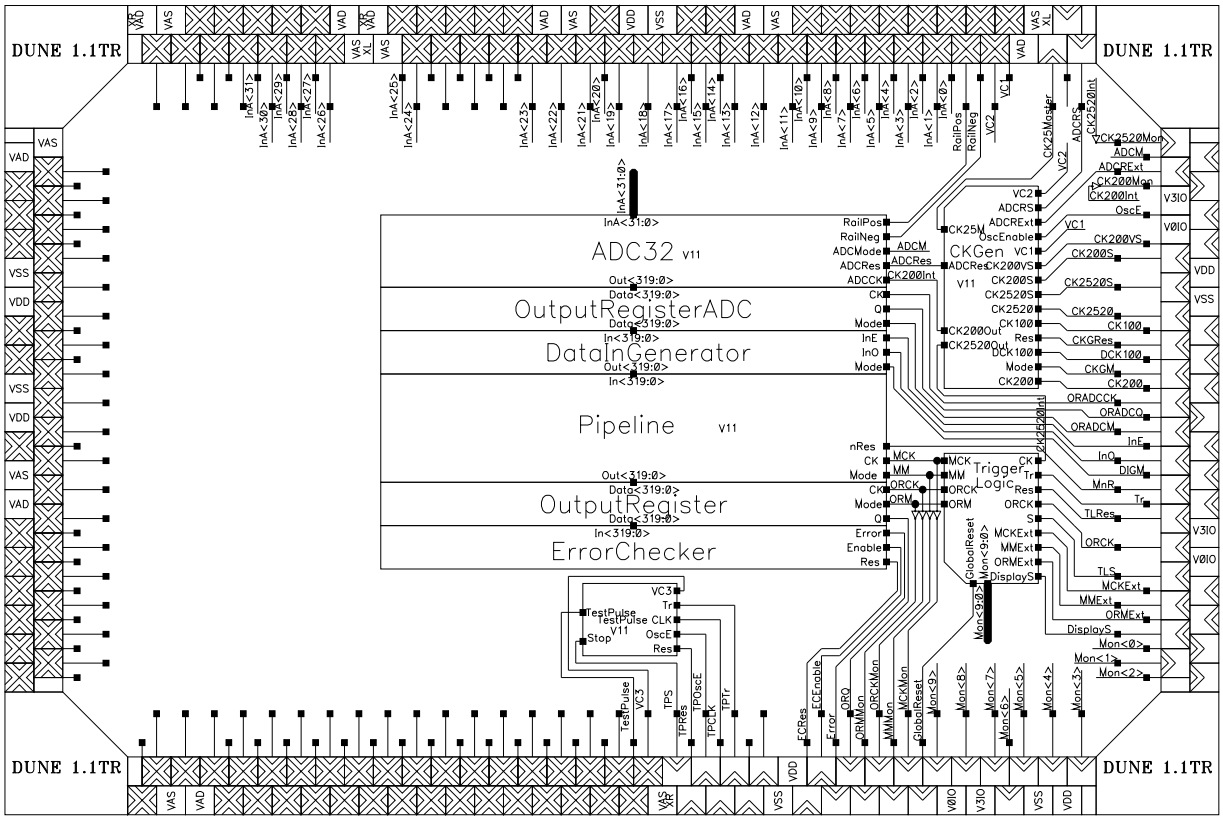

Figure 3.8: DUNE 1.1TR top-level schematic and pad assignment. The 32 analog inputs InA$< 31:0 >$ are routed to the 32 ADCs (ADC32). The 320 bit wide data stream is then stored in the pipeline. The output register is controlled by the trigger logic and serializes the parallel data stream on readout.

For compatibility reasons, the chip ring of DUNE 1.0 is utilized. This explains the large number of unused pads, since the front-end unit is no longer placed on this die. The 32 analog input signals InA$< 31:0 >$ are routed single ended to the 32 ADCs (ADC32). The succeeding block in the data path is the pipeline. It has to store the ADC data, which has a width of 320 bit (32 channels with 10 bit resolution). On a trigger event, the whole content of the pipeline has to be read out. This action is controlled by the trigger logic. It stops the cyclic recording on a trigger immediately and waits for the output register clock sequence. In conjunction with the output register, data is serialized and read out. A reset signal resumes the recording mode.

3.2.1 Analog-to-Digital Converter (ADC)

The data conversion of the DUNE charge signals is done with 10 bit Successive Approximation Register (SAR) ADCs. Their algorithm determines one bit per clock cycle, starting from the most significant bit (MSB). Thus, for a conversion rate of 25 MS/s, an internal operation of 250 MHz is required. Figure 3.9 shows the schematic of the ADC. The layout is presented in figure 3.10. The power consumption of this unit is approximately 3.5 mW, which is extremely low for a 10 bit ADC of this conversion rate. The on-chip power stability profits a lot from this fact, since 32 ADCs have to be operated in parallel.

The SAR, which is hard-wired to the D/A converter (DAC), is initially set to the 10 bit number 512 (1000000000) and a corresponding analog reference voltage V_{DAC} is produced by the DAC. This reference voltage is then compared with the sample voltage V_{S} to be converted. The output of the comparator drives a NAND-logic which sets the SAR to the next reference code. Automatically, the comparator receives a new reference voltage from the DAC and starts a new comparison. After ten cycles, the least significant bit (LSB) is determined and the conversion data is latched in the output register. A shift register is used to highlight the bit, that is currently processed. A controller generates the signals for the individual flip-flops of the registers. Figure 3.11 shows a simulation of the circuit at a 250 MHz operation.

Comparator

The comparator is the actual analog-to-digital interface. Its task is to compare the sample voltage with a reference voltage and indicate by a digital state, if the input is above or below the reference. The device has to cover the whole supply voltage range of 0 .. 1.8 V (VDD) in order to enable rail-to-rail conversion. Its propagation delay has to be smaller than 1 ns, and it must be sensitive to voltage differences smaller than 1 mV. These are quite strong constraints that are not easy to be met. In order to amplify sub-mV differences to a digital signal, a strong voltage amplification is required. This is achieved by five differential amplifier stages, that are connected in series. The first stage is built up by zero-V_{t} (threshold voltage) and low-V_{t} transistors in order to achieve an amplification even if the input voltages are close to a rail. After the first stage the common mode is rejected sufficiently, so standard transistors can be used. For maximum repetition rate and minimum propagation delay, the comparator is equipped with a self reset. It automatically detects, when a decision has been made and will reset itself ultimately for the next cycle. During the reset, the output lines of the differential stages are short circuited, so their voltage differences are eliminated. So, the succeeding conversion starts with a balanced amplifier and no extra charges have to be moved. Without the reset, the propagation delay would be dependent on the decision of the previous comparison. This was the case in the DUNE 1.0 ADC. The simulation clearly showed this dependence especially in the case of small voltage differences. Figure 3.12 shows the schematic of the comparator.

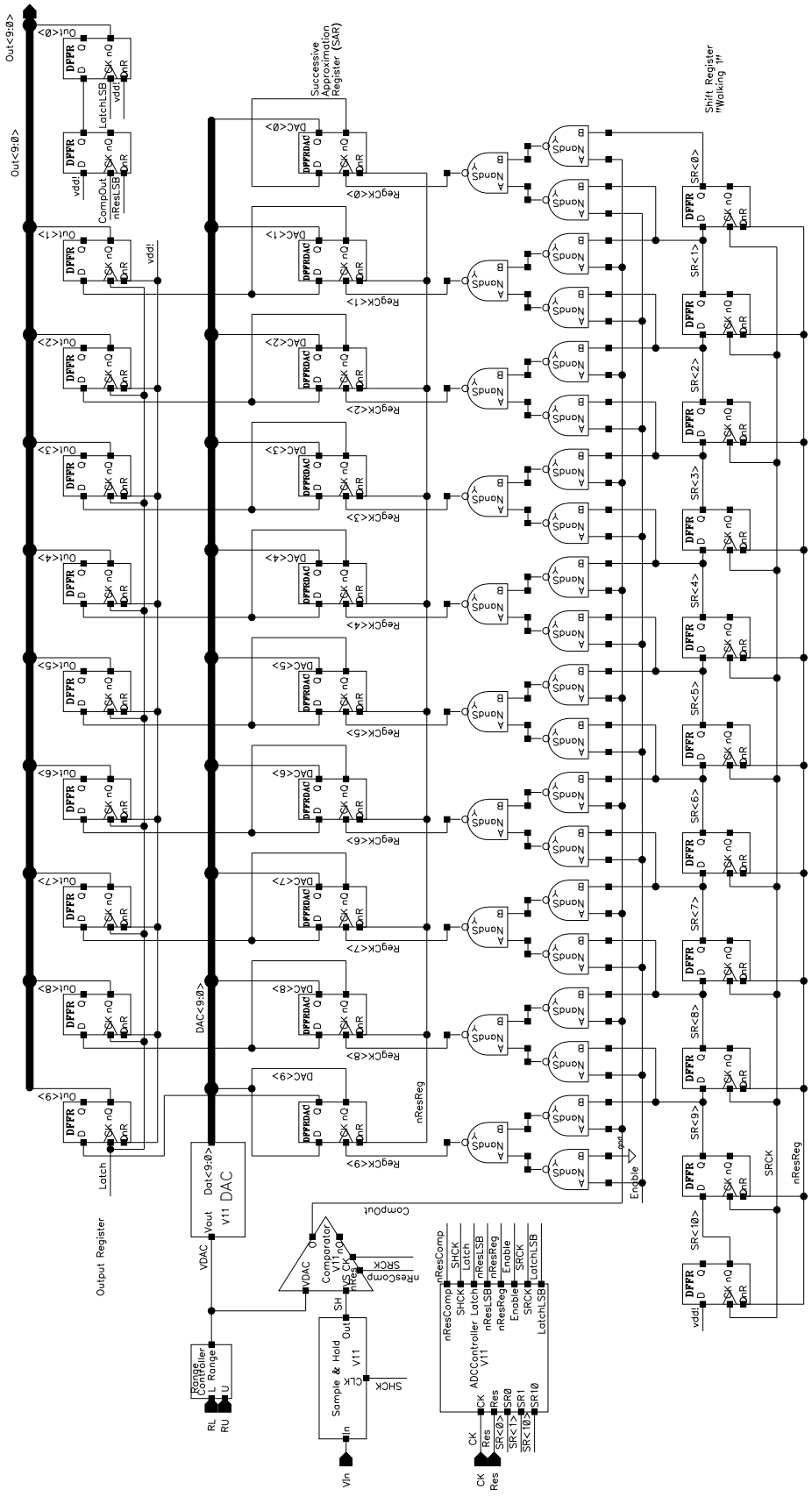

Figure 3.9: ADC schematic.

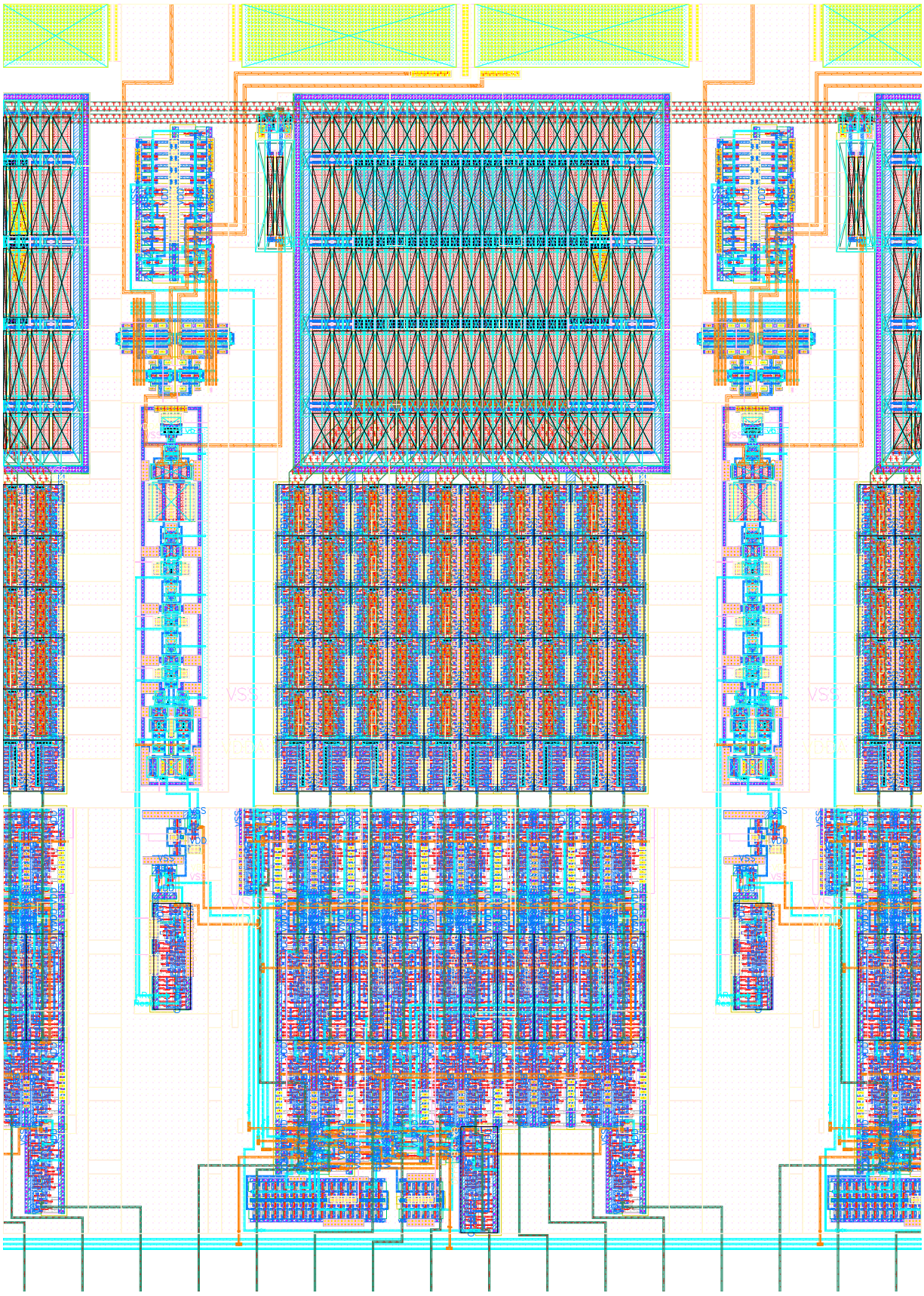

Figure 3.10: ADC layout.

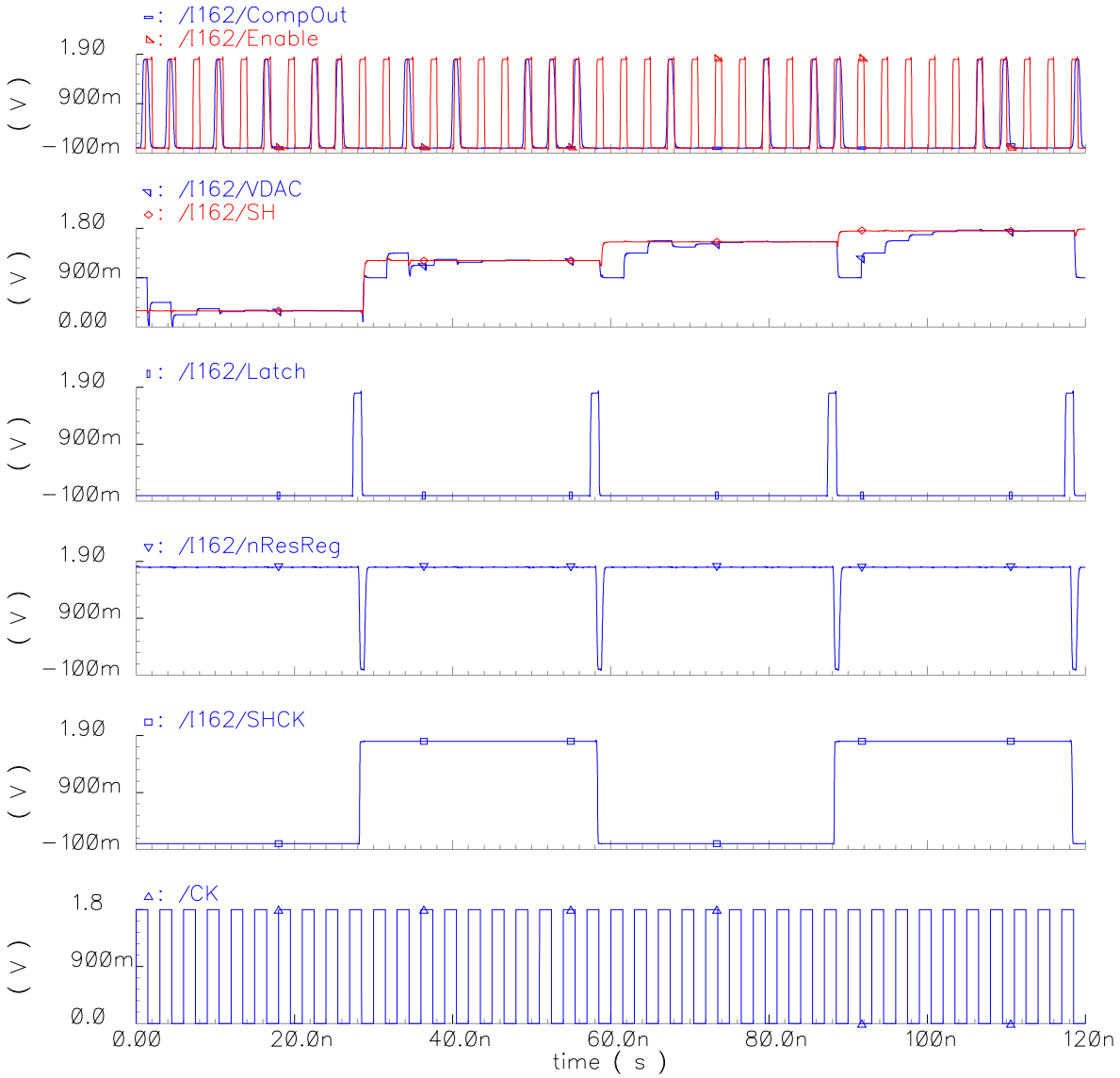

Figure 3.11: Simulation of the ADC. From top to bottom: comparator output and enable signal steering the SAR register, sample & hold voltage and approximating DAC reference voltage, output latch signal, register reset signal, sample & hold clock, ADC clock.

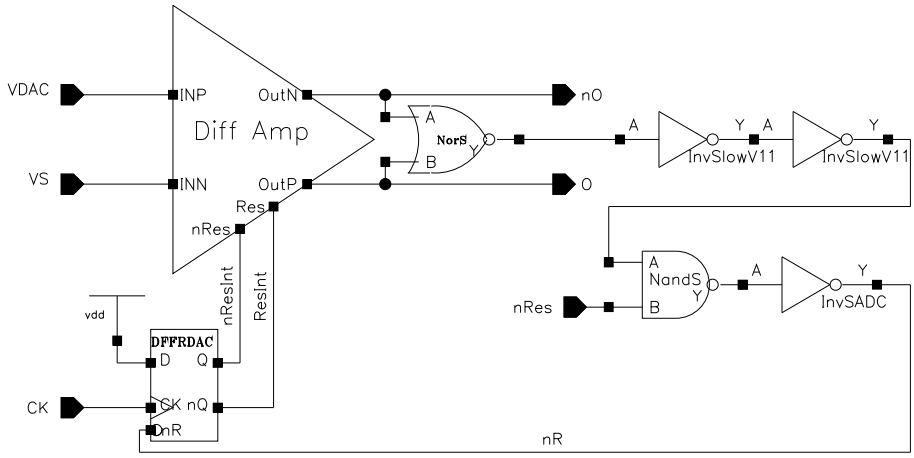

Figure 3.12: Comparator schematic. After reset, inverting and noninverting output (nO and O) are low. The comparison is started on the rising edge of a clock signal (CK), which releases the internal reset of the differential amplifier chain. One of the outputs transits to high depending on the input polarity. The transition on either output line is sensed by a NOR and a slightly delayed automatic reset is issued. So, output pulses of defined width are created, independent of the propagation delay. An additional reset signal (nRes) is sent from the ADC controller to limit the maximum time for a comparison.

Digital-to-Analog Converter (DAC)

The DAC is implemented as a standard R-2R ladder, which is driven by inverters (figure 3.13). The resistors are made of high resistive poly-silicon. Their resistance R is 2 kΩ and the dimension is 6 μm × 3 μm. Here, a clear tradeoff occurs between accuracy and speed of the circuit. The larger the area of the resistors, the better their matching, but the higher their parasitic capacitance. The parasitic capacitance of the resistors limits the switching speed of the converter and also causes high currents peaks, especially, when multiple converters are operated in parallel. Thus, the geometry of the resistors has to be chosen carefully to meet the specified requirements. Since the resistance of the driving inverters is not negligible, the resistors connected to these are slightly smaller, so the sum of the series resistances is exactly R.

Successive Approximation Register (SAR)

The SAR is build up of ten standard D-flip-flops with reset function. The state of this register is directly linked to the data input of the DAC. It is controlled by the comparator output and follows systematically the characteristic codes of the SAR algorithm. Therefore, two operations have to run synchronously: In the n^{th} clock cycle of the conversion the n^{th} MSB is set to high. At the same time, the $(n-1)^{th}$ MSB will be set back to low, if the comparator indicates that the actual reference voltage generated by the DAC is larger than

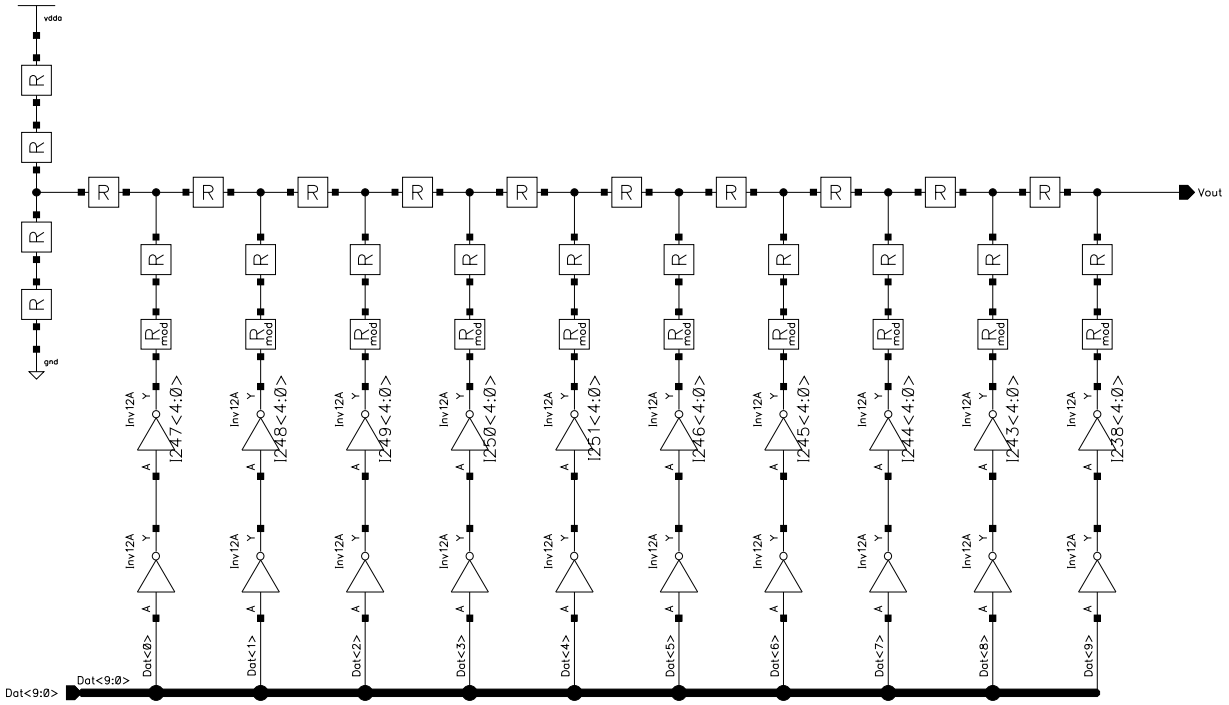

Figure 3.13: DAC schematic. The R-2R resistor ladder is driven by inverters. The resistors directly connected to the drivers are slightly smaller than R in order to account for the driving impedance of the inverters.

the input voltage. The register is clocked by an enable signal and the comparator output. Both are synchronously propagated to the currently processed bit, which is selected by the shift register. A delay chain in the enable signal compensates the propagation delay of the comparator.

Shift Register

The shift register contains a walking 1, a logic high state (pointer) propagating from one flip-flop to the next while keeping all other states low. Starting at the MSB, it indicates which bit in the SAR is currently being processed. In the 10^{th} cycle this register signals the ADC controller, that the pointer has reached the last stage and a reset signal is issued to setup the succeeding conversion.

Output Register

The 10 bit output code is determined successively during ten cycles. Therefore, the SAR never contains the conversion result completely. Not even in the last cycle, since the LSB is not latched in the SAR. As soon as the last comparison has been completed, the SAR is reset for the succeeding conversion. It is convenient to store the converted code in a 10 bit

output latch which enables a data valid time of roughly the conversion time (40 ns). This also simplifies the interface between ADC and pipeline. The first nine MSB are latched in the beginning of the 10^{th} cycle. The comparator output is latched as the LSB in this cycle. This is triggered with the falling edge of the ADC clock. Therefore, an effective data valid time of 38 ns is achieved.

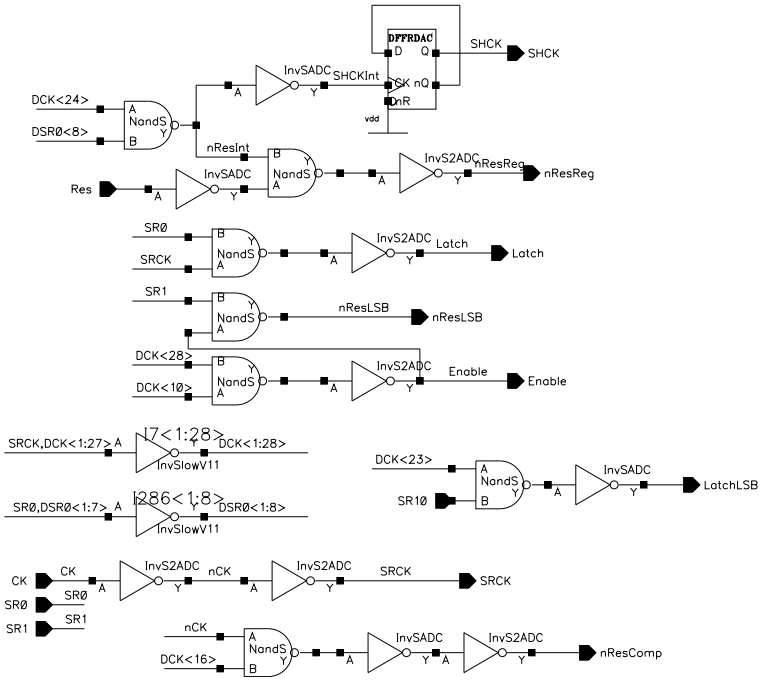

Figure 3.14: ADC controller schematic. From the 250 MHz ADC clock (CK) the S/H clock (SHCK), internal reset signals (nResReg, nResLSB and nResComp) and output latch signals (Latch, LatchLSB) are generated. The last two stages of the ADC shift register are connected to the controller (SR0, SR1). They indicate the last two cycles of the conversion and provide timing information for latching and reset.

ADC Controller

By handling the latching of the LSB in the mentioned way, the algorithm that does not require an extra cycle for setup. Ten bits are determined in ten cycles. The reset for the succeeding conversion is completed in the 10^{th} cycle. All control signals are derived from the ADC clock (250 MHz). By a delay chain, delayed clock signals are produced, which are then combined to create pulses at different times within the conversion cycle. Every clock period of 4 ns, the input voltage has to be compared to a reference voltage. The result of the comparison is needed to set the SAR, which drives the DAC to create the reference voltage for the successive comparison. It is obvious, that a tight timing schedule is required to guaranty functionality. Figure 3.14 shows the schematic of the ADC controller.

Sample & Hold Unit (S/H)

The S/H holds the input voltage constant during the conversion. The method chosen for this application is interleaved sampling, using two capacitors (C = 2.8 pF). While one capacitor is supplying its potential to the comparator, the second is connected to the input signal and charged to the sample voltage. When the S/H clock switches the connections of the two capacitors are exchanged. So, a valid sample voltage is achieved during the whole conversion cycle. The transmission gates on the input side are sized to form a low-pass filter with the sample capacitor, so frequencies above half the sampling frequency are filtered out. In order to avoid a shortage between the two capacitors non-overlapping clocks have to be generated. A short delay chain handles this by causing a time gap between the corresponding switching actions. Figure 3.15 shows the schematic of the S/H unit.

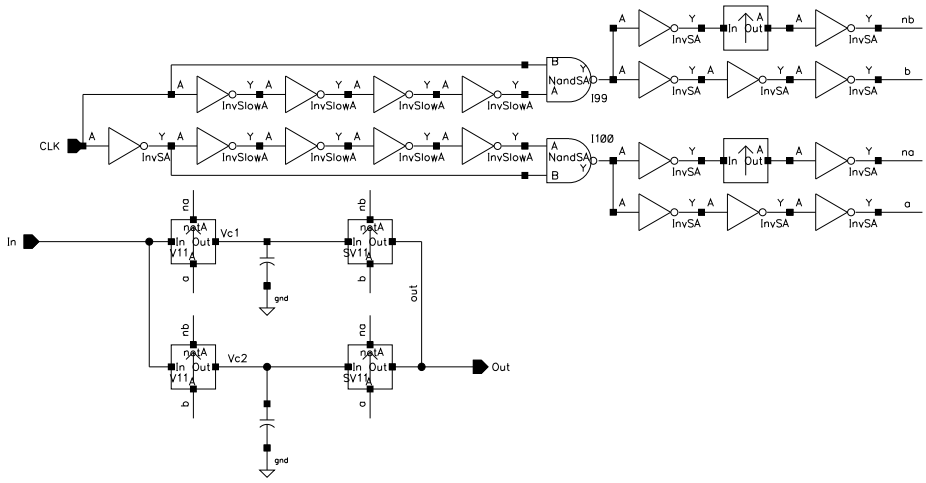

Figure 3.15: Schematic of the sample & hold unit. Interleaved sampling structure with non-overlapping differential clock generator. While one capacitance is charged to the input voltage, the other provides its potential to the comparator. The transmission gates are charge injection compensated.

Range Controller

The range controller is connected to the output of the DAC and forms switchable voltage dividers with respect to GND and VDD. The conversion range can be narrowed down from 0 .. 1.8 V to 0.4 V .. 1.4 V in order to avoid nonlinearity at the rails. For the DUNE readout chain this unit is rather unsuitable, since large particle charges cause signals that drop below 0.4 V. Also baseline fluctuations due to external disturbances (e.g. plasma currents) can easily push the signal above 1.4 V what in case of an activated range controller would lead to a clipped signal.

3.2.2 Pipeline

A SRAM (Static Random Access Memory) is chosen to buffer the converted data. The specified latency for the dust telescope is 40 μs, so a buffer depth of 1024 samples is suitable. The data bus width is 320 bit corresponding to 32 channels with 10 bit resolution. The layout is adapted to the ADC unit which determines the spacing between the channels. Since the spacing of memory cells is much smaller than the one of the ADCs, the memory columns are staggered fourfold. This way, no space is wasted on the die, but extra care has to be put into the control of the four sub-columns. On readout, the recording of new data is paused and the memory content can be read out. With more than 1.8 million transistors this unit is by far the largest one of DUNE 1.1. Figure 3.16 demonstrates the sub-column architecture.

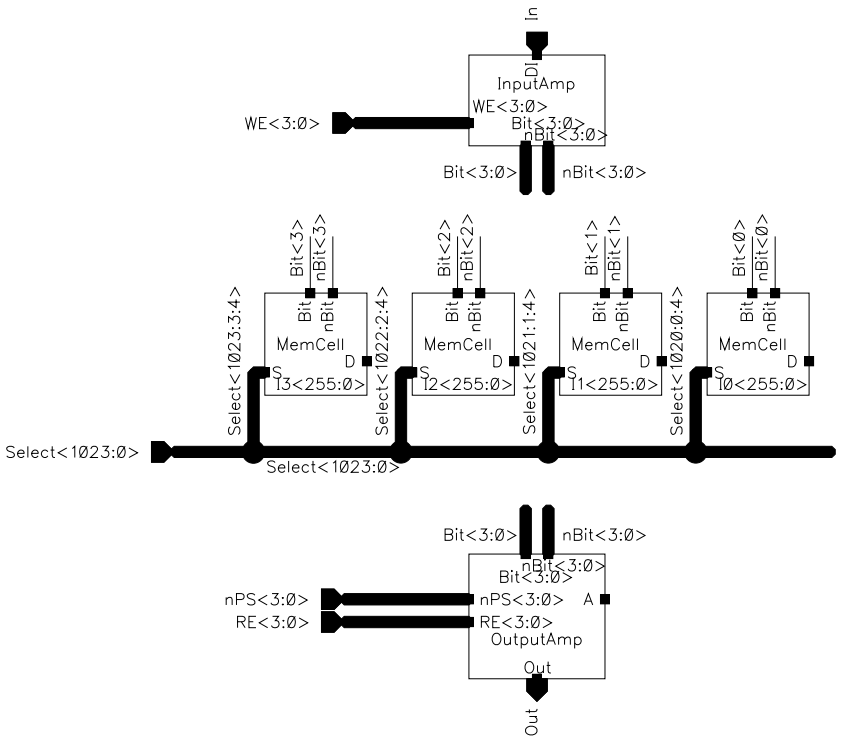

Figure 3.16: Pipeline Column with four sub-columns. Four pairs of bit lines have to be connected selectively to the I/O amplifiers. Therefore, all control signals have to be implemented fourfold.

Memory Cell

The bi-stable behavior of an SRAM cell is created by the direct feedback of two inverters. This inverter pair can be addressed by pass transistors, which connect the cell to the bit lines. When its select line is pulled the cell is forced to the state of the bit lines in case of a

write cycle, or it forces its state to the bit lines during a read cycle. Figure 3.17 shows the layout of a 8 bit memory cell array unit. The schematic of the memory cell can be found in figure 3.18.

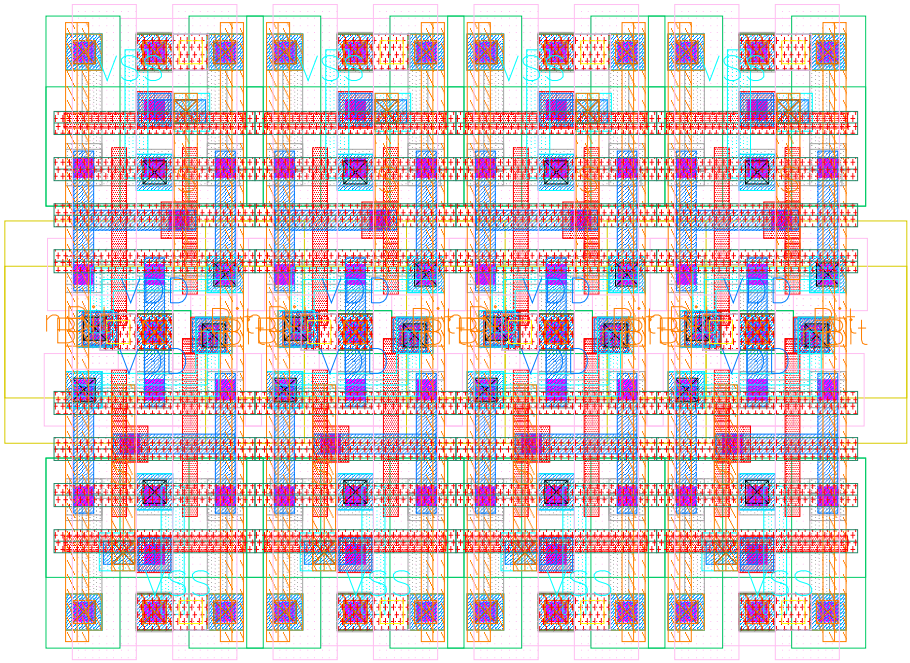

Figure 3.17: Layout of a 8 bit memory cell array unit. Four select lines (red crossed horizontal bars) have to be implemented per memory row to achieve the sub-column architecture.

Input Amplifier

This is a quite simple stage. It consists of two inverters that drive the bit lines of a preselected sub-column. These are connected via pass transistors which are switched by the write enable lines WE$< 3:0 >$ (see figure 3.18). During the write enable high phase data at the input of the memory has to be valid.

Output Amplifier

After a memory cell has forced the bit lines to a voltage difference during readout, the output amplifier stores this state in an output latch (figure 3.18). The read cycle is not finished at this point. The bit lines must be balanced again, so the succeeding read cycle will be successful. This procedure is called precharging. Therefore, the bit lines are shorted and connected to a common reference voltage. After this phase, a new readout can begin. Precharger and memory cell should never be attached to the bit lines simultaneously. This would lead to an unstable performance. On the other side the time between precharging

and readout should not exceed a few μs because leakage currents of the port transistors will disturb the balance. The succeeding read cycle will then destroy the memory cell content (compare Chapter 2.3.4).

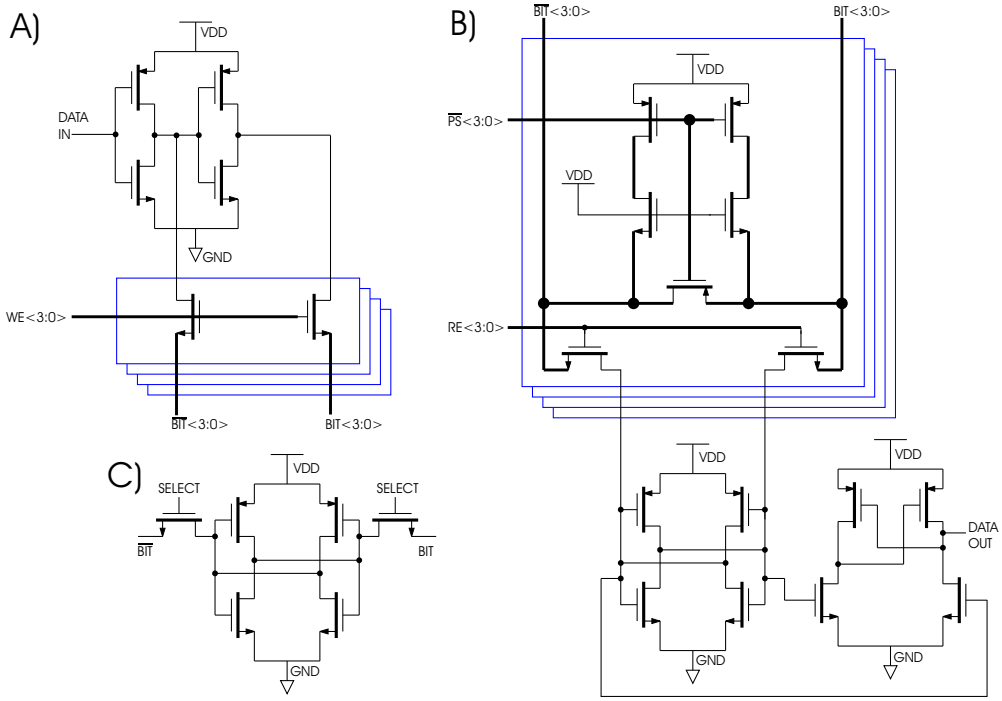

Figure 3.18: Pipeline components. The circuit parts highlighted with blue boxes are implemented fourfold in parallel. A) Input amplifier. B) Output amplifier. C) Memory cell.

Address Decoder

There are different possibilities to address data in a static memory. In a parallel structure like the 8 bit OTIS memory decoder [12], each select line is driven by a 9-input logic AND gate that combines an 8 bit address and one enable signal. The AND gates are hard wired to the address code, so each AND gate will switch on exclusively on an individual address. This technique is quite fast but scales strongly with the number of address bits. For a 10 bit address a binary tree configuration is more suitable to propagate a logic high state to one out of 1024 select line drivers. Figure 3.19 shows the schematic of the address decoder.

The addressing of the memory array has been specialized for the requirements of a ring buffer. A real random access is not required for the pipeline, since it acts as a ring buffer. A synchronous 10 bit counter that is driven by the memory clock provides the cycling address which propagates the decoder enable signal to one of the 1024 select lines.

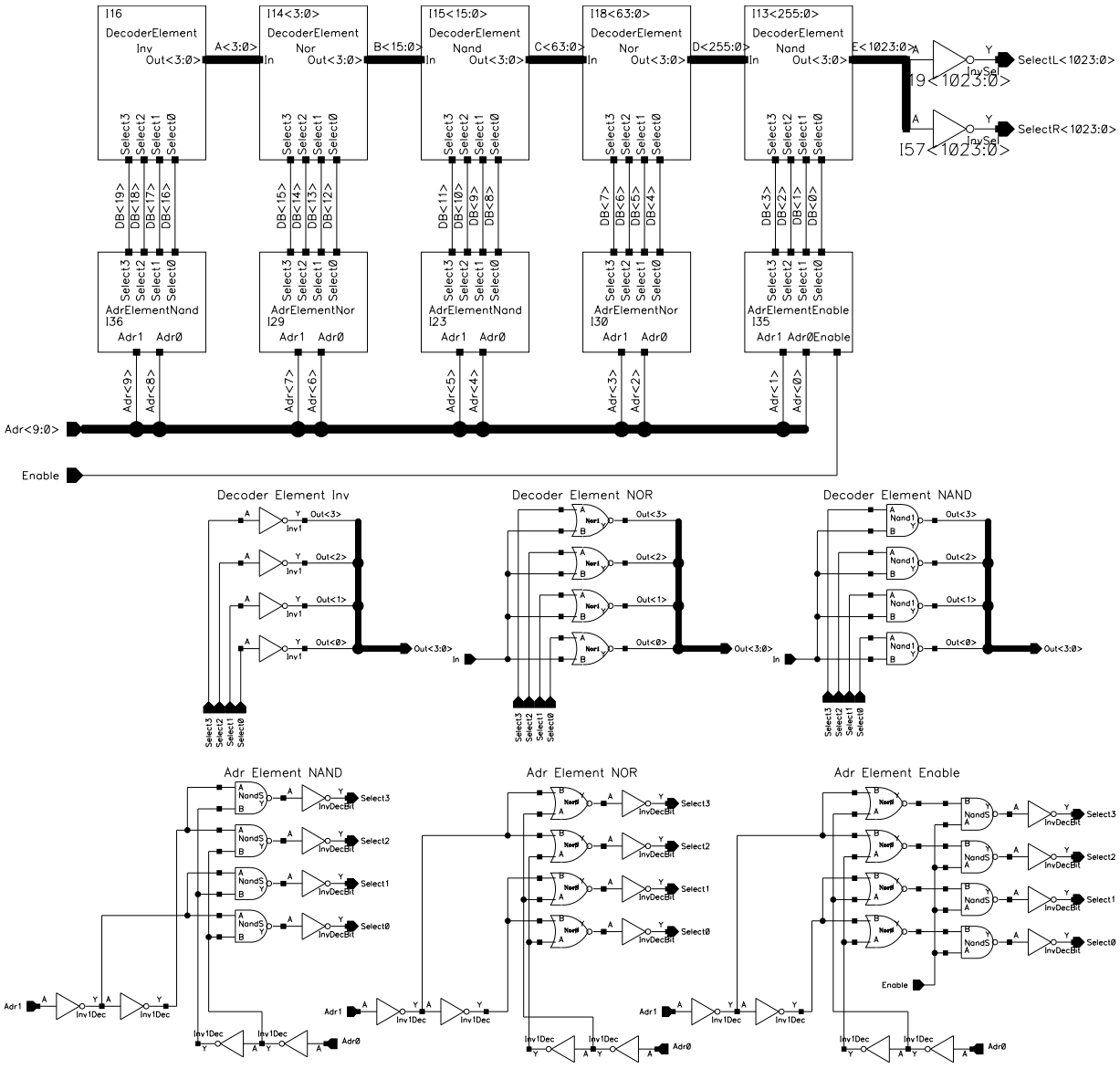

Figure 3.19: Address decoder of the pipeline. This is a binary tree configuration. The first stage decodes the two MSBs of the address code and selects one out of four lines (A$< 3:0 >$). The signals A$< 3:0 >$ are routed to four parallel decoder units that decode the next address bits in order to select one out of 16 lines (B$< 15:0 >$) etc. Finally, after five decoder stages one out of 1024 select lines is switched. With the enable signal the decoder output is propagated to the memory array.

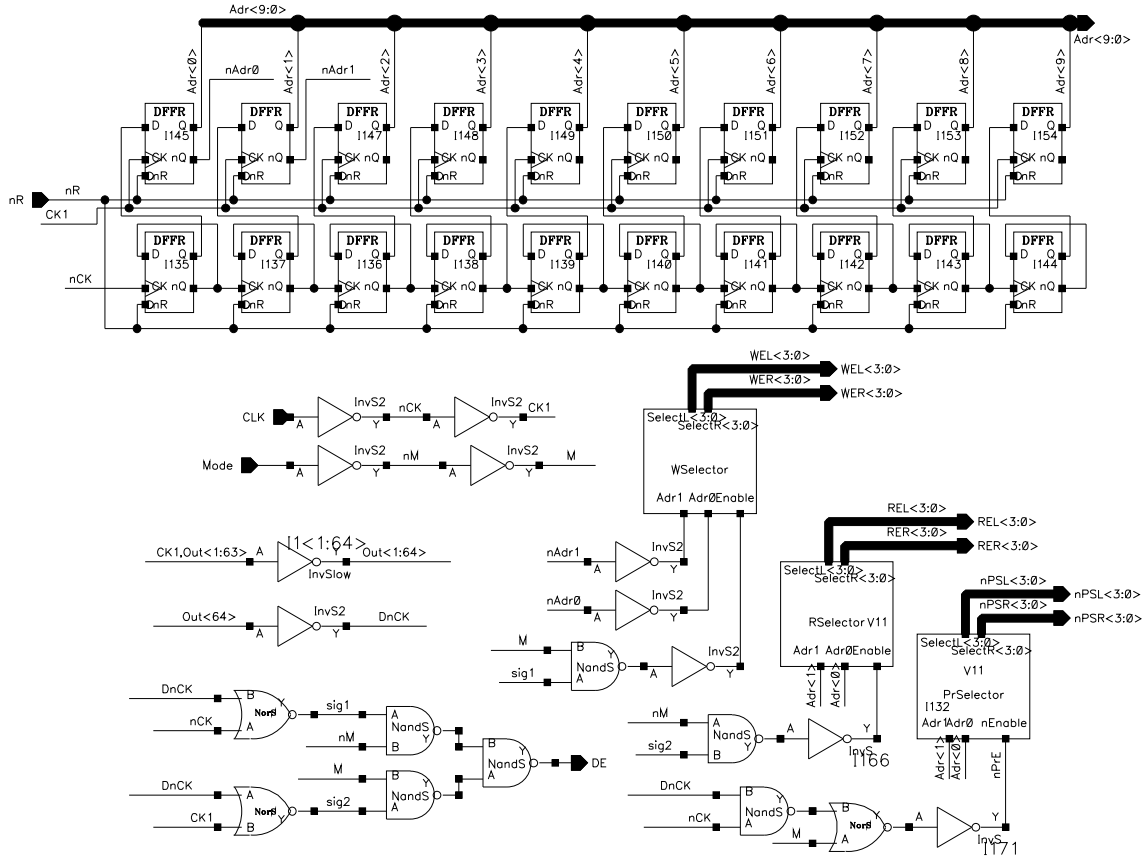

Figure 3.20: Pipeline Controller schematic. A 10 bit counter with output register generates a synchronous address signal. The two LSBs of the address (nAdr0 and nAdr1) are decoded internally to provide the sub-column information. The decoder enable signal (DE), the read and write enable signals (REL, RER, WEL, WER) and the precharge select signal (nPSL, nPSR) are produced by this unit.

Pipeline Controller

The pipeline controller coordinates the data flow from the input via the bit lines to the memory array during write and from the memory array via the bit lines to the output latch during read by switching the read and write enable, the precharge and the select signals in a pre-determined way. Figure 3.20 presents the schematic of the pipeline controller. Figure 3.21 shows the associated simulation results for an operation in read mode.

Since the whole procedure is clock driven and address and enable signals are synchronously generated, the timing constraints are easily obeyed. Only data setup and valid times have to be considered. While the output latch offers a data valid time of basically a whole memory clock cycle, a much smaller time window has to be covered with valid input data.

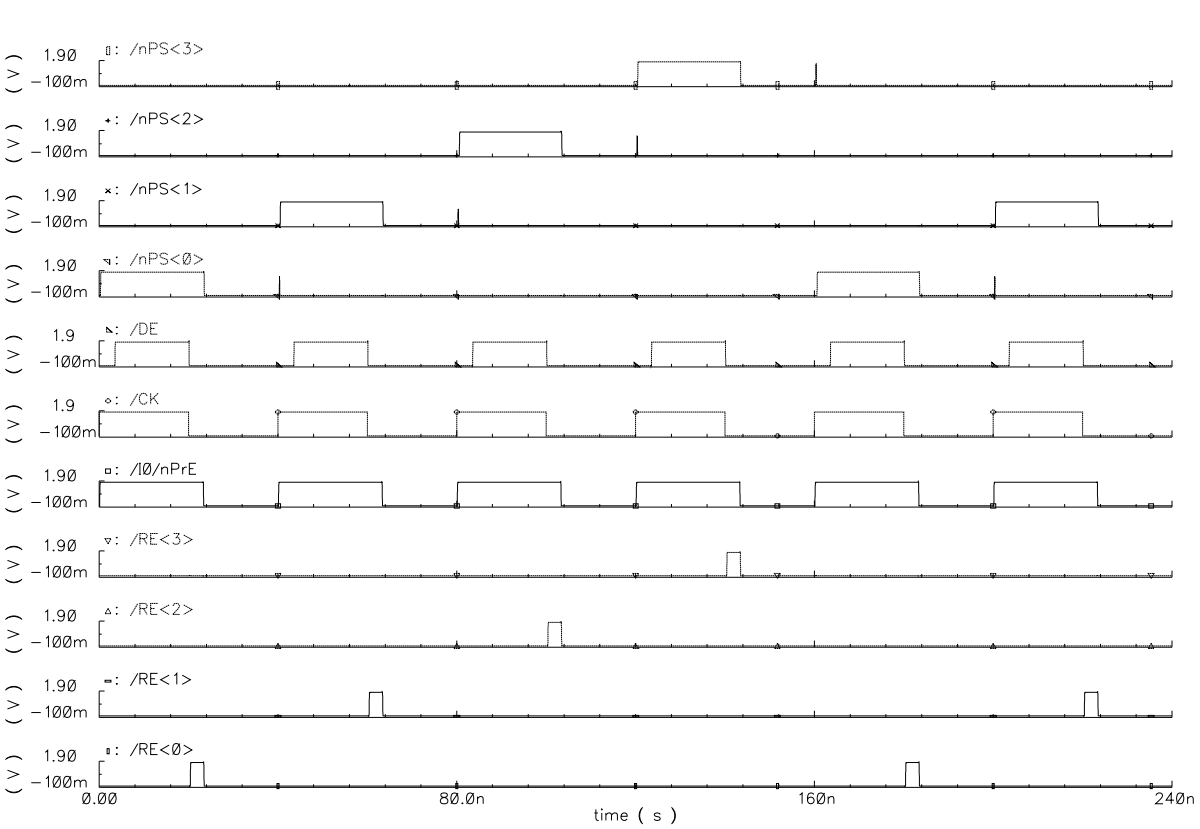

Figure 3.21: Simulation of the pipeline controller in read operation. From top to bottom: Precharge select signals (nPS$< 3:0 >$; active low), decoder enable signal (DE), memory clock (CK), precharge enable (nPrE; internal signal that is propagated to one of the sub-channels by the precharge selector), read enable (RE$< 3:0 >$)

3.2.3 Output Register

For readout, the 320 bit parallel output from the pipeline is serialized by the output register. It is a simple register circuit assembled by standard flip-flops and multiplexers. At the data pin of each flip-flop a multiplexer switches between parallel data input and the output of the preceding flip-flop. So a shift register configuration is achieved, which serializes the latched data set.

3.2.4 Control Logic

The whole data acquisition procedure of the transient recorder is directed by two clock signals, a trigger and a reset function. The main clock can be synthesized on-chip with a ring oscillator, which is part of the clock generator. By default, the trigger logic runs the memory in cyclic write mode. A trigger signal stops this performance and switches the memory to standby in readout mode. With the output register clock (ORCK) data can be

read out serially. The output register is loaded in one cycle with a whole data set from the memory. All 512 cycles the next data set is loaded automatically for serial readout. After the complete pipeline is read out, a global reset signal is issued.

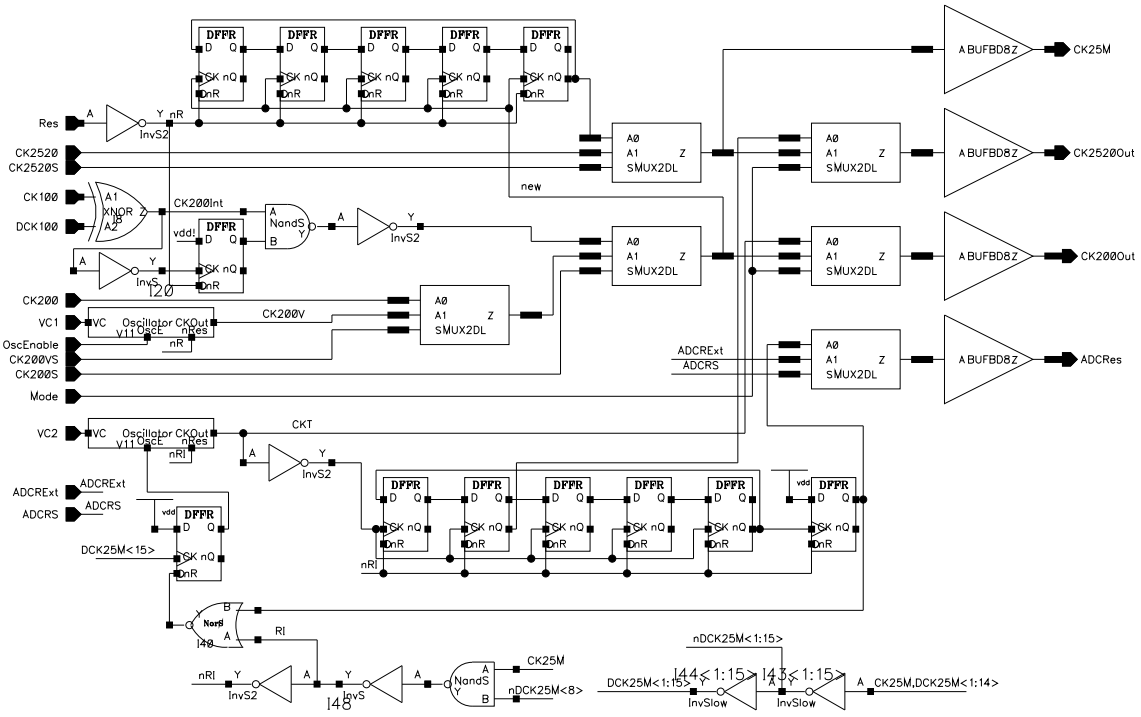

Figure 3.22: Schematic of the clock generator. Synchronized clock signals for the ADCs and the memory are produced by a voltage controlled oscillator (VCO). Optionally, the clocks can be provided externally.

On-Chip Clock Generator

The clock generator contains a voltage controlled oscillator (VCO), which receives an external control voltage V_{C1}. Its adjustable frequency ranges from 0 to 500 MHz. Nominally, it is set to generate a 250 MHz clock, which drives the ADCs. The 25 MHz memory clock is synchronously produced by a divide-by-ten register. Figure 3.22 shows the schematic of the clock generator.

A special operating mode has been implemented in this circuit. For the synchronization of multiple transient recorders in a complete detector setup a clock signal has to be sent over large distances off-chip. The setup is much simplified, if the synchronization is achieved with a clock of the conversion frequency rather than with the ten times faster ADC clock. Therefore, a second VCO (controlled by V_{C2}) is implemented in the clock generator, which is enabled for exactly ten clock periods. Triggered by a 25 MHz clock, it generates a train of ten pulses sent to the ADCs. The speed of this second VCO has to be slightly higher than

250 MHz in order to assure completion of the conversion. After a conversion is completed the VCO waits for the next rising edge of the 25 MHz clock, which will trigger the next ADC clock pulse train.

Additionally, an automatic ADC reset signal can be sent to the ADCs after each conversion. This option inherently makes the operation of the ADCs insensitive to Single Event Upsets (SEU: bit-flip due to interaction with nuclear radiation), since any bit-flip in the ADC state machine will be corrected at the end of the current conversion. Thus, only statistical errors would occur due to SEU effects, but the operation would be maintained.

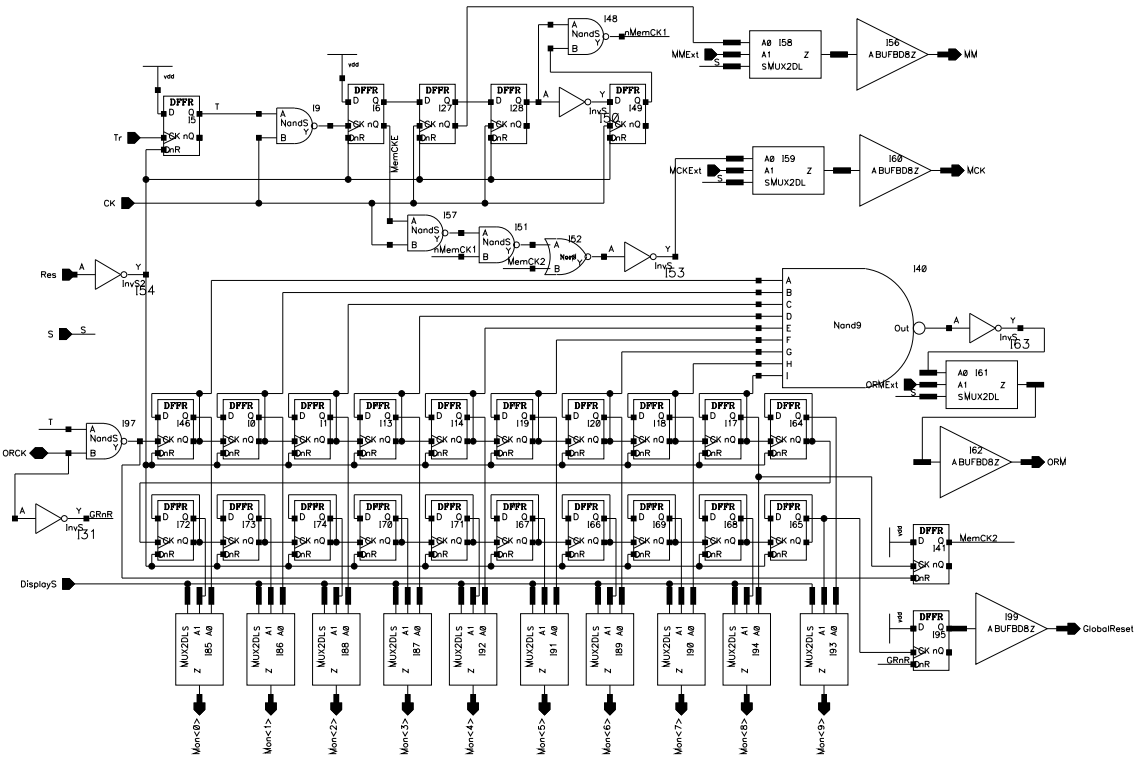

Figure 3.23: Schematic of the trigger logic. This unit controls the read and write operation of the transient recorder. During readout, it gates the 25 MHz memory clock (CK) and reacts on the external output register clock (ORCK). A 20 bit counter keeps track of the number of bits readout. Its state can be displayed via the status bits Mon$< 9:0 >$.

Trigger logic

The trigger logic handles the clock and mode signals of memory and output register. In recording mode, the output register is idle, and the memory clock is propagated from the clock generator. The memory mode is set to high (write mode). On a trigger, the current write cycle is completed, before the mode signal is switched to low (read mode). The first memory readout cycle is automatically performed. Then, the output register clock

(ORCK) is required, which shifts out the whole memory content bit by bit. The trigger logic also coordinates the refill of the output register with a new memory word, once the old word is completely read out. When the readout is completed, a trigger logic reset signal is required to resume the cyclic write mode. Figure 3.23 shows the schematic diagram of the trigger logic. Figure 3.24 presents the simulation result.

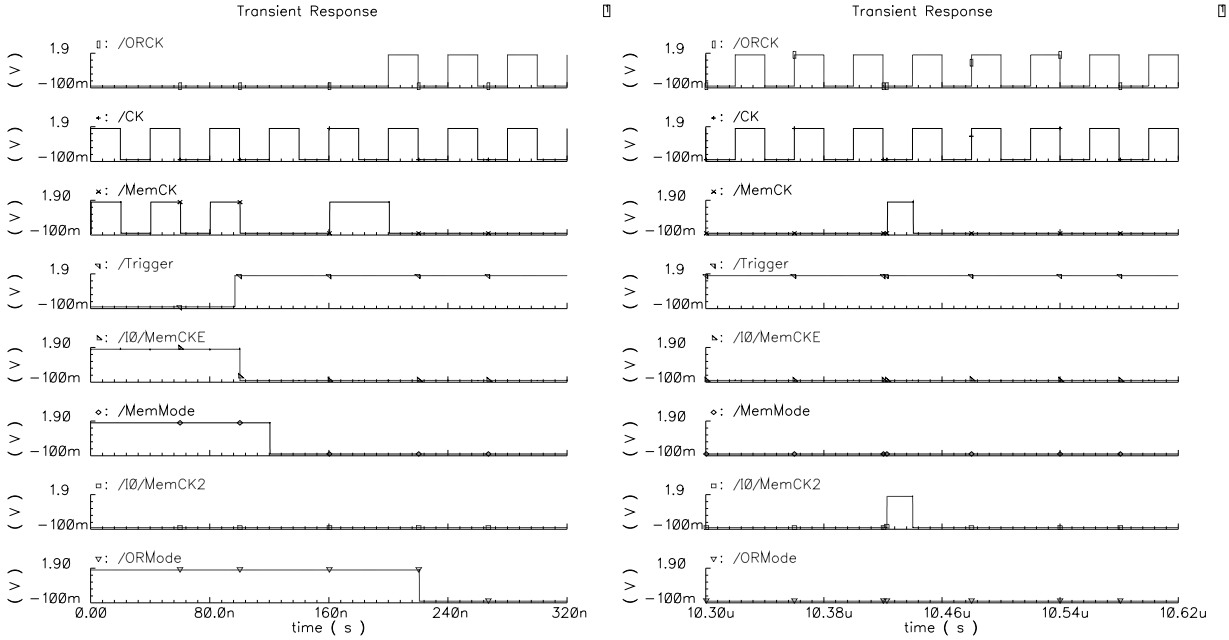

Figure 3.24: Simulation of the trigger logic. The trigger signal stops the memory clock (MemCK), switches the memory to readout mode (MemMode) and finally clocks the memory again to readout the first data word. Then, the output register clock (ORCK) can be sent, which reads out the latched data word serially. After 256 output register clock cycles, a memory clock pulse (MemCK2) is produced, which transports a new data word to the output of the memory. This is latched in the output register another 256 clock cycles later. Thus, 512 cycles are required to readout 320 bit.

Chapter 4

Measurement of DUNE 1.1

The first two sections of this chapter deal with the integration of the DUNE readout electronics in the trajectory sensor and the remote operation of the system from a computer. Section 4.3 covers system performance tests including operation of the complete readout chain. In section 4.4, the detector performance under realistic conditions is examined with tests at the Heidelberg dust accelerator facility. The last section summarizes the measurement results.

4.1 Front-End Setup

In order to achieve proper functionality of the front-end unit, a correct shielding and grounding strategy is essential. An incorrect setup may lead to oscillation of the amplifier due to ground bounce and coupling. Therefore, DUNE 1.1FE is exclusively tested at its designated location in the detector, which is optimized with respect to these issues.

4.1.1 Detector Board

A special detector board serves as mount for the amplifier chips and provides shielded strip lines on the board for the output signals. The output signals are then coupled via 1 kOhm resistors into wires, which are routed out of the sensitive volume through holes in the shielding. Power on the detector boards is provided by LM317 voltage controllers, which are set up to supply 1.8 V. Modern voltage controllers offer low noise and low drop characteristics. Nevertheless, after some tuning, a stable and convincing performance could be achieved with the standard LM317.

The most critical setup issue turns out to be grounding. Numerous connections have to be made between the detector board ground and the grounded detector shield in order to avoid mentioned high frequency oscillations. This requirement increases with the number of operated front-ends per board. For the complete assembly with 15 chips per detection plane, ground connections are made all 20 mm (one connection per amplifier).

The signal bandwidth can be adjusted by two SMD resistors on the board. Different

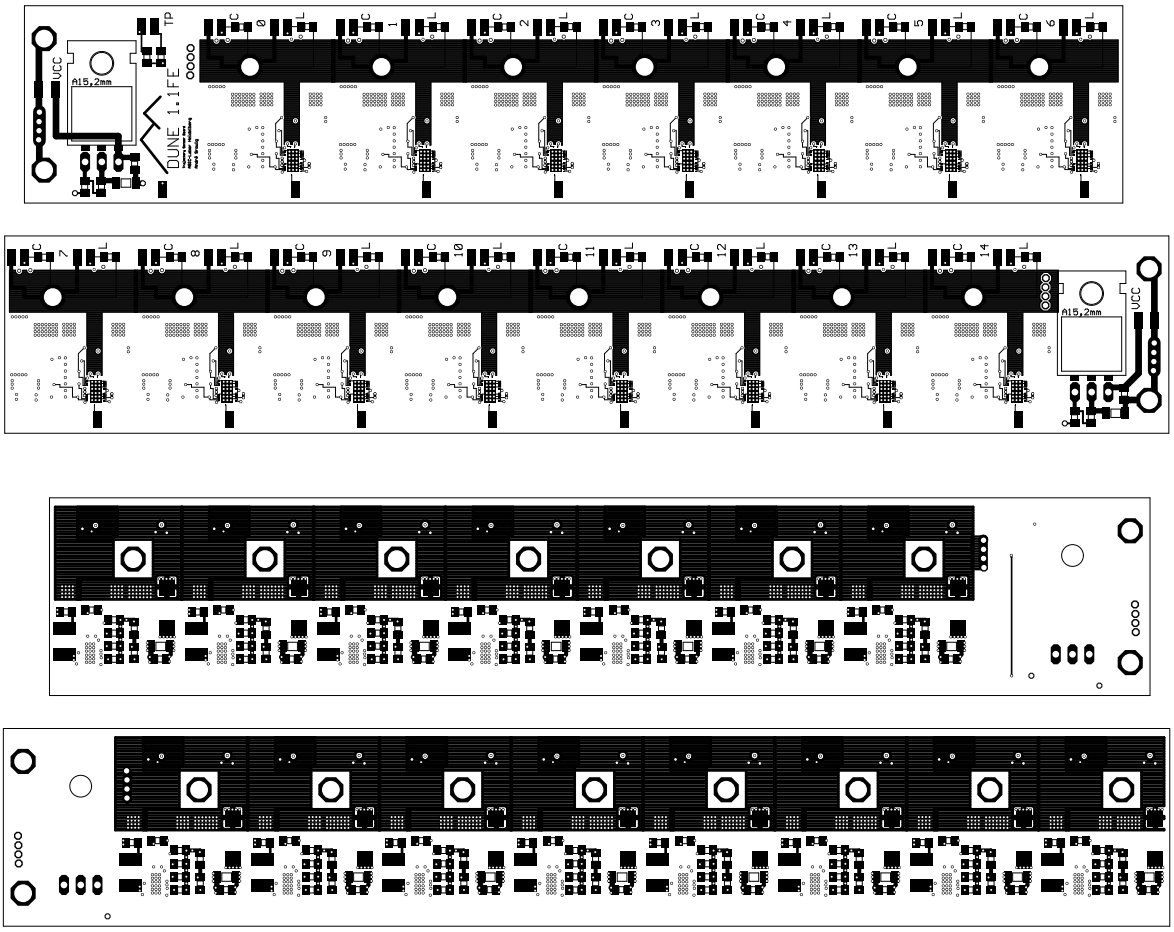

Figure 4.1: DUNE 1.1 detector board. The printed circuit board is a four-layer design with shielded output lines. Chip-on-board technology is applied. Filter components are placed on the backside of the board.

settings have been implemented on the various channels to examine the influence of these filter components. Figure 4.1 shows the layout of the detector board. The mounted front-end circuitry can be seen in figure 4.2.

4.1.2 Conversion Gain

The conversion gain of the complete front-end is determined by connecting a small capacitor (e.g. 1 pF) to the input of the charge sensitive amplifier. So, defined charges can be injected by applying a voltage pulse to the second pin of the capacitor. For this measurement, the charge has to be smaller than 1 fC in order to assure operation of the logarithmic amplifier in the linear range. The overall conversion gain of the front-end was so quantified to 404 mV/fC.

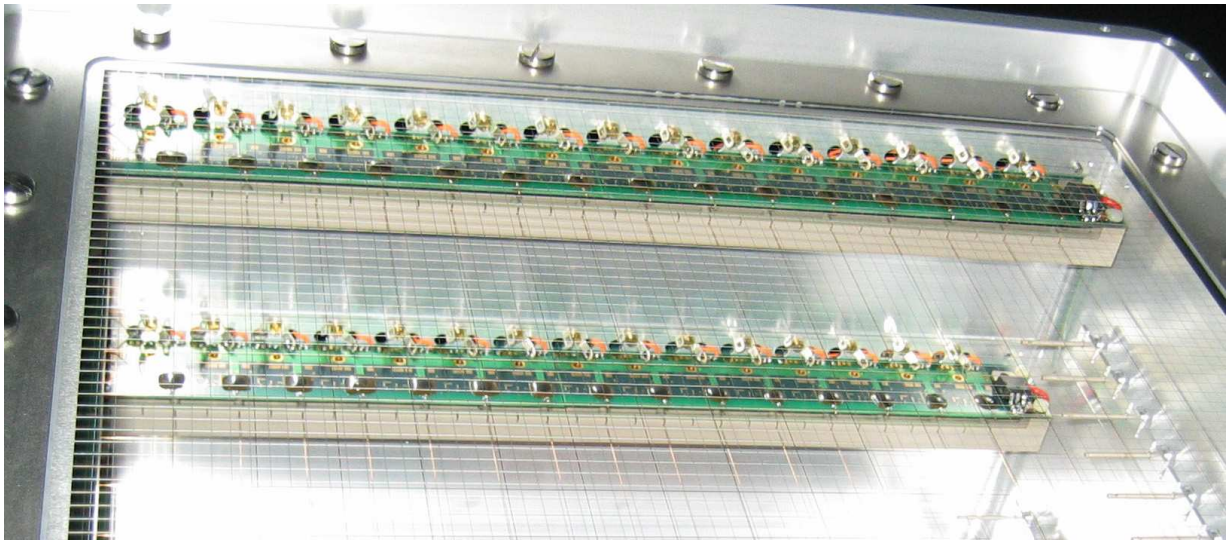

Figure 4.2: Detector inside. 30 front-end ASICs are bonded onto two detector boards and covered with glob top for protection. Ground connections between shield and boards are provided all 20 mm.

4.2 Transient Recorder Setup

4.2.1 Readout Board

For the operation of DUNE 1.1, the test board of version 1.0 can be utilized. Chip-on-board technology is applied, which minimizes the space requirements. The bonding area on the board is optimized for the pad layout of the chip. 208 pads are distributed in double staggered rows along the chip edge. The resulting bond wire pitch is 60 μm. Parallel bonding is so enabled, which minimizes the bond wire length.

For the interaction with the digital control logic, several switches and status LEDs are provided on the board. Further, there are potentiometers for controlling the on-chip oscillator speed and the test pulse shape. The majority of signals are accessible via connectors. Hence, external patterns can be applied to control the individual components of the readout chain. Also, the analog inputs are routed to those connectors. Figure 4.3 shows the bottom and the top side of the four-layer circuit board. One transient recorder chip is used for two detection planes. It is mounted on the detector frame outside the sensitive volume. So, the analog links between front-ends and recorder can be kept reasonably short.

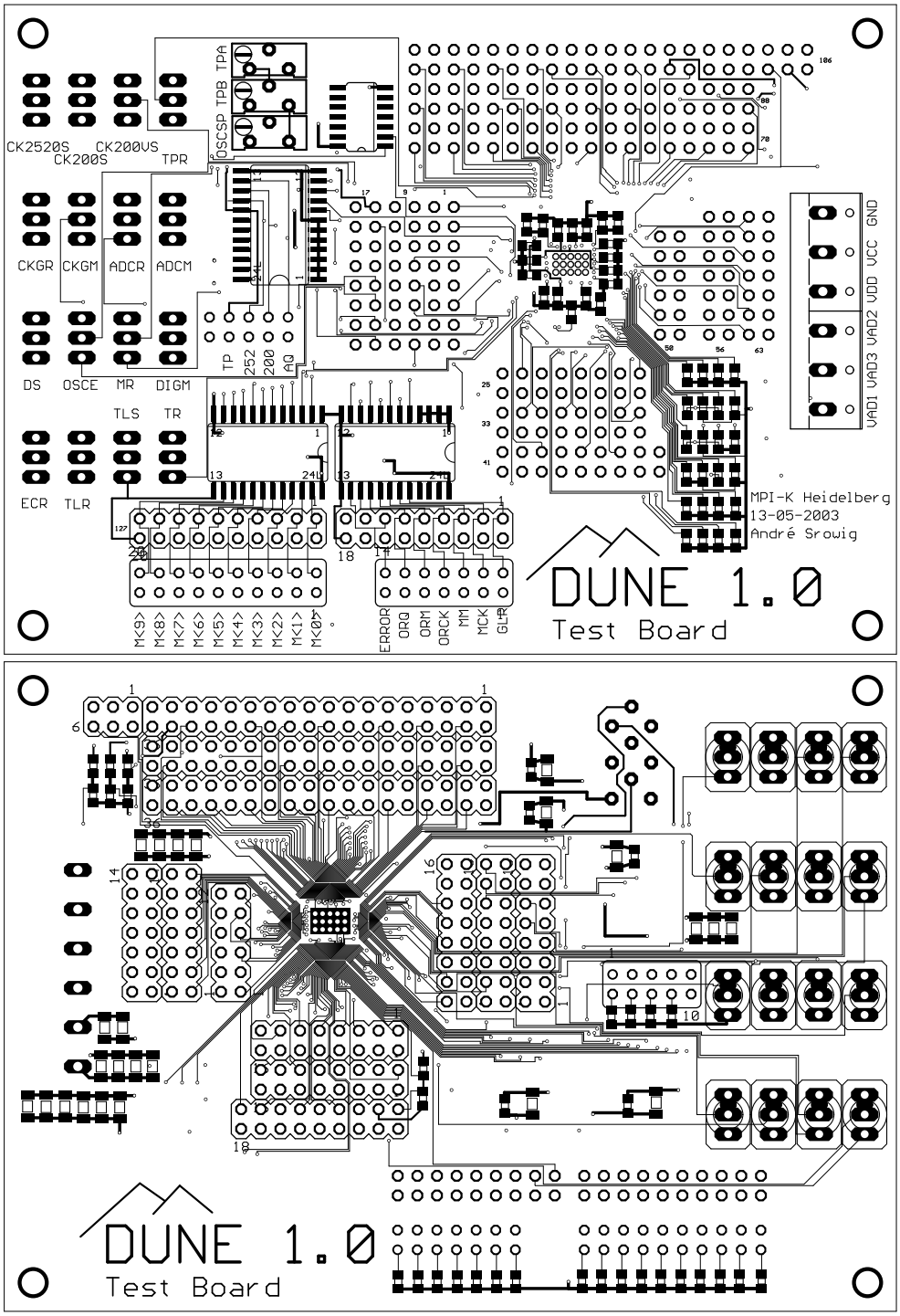

Figure 4.3: DUNE 1.0 test board with chip-on-board technology. The bond wire pitch is 60 μm. 16 switches and 21 LEDs enable simple control and testing of the circuit. Since the pad layout of DUNE 1.1TR and DUNE 1.0 are identical, the test board could be utilized for the detector assembly.

4.2.2 Control Interface

For readout control, a LabVIEW program is used. During the dust beam experiments the detector is mounted inside a vacuum chamber and linked via a flat band cable to a National Instruments data acquisition PC card. Thus, the operation of the readout chain can be controlled remotely from a computer. Six signals are required to control the DUNE readout scheme. Starting from power up, reset signals have to be sent for the clock generator (CKGRes), the trigger logic (TLRes) and the ADCs (ADCRExt). With the release of the clock generator reset signal, the internal clocks of DUNE start to run. Therefore, a suitable initialization sequence is to disable the on-chip clock generator via its reset signal, then perform a reset of the 32 ADCs and the trigger logic and then start the recording with releasing the clock generator reset. Figure 4.4 shows the sequence of the control signals.

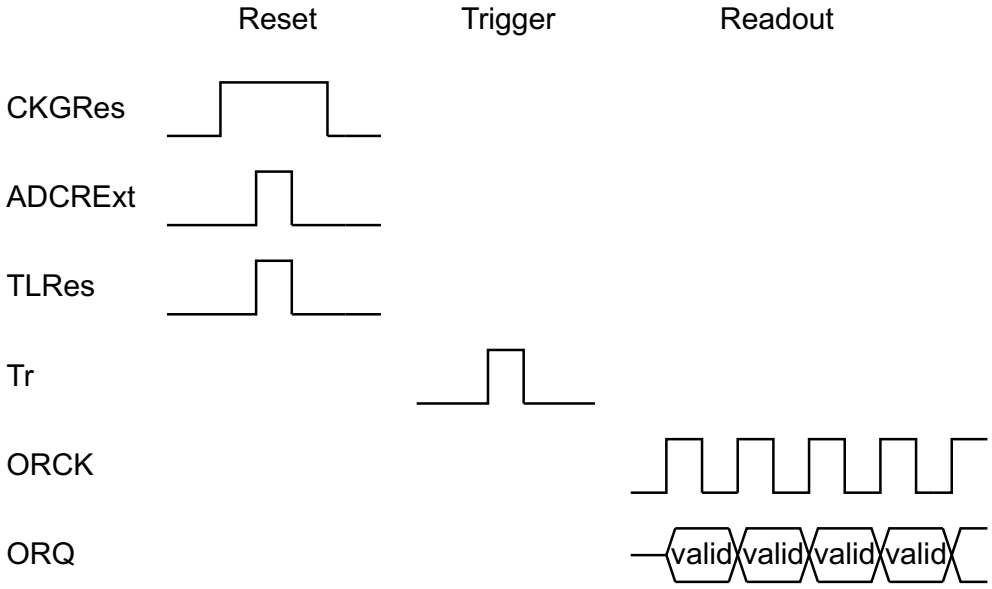

Figure 4.4: DUNE 1.1 control sequences. After reset, the system is in recording mode. A trigger signal stops the recording, so data can be read out. 2^{19} clock pulses have to be sent to the output register (ORCK), in order to read out the complete memory.

The trigger (Tr) of DUNE 1.1TR is connected to a wired-OR gate mounted on the adapter of the digital flat band cable. So, a trigger can either be propagated from the computer or from an external source like the impact target. For the performance measurement of the ADC, triggers are sent from the computer and data is taken out of the pipeline. Although the 32 ADCs have their own readout register, it is easier to incorporate the memory for the measurement, since it is operated synchronously with the ADCs and thus automatically obeys their data valid time. Also, consecutive samples can be readout and analyzed.

Data is read out by sending an output register clock signal (ORCK) from the computer. The LabVIEW program then reads the whole memory content serially from the data output pin (ORQ) and stores it as decimal numbers representing the output codes of all channels.

4.3 System Performance Tests

4.3.1 Functionality

Figure 4.5 presents a linear rail-to-rail sweep of 24 ADCs. the other eight ADCs on DUNE 1.1TR are copies of the DUNE 1.0 version (not shown). Channels 1 .. 16 are equipped with the nominal configuration of the ADC. Channels 17 .. 20 have a S/H unit with smaller sample capacitors (C = 1.4 pF). Channels 21 .. 24 are implemented without S/H unit. The conversion rate is 25.7 MS/s.

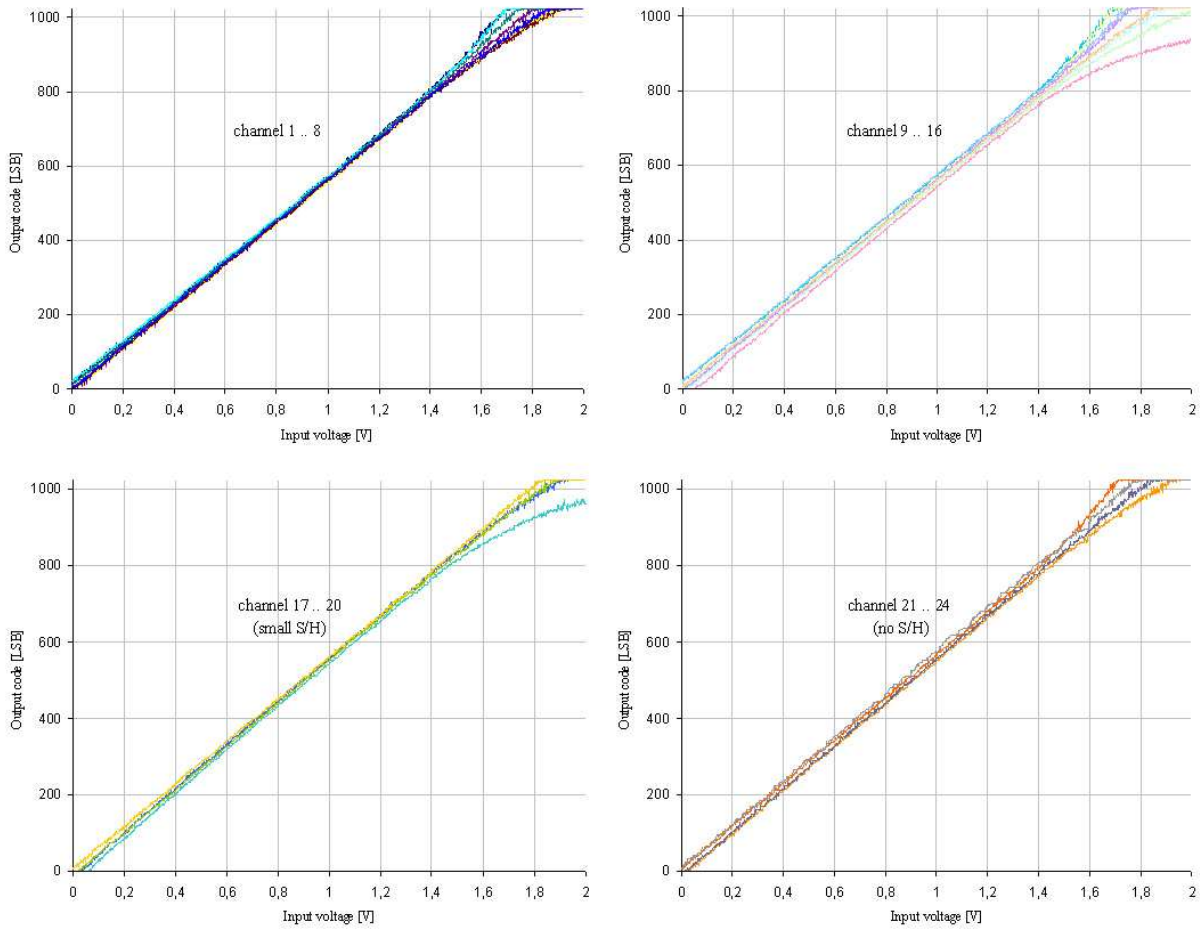

Figure 4.5: ADC rail-to-rail sweep at 25.7 MS/s conversion rate. 1024 samples per channel are recorded.

4.3.2 ADC Characterization

In order to quantify the performance of the ADCs, a curve fit to the measured conversion function is performed. The deviation of the ADC data from the fitted curve represents the effective noise of the converter. This procedure is visualized in figure 4.6. The RMS value of the effective noise is 2.1 LSB.

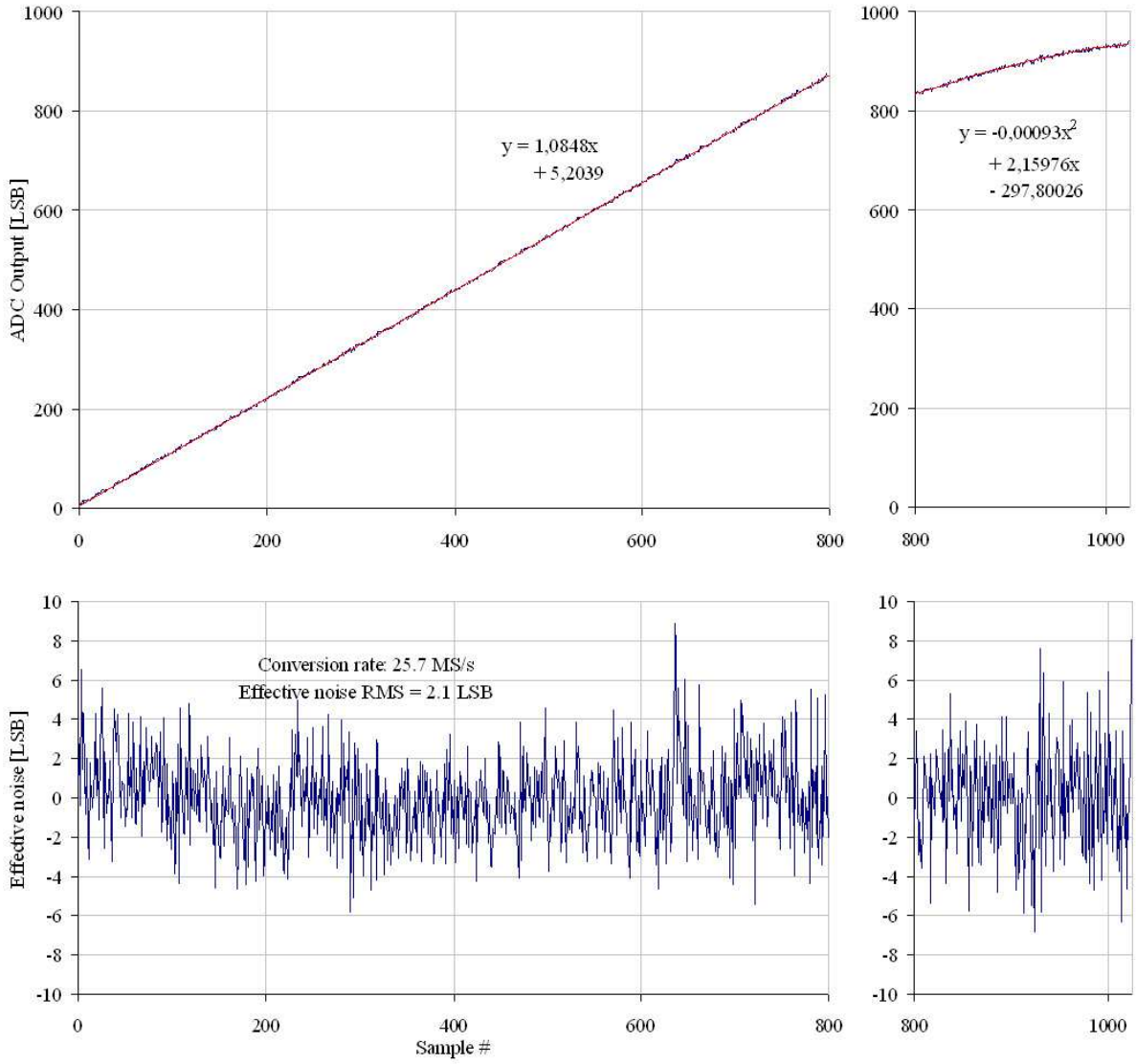

Figure 4.6: ADC linearity and effective noise. Left: Linear fit to a typical channel. Right: Quadratic fit to the worst case channel at the upper rail.

Excellent linearity is given in the whole operating range of the DUNE readout chain (V_{in} = 0 .. 1.3 V, codes 0 .. 740, compare figure 4.9). The baselines of the front-end

amplifiers are situated below 740 bins and charge signals are recorded with negative amplitude. The curve fit in figure 4.6 demonstrates, how the relation between input voltage and output code can be described by a linear function. Output codes close to the upper rail in the full range mode are slightly distorted due to mismatch of the low-V_t transistors in the comparator. This range can be represented by a nonlinear function.

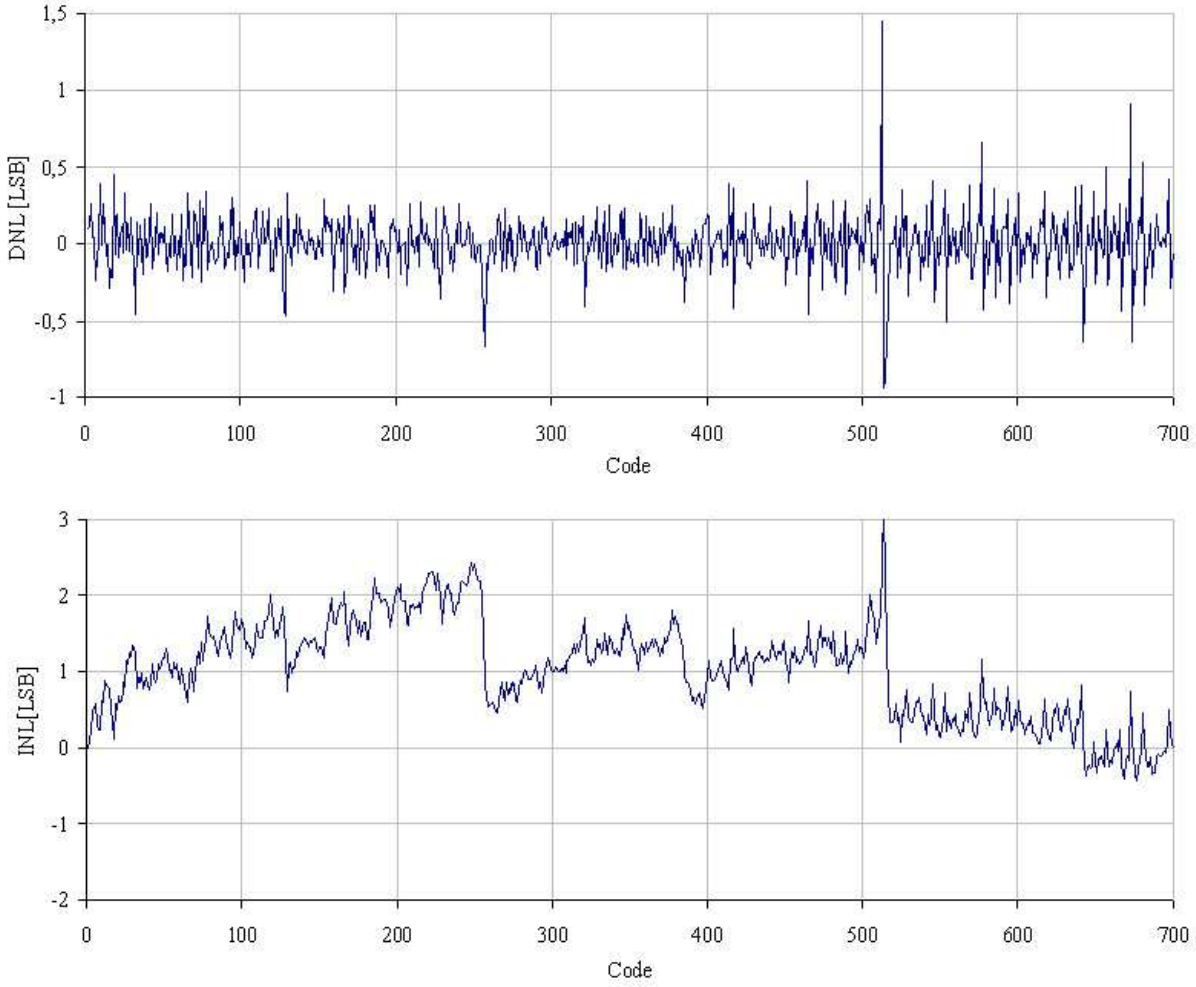

Figure 4.7: DNL and INL of the ADC in the DUNE operating range.

The performance of a converter can be expressed by its differential and integral nonlinearity (DNL and INL). These values are determined by statistical methods. The linear voltage sweep is therefore repeated with 65000 samples taken and histogrammed. The cumulative percentage of an output code then represents the step width of this code in the ADC transfer curve. The DNL is the difference between the actual code width of a nonideal converter and the ideal case. The INL is defined as the integral of the DNL. The results are plotted in figure 4.7.

The largest error in the linearity of the ADC appears at code 512. This is where the MSB is transiting. Mismatch of the DAC resistors determining the MSB causes this error.

In order to improve the linearity of the ADC at the upper rail, the range controller has been implemented. It can be set to decrease the upper rail of the input voltage range from 1.8 V to approximately 1.4 V. In this range, the nonlinearity of the comparator is negligible and good DNL and INL is achieved for all output codes (see figure 4.8).

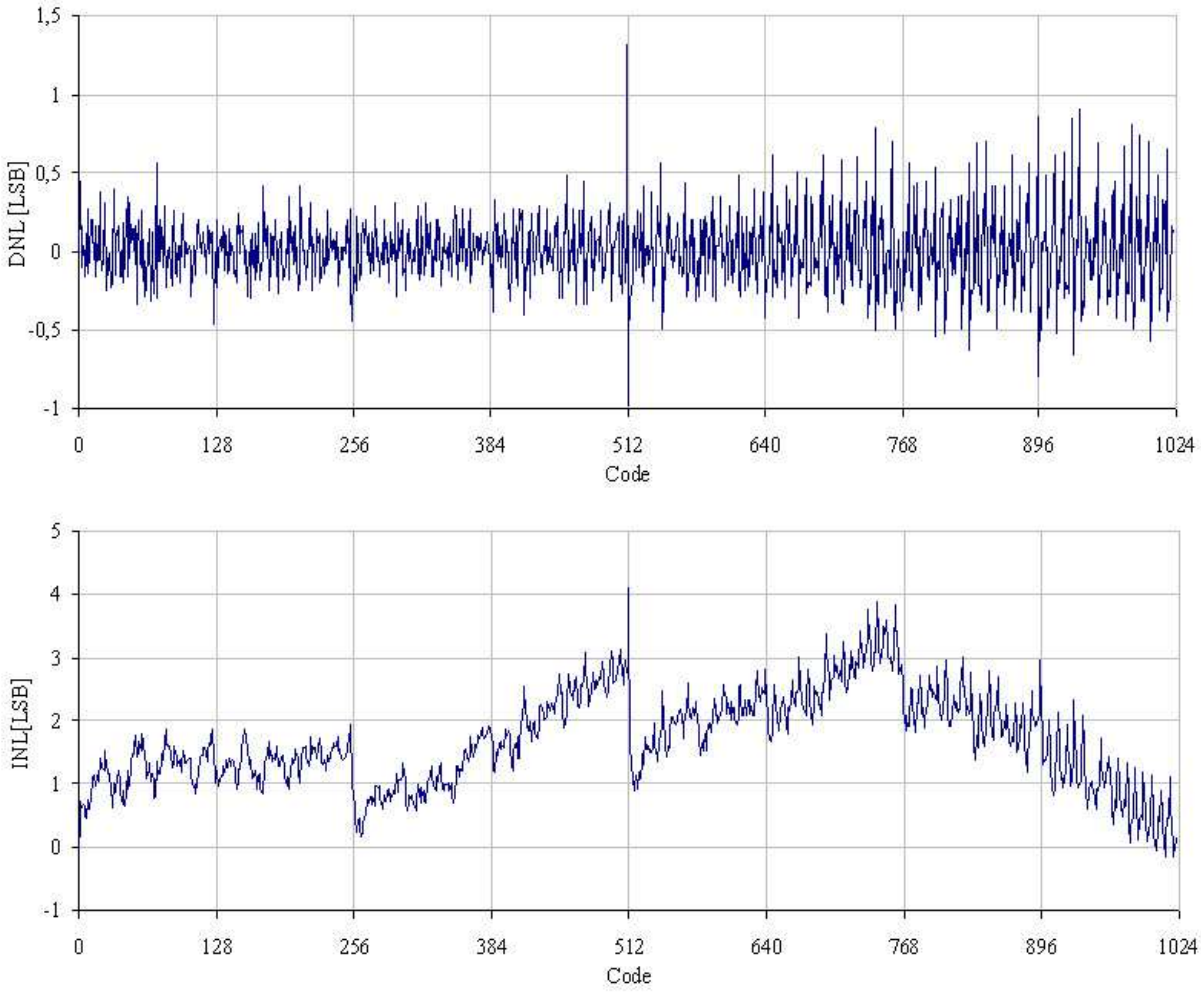

Figure 4.8: DNL and INL of the ADC with activated range controller. Input voltage range is 0 .. 1.4 Volts. The INL is dominated by mismatch of the R-2R DAC resistors determining the MSBs.

For the DUNE readout scheme, the range controller is disabled. The intension is to allow reasonable baseline shifts of the front-ends due to external disturbances such as plasma currents in space without ending up with a saturated signal. Therefore, sufficient signal

range should be provided for both polarities. Additionally, the logarithmic amplifier also has a nonlinear amplification in this range. Performing an overall per-channel calibration, the nonlinearity of the ADC can be corrected.

4.3.3 Front-End Calibration

Every detection plane is equipped with one test pulse wire. If a voltage signal is applied to it, charges are induced on the wires of the adjacent planes. Except of the outer wires, the coupling capacitances between test pulse wire and sensor wires match well, since they are determined geometrically by the distance of the detection planes. Figure 4.9 shows the 30-channel transient response corresponding to a 5 mV test pulse.

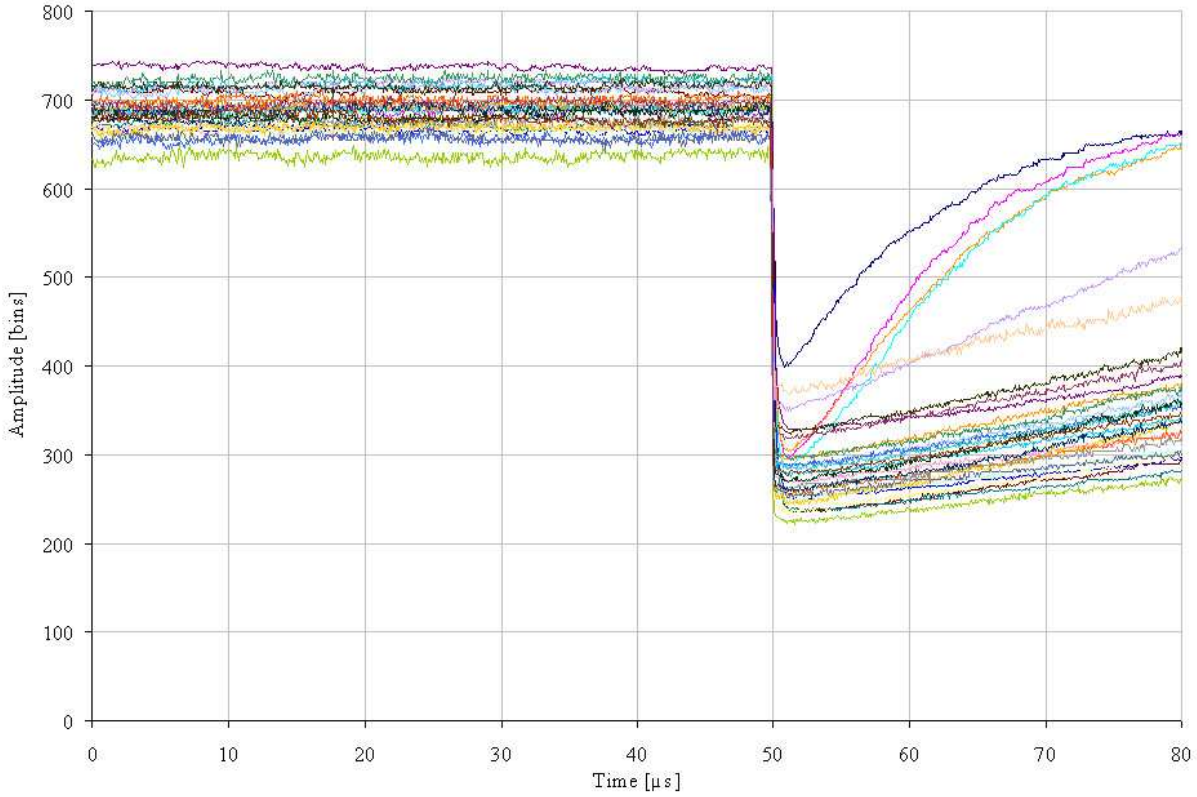

Figure 4.9: Test pulse transient signal. Channels 1 .. 4 (dark blue, red, yellow and light blue curve) are filtered stronger than the other at the low band edge. Hence, their baselines recover faster.

Test pulses ranging from 10 mV to 10 V are applied in order to quantify the nonlinear amplification of the logarithmic amplifier. The offsets of the individual channels are corrected by the determination of a local baseline. Therefore, the first sequence of samples from a recording is taken to calculate the position of the baseline. Amplitudes measured

for calibration are referenced to the actual baseline. Figure 4.10 shows the measured conversion function.

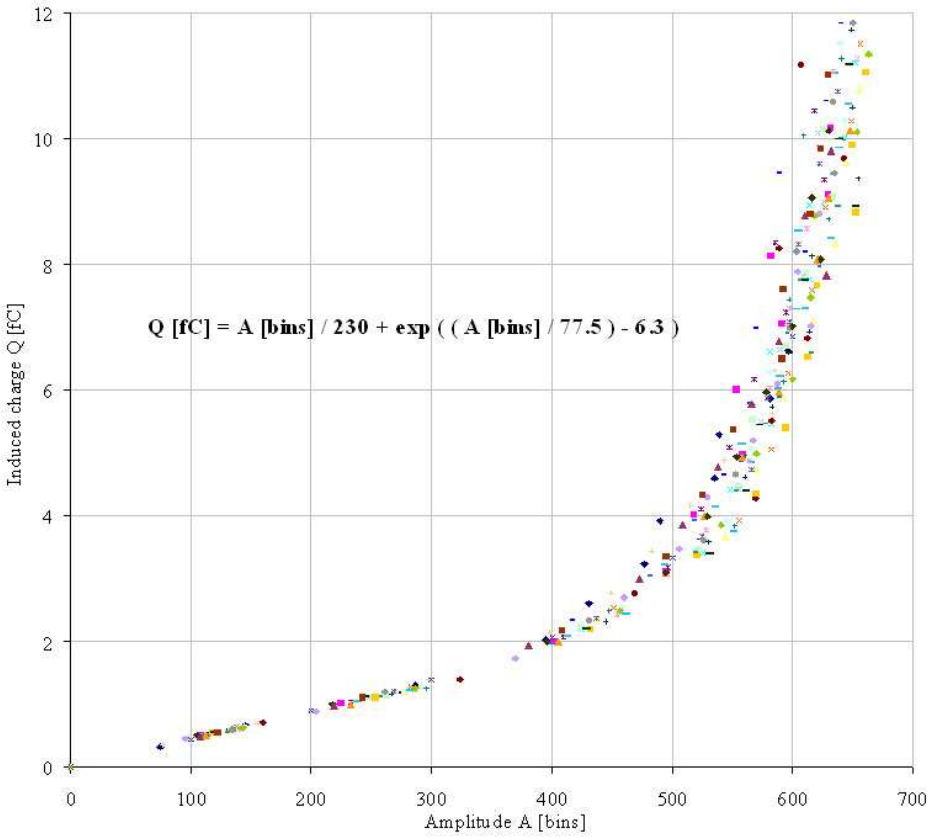

Figure 4.10: Logarithmic amplification. The conversion gain in the linear range is 230 bins/fC.

4.4 Dust Beam Experiments

4.4.1 Dust Accelerator

In order to test the detector under realistic conditions, measurements are performed at the Heidelberg dust accelerator. This facility enables the charging and acceleration of artificial dust particles. Although already designed in 1962, the dust accelerator in Heidelberg is still the leading facility of its kind. It uses a Van-der-Graaf generator in order to produce a high voltage of 2 MV. This voltage accelerates dust particles, which are charged at the tip of an electrode. Figure 4.11 explains the concept of the accelerator. With the particle selection unit (PSU), particles can be selected within a specified charge and speed window.

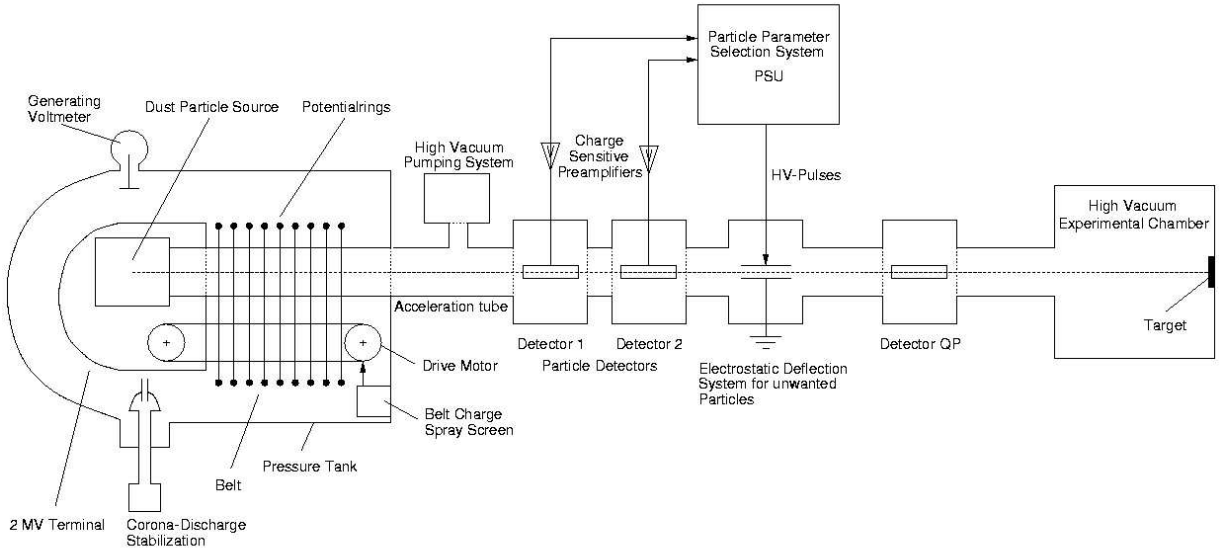

Figure 4.11: Dust accelerator with particle selection unit (PSU) and experimental chamber.

4.4.2 Experimental Setup

One goal of the dust beam measurements is the characterization of the detector signals in dependence of the particle's position. Therefore, a precise dust beam focus is required in order to achieve reproducible trajectories. This is realized with a slit aperture of 0.5 mm width, which can be positioned in the beam center by an electromotor. The optimum position is reached, where the rate of transmitted particles is maximum. Figure 4.12 displays the experimental setup in the vacuum chamber.

The triggering of the readout electronics is done with an impact target, which is mounted behind the exit shielding grid of the detector. Impact signals of dust particles are much stronger than corresponding induced charge signals, since an impact plasma of the dust constituents is produced. A high voltage on the target causes the separation of the positive and negative charges of the impact plasma. A unipolar charge signal is so produced. With a band-pass filter, the signal-to-noise ratio of the target signal can be improved, so even the smallest particles cause clear trigger signals on impact. When a trigger signal is created, the trajectory sensor has already recorded the particle's trace. Thus, the trigger has to stop the recording of the signals immediately, so valid data remains stored in the digital pipeline.

For the variation of the intersection coordinates, the detector can be moved horizontally. A position sensor delivers accurate information of the actual position over a range of 200 mm. The accuracy of the position is better than 0.1 mm, so in conjunction with the collimated beam, reproducible trajectories can be generated.

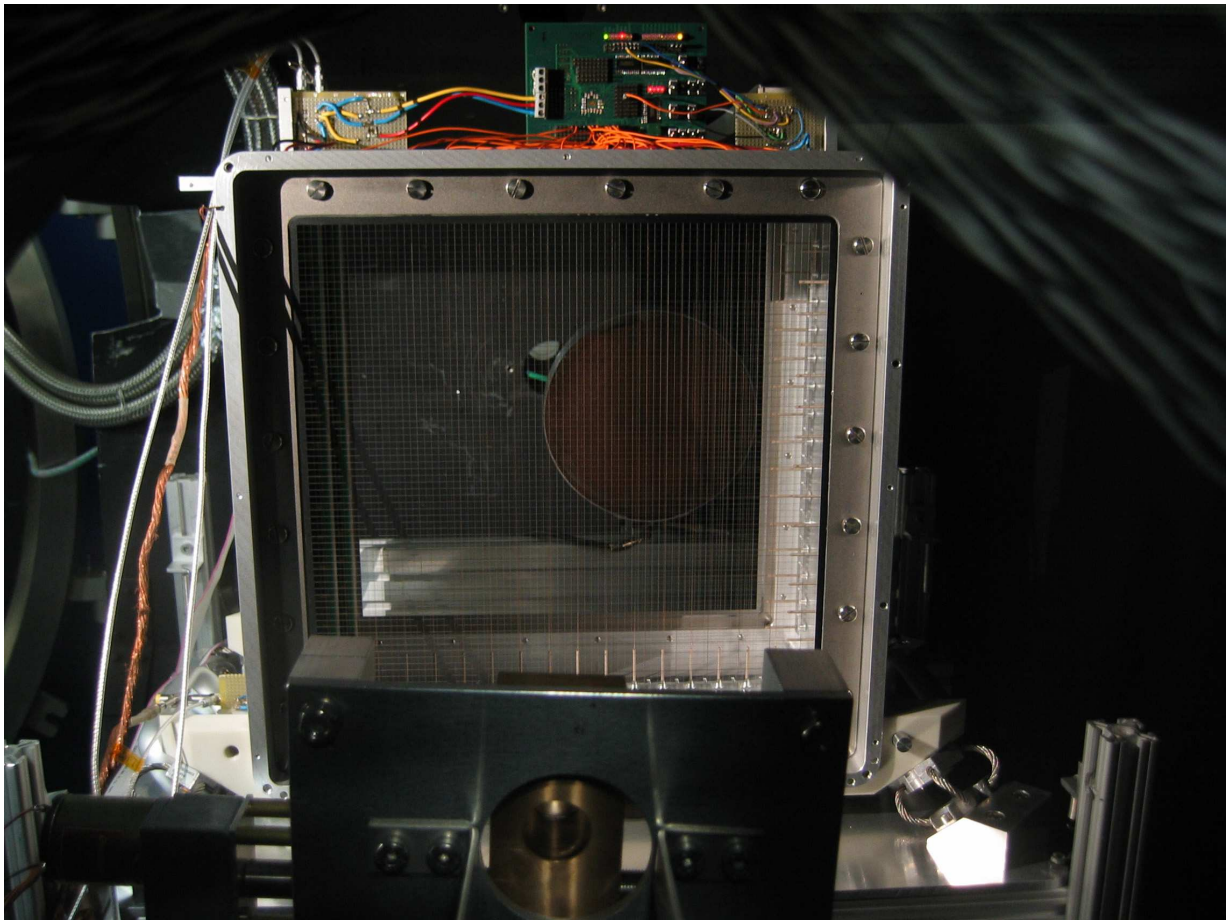

Figure 4.12: Dust accelerator setup. The detector is equipped with 31 microchips (30 front-end amplifiers and one transient recorder). In order to achieve a precise beam focus, the dust beam is sent through a slit aperture (front). The trajectory sensor is triggered by an impact target at the backside of the detector (round copper plate).

4.4.3 Particle Measurements

Figure 4.13 shows typical charge signals of a dust particle. The baselines of the signals are restored after interaction with the particle, since the net charge of an induced signal is zero. Only slight offsets remain due to the lower band limit of the front-end. The detected particle was intersecting the detection planes exactly between two wires. Thus, the distance to the sensor wires was maximum, what represents the worst case for the measurement in terms of sensitivity. According to the theoretical distance function, only 30% of the particle charge is induced on the closest wires.

Before the exact detector position relative to the dust beam can be determined, the position signal has to be calibrated. Since the exact dust beam path can not accurately be measured geometrically, particle impacts on a sensor wire are helpful events to find the

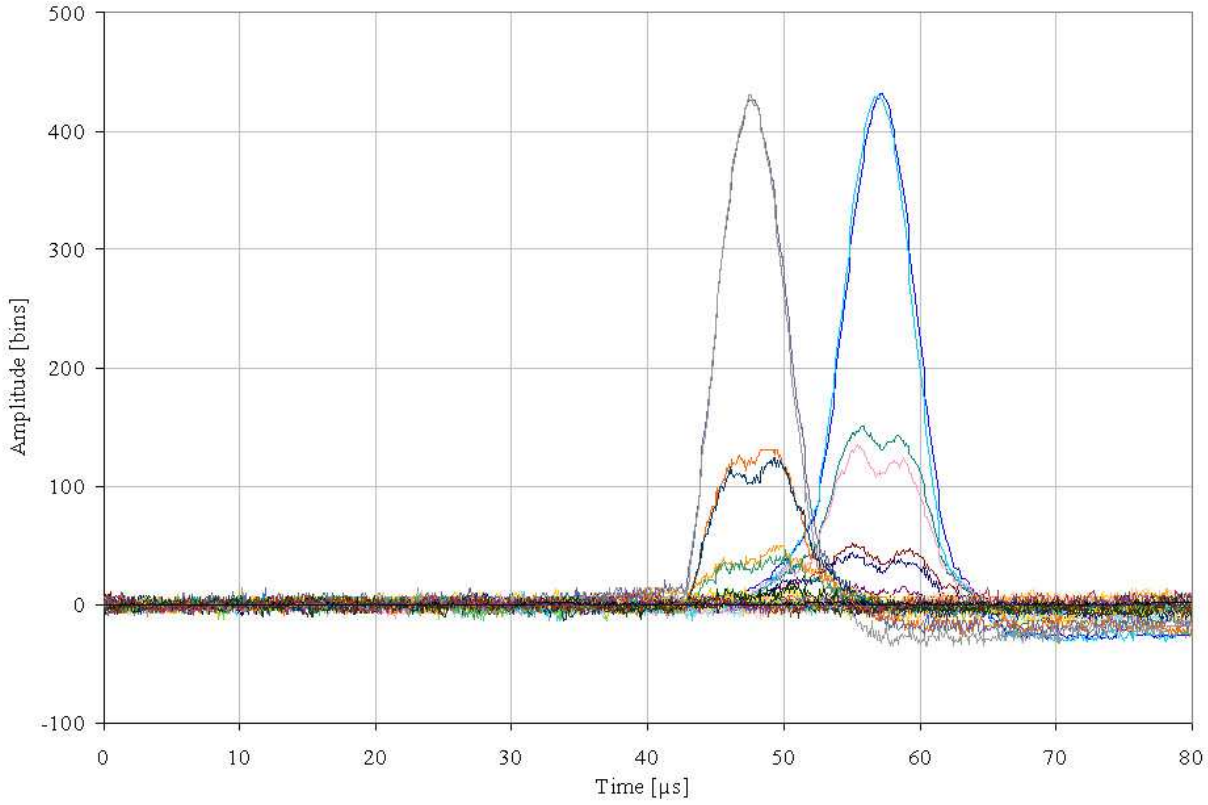

Figure 4.13: Typical charge signals of a dust particle (Q = 2.2 fC, v = 8 km/s).

positions, where sensor wires cross the beam. In case of an impact the corresponding charge signal doesn't recover in the expected time frame, since charge is deposited on the wire. Only via the feedback resistor of the charge sensitive amplifier this charge can be removed, which happens on a much longer time scale. Figure 4.14 shows two of such impact events.

Usually, impact events cannot be readout by triggering with the impact target behind the detector, since these particles are destroyed inside the detector. Thus, when looking for these special events, a trigger from the PSU with appropriate delay was utilized to readout wire impacts. Nevertheless, the first impact displayed in figure 4.14 was unintentionally found during the particle measurements. It was indeed triggered by the impact target on the backside of the detector. An explanation could be, that the particle just touched the wire and transferred its charge, while the matter or at least a fraction of the particle proceeded to the impact target, where it caused a second impact signal.

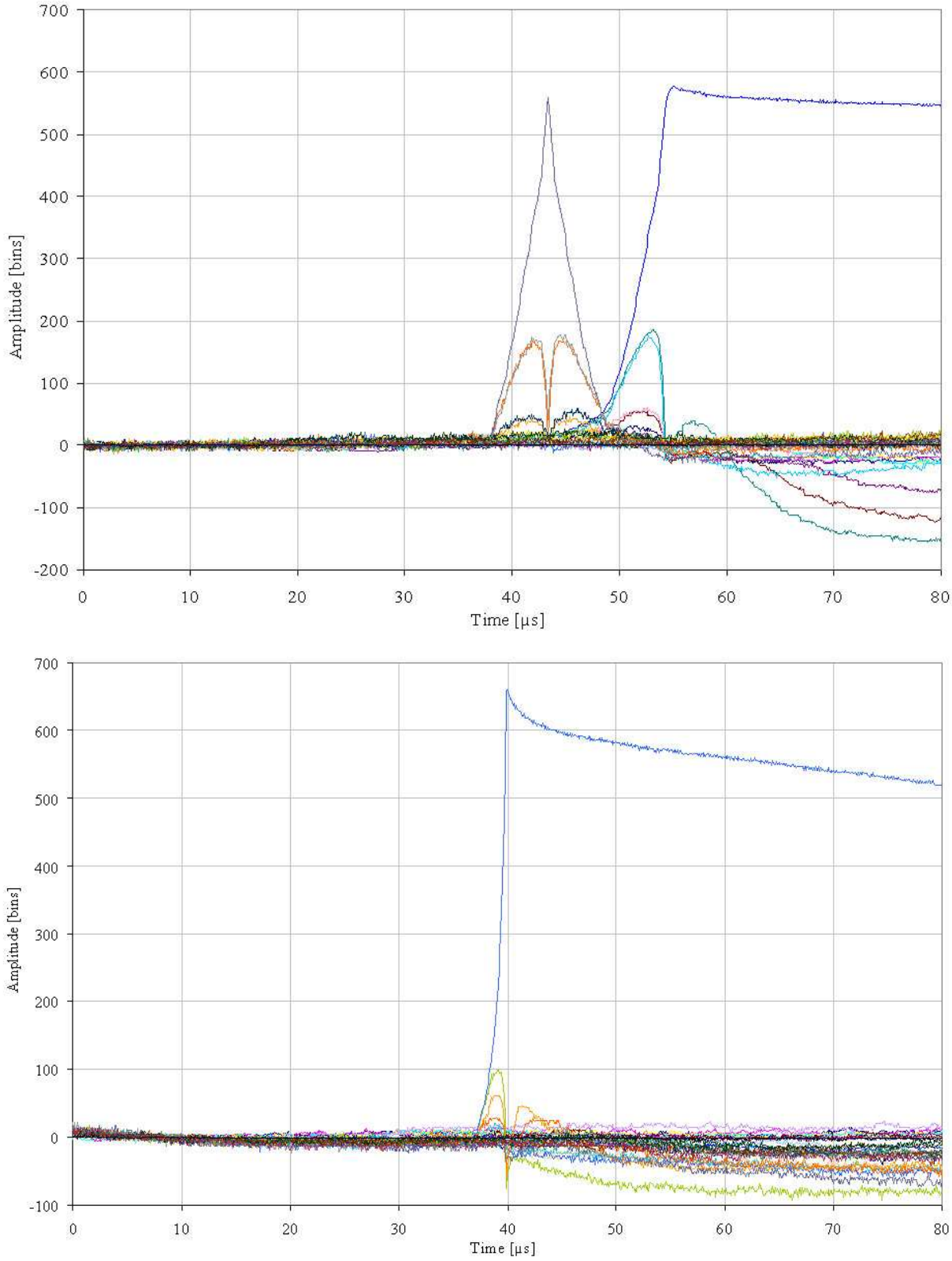

Figure 4.14: Wire Impacts. Top: Impact on second sensor plane. The first plane shows the signal shape typical for trajectories close to a wire. Bottom: Impact on the first plane.

4.5 Data Evaluation

4.5.1 Detector Sensitivity

The total noise of the complete detector system including front-end amplifiers, analog link and ADCs is determined from channels 5 .. 16. These twelve channels are characterized by a full bandwidth setting and nominal S/H units in the ADCs. Figure 4.15 shows the transient signals of the twelve considered channels.

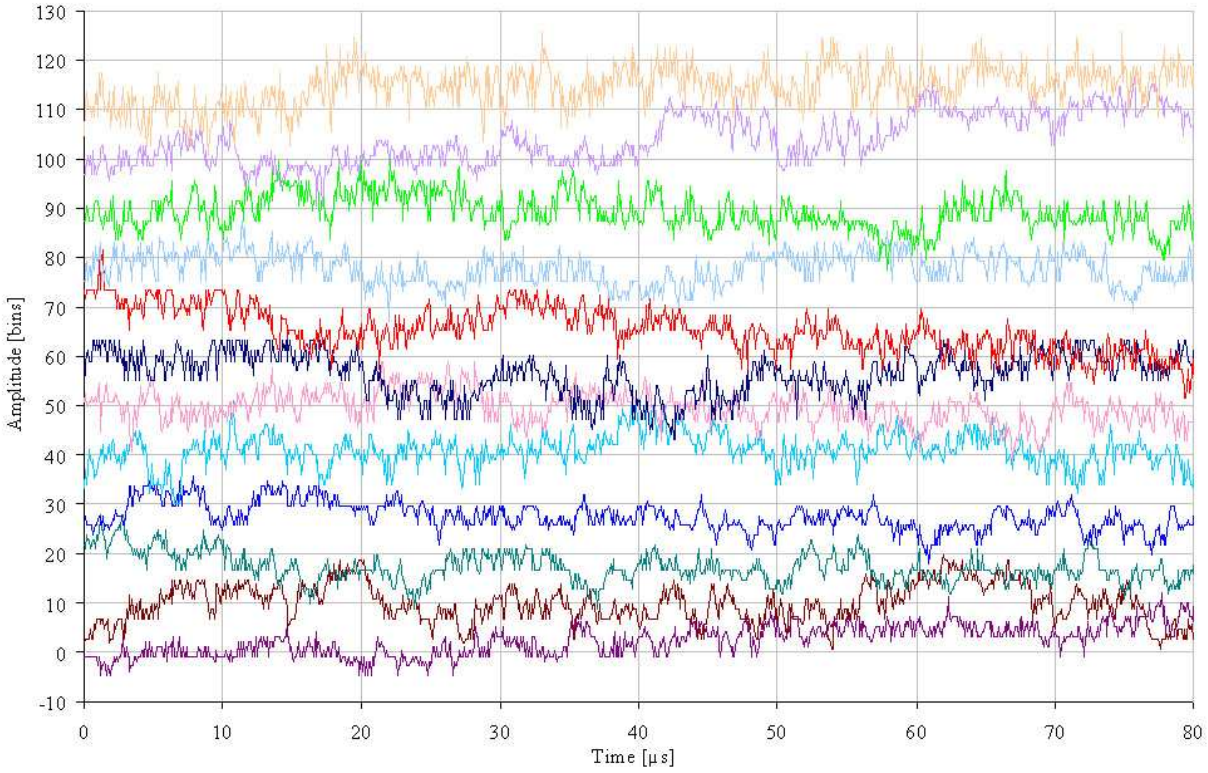

Figure 4.15: Total noise of the DUNE 1.1 readout chain on channels 5 .. 16. The RMS values range from 2.9 LSB to 4.9 LSB. The average RMS value is 3.7 LSB.

The RMS noise determined from these twelve channels is 3.7 LSB. Regarding the conversion gain of 230 bins/fC (compare figure 4.10), this relates to a charge of 1.61×10^{-17} C or 100.5 electrons. Thus, the targeted noise level has exactly been met. Assuming uncorrelated noise of front-end and ADC, the noise contribution of the front-end can be extracted. The effective noise of the ADC was measured to be 2.1 LSB. Since uncorrelated noise sources add quadratically, the front-end noise results in 3 LSB or 83 electrons. This is very close to the simulated value of 65 electrons, what clearly indicates, that the low noise RF transistors used for the front-end are well modeled, including the crucial influence of flicker noise.

To conclude the experimental part of this thesis, the sensitivity of the detector is demonstrated with the smallest particle detected during the measurement campaign. The transient recording of this particle can be found in figure 4.16. The charge of the particle was only 0.9 fC. This grain is also characterized by the largest speed of all particles measured (v = 27 km/s). The baselines of the 30 channels have been spread out in the plot by steps of 10 bins for better visibility.

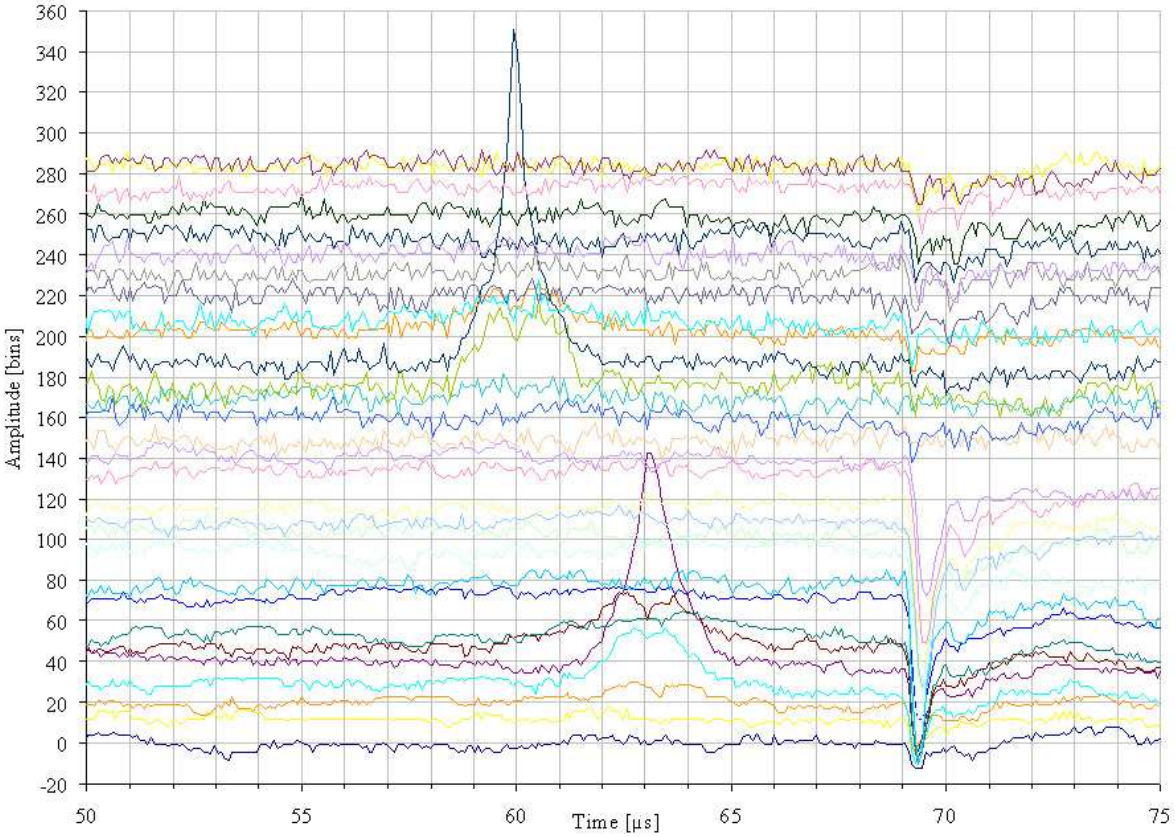

Figure 4.16: Small particle. The speed of this dust grain was 27 km/s, and it carried a charge of only 0.9 fC. The signal-to-noise ratio of the dominant signal is 45. On impact, fast ejectors of opposite polarity were repelled and produced additional signals, mainly on the second sensor plane.

The signal-to-noise ratio of this measurement is 45 on the dominant channel. The project goal was to be sensitive to dust particle charges of 10^{-16} C with a signal-to-noise ratio of 3. Unfortunately, the dust source in the accelerator did not provide such small particles. Nevertheless, the demonstrated example illustrates, that this sensitivity has been achieved with the DUNE 1.1 readout electronics.

4.5.2 Measurement Summary

Property	Value
Front-end conversion gain	404 mV/fC
Front-end noise	1.33×10^{-17} C (83 electrons)
Front-end logarithmic function	Q [fC] = A[bins]/230 + exp ((A[bins]/77.5) - 6.3)
ADC effective noise	2.1 LSB
ADC DNL	- 0.9 LSB / + 1.4 LSB
ADC INL	- 0.3 LSB / + 3 LSB
Total system conversion gain	230 bins/fC
Total system noise	3.7 LSB (100.5 electrons)

Table 4.1: Measurement summary.

Chapter 5

Conclusion and Outlook

5.1 Project Summary

Several innovations have been made in order to create new solutions for precise and sensitive cosmic dust trajectory measurements. Improvements do not only concern the electronics for data processing, but as well the detector geometry. A high sensitivity could be achieved by providing small detector capacitances and optimized low noise amplifiers. Consequently, charge sensitive measurements are performed on multiple electrodes. For the prediction of the signal bandwidth and sensitivity required for dust particle measurements within the desired velocity range, a finite element simulation tool has been used to solve the electric field distribution of a dust particle interacting with the detector. The resulting induced charges on the electrodes were calculated for different particle locations along a specified trajectory. With DUNE 1.0, the prototype ASIC handling the complete data acquisition procedure from pre-amplification of the charge signals to digital readout, the basic functionality of a completely integrated deep sub-micron CMOS implementation could be demonstrated. On the basis of the experience gained from the prototype version, an improved design was developed, consisting of two individual chips: DUNE 1.1FE, a charge sensitive front-end amplifier with logarithmic compression and a noise level of 83 electrons, and DUNE 1.1TR, a 32 channel digital transient recorder. A 10 bit SAR ADC has been designed for this unit with low-power consumption. So, decoupling of the individual channels could be achieved with moderate space requirements for on-chip blocking. A lab model of the trajectory sensor has been equipped with 30 front-end amplifiers on two sensor planes. The pre-amplified signals are processed with one transient recorder chip, and data is sent digitally to a computer. With this setup, measurements of real dust particles could be performed at the Heidelberg dust accelerator facility. The remarkable sensitivity of the detector could so be proven under realistic conditions.

5.2 Future Missions

In order to expose the novel detector to cosmic dust, the DUNE-eXpress mission is under investigation. ConeXpress is a payload adapter of Ariane 5 with solar electric propulsion and is the targeted platform for this mission.

The dust observatory onboard ConeXpress consists of two LAMA instrument modules and four dust trajectory sensor with a total weight of 60 kg. LAMA measures the composition of interstellar dust whereas the trajectory sensor determines the orbital parameters of interstellar and interplanetary grains. DUNE-eXpress shall reach an orbit outside the geostationary orbit to avoid interferences with the Earth debris and magnetosphere environment. A position at the Sun-Earth Lagrange points L1 and L2 or a SMART 1 like orbit are well suited and reachable with ConeXpress [13]. Figure 5.1 visualizes the ConeXpress platform and its location on Ariane 5.

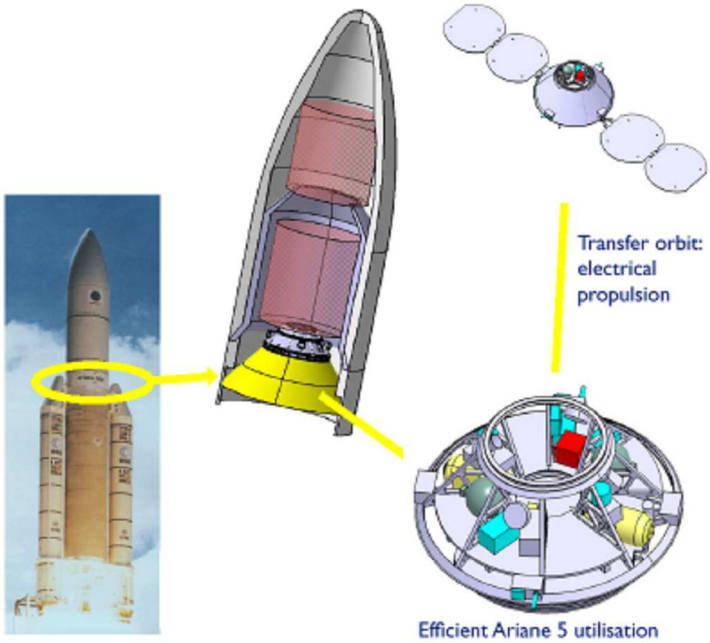

Figure 5.1: ConeXpress platform.

The spacecraft is three axis stabilized and provides a far better pointing accuracy than the 1° required for the measurements. The power demand of the instruments is largely covered by the electrical power provided by the solar arrays, since the electrical propulsion is needed only occasionally for small orbit corrections after the L2 orbit insertion. However, in order to point for a long time into a defined direction, the solar arrays should be articulated towards the Sun in order to ensure a continuous power supply.

The goal of this mission is the in-situ characterization of galactic interstellar dust, in order to provide crucial information not achievable with astronomical methods. Galactic dust constitutes the solid phase of interstellar matter, from which stars and planetary systems form. Information on this fundamental material is extremely sparse. However, following the discovery by the Ulysses spacecraft of micron-sized ISD grains passing through the solar system, the analysis of data sets obtained by different spacecraft (Helios, Galileo, and Cassini) within and beyond the Earth orbit has shown that a significant amount of ISD is within our reach.

Appendix A

DUNE 1.1FE Pad List

Pad	Signal	Type	Description
1	IN	Analog input	Input of charge amp
2	VDDE1	Power input	Positive supply of ESD protection
3	GNDE1	Power input	Negative supply of ESD protection
4	GNDB	Power input	Negative supply of charge amp bias
5	GNDC	Power input	Negative supply of charge amp current source
6	GNDS!	Power input	Substrate ground of charge amp
7	GNDCL	Power input	Clean ground for charge amp decoupling
8	GNDE2	Power input	Negative supply of ESD protection
9	VDDE2	Power input	Positive supply of ESD protection
10	VDDN	Power input	Positive supply of N-well trench
11	VDDE3	Power input	Positive supply of ESD protection
12	GNDE3	Power input	Negative supply of ESD protection
13	GNDBL	Power input	Negative supply of log amp bias
14	GNDCLL	Power input	Clean ground for log amp decoupling
15	GNDS!	Power input	Substrate ground of log amp
16	GNDL1	Power input	Negative supply of 1st stage of log amp
17	GNDL2	Power input	Negative supply of 2nd stage of log amp
18	OUTL	Analog output	Output of log amp
19	OUTC	Analog output	Output of charge amp
20	GNDE4	Power input	Negative supply of ESD protection
21	VDDE4	Power input	Positive supply of ESD protection
22	VDDL	Power input	Positive supply of log amp
23	VBL	Analog I/O	Access to log amp bias for external decoupling
24	INN	Analog input	Inverting input of log amp
25	GNDE5	Power input	Negative supply of ESD protection
26	VDDE5	Power input	Positive supply of ESD protection
27	VDDC	Power input	Positive supply of charge amp

28	VDDC	Power input	Positive supply of charge amp
29	VB	Analog I/O	Access to charge amp bias for external decoupling
30	VFB	Analog input	External bias of charge amp feedback resistance
31	VDDC	Power input	Positive supply of charge amp

Table A.1: DUNE 1.1FE pad list

Appendix B

DUNE 1.1TR Pad List

Pad	Signal	Type	Description
1	VAS	Power input	Negative analog supply
2	VAD	Power input	Positive analog supply
3-9	nc		Not connected
10	VSS	Power input	Negative digital supply
11	nc		
12	VDD	Power input	Positive digital supply
13-17	nc		
18	VSS	Power input	Negative digital supply
19	nc		
20	VDD	Power input	Positive digital supply
21-23	nc		
24	VAS	Power input	Negative analog supply
25	nc		
26	VAD	Power input	Positive analog supply
27-40	nc		
41	VAS	Power input	Negative analog supply
42	nc		
43	VAD	Power input	Positive analog supply
44-72	nc		
73	TestPulse	Analog output	Test pulse output
74	VC3	Analog input	Control voltage of test pulse speed
75	VAS	Power input	Negative analog supply
76	TPS	Digital output	Test pulse stop signal
77	TPRes	Digital input	Test pulse reset
78	TPOscE	Digital input	Test pulse oscillator enable
79	TPCLK	Digital input	Test pulse clock
80	TPTr	Digital input	Test pulse trigger

81-82	nc		
83	VSS	Power input	Negative digital supply
84	VDD	Power input	Positive digital supply
85	ECRes	Digital input	Error checker reset
86	ECEnable	Digital input	Error checker enable
87	Error	Digital output	Error signal indicating memory malfunction
88	ORQ	Digital output	Output register data out (serial readout)
89	ORMMon	Digital output	Output register mode monitor
90	ORCKMon	Digital output	Output register CK monitor
91	MMMon	Digital output	Memory mode monitor
92	MCKMon	Digital output	Memory clock monitor
93	GlobalReset	Digital output	Reset signal issued on completed readout
94	Mon< 9 >	Digital output	Trigger logic address monitor
95	V0IO	Power input	Negative digital I/O supply
96	Mon< 8 >	Digital output	Trigger logic address monitor
97	V3IO	Power input	Positive digital I/O supply
98	Mon< 7 >	Digital output	Trigger logic address monitor
99	Mon< 6 >	Digital output	Trigger logic address monitor
100	Mon< 5 >	Digital output	Trigger logic address monitor
101	VSS	Power input	Negative digital supply
102	Mon< 4 >	Digital output	Trigger logic address monitor
103	VDD	Power input	Positive digital supply
104	Mon< 3 >	Digital output	Trigger logic address monitor
105	Mon< 2 >	Digital output	Trigger logic address monitor
106	Mon< 1 >	Digital output	Trigger logic address monitor
107	Mon< 0 >	Digital output	Trigger logic address monitor
108	DisplayS	Digital input	Switches between 10 MSB and 10 LSB of TL
109	ORMExt	Digital input	External output register mode
110	MMExt	Digital input	External memory mode
111	MCKExt	Digital input	External memory clock
112	TLS	Digital input	Switches between int. and ext. signals
113	V0IO	Power input	Negative digital I/O supply
114	ORCK	Digital input	Output register clock (readout clock)
115	V3IO	Power input	Positive digital I/O supply
116	TLRes	Digital input	Trigger logic reset
117	Tr	Digital input	Trigger signal
118	MnR	Digital input	Memory not reset
119	DIGM	Digital input	Data in generator mode
120	InO	Digital input	DIG input for odd channels
121	InE	Digital input	DIG input for even channels

122	ORADCM	Digital input	ADC output register mode
123	ORADCQ	Digital output	ADC output register data output
124	ORADCCK	Digital input	ADC output register clock
125	CK200	Digital input	External ADC clock
126	CKGM	Digital input	Clock generator mode
127	DCK100	Digital input	Delayed clock input (XORed with CK100)
128	CKGRes	Digital input	Clock generator reset
129	CK100	Digital input	Clock input
130	CK2520	Digital input	External memory clock
131	VSS	Power input	Negative digital supply
132	CK2520S	Digital input	Switches between int. and ext. memory clock
133	VDD	Power input	Positive digital supply
134	CK200S	Digital input	Switches between ext. ADC clock sources
135	CK200VS	Digital input	Switches between int. and ext. ADC clock
136	V0IO	Power input	Negative digital I/O supply
137	OscE	Digital input	Oscillator enable
138	V3IO	Power input	Positive digital I/O supply
139	CK200Mon	Digital output	ADC clock monitor
140	ADCRExt	Digital input	External ADC reset
141	ADCM	Digital input	ADC mode (only for DUNE 1.0 ADCs)
142	CK2520Mon	Digital output	Memory clock monitor
143	ADCRS	Digital input	Switches between int. and ext. ADC reset
144	nc		
145	CK25Master	Digital output	Master clock output
146	VAS	Power input	Negative analog supply
147	VAD	Power input	Positive analog supply
148	VC1	Analog input	On-chip oscillator control voltage
149	VC2	Analog input	ADC pulse-train speed for SEU robust mode
150	RailNeg	Analog input	Controls lower rail of ADC
151	RailPos	Analog input	Controls upper rail of ADC
152	InA< 0 >	Analog input	ADC input
153	InA< 1 >	Analog input	ADC input
154	InA< 2 >	Analog input	ADC input
155	InA< 3 >	Analog input	ADC input
156	InA< 4 >	Analog input	ADC input
157	InA< 5 >	Analog input	ADC input
158	InA< 6 >	Analog input	ADC input
159	InA< 7 >	Analog input	ADC input
160	InA< 8 >	Analog input	ADC input
161	InA< 9 >	Analog input	ADC input

162	InA< 10 >	Analog input	ADC input
163	InA< 11 >	Analog input	ADC input
164	VAS	Power input	Negative analog supply
165	InA< 12 >	Analog input	ADC input
166	VAD	Power input	Positive analog supply
167	InA< 13 >	Analog input	ADC input
168	InA< 14 >	Analog input	ADC input
169	InA< 15 >	Analog input	ADC input
170	InA< 16 >	Analog input	ADC input
171	InA< 17 >	Analog input	ADC input
172	VSS	Power input	Negative digital supply
173	InA< 18 >	Analog input	ADC input
174	VDD	Power input	Positive digital supply
175	InA< 19 >	Analog input	ADC input
176	InA< 20 >	Analog input	ADC input
177	InA< 21 >	Analog input	ADC input
178	VAS	Power input	Negative analog supply
179	InA< 22 >	Analog input	ADC input
180	VAD	Power input	Positive analog supply
181	InA< 23 >	Analog input	ADC input
182-188	nc		
189	InA< 24 >	Analog input	ADC input
190	InA< 25 >	Analog input	ADC input
191	VAS	Power input	Negative analog supply
192	VAD	Power input	Positive analog supply
193	VAS	Power input	Negative analog supply
194	VAD	Power input	Positive analog supply
195	InA< 26 >	Analog input	ADC input
196	InA< 27 >	Analog input	ADC input
197	InA< 28 >	Analog input	ADC input
198	InA< 29 >	Analog input	ADC input
199	InA< 30 >	Analog input	ADC input
200	InA< 31 >	Analog input	ADC input
201-205	nc		
206	VAS	Power input	Negative analog supply
207	nc		
208	VAD	Power input	Positive analog supply

Table B.1: DUNE 1.1TR pad list

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