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Feasibility study to use an SRAM-based FPGA in the readout electronics of the upgraded LHCb Outer Tracker detector

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Abstract:

This thesis presents a study of the feasibility to use SRAM-based FPGAs as central component of the upgraded LHCb Outer Tracker readout electronics. The FPGA should contain the functionality of a TDC and should provide fast data links using multi-GBit/s transceivers. The TDC core that was developed provides 5 bit time measurements for 32 channels with a bin size of 780 ps. The TDC has the required time resolution of better than 1 ns. This was achieved by manually placing every logic element of the TDC channels and with an iterative procedure feeding timing measurements back to the Place&Route step of the router software. A transceiver and TDC card, and an adapter board for the existing readout electronics was developed. Both boards were used successfully to read out drift times from an Outer Tracker straw-tube module in a cosmic setup. To qualify the proposed electronics for the expected radiation levels an irradiation test with 22 MeV protons and two FPGA boards was performed up to a total ionization dose of 30 Mrad. Both chips sustained the irradiation expected for the full life time of the upgraded LHCb detector of up to 30 krad. After an irradiation dose of 150 krad the first deteriorations of the performance of the chips were observed. The proton cross section for configuration bit flips was determined to be $1.6 \cdot 10^{-16}$ cm^2 per bit. The measured error rate scaled to the upgrade environment would correspond to a manageable firmware error rate.

Kurzfassung:

In der vorliegenden Arbeit wird eine Machbarkeitsstudie zur Nutzung SRAM basierter FPGAs als zentrales Element für die Ausleseelektronik des LHCb Outer Tracker Detektors vorgestellt. Der FPGA soll als TDC und schneller Datenlink mit Multi-GBit/s Transceivern genutzt werden. Ein FPGA basierter 32 Kanal TDC mit 5 Bit Zeitinformation bei einer Bingröße von 780 ps wurde entwickelt. Der TDC hat die erforderliche Zeitauflösung von besser als 1 ns. Dies wurde durch manuelle Plazierung der Logikelemente des TDCs auf dem FPGA, sowie durch eine iterative Prozedur erzielt, bei der Zeitmessungen auf die Verschaltung der Logikzellen rückwirken. Die Zeitauflösung wurde mit Messungen für jeden TDC Kanal individuel optimiert. Ein TDC und GBit/s Transceiver Board sowie ein Adapter Board für die vorhandene Ausleseelektronik wurde entwickelt. Beide Boards wurden erfolgreich beim Auslesen von Driftzeiten eines Outer Tracker Moduls mit kosmischen Myonen getestet. Ein Bestrahlungstest mit 22 MeV Protonen wurde durchgeführt, bei dem 2 FPGAs mit bis zu 30 Mrad ionisierender Strahlungsdosis bestrahlt wurden. Beide Chips überstanden die für das LHCb-Upgrade erwartete Strahlungsdosis von 30 krad. Erste Verschlechterungen der Chips wurden nach einer Strahlungsdosis von 150 krad beobachtet. Der Wirkungsquerschnitt für durch Protonen induzierte Fehler der FPGA Konfiguration wurde zu $1.6 \cdot 10^{-16}$ cm^2 pro Bit bestimmt. Die gemessene Fehlerrate zum erwarteten Strahlungsumfeld skaliert scheint den Einsatz des FPGAs möglich zu machen.

Contents

CHAPTER 1

Introduction

The idea that every object in the universe is built from indivisible particles is old. Already, the Greek philosopher Democritus claimed 24 centuries ago that the natural world consists of indivisible atoms and empty void. Every object is built from these atoms which only differ in intrinsic properties like size and shape [1].

This fundamental concept for the buildup of the universe is not far from our current understanding in particle physics. In the last hundred years many fundamental particles have been found which build up the universe. Every discovery provided a deeper understanding of the microcosm than before. The current status is that matter is build from quarks and leptons. The fundamental interactions between these particles are described by the Standard Model (SM) of particle physics. It is important to note that this theory was confirmed by many experiments during the last 40 years to very high accuracy.

Although the Standard Model of particle physics is a very successful theory, some questions remain open. For example:

- In the Big Bang equal amounts of matter and antimatter were produced. Nevertheless, observations today show a matter dominated universe. The origin of this baryon asymmetry of the universe is not completely understood.

- Astronomical observations confirm the existence of Dark Matter for which the SM provides no candidate. Furthermore, the Dark Matter and the

matter described by the SM make up only ∼27 % of the energy density of the universe. The remaining part of is called Dark Energy and not explicable with the SM, either.

Possible explanations of both phenomena must be theories beyond the SM which, at lower energies that we have probed, are approximated by the Standard Model. These theories are also referred to as New Physics.

Beside the search for the Higgs particle and the Quark gluon plasma the Large Hadron Collider (LHC) at CERN in Geneva has been built to search for signs of New Physics. The LHC uses proton-proton collisions with center-of-mass energies of up to $\sqrt{s} = 14\,\text{TeV}$, which is currently the highest energy for particle accelerators. Two approaches are taken to search for New Physics. In the *direct approach* experiments look for new heavy particles which are directly produced in the collision. The ATLAS and CMS experiments are following this approach. The other possibility is to measure precisely the effects of quantum loop corrections in which new particles can be present and lead to a modification of related observables. This method is sensitive to particles masses 10 × higher than the *direct approach*. The LHCb experiment uses the second approach to search for signs of new heavy particles.

The LHCb experiment exploits the enormous production rates of beauty and charmed hadrons at the LHC. Precision measurements of CP asymmetries and rare decays are performed to investigate potential effects of physics beyond the Standard Model. The recent LHCb results underline the potential of flavor physics at the LHC. Furthermore, the detector shows an excellent performance.

In order to perform studies of rare decays with even higher precision the LHCb collaboration is planning to upgrade the detector in 2018 to a 40 MHz readout with a more flexible software-based triggering system that will increase the data rate as well as the efficiency of selecting B decays with hadronic final states. It is foreseen to run the detector at instantaneous luminosities of up to $2\times10^{33}\text{cm}^{-2}\text{s}^{-1}$ and to collect $>50\,\text{fb}^{-1}$ of data.

To increase the readout rate by a factor 36 to 40 MHz, the readout electronics of the sub-detectors must be modified. In the past, radiation hard custom made ASICs[1] were the only possibility to construct a high performance readout. Especially for projects which need only a small number of readout chips, the development of ASICs is time consuming and expensive. Currently, there are high performance FPGAs[2] available which have a large number of logic elements and multi-GBit/s transceivers. These chips open new technical possibilities for the readout of sub-detectors in regions with low radiation levels. The advantage of using FPGAs in the readout electronics is a higher flexibility and smaller cost than using ASICs.

[1] Application Specific Integrated Circuit
[2] Field Programmable Gate Array

This thesis presents a feasibility study to use SRAM-based FPGAs as central component in the readout electronics for the LHCb Outer Tracker detector in the LHCb upgrade. The FPGA would be used as a TDC and provide fast data links using multi-GBit/s transceivers. The TDC needs to have a time resolution smaller than 1 ns and should have 32 channels. Furthermore, the FPGA has to sustain a total ionization dose of 30 krad and the rate of radiation induced configuration register flips has to be low. Both effects were tested during an irradiation campaign with 22 MeV protons.

First, an FPGA-based TDC was developed on an Arria GX FPGA with 32 channels and a time resolution below 1 ns. Afterwards, the Arria GX FPGA with the TDC functionality and multi-GBit/s transceivers has been integrated in a newly developed PCB[3]. This board is already a prototype for the upgraded Outer Tracker readout electronics and is pin compatible to the existing readout electronics. The FPGA test board was tested with a second developed connector board in a cosmic setup to measure the LHCb Outer Tracker drift time spectrum. Furthermore, the Arria GX test board was used for an irradiation test with 22 MeV protons at the Max Planck Institute for Nuclear Physics in Heidelberg. For the dosimetry and careful assessment of the radiation induced deteriorations of the FPGAs under test, the beam profile was measured.

The thesis is laid out as follows: Chapter 2 provides an introduction to the theoretical background for the LHCb physics program, beginning with a short review of the Standard Model and presenting some measurements relevant for the LHCb upgrade. Chapter 3 describes the current LHCb detector with special focus on the Outer Tracker. The plans for the LHCb upgrade are shown in Chapter 4. Chapter 5 presents the realization of an FPGA-based TDC and Chapter 6 shows the measurement of the LHCb Outer Tracker drift time spectrum in a cosmic setup. The proton irradiation test of the Arrix GX FPGA is described in Chapter 7 and Chapter 8 summaries the thesis.

[3]Printed circuit board

CHAPTER 2

Theoretical background

The beginning of this chapter shows a short introduction of the Standard Model of particle physics. Afterwards, the CKM matrix and the Unitarity Triangles are described. At the end, the physics motivation of the LHCb upgrade is given by showing two analyses from the LHCb upgrade program.

2.1 The Standard Model of particle physics

The Standard Model of particle physics (SM) is a successful theory for three of the four fundamental forces in the universe [3, 4, 5]. It describes the electromagnetic interaction, the weak interaction and the strong interaction in the framework of quantum field theory. The electromagnetic force is responsible for the interaction between electrically charged particles. The weak force acts between particles carrying weak charge and is seen for example in the β-decay of the neutron. The strong force appears between particles with color-charge and is responsible for the bindings of hadrons. The fourth force, gravity, is not described by the SM.

The interaction between particles is described via the exchange of gauge-bosons which have spin 1. Table 2.1) shows the mass and relative strength of these bosons. The electromagnetic force is mediated by the photon and has unlimited range. The weak force uses the heavy $W^{\pm}$ and Z^0 bosons, and has only a very short range ($\sim$ fm). Also, the strong force which is described within Quantum Chromo Dynamics (QCD), has effectively a short range of roughly one nucleon (1 fm). A big difference between the interactions is the self-coupling of

Interaction	Boson	Mass	Relative strength
strong	gluons	0	1
electromagnetic	photon	0	10^{-2}
weak	$W^{\pm}$	$\sim$80 GeV/c^2	10^{-13}
	Z^0	$\sim$91 GeV/c^2	

Table 2.1: The three forces described by the Standard Model and their corresponding gauge-bosons. The mass values are taken from [6].

	Quarks			Leptons		
Generation	Type	Charge [e]	Mass	Type	Charge [e]	Mass
I	u	$+\frac{2}{3}$	1.5 - 3.3 MeV/c^2	ν_e	0	$\leq$ 2 eV/c^2
	d	$-\frac{1}{3}$	3.5 - 6.0 MeV/c^2	e	-1	511.0 keV/c^2
II	c	$+\frac{2}{3}$	$\sim$ 1.27 GeV/c^2	ν_μ	0	$\leq$ 2 eV/c^2
	s	$-\frac{1}{3}$	$\sim$ 104 MeV/c^2	μ	-1	105.7 MeV/c^2
III	t	$+\frac{2}{3}$	$\sim$ 171.2 GeV/c^2	ν_τ	0	$\leq$ 2 eV/c^2
	b	$-\frac{1}{3}$	$\sim$ 4.2 GeV/c^2	τ	-1	1.78 GeV/c^2

Table 2.2: The fermions in the Standard Model consist of quarks and leptons grouped in three generations. To each particle in this table an antiparticle exists with the same mass but opposite charge. The mass values are taken from [6].

the bosons for the weak and strong force, which is a result of a non-Abelian gauge theory. The neutral photon can not couple to itself, but the $W^{\pm}$ and Z^0 bosons and the gluons create self-coupling vertices.

The building blocks of matter are quarks and leptons which are spin $\frac{1}{2}$ fermions. Leptons and quarks are grouped into three families with same features but different mass which are shown in Table 2.2. The leptons react via the electromagnetic and weak forces the quarks react in addition via the strong force. The origin of the three generations has not been understood yet. In the first generation are the lightest and therefore stable elementary particles which are the main constituents of the matter of the universe. In the SM there exists to each particle an antiparticle with the same mass and lifetime but opposite charge, which is a consequence of CPT invariance, a fundamental property of Lorentz invariant quantum field theories.

Explicit mass terms in the Lagrangian to describe the massive bosons ($W^{\pm}$, Z^0) would violate gauge invariance. This conflict is solved by the mechanism of spontaneous symmetry breaking of the $\mathrm{SU}(2)_L \otimes \mathrm{U}(1)_Y$ electroweak symmetry (Higgs-mechanism). The heavy gauge bosons aquire mass via the coupling to the Higgs field. The fermion masses are introduced by explicit Yukawa couplings to the Higgs. The masses of the $W^{\pm}$ and Z^0 bosons are given by the coupling

constants of the theory, the masses of the fermions in the Yukava sector are not given directly from the theory, but are parameters of the theory.

The Higgs-mechanism predicts one observable massive spin 0 particle, which is called Higgs-boson. One of the main motivations for the Large Hardon Collider at CERN was the search for this particle. Results from CMS and ATLAS showed the observation of a particle consistent with the Higgs-boson in July 2012 which is a big success of particle physics [7, 8].

2.2 CKM matrix

For quarks the mass and weak eigenstates are not the same, the Cabibbo-Kobayashi-Maskawa (CKM) matrix was introduced to change the mass base to the weak base [9]. The Cabibbo-Kobayashi-Maskawa matrix is a unitary 3×3 matrix ($\mathrm{U}^\dagger \cdot \mathrm{U} = \mathrm{U} \cdot \mathrm{U}^\dagger = \mathbb{1}$), which rotates the mass-eigenstates of the down-type quarks $(d, s, b)^T$ into the weak-eigenstates $(d', s', b')^T$.

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = V_{CKM} \cdot \begin{pmatrix} d \\ s \\ b \end{pmatrix} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{td} \end{pmatrix} \cdot \begin{pmatrix} d \\ s \\ b \end{pmatrix} \tag{2.1}$$

The weak eigenstates q' are a linear combination of the mass eigenstates q. The CKM matrix elements V_{ij} describe the relative transition probability ($\sim |V_{ij}|^2$) of an up-type quark q_i into a down-type quark q_j or vice versa. The complex matrix has in principle 18 parameters from which 9 parameters are fixed due to the unitarity condition of the CKM matrix, 5 more parameters describe unobservable relative quark phases and can be rotated away. The remaining four parameters can be chosen as three quark mixing angels and one complex phase which is the source of CP-violation in the Standard Model.

One very common parametrization of the CKM matrix is the Wolfenstein parametrization with λ, A, ρ and η [10]. The size of each matrix element is given in the expansion of the parameter λ=sin$\theta_c \approx 0.22$ where θ_c is the Cabibbo angle:

$$V_{CKM} = \begin{pmatrix} 1 - \frac{\lambda^2}{2} & \lambda & A\lambda^3(\rho - i\eta) \\ -\lambda & 1 - \frac{\lambda^2}{2} & A\lambda^2 \\ A\lambda^3(1 - \rho - i\eta) & -A\lambda^2 & 1 \end{pmatrix} + (\lambda^4) \tag{2.2}$$

Quark transitions are most common within a generation, what can be seen in the diagonal entries of the CKM matrix, which are approximately equal to one. The transition from the first to the second generation are still likely ($\propto \lambda^2$), and transitions from the second and the third generation are more unlikely ($\propto \lambda^4$). The most unlikely transitions are between the first and the third generation ($\propto \lambda^6$).

Due to the unitarity relations it is possible to construct 6 relations of the form:

$$V_{ud}V_{ub}^* + V_{cd}V_{cb}^* + V_{td}V_{tb}^* = 0. \tag{2.3}$$

It is possible to draw the Equation 2.3 as triangles in the complex plane. The corresponding unitarity triangle is shown in Figure 2.1 normalized to $V_{cd}V_{cb}^*$. The area of these triangles represent the size of the CP-violation in the SM. The

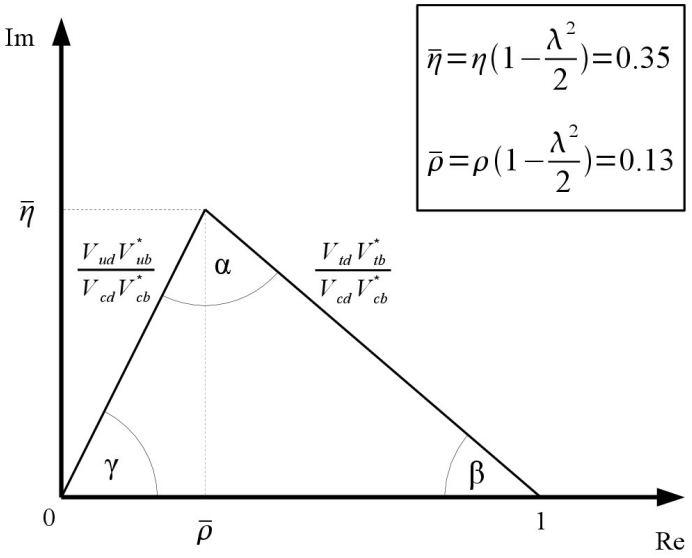


Figure 2.1: Unitarity triangle, corresponding to Equation 2.3.

triangle parameters can be determined by measuring the different CKM matrix elements with several different physics processes. Figure 2.2 shows the current experimental status of the unitarity triangle corresponding to Equation 2.3. The results are in agreement with the Standard Model prediction. The upgrade of the LHCb detector will reduce the error of the angle γ to the degree-level. The theoretical errors for the two angles are negligible [2]. If a discrepancy to the unitarity prediction of the SM is observed this would be a sign of physics beyond the description of the SM (New Physics).

2.3 Physics with the upgraded LHCb detector

The physics program for the upgraded LHCb detector can be divided into two equally important categories [12] like for the current physics program. Firstly, the "Exploration" category. These are studies which are very sensitive to new phenomena beyond the Standard Model and have not been accessible at previous experiments. Secondly, the "Precision Studies" which are done with known decay

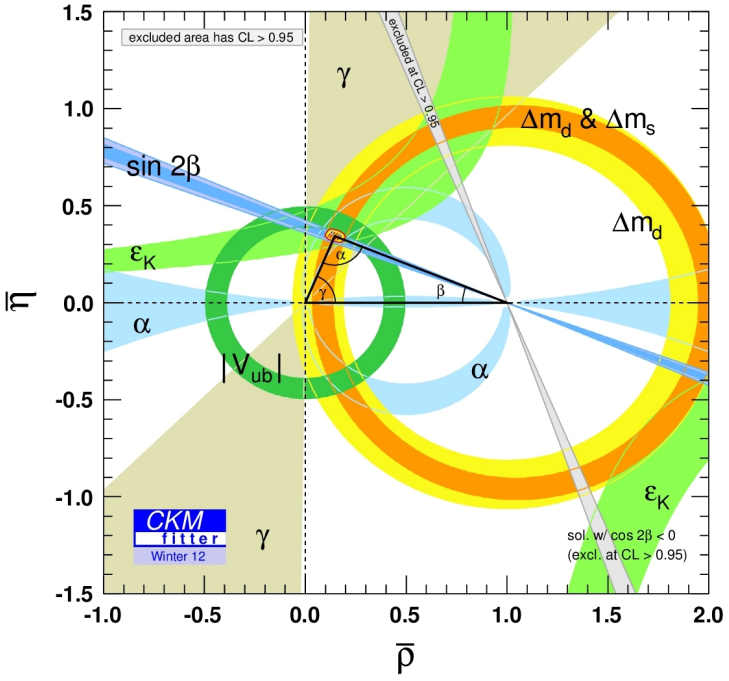


Figure 2.2: Current experimental status of the unitarity triangle corresponding to Equation 2.3. The figure was taken from [11].

modes or observables with improved sensitivity. These are compared with precise theory predictions.

In the following two analyses from the broad LHCb upgrade physics program are discussed as representative examples for the 2 categories.

2.3.1 CP-violation in the B_s^0-system

The weak eigenstates B_s^0 and $\bar{B}_s^0$ are a mixture of the mass eigenstates B_H and B_L[1]. Neutral B-mesons can oscillate into their anti-mesons in the Standard Model by box-diagrams. Figure 2.3 shows the two contributing Feynman diagrams in the Standard Model. The dominating contribution comes from the top quark in the loop.

The time evolution of B_s^0-mesons with oscillation and decay can be described by the phenomenological Schroedinger equation

$$i\frac{d}{dt}\begin{pmatrix} B_s^0 \\ \bar{B}_s^0 \end{pmatrix} = \left(\mathbf{M} - i\frac{\mathbf{\Gamma}}{2}\right)\begin{pmatrix} B_s^0 \\ \bar{B}_s^0 \end{pmatrix}. \tag{2.4}$$

The mass matrix $\mathbf{M}$ and the decay width matrix $\mathbf{\Gamma}$ are 2×2 hermitian matrices. Their diagonal elements are identical due to the CPT invariance theorem. $\mathbf{M}$ is

[1]H: heavy and L: light

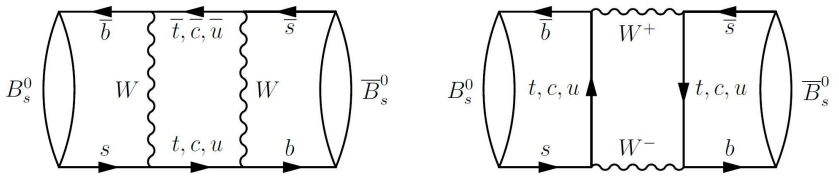


Figure 2.3: Feynman diagrams for B_s^0 meson oscillation. The figure is taken from [15]

non-diagonal so the flavor eigenstates are not equal to the mass eigenstates. To get the mass eigenstates for t = 0 the matrix $(\mathbf{M} - i\frac{\mathbf{\Gamma}}{2})$ is diagonalized:

$$|B_L\rangle = p\left|B_s^0\right\rangle + q\left|\bar{B}_s^0\right\rangle, \tag{2.5}$$
$$|B_H\rangle = p\left|B_s^0\right\rangle - q\left|\bar{B}_s^0\right\rangle, \tag{2.6}$$

where $|p|^2 + |q|^2 = 1$. The following parameters are introduced to describe the mixing:

$$\begin{aligned} \Delta m_s &= m_H - m_L = 2\,|M_{12}|\,, \\ \Delta\Gamma_s &= \Gamma_L - \Gamma_H, \\ \phi_M &= arg(M_{12}). \end{aligned} \tag{2.7}$$

The mass difference Δm_s is the oscillation frequency of the mixing process, $\Delta\Gamma_s$ is the decay width difference between light and heavy and ϕ_M is the mixing phase.

The $B_s^0 - \bar{B}_s^0$ oscillation frequency Δm_s has been measured by the LHCb experiment to be Δm_s=$(17.768 \pm 0.024)\text{ps}^{-1}$ [13].

Furthermore, for the decays in which both B_s^0 and $\bar{B}_s^0$ can decay into the same CP final state, the direct decay and the decay following the mixing can interfere with each other. This allows to measure the phase difference of the two decay paths a depicted in Figure 2.4. The phase difference $\phi_S = \phi_M - 2\phi_D$, where the phase ϕ_D is the decay phase and is approximately zero, can be determined through the measurement of the time-dependent CP asymmetry. The "golden decay mode" to perform this measurement is the decay

$$B_s^0(\bar{B}_s^0) \to J/\psi(\mu^+\mu^-)\phi(K^+K^-).$$

A 4-dimensional fit to the decay angles and the decay time allows to measure $\Delta\Gamma_s$ and the CP-violating phase ϕ_s in a simultaneous fit. For the phase ϕ_s, the SM predicts a very small value (-0.0364±0.0016) rad [14] with very small uncertainty. The measurement is therefore very sensitive to possible contributions from New Physics. The LHCb experiment has already performed a measurement of ϕ_s and the result is consistent with the small value predicted by the SM, however the result include still a relatively large statistical error

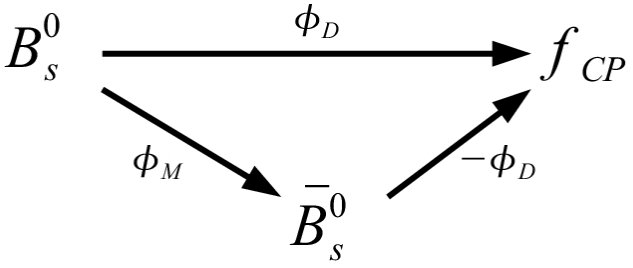


Figure 2.4: Illustration of the interfering amplitudes contributing to CP violation in interference of decay and mixing.

(ϕ_s=0.07 ± 0.09(stat) ± 0.01(syst) rad [15]). To measure a small deviation from the SM prediction much higher statistics are needed. The 50 fb^{-1} of data collected during the LHCb upgrade would reduce the statistical uncertainty for ϕ_s from 0.09 rad [15] now to 0.009 rad after the LHC run 4 [2].

2.3.2 The rare decay $B_s^0 \rightarrow \mu^+\mu^-$

$B_s \rightarrow \mu^+\mu^-$ is an effective channel to search for phenomenon beyond the Standard Model which predicts a branching ratio of $(3.23 \pm 0.72)\cdot 10^{-9}$ [16].

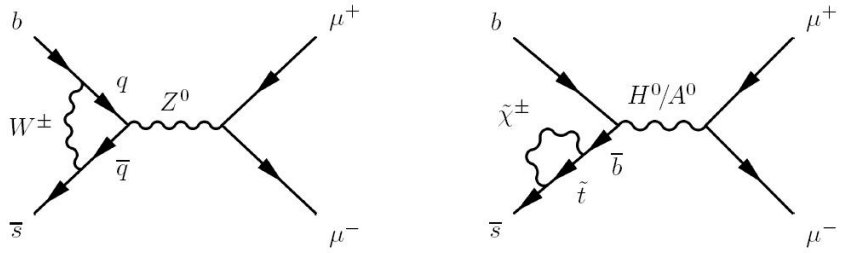


Figure 2.5: Examples for Feynman diagrams for $B_s^0 \rightarrow \mu^+\mu^-$ in the SM (left) and in the MSSM (right). The figure is taken from [17]

Figure 2.5 shows examples for Feynman diagrams contributing to the decay. The branching ratio increases for the MSSM[2] with the sixth power of tanβ which is the ratio of the vacuum expectation values of the Higgs bosons [18]. The recent observations of this decay by LHCb [19, 20] and CMS [21] rule out new contributions of comparable size to the SM. Since the theoretical prediction of the branching ratio has a small error of $0.3\cdot 10^{-9}$ and the uncertainty of the measurement would decrease to $0.19\cdot 10^{-9}$ with a data set of 50 fb^{-1} [2], the LHCb upgrade is important for this study.

[2]Minimal Supersymmetric Standard Model

Furthermore, the very rare decay $B_d^0 \rightarrow \mu^+\mu^-$ will also be accessible with the upgraded LHCb detector ("Exploration" category). The Standard Model prediction for the branching ratio is $(1.07 \pm 0.10)\cdot 10^{-10}$ [16]. In addition, the ratio of the two branching ratios of B_s^0 and B_d^0 is given by the CKM matrix elements which makes a measurement of both branching ratios to an interesting test of the Standard Model and of minimal flavor violating new physics models.

CHAPTER 3

LHCb detector

The LHCb experiment is one of four big experiments at the Large Hadron Collider (LHC) at CERN[1] in Geneva. This chapter begins with an introduction of the Large Hadron Collider at CERN in Geneva. Followed by the different LHCb sub-systems which are briefly described. Next the Outer Tracker is described in detail, and its different readout boards are shown.

3.1 Large Hadron Collider

The LHC consists of two 27 km long accelerator rings which accelerate protons in opposite directions up to an energy of 7 TeV with collisions in four experimental positions. The LHC was built in the existing LEP tunnel. A schematic of the LHC can be seen in Figure 3.1. Beside the proton-proton physics there is also a heavy ion physics program at the LHC. Lead-lead or lead-proton are brought into collision in special runs. The LHC design energy is $\sqrt{s} = 14\,\text{TeV}$ with a design luminosity of $\mathcal{L} = 10^{34}\,\text{cm}^{-2}\text{s}^{-1}$. The proton beam is separated into 2808 bunches with a bunch spacing of 25 ns. Each bunch contains $\sim 10^{11}$ protons. Superconducting magnets with a field of 8.3 T are used to force the protons on a circular orbit.

At the LHC there are four large experiments placed: ATLAS, ALICE, CMS and LHCb. ATLAS and CMS are 4π multi-purpose detectors, ALICE is special-

[1] Conseil Européen pour la Recherche Nucléair.

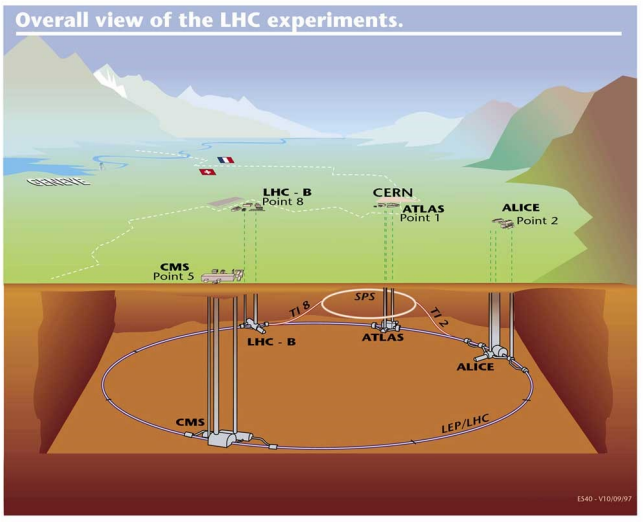


Figure 3.1: LHC tunnel with the four experiments ATLAS, ALICE, CMS and LHCb [22].

ized for heavy ion collisions and the LHCb experiment investigates rare heavy-flavor meson decays to test the quark flavor sector of the Standard Model. CP-violation, which is small in the Standard Model, is a well suited observable for New Physics searches.

3.1.1 Proton-proton interaction rate

The proton-proton interaction rate R at the LHC can be calculated from the LHC luminosity $\mathcal{L}$ at the experiment and the proton-proton cross section σ

$$R = \mathcal{L} \cdot \sigma. \tag{3.1}$$

The design luminosity of the LHCb detector is $4{\times}10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and the proton proton cross section at 7 TeV is 98.3 mb, from which the detector "sees" only the inelastic collisions (73.5 mb), reaction products of the elastic and single diffractive events stay inside clode to the beam axis and outside the rapidity covery of $\eta \leq 4.9$. This results in an average event rate of 24 MHz for the original detector design. For the LHCb upgrade in 2018, it is foreseen to increase the luminosity to $2{\times}10^{33}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, which would result in a 5 times higher event rate.

The collision rate is important to estimate the radiation environment of the detector components.

3.2 LHCb sub-systems

The LHCb experiment exploits the production of $b-$ and $c-$hadrons at the LHC and is dedicated to the study of rare B and D mesons decays. The b-quarks are

predominantly produced in inelastic proton-proton collisions in pairs of quark and anti-quark ($b\bar{b}$). The dominant processes for the $b\bar{b}$ production are gluon fusion and quark fusion. The mass of the $b\bar{b}$ pair is small enough that they can be produced by partons with a quite different momentum. The result is a boost of the quark pair forward or in backward direction relative to the beam line. So LHCb has been built as a single-arm forward spectrometer to maximize detection efficiency and minimize costs.

3.2.1 Detector design

The LHCb detector consists of several sub-components, which can be grouped into a vertex and tracking system, a particle identification system and the dipole magnet. The LHCb detector is shown in Figure 3.2.

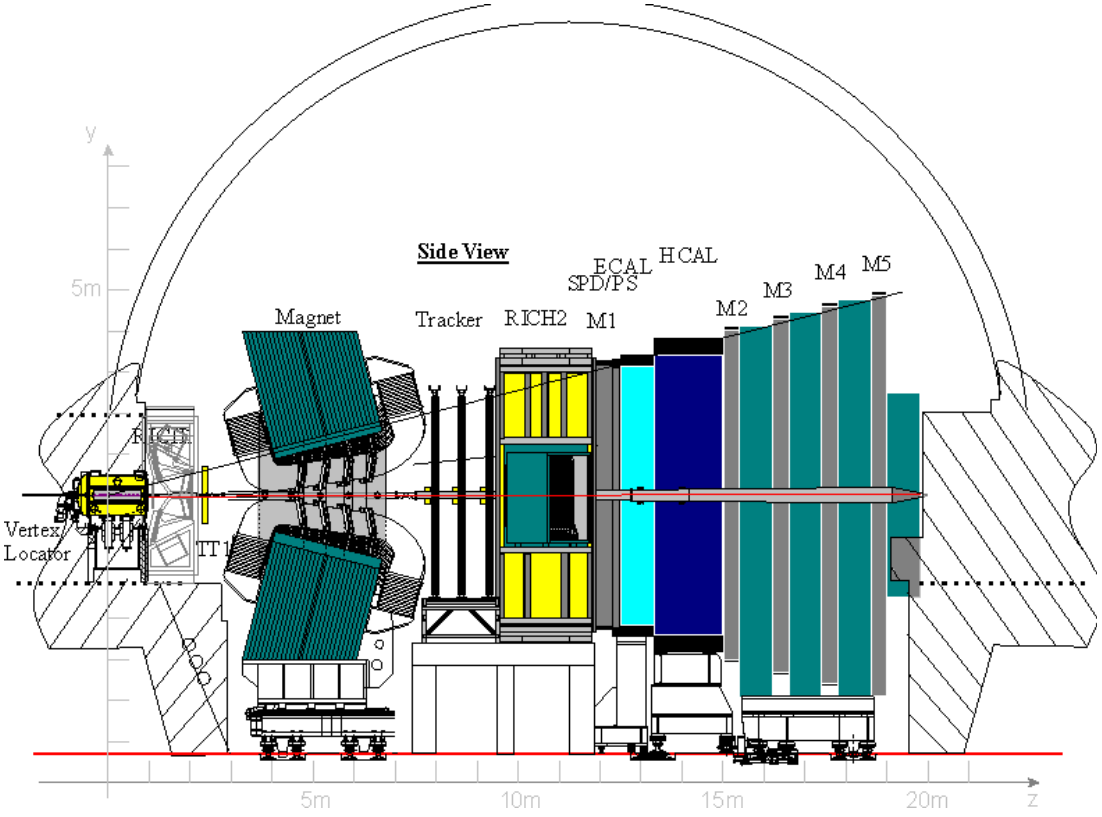


Figure 3.2: Side-view of the LHCb detector [23].

The Vertex and Tracking system:

The Vertex and Tracking system consists of the Vertex Locater (VELO), the Tracker Turicensis (TT), the Inner Tracker (IT) and the Outer Tracker (OT).

Vertex detector

The purpose of the Vertex Locater is the precise measurement of the tracks in the vicinity of the collision point and to detect the primary and secondary vertices of particles and their decay fragments. The VELO is built of two halves, which can be positioned very precisely around the interaction point [25]. The VELO consists of silicon strip sensors. During injection of the LHC beam, the VELO is opened and after stable beam is declared the two halves are moved closer to the beam. The minimal distance from the detector to the beam is only 5 mm, which makes the LHCb VELO the detector which is closet to the interaction point at the LHC and results into a spatial resolution of 10-20 μm. The whole detector consists of 42 semi-circular silicon micro-strip sensors, with always two strip sensors mounted back-to-back: One sensor has strips placed in radial coordinates and the other sensor has strips in the azimuthal angle, φ. Each sensor contains 2048 strips with a pitch varying between 40 μm and 100 μm to have a similar occupancy in all strips. In the Figure 3.4, a schematic of the LHCb Vertex Detector is shown.

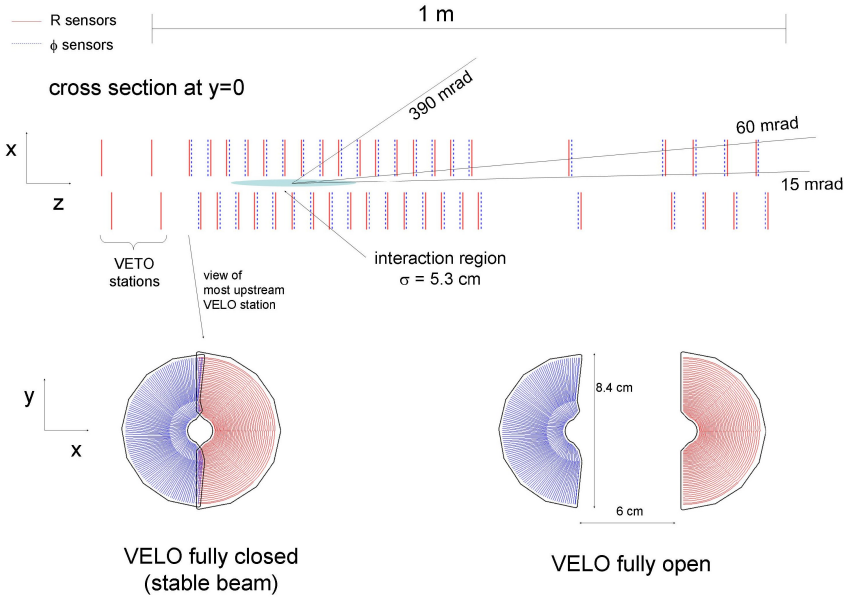


Figure 3.3: Schematic of the Vertex Detector [24].

Tracker Turicensis

The Tracker Turicensis (TT) is placed in between the first RICH[2] detector and the LHCb magnet and is also built from silicon-strip sensors. The sensors are 500 μm thick and have a pitch of 183 μm. The TT consists of 4 layers where two layers are rotated by a stereo angle of $\pm$ 5° with respect to the other two layers.

[2]RICH: Ring Imaging Cherenkov Detector.

This makes a three dimensional measurement possible. Two layers are grouped to pairs and arranged in one station. These stations are 13 cm high and 14.5 cm wide.

Inner Tracker and Outer Tracker

The Inner Tracker (IT) [26] and the Outer Tracker (OT) [27] are placed behind the magnet and in front of the second RICH detector and both are arrange in three tracking stations. The charged particle tracks are measured in the area around the beam pipe with silicon-strip technology in the Inner Tracker and further outside with straw-tube technology in the Outer Tracker.

The **Inner Tracker** covers only 2 % of the acceptance but covers 20 % of the particles tracks. The IT has a cross like shape with the width of 125 cm and a height of 40 cm covering roughly 4 m^2. In each station are placed four detector layers (x,u,v,x) where the u and v layer are tilted in the stereo angle by $\pm 5°$. The strip pitch is 200 μm and the detector thickness for the modules amounts to 320 μm for the module above and below the beam pipe and to 410 μm for the modules at the sides of the beam pipe. The modules are cooled to reduce the effects of the irradiaton and to avoid condensation the modules are flushed with nitrogen at all time.

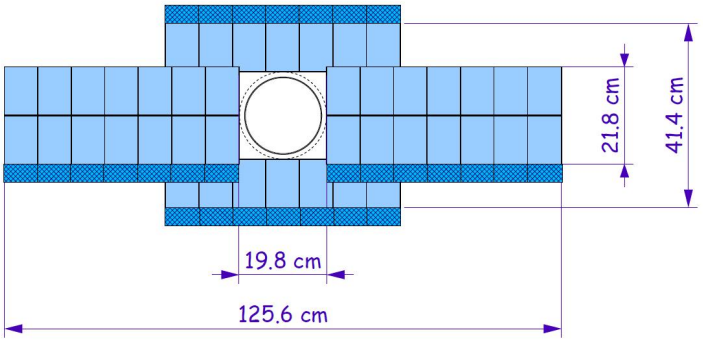


Figure 3.4: Schematic of the Inner Tracker x-layer. Four detector boxes around the beam pipe are visible. The dark blue edges represent the readout electronics. The figure was taken from [28].

The **Outer Tracker** uses 2.5 m long straw-tubes with an inner diameter of 4.9 mm each. The area covered by the Outer Tracker is roughly 30 m^2.In the Section 3.3, the Outer Tracker is described more in detail.

Particle ID systems

For the particle identification (PID) two Ring Imaging Cherenkov Detector (RICH) detectors, an electromagnetic calorimeter, a hadron calorimeter and the muon stations are used. The separation of pions and kaons is very important for the physics goals of the LHCb experiment.

RICH detectors

The RICH detectors use the Cherenkov effect to identify the mass of a particle [29]. When particles pass through a medium (radiator) faster than the speed of light of the medium c_m, they radiate Cherenkov-light in a cone with an opening angle, Θ_c, around the particle direction:

$$\cos(\Theta_c) = \frac{c_m}{v} = \frac{1}{\beta n}. \tag{3.2}$$

Where n is the refraction index of the medium and β is equal to the ratio of the velocity and the speed of light in vacuum. The measured angle Θ_c provides a measurement of the particle velocity. In combination with the particle momentum, it is possible to identify the particle by its mass.

The RICH-1 detector is placed between the vertex detector and the Trigger Turicensis and consists of two radiator materials: 5 cm of silica aerogel (n=1.03) and 85 cm of C_4F_{10} gas (n=1.0014). Using the emitted light from both radiators it is possible to separate kaons and pions in the range of particle momenta from 1 GeV to 60 GeV. On the left side of Figure 3.6 is a schematic of the RICH-1 detector. Hybrid Photon Detectors (HPDs) are used to detect the emitted photons and to record an image of the resulting rings of Cherenkov light formed by the arrangement of mirrors with a 2.5 mm $\times$ 2.5 mm granularity. The RICH 2 detector is situated between the Inner Tracker/Outer Tracker and the electromagnetic calorimeter and uses CF_4 gas with a refractive index of n=1.0005. On the right side of Figure 3.6 is a schematic of the RICH-2 detector. RICH-2 allows PID for particles in the momentum range of 15 GeV up to 100 GeV.

Calorimeter systems

The electromagnetic and hadronic calorimeters are used to measure the energy and position of the particles and to distinguish electrons, photons and hadrons [32]. The system is divided into four components and all four are placed between the M1 and M2 muon stations.

The first component is the Scintillating Pad detector (SPD), which consists of 15 mm thick scintillator tiles used to disentangle electrons and photons. The electrons are detected in the SPD. Behind the scintillator layer a 12 mm lead layer is placed, which induces electromagnetic showers from photons.

The second component is the Pre-shower (PS), which is built with scintillators, which measure the electromagnetic showers induced in the lead layer and SPD in order to disentangle electromagnetic showers from hadronic interactions.

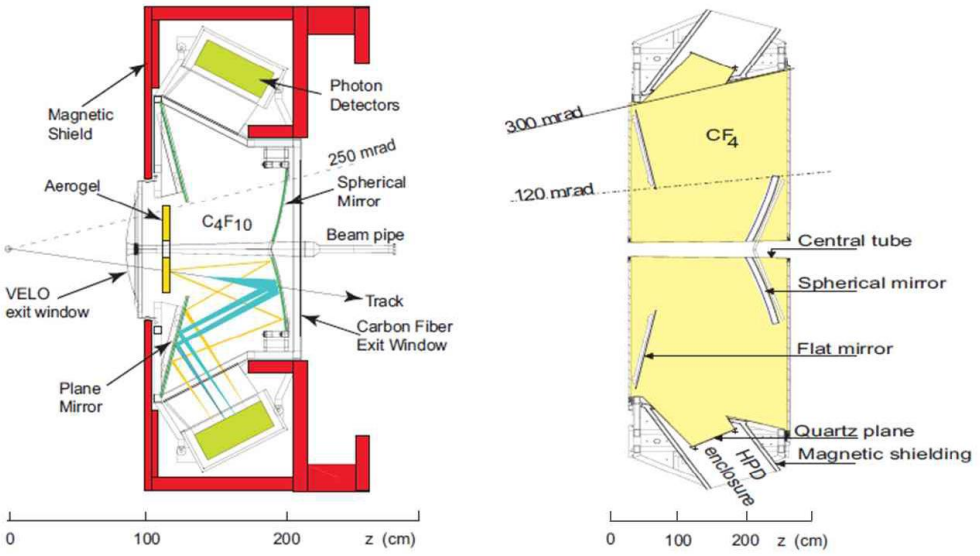


Figure 3.5: Schematic of the LHCb RICH detectors.
Left: Side View of RICH 1
Right: Top View of RICH 2. [29]

The electromagnetic calorimeter (ECAL) is built as a sampling calorimeter with alternating layers of 2 mm thick lead and 4 mm thick plastic-scintillators connected to PMTs. The depth of the ECAL corresponds to 25 radiation length and about 1 interaction length for hadronic particles. The ECAL measures showers of electrons and photons which are produced through bremsstrahlung and pair-production. The energy resolution of the ECAL is:

$$\sigma(E) \sim \frac{10\%}{\sqrt{E}} \oplus 1\% \tag{3.3}$$

The hadron calorimeter (HCAL) is a sampling calorimeter build from layers of 4 mm scintillators and 16 mm thick iron. The scintillators are connected to PMTs. The total depth of the HCAL is 1.2 m, which corresponds to 5.6 hadron interaction lengths. The energy resolution for hadrons is:

$$\sigma(E) \sim \frac{80\%}{\sqrt{E}} \oplus 10\% \tag{3.4}$$

Muon detector

The information of the muon stations is used in the hardware and software trigger and is important for many LHCb measurements. The detector consists of 5 stations placed in front and behind the calorimeters. Four muon stations are placed behind the calorimeters, and the M1 station is placed in front of the calorimeters to improve the tracking [33]. Between all stations of M2-M5 80 cm

thick iron absorbers are placed. The majority is built of Multi Wire Proportional Chambers and only around the beam pipe of M1 Gas Electron Multipliers (GEMs) are used.

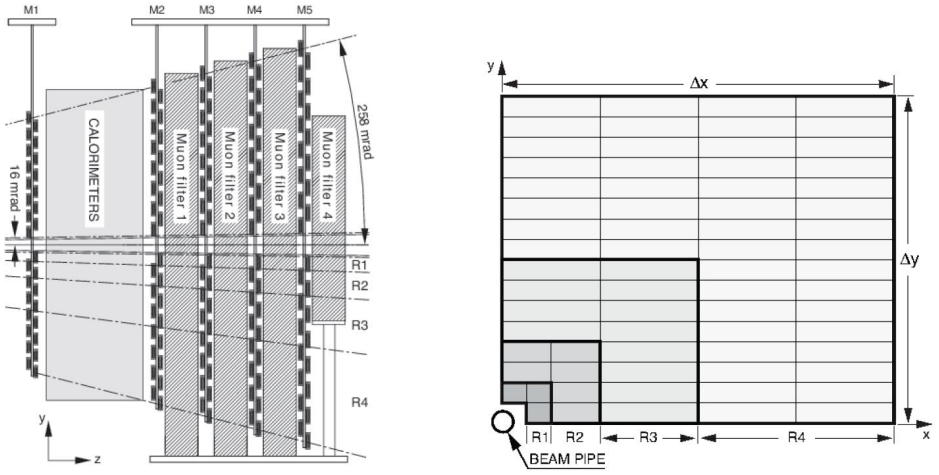


Figure 3.6: Schematic of the LHCb muon stations.
Left: Side View of the five muon stations.
Right: Front View of a muon station showing the different granularity. [24]

Dipole magnet and beam pipe

The dipole magnet generates a magnet field of 1.1 T with an integrated magnet field $\int Bdl$ equal to 4 Tm, which is sufficient to bend the charged particle tracks and measure the particle momentum with a resolution of 0.35 % to 0.5 %. The LHCb magnet is a warm magnet and must be cooled with water [31]. The weight of the magnet is 1600 tons.

The LHC beam pipe in the LHCb region is made partially of a beryllium alloy and has a length of 13 m. Beryllium is expensive, toxic and fragile, but the advantage is that beryllium has small Z and therefore a large radiation length. This minimizes the scattering of particles when they pass the beam pipe.

3.2.2 LHCb Trigger

The bunch spacing at the LHC is 25 ns with an average event rate of 24 MHz at the LHCb experiment. As it is not possible to store all these events for off-line analysis, it is necessary to trigger the data acquisition only on the interesting physics events to reduce the event rate to roughly 5 kHz [30]. This is realized with a three level trigger system: L0, the lowest trigger level is implemented in hardware, and the two HLT trigger systems are implemented in software running

on a PC farm via software. A diagram of the trigger flow in LHCb, and various classes of so-called trigger lines are shown in Figure 3.7.

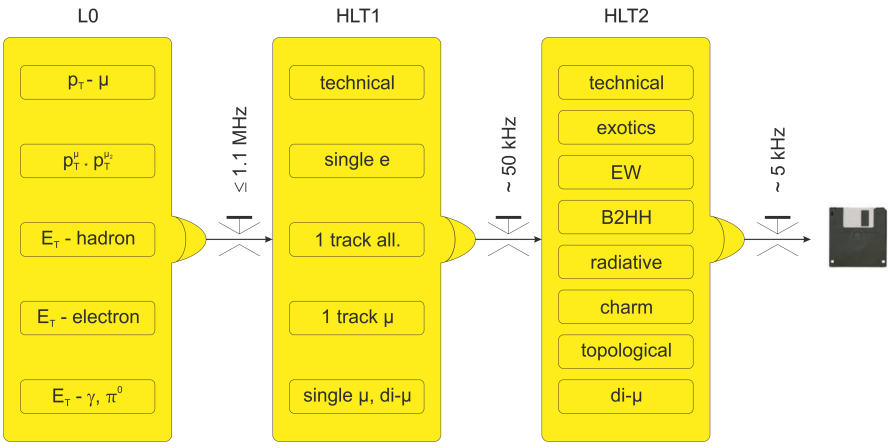


Figure 3.7: A Schematic of the different stages of the LHCb trigger. The Figure was taken from [30] and modified.

L0 Trigger

The L0 Trigger was built with custom electronics, and is synchronized to the 40 MHz LHC bunch clock. It reduces the event rate to 1.1 MHz, which is the input rate for the next trigger level, the HLT 1. The L0 trigger exploits the fact that B mesons have a relative large mass, which gives their decay particles a large transverse momentum (p_T) and a large transverse energy (E_T). The decision time for the L0 Trigger is constrained by the depth of the buffers of the on-detector readout boards to buffer the events during the L0 decision, which is 160 LHC clock cycles deep. The decision time of the trigger including the time to transfer the events and the decision must be shorter than 4 μs.

The L0 trigger decision is based on a logical OR of several requirements listed in the following:

- hadron $E_T > 3.5\,\text{GeV}$
- electromagnetic $E_T > 2.5\,\text{GeV}$
- muon $p_T > 1.48\,\text{GeV/c}$
- $p_{T_1} \cdot p_{T_2} > 1.68\,\text{GeV}^2/\text{c}^2$ for di-muon events

On a positive L0 decision, the trigger is sent to all other sub-detectors to read out the full detector information of the triggered event.

HLT Trigger

The HLT is a software trigger, running asynchronously to the LHC clock on roughly 10000 CPUs in parallel, used to select the interesting events and to reduce the output rate to 5 kHz, which is low enough to write these events to tape for the off-line analysis. The HLT is subdivided into two stages: HLT1 and HLT2.

The HLT1 decision uses a logical OR of all HLT1 trigger lines, which are the following:

- technical trigger (e.g. minimum bias)
- one track trigger
- single muon trigger
- di-muon trigger

The output rate of the HLT1, which is directly the input rate of the HLT2, is 50 kHz.

The HLT2 uses all the detector information and performs an track reconstruction. These tracks are used to reconstruct and select composite particles, based on variables like invariant mass and decay time. The different trigger lines in the HLT2 correspond to the different physics analysis of the LHCb experiment. The HLT2 decision is based on a logical OR of all the HLT2 trigger lines. After a positive HLT2 decision, the event is written to tape. It is possible to prescale the HLT rate, if the output rate does not fit the bandwidth with which it is possible to write to tape. Typically this is 5 kHz and the event size is ∼50 kByte.

3.3 Outer Tracker

The Outer Tracker and the Inner Tracker provide positive information for charged particles for the tracking between the magnet and the second RICH detector [27]. The spatial resolution of the straw-tube detector is ∼200 μm and it covers an area of $\sim 5{\times}6\,\mathrm{m}^2$ with 12 layers of straw-tube modules. The straw-tubes have a inner diameter of 4.9 mm and a length of 2.5 m. The detector is filled with a $Ar/CO_2/O_2$ (70/28.5/1.5) gas mixture, which has a fast drift velocity and results into a maximum drift time of 45 ns. The oxygen was added to the detector gas mixture to prevent aging, which is caused by a contamination of the counting gas due to outgassing of the plastifier di-isopropyl-naphthalene in the epoxy glue Araldite A: AY103-1 [34], which was used for the construction of the modules. The straw-tubes work as proportional counter with an anode wire, which has a diameter of 25 μm and is made of gold plated tungsten. The cathode of the straw-tube is a three layer foil. The two inner layers are a double layer of conducting Kapton-XC foil, where the inner Kapton layer serves as the cathode. The outer

layer is a 12.5 μm layer of Kapton-aluminum, which guarantees gas tightness and electrical shielding. The straw-tubes are arranged in a gas-tight module, which is made of panels sealed with 400 μm thick carbon fiber.

The complete Outer Tracker consists of 168 long and 96 short modules and comprises 53,760 single straw-tube channels. Four module layers are placed in each of the three T-stations, and results into a radiation length of only 2 % X_0. The corresponding four module layers are arranged in three T-stations in an x-u-v-x geometry: the modules in the x-layers are oriented vertically, whereas those in the u and v layers are tilted by $+5^o$ and -5^o with respect to the vertical. Each T-station is divided in 4 C-frames, two on the left side of the beam pipe and 2 on the right side of the beam pipe. Each C-frame hosts two layer of modules (x-u or v-x) and it is possible to move the C-frames on rails to the outside away from the beam pipe. At the end of the C-frames all the cables and tubes for the power, high voltage, slow control and fast control, data fiber, water cooling and gas are hosted in cable chains.

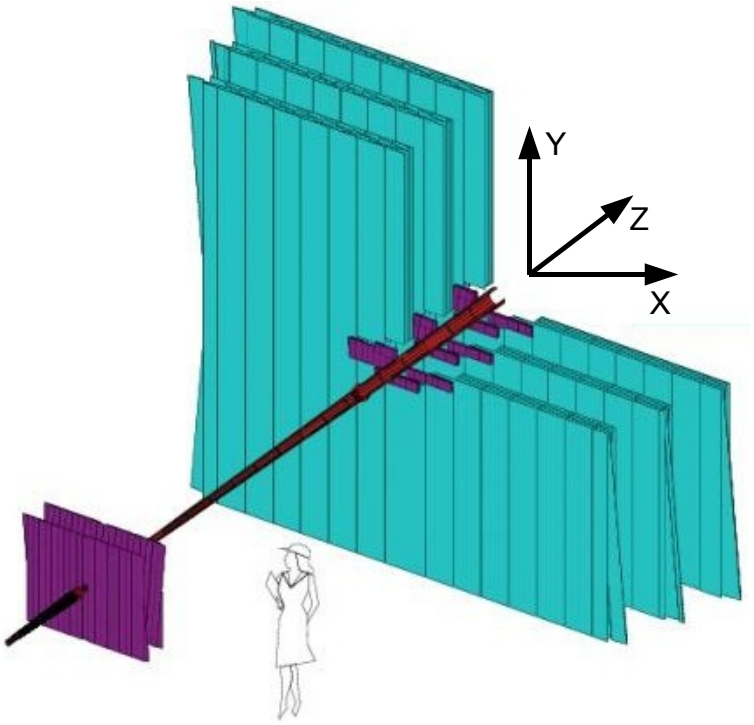


Figure 3.8: Figure of the Outer Tracker (turquois) and the Inner Tracker, Trigger Tracker (purple). The modular structure of the Outer Tracker is visible. The Figure was taken from [38] and modified.

3.3.1 Functional principle of the straw-tubes

The charged particles traversing the gas filled straw-tube generate ionization clusters along the particle track's length. The electric field in the straw-tube separates the ions and electrons and the electrons drift to the anode wire in the center. The average drift velocity is around 62.5 μm/ns [36]. When the distance to the wire is only in the order of the wire diameter, gas amplification starts. The average kinetic energy of the electrons, which they gain between two collisions from the electric field, is high enough to ionize the gas atoms in this region. The gas amplification for the Outer Tracker straw-tubes with nominal high voltage of 1550 V is roughly 50,000 [37]. This amplification results into a detectable charge, which is high enough for the sensitive ASDBLR channel input.

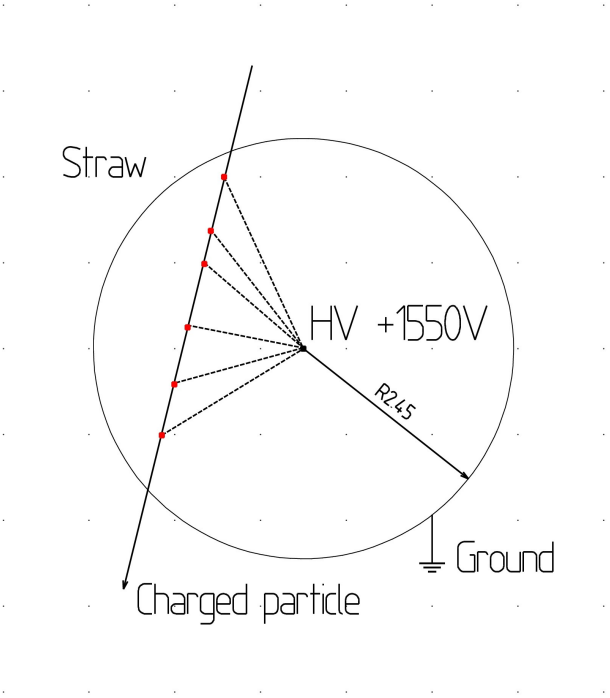


Figure 3.9: Figure of the Straw-tube. When a charged particle travels through the gas filled tube, it generates ionization clusters, which drift in the direction of the electric field.

To determine the distance of the track to the anode wire, the arrival time relation to the LHC clock is measured. With the knowledge of the time of flight of the particle and the signal propagation time, the drift time can be calculated. The distance of the track is calculated with the drift time and the r-t-relation.

3.3.2 Outer Tracker readout electronics

In this part, the existing readout electronics of the Outer Tracker is described. The main parts of the electronics is hosted in the on-detector front-end box. In Figure 3.10 a schematic of the front-end electronics can be seen.

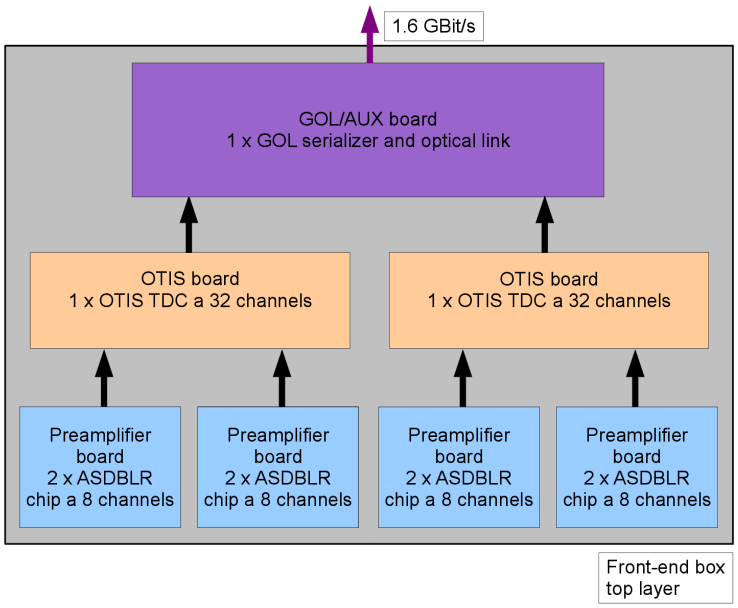


Figure 3.10: Schematic of an Outer Tracker front-end box. The hit signals from the ASDBLR pre-amplifier chips are connected to OTIS TDCs which measure the timing of the hit signals. The time and hit information is transmitted to the GOL serializer chip. This chip serializes the data from 4 OTIS chips and the data are sent to the back-end electronics with a 1.6 GBit/s optical link.

The front-end box is a metal box, which is mounted to the end of an Outer Tracker module, to read out the detector signals and to measure the drift times of the straw-tube detector. The front-end box is connected with 2 long screws to a module, which guaranties a good grounding of the readout boards. The readout electronics inside the front-end box is divided into three types of PCBs. The first board is the ASDBLR pre-amplifier board. Two of them are connected to one TDC board the OTIS board. Four OTIS boards are connected to one Gbit optical link board the GOL board. Each front-end box has only one GOL board. In addition to the readout electronics, also the high voltage of the straw-tubes, are distributed through four high voltage boards inside the front-end box. All the electronic in the front-end box has to sustain a radiation dose of 2 krad. In Figure 3.11 a picture of an opened front-end box can be seen.

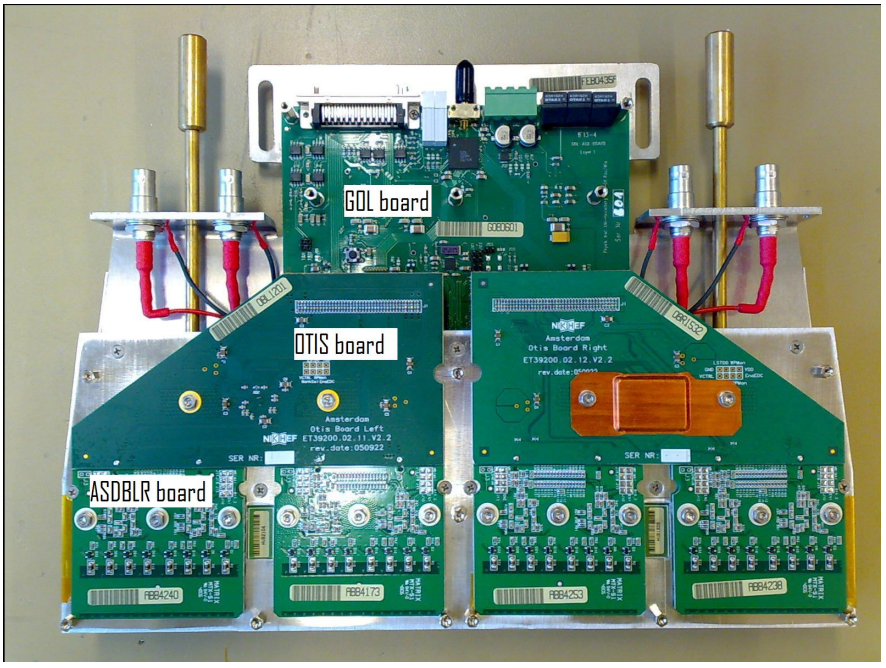


Figure 3.11: Picture of an Outer Tracker front-end box. The 4 top-side ASDBLR preamplifier boards are visible, the other 4 are mounted on the down-side of the front-end box. Furthermore, the corresponding 2 TDC boards (OTIS boards) and the one GOL board for the ECS, TFC and data transmission are visible. The high voltage boards are not visible. They are mounted in the layer below the ASDBLR boards. The picture was taken from [39] and modified.

HV board

Each of the four HV boards in a front-end box distributes the high voltage to 32 straw-tubes, and decouples the detector signal from the anode voltage and provides it to the ASDBLR inputs with a 330 pF capacitance. A schematic picture of the signal readout is shown in Figure 3.12.

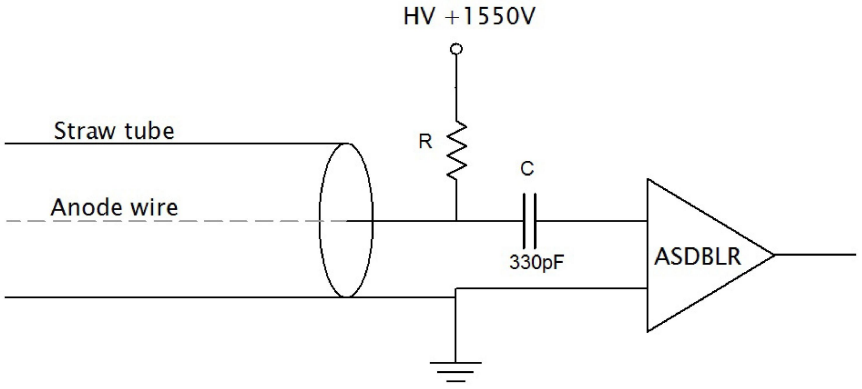


Figure 3.12: Schematic picture of the Outer Tracker front-end HV board. The straw-tube is grounded (cathode) and the anode wire is connected to the high voltage (1550 V). The straw signal is coupled with a 330 pF capacitance to the ASDBLR channel.

ASDBLR board

The ASDBLR board hosts two ASDBLR chips (Amplifier Shaper Discriminator with BaseLine Restoration) [40], which were developed for the TRT of the ATLAS experiment. The ASDBLR chip has 8 input channels, and if a pulse is higher than the threshold value, the chip generates a digital differential signal, which is used for the drift time measurement in the OTIS (TDC) chip. The threshold value is set with a DAC in the OTIS chip.

OTIS board

The OTIS chip (**O**uter Tracker **T**ime **I**nformation **S**ystem) is a custom made ASIC to measure the drift time for 32 channels with respect to the rising edge of the 40 MHz LHC clock with a precision of $<$1 ns [41]. To achieve this, the OTIS chip divides the LHC clock in 64 time bins with a chain of 64 inverters arranged in a DLL (delay locked loop). Each of the time bins has a size of 390 ps. For each of the 32 straw-tubes the OTIS chip has 64 register cells to store the status of the inverter chain. In case of a digital hit signal from the ASDBLR the status of the inverter chain is stored in the corresponding 64 registers for this channel and the decoder of the OTIS chip decodes the 64 time bit information for each channel

to a 6 bit time stamp with an additional hit bit. In addition to this information the OTIS chip stores also the BX-counter and status information bits in the L0 buffer. This memory is 240 bit wide and 163 words deep. After a L0 decision time of 4 μs (160 LHC clock cycles) the L0 trigger decides whether the data is read out via the GOL/AUX board or the data is overwritten by new events. The maximal average LO trigger rate is 1.1 MHz. In addition to the TDC function, the OTIS chip provides four 8 bit DAC to control the ASDBLR thresholds.

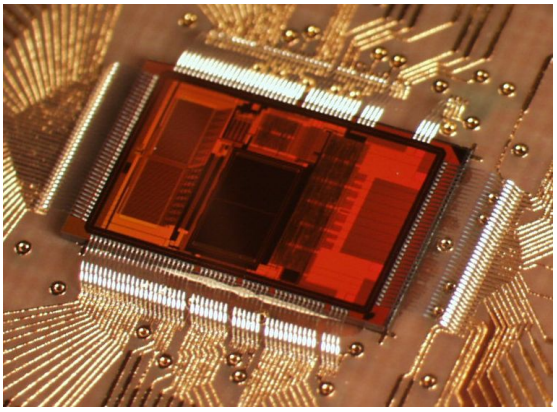


Figure 3.13: The OTIS-TDC chip developed in Heidelberg for the drift time measurement of the LHCb Outer Tracker. The TDC can measure the drift time for 32 channels with a time resolution below 1 ns. The Figure is taken from [42].

GOL/AUX board

The GOL/AUX board connects to four OTIS boards. It provides the fast control and slow control interface as well as the power to the connected electronics. Using the GOL chip the board serializes the TDC data. An optical link with 1.6 GBit/s is used to transmit the data to the back-end electronics, the TELL1 board which is placed in the counting house behind the shielding wall. The data are 8/10 bit encoded for the transmission.

TELL1 buffer board

A TELL1 board in the Outer Tracker receives the data of the nine front-end boxes of one quarter layer. The main purpose of the TELL1 board is to synchronize the L0 triggered events and to do consistency checks, zero-suppression of the data and to buffer the data. The data are formatted and send to the HLT farm. In Figure 3.14 a picture of the TELL1 board is shown. The Outer Tracker TELL1 uses only one optical receiver card the ORx-card. The TELL1 is a 9U VME-PCB and is placed in a VME crate in the counting house behind the shielding wall, which makes the usage of commercial electronics possible. The TELL1 board

uses 1 GBit/s Ethernet to send the data to switches which distributes the data further into the HLT farm. The maximal output bandwidth of the TELL1 board is 4 GBit/s (4 × 1 GBit Ethernet) and the maximal input bandwidth is 24 × 1.6 GBit/s = 38.4 GBit/s, which makes a zero-suppression very important.

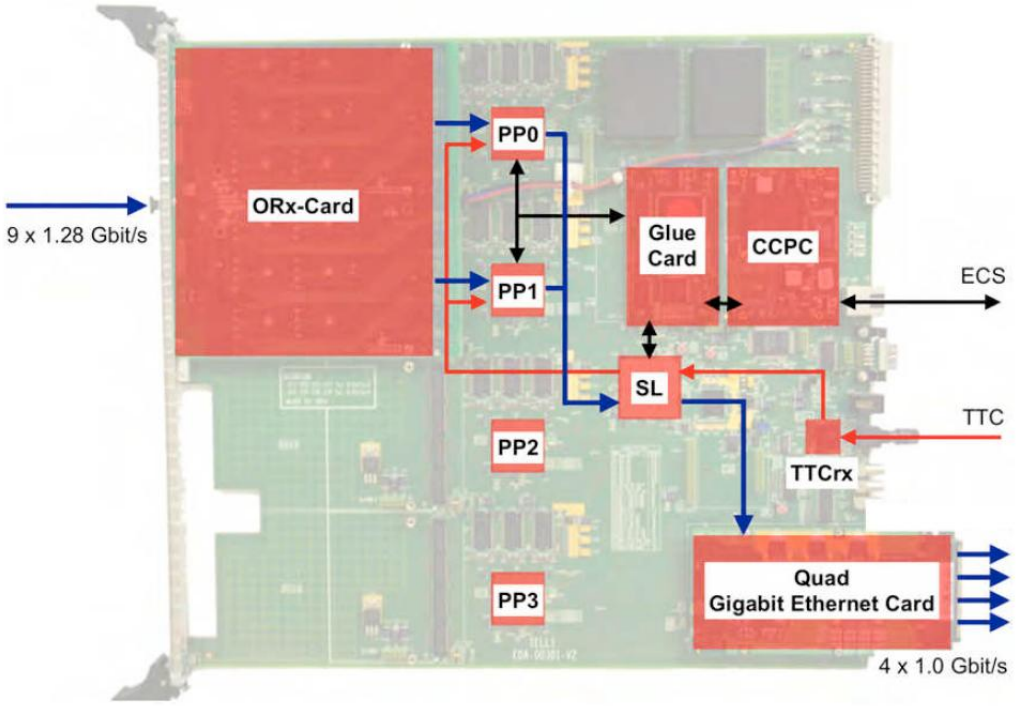


Figure 3.14: Picture of the LHCb TELL1 board [43]. The data from 9 optical fibers are deserialized with one ORx card and send to the 2 pre-processing FPGAs, which perform a consistency check and suppress empty channels. After this, the data is sent to the Sync-Link-FPGA. The second FPGA stage builds the events and prepares the data package for the 4 × 1 GBit/s Ethernet ports (Quad-GBE-Card). Reset and Trigger signals coming from the Timing Trigger and Control receiver (TTCrx), which is connected to the TFC system. The information of the Experiment Control System (ECS) is distributed through a Credit Card sized PC (CCPC).

3.4 Luminosity leveling

To maximize the event yield for the different analysis, LHCb is running at a constant luminosity of $4{\cdot}10^{32}$ cm^{-2}s^{-1} during a proton fill [35]. For ATLAS and CMS the instant luminosity is higher at the beginning of a fill but it decreases exponentially during the fill. The LHCb experiment realizes the constant luminosity

by displacing the two proton beams and monitoring the instant luminosity. In case the instant luminosity falls below a certain level the two beams are moved closer to each other. In this way it is possible to realize constant data tacking conditions throughout the fill and a maximum amount of high quality events can be recorded.

CHAPTER 4

LHCb upgrade

In the data taking period from March 2010 to December 2012, the LHCb experiment was operated at a luminosity up to $4{\cdot}10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ with an average number of interactions per crossing of $\mu \approx 1.5$. The detector recorded a data sample which corresponds to an integrated luminosity of $3.2\,\mathrm{fb}^{-1}$. Extrapolating from the 2012 operation the collaboration expects for the period 2015-2017 to record data corresponding to a total integrated luminosity of $8\,\mathrm{fb}^{-1}$ [2].

After this, the plan is to upgrade the detector in 2018 to be able to collect $>50\,\mathrm{fb}^{-1}$ in the following years with an instantaneous luminosity of $2{\cdot}10^{33}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. As already discussed in Chapter 2.3 the data set would improve measurements which are limited by statistics so far for example the branching ratio of the decay channel $B_d^0 \to \mu^+\mu^-$. It is also worth to mention that the LHCb upgrade is independent of the LHC high luminosity upgrade, because the foreseen instantaneous luminosity of $2{\cdot}10^{33}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ is well below even the current LHC luminosity of $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ for ATLAS and CMS.

In March 2011, the collaboration submitted a Letter of Intent (LOI) describing the upgrade procedure [12]. In May 2012 the Framework Technical Design Report (TDR) was released and subsequently endorsed by the LHCC [45]. The informations shown in this chapter are taken from these two documents. The necessary R&D is in full progress and the corresponding subsystem TDRs will follow until early 2014.

4.1 Upgrade of the Trigger

Only increasing the instantaneous luminosity does not guarantee a higher number of recorded heavy flavor events. First, these events have to be triggered and later to be recorded. It was investigated how the trigger yield would develop with the current readout electronics of the LHCb detector and the current trigger. In addition, the trigger yield for final states with muons was investigated which would increase linearly with an increasing luminosity, but for hadronic and semileptonic final states the trigger yield would saturate at a luminosity of above $4{\cdot}10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The trigger yield for final states with muons and for hadronic and semileptonic final states as function of the instantaneous luminosity can be seen in Figure 4.1. The maximum detector readout rate, which is limited to 1.1 MHz causes the described trigger yield saturation. This can be explained as follows. If the luminosity is increased the rate for hadronic and semileptonic final states would exceed 1.1 MHz. To limit the trigger rate to 1.1 MHz the L0 hadron thresholds E_T and p_T have to be increased, but this also decreases the trigger yield for these channels.

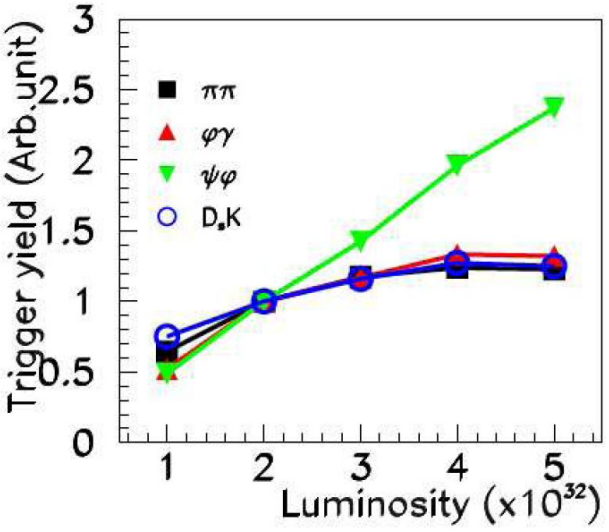


Figure 4.1: The trigger yield of final states with muons and final states with hadrons against luminosity. Muon final states increase linearly with higher luminosities but final states with hadrons approach saturation around a luminosity of above $4{\cdot}10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The Figure was taken from [12].

To improve the trigger yields for the hadronic modes, one would like to lower the L0 hadron thresholds E_T and p_T. This cannot be done using a hardware trigger which is only based on E_T and p_T of the particles. A full event reconstruction is needed for the event selection, using the complete detector information and all

the event information in a flexible software trigger (upgraded HLT). All LHCb sub-detectors have to be read out with 40 MHz.

4.2 Upgrade of the LHCb sub-detectors

In the following the upgrade plans for the different sub-detectors will be presented. The sequence goes from the vertex detector at the proton-proton collision point to the muon stations.

4.2.1 Vertex detector upgrade

The LHCb Vertex Detector has been built to collect a data set of $\sim$10 fb^{-1} which will be reached 2018. Afterwards, the vertex detector has to be replaced, due to radiation damages. The VELO is the LHC sub-detector with the smallest distance to the beam. The replacement for the installed vertex detector will be improved compared to the current detector to cope with the higher multiplicity and the 40 MHz readout. It is foreseen to use a smaller segmentation for a more efficient secondary vertex reconstruction in events with multiple interactions per crossing, a much higher radiation hardness (370 Mrad in 10 years) and a low material budget to avoid multiple scattering. It is planned to use the VeloPix chip with 55 μm $\times$ 55μm pixels which is based on the Timepix3 and uses a 130 nm process technology, which is proven to sustain a total radiation dose of more than 400 Mrad. Extensive R&D is ongoing to investigate the optimal module layout and mechanics, sensor material like planar or 3D silicon and a possible diamond cooling substrate. Furthermore, another topic of interest is the construction of the new RF foil.

4.2.2 RICH detector upgrade

The RICH detectors are necessary for particle identification (PID), so the RICH detectors on both sides of the magnet will remain. The aerogel in RICH1 will be removed to reduce the occupancy. In addition, new photon detectors and new readout electronics are needed to allow the readout with 40 MHz, because the front-end electronics is embedded into the vacuum of the current used Hybrid Photon Detectors. The baseline solution for the new photon detectors are 64-channel multi anode Photomultiplier tubes with a new readout chip.

4.2.3 Tracker Turicensis upgrade

The Tracker Turicensis has to be replaced as the front-end electronics are part of the silicon sensors and it has a maximal readout rate of 1.1 MHz. For the optimal operation in the upgrade environment, it is being considered to have a TT nearer to the beam axis and a smaller vertical segmentation.

4.2.4 Tracking station upgrade

The readout electronics of the tracking system behind the magnet have to be changed to a 40 MHz readout. In addition to the new front-end development the current Outer Tracker would have to be replaced close to the beam pipe, due to the fact that the occupancy with an instantaneous luminosity of $2{\cdot}10^{33}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ can reach more than 25% where an effective tracking is not possible [12]. It should be kept in mind, that the current Outer Tracker is a gaseous detector using straw tube technology. Two options are possible to cope with the high occupancies in the inner part:

1. Double the width and height of the Inner Tracker and use shorter Outer Tracker modules in the vicinity of the beam pipe. The new Inner Tracker area would rise by a factor of 4. This option is depicted on the top of Figure 4.2.

2. Replacing the Inner Tracker and the Outer Tracker modules in the central region with a fiber tracker. This option is depicted on the bottom of Figure 4.2. The fiber modules would consists of 5 fiber layers in each module, each fiber with a diameter of 250 μm. For the readout, silicon photo multiplier (SiPM) arrays are considered. Active R&D is ongoing to investigate the radiation hardness of the fibers and the SiPM arrays. In addition, questions regarding construction and assembly of such a detector have to be solved and a complete new readout electronics has to be developed.

In both solutions the remaining Outer Tracker modules need new readout electronics to cope with the new 40 MHz readout. It is considered to replace the custom made OTIS readout chips by an FPGA on which the time measurement is implemented. The crucial point about this design is the radiation tolerance of the FPGA, which was tested. The LHCb group of the Physikalische Institut Heidelberg tested a SRAM-based FPGA from Altera and a second group from NIKHEF[1] investigated the feasibility to use a flash-based FPGA from Mirosemi (Actel). The Heidelberg studies are the work of this thesis.

It should also be kept in mind that a third solution is possible, for which the whole IT and OT would be replaced by a fiber tracker. In this case no new readout electronics for the LHCb Outer Tracker is necessary. However, for the readout of the Fiber Tracker, FPGAs are also considered.

4.2.5 Calorimeter upgrade

The calorimeters will keep all modules and PMTs, but the PMT gain will be reduced by a factor of 5 to keep the current constant due to higher occupancy. In addition, the front-end electronics will be changed to compensate for the lower

[1] National Institute for Nuclear and High energy physics Amsterdam

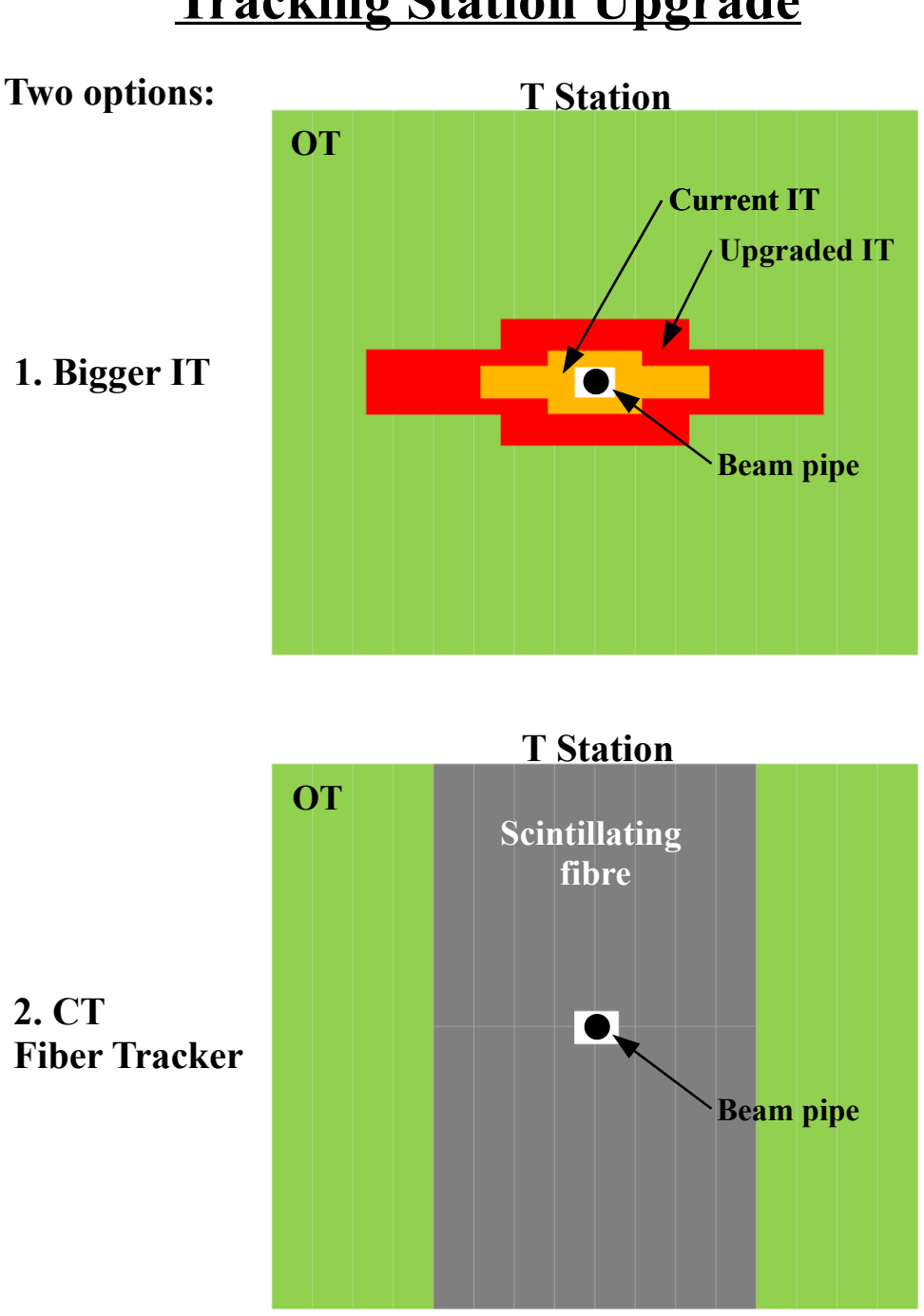


Figure 4.2: The two options for the tracking stations to replace the high occupancy part of the Outer Tracker.
1. Using an increased Inner Tracker with shortened Outer Tracker modules around the beam pipe.
2. Replacing the Inner Tracker and the the Outer Tracker modules in the central region with fiber tracker modules.

gain and to allow for a readout with 40 MHz. The PS and SPD will be removed and the $e/\gamma/hadron$ separation at the higher level will take place in the new HLT using the tracking information.

4.2.6 Muon detector upgrade

The muon chambers are expected to fulfill the upgrade requirements nevertheless aging and occupancy studies are ongoing to confirm the present expectations. Furthermore, the muon chambers are already readout at 40 MHz in the current L0 trigger, which results in the fact that the front-end electronics can be kept. The M1 station in front of the calorimeters will be removed, because the tracking stations will perform a better muon momentum resolution in the upgraded trigger and the M1 station is not useful any more.

4.3 Upgrade of the LHCb readout electronics

To migrate the LHCb detector to a trigger-free 40 MHz front-end readout, almost all sub-detectors have to upgrade their readout electronics. The front-end electronics will host the pre-amplifiers, ADCs or TDCs, zero suppression, derandomising buffer and fast optical transceivers. Figure 4.3 shows a schematic of the readout electronics changes. The current L0 buffers in the front-end will be removed, due to the fact that all events will be transmitted to the new buffer board, namely TELL40 board. These events will be already zero-suppressed in the front-end to reduce the necessary bandwidth for the optical GBit/s transceivers. The TELL40 board is the upgraded version of the TELL1 board. The TELL40 board will host fast optical receivers and the low level trigger rate control. After the data is formated, it is transmitted to the event filter farm (upgraded HLT) using 10 GBit/s Ethernet ports. The upgraded HLT will have roughly a 5-7 times higher output rate compared to the current HLT output rate of 5 kHz. A bigger CPU farm, more disk space and more computing power will be needed to cope with the higher number of events at the output of the HLT.

4.3.1 Upgrade of the OT front-end box to 40 MHz readout

The readout chips inside the front-end box of the LHCb Outer Tracker have to be exchanged for the upgrade to a 40 MHz readout. Figure 4.4 depicts a opened front-end box with the three types of PCBs visible. The ASDBLR board can be kept, as the ASDBLR chip is radiation hard beyond the radiation level of the upgrade. The OTIS TDC chip would be radiation hard enough, but the readout rate of the chip is limited to 1.1 MHz. In addition, the GOL/AUX board had also to be redeveloped. The expected bandwidth of the upgraded Outer Tracker front-end box is between 20-30 GBit/s, depending on the data formatting and the number of TDC bits used for the drift-time measurement. TDC bits for the

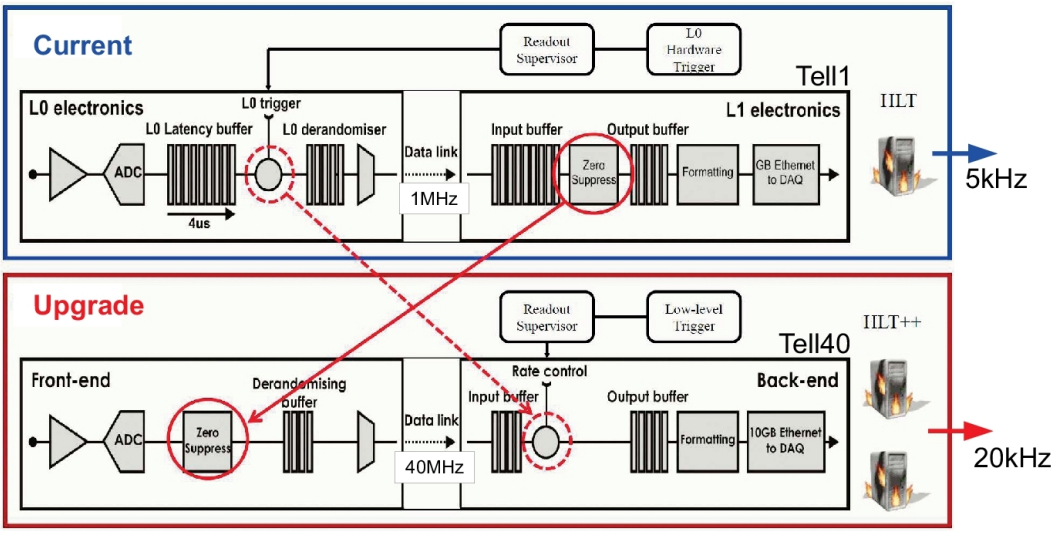


Figure 4.3: Figure of the current and upgraded LHCb readout electronics. The Figure was taken from [46] and modified.

drift-time measurement are used. A drift-time with 4 bits, corresponding to a TDC bin size of 1.6 ns, would be the lower limit to reach the spacial resolution of 200 μm, which is the requirement for the track reconstruction.

4.4 LHCb upgrade schedule

In the first long LHC shutdown till 2013 - 2014 the LHCb detector will be maintained and preparations for optical fibers and cables will be done. In addition, the LHCb subsystem TDRs will be submitted to LHCC.

After the first long shutdown LHCb is to take data with a center of mass energy of 14 TeV and 25 ns bunch spacing from 2015-2017. In parallel the production and quality control of new components will be conducted.

The schedule for the LHCb upgrade sees the installation and commissioning of the upgraded detector during the second long shutdown in 2018/2019. After 2019, LHCb will run at a higher luminosity and with new sub-detector components.

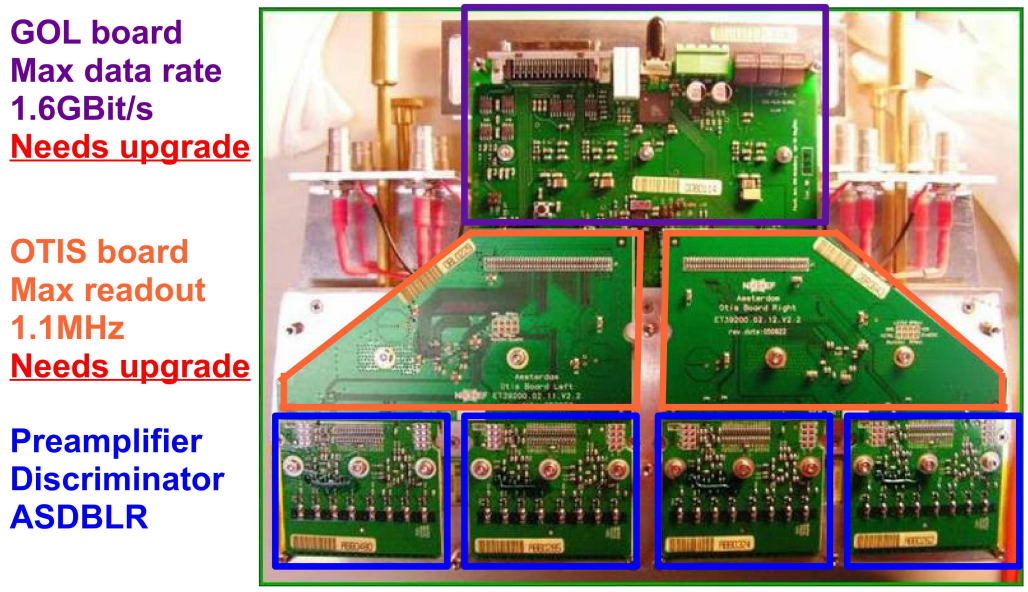


Figure 4.4: The current front-end box with the three PCB types: the ASDBLR board, OTIS board and GOL/AUX board. The eight ASDBLR boards can be reused for the upgrade. The OTIS chip readout rate of 1.1 MHz is too low for the upgrade and also the GOL/AUX board has to be redesigned, because the bandwidth of 1.6 GBit/s is too low. The picture was taken from [47] and modified.

CHAPTER 5

FPGA-based time measurement

The front-end electronics of the Outer Tracker must be modified for the LHCb upgrade as the readout rate changes from 1.1 MHz to 40 MHz. As discussed in the detector Chapter 4.3.1, the TDC chip for the drift-time measurement and the serializer chip GOL have to be replaced. This thesis presents tests to use an FPGA[1] as TDC and serializer in the new front-end box, rather than developing a new TDC ASIC as this would be very time consuming and expensive. However FPGAs are usually not designed for the usage in radiation environments. The idea was to test different commercial FPGAs as the main component in the new readout board. A research group from NIKHEF decided to test a flash-based FPGA from former Actel now Microsemi [48], while our research group has tested a SRAM-based FPGA with multi GBit/s transceivers from Altera. The main difference between the two FPGAs is that the flash-based FPGA does not lose its configuration during irradiation, the result is that the firmware does not have to be reloaded frequently. But the SRAM-based FPGA provides GBit/s transceivers and sustains a higher total ionization dose (TID).

The following chapter begins with a short introduction to FPGAs and the principle of FPGA-based time measurements. After this the implementation for the Outer Tracker drift-time measurement with the FPGA will be presented. Two versions of TDC firmware were written, one for the Stratix FPGA[2] [59] and one for the Arria GX FPGA. For the Arria GX chip a test board was built and

[1] Altera Arria GX (EP1AGX35DF780I6)
[2] EP1S25F1020

irradiation tests were performed.

5.1 General description of an FPGA

An FPGA is an integrated circuit which provides a large number of programmable logic gates and RAM[3] blocks which can be connected by programming the FPGA [49]. In addition, the functions of the logic gates can be programmed, and makes it possible to implement complex digital functions. One logic unit of an FPGA is the logic block (LB), which consists of inputs and outputs (I/O), lookup tables (LUT) and a flip-flop in front of the outputs as depicted schematically in Figure 5.1. The logical function of the logic block can be controlled with the configuration of the LUT. The exact architecture of the logic block varies from vendor to vendor and even from FPGA family to FPGA family. Between six and ten logic blocks

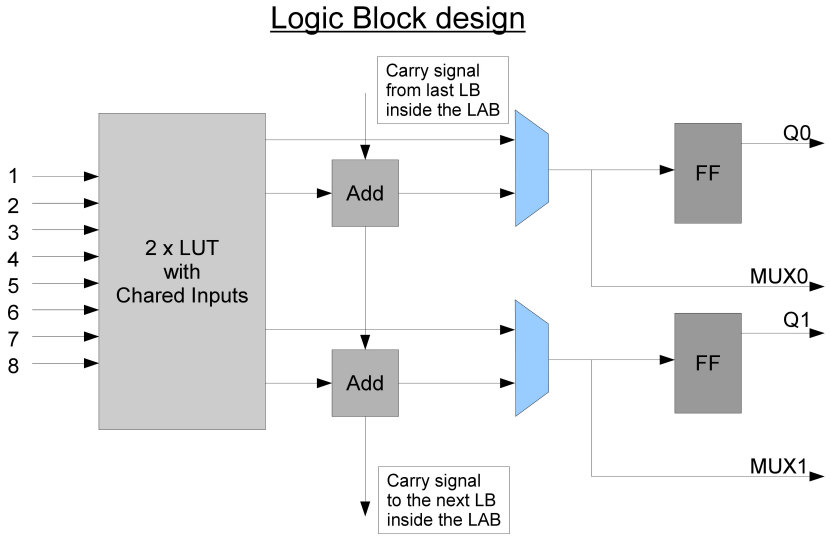


Figure 5.1: Architecture of a logic block of an FPGA. The LB are arranged inside the LAB in a column. Fast carry signals connect the neighboring LB. The schematic has been taken from the Altera web page [50].

are arranged in a logic array block (LAB). The logic blocks inside the logic array block are normally interconnected with fast carry signals. The logic array blocks are arranged in a grid and, around the LAB, a net of wires is placed. The typical architecture is shown in the schematic in Figure 5.2. The signal routing of these wires is controlled by the FPGA configuration, which is referred to as firmware.

The FPGA functions are determined by the firmware, which makes the usage of FPGAs very flexible. The number of I/O cells (connectable pins) ranges from

[3]Random-access memory

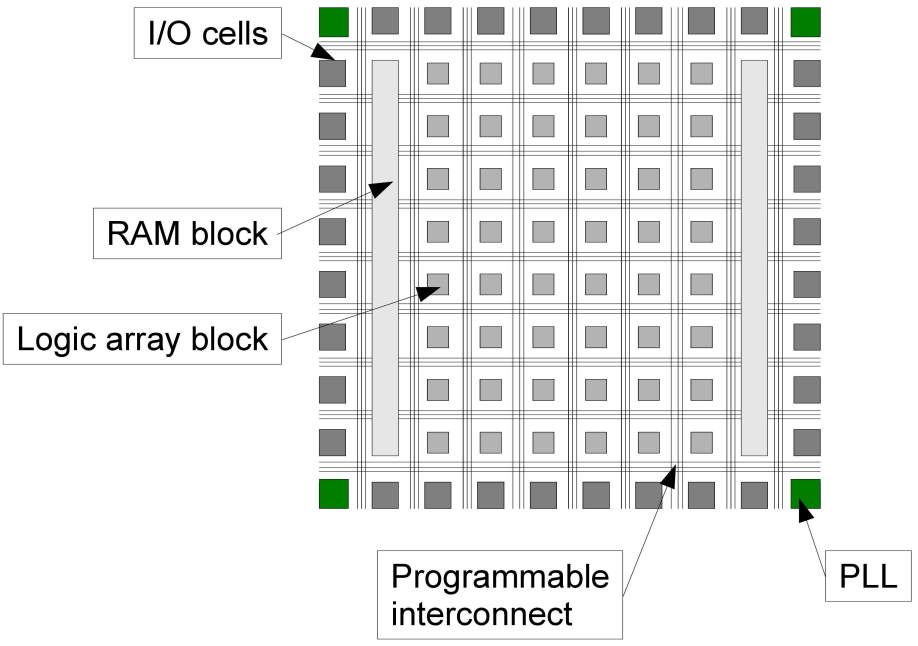


Figure 5.2: Architecture of an FPGA. The LAB are arranged in a grid surrounded by programmable interconnects.

around 50 to 1,100 and the number of LB variates from 3,000 to 800,000, which makes it possible to choose the appropriate size for the application.

5.1.1 Workflow of FPGA programming

The programming file for an FPGA is created in 4 major steps [51].

The first step is the description of the function of the design. The most common way to describe a design is a hardware description language (HDL). There are two main HDLs for FPGAs, which are VHDL[4] and Verilog. In addition, design software exists that makes it possible to generate a design in block diagrams with already pre-defined logic modules e.g. adder or FIFOs[5]. The design is programmed by linking the signals of the modules in the block diagrams. The design software creates from the generated block diagrams again VHDL or Verilog code. The description in this step can be completely functional so no information of how the design is implemented in the FPGA logic has to be included.

The second step is the simulation of the design to test the functionality of the design. As in this step no timing information is included this simulation is called functional simulation.

The third step is the synthesis of the design which generates the netlist which describes the whole design. The netlist describes how the different signals and design components are connected. In addition, the netlist description shows the design already in FPGA logic block level how the different blocks are realized.

The last step is the "Place & Route" step. Here the design is placed on the FPGA and the used logic elements are connected by the place and route fitter. This step needs constraints from the designer who has to define the pins for the design I/Os. In addition, the place and route fitter can be influenced by constraints like placement assignments for logic elements or timing assignments for signal delays. This possibility was used in this thesis to realize and optimize the FPGA-based TDC. More details about the usage of assignments are shown in Subsection 5.4.1. At the end of this step the FPGA programming file is generated.

The following list shows the software used during this thesis:

1. Design software: HDL Designer 2009 - 2012 from Mentor Graphics [52]
2. Simluation: ModelSim SE 6.5 from Mentor Graphics [53]
3. Synthesis: Quartus II 9.0 - 11.1 from Altera [54]
4. Place & Route: Quartus II 9.0 - 11.1 from Altera

[4] Very High Speed Integrated Circuit Hardware Description Language
[5] Data buffer using the "First In Ũ First Out" method

5.1.2 Using an FPGA for the 40 MHz upgrade of the LHCb Outer Tracker

Modern FPGAs have a lot of logic elements that allow to generate even complex functions like TDCs. The clock speed of an FPGA is fast enough to achieve TDC time resolutions below 1 ns, which is fast enough for the LHCb Outer Tracker drift-time measurements. In addition, most of these chips have several GBit/s transceivers for high bandwidth applications which can be connected easily to optical links. The bandwidth needs for the LHCb Outer Tracker upgrade can be fulfilled by many modern FPGAs. Furthermore, FPGAs are very flexible because it is possible to change the firmware. The development time for new readout electronics based on FPGAs is short. One reason for the short development time is the possibility to start with the development of the PCB before the firmware is finished. Another reason to use an FPGA for the upgrade is the small number of chips (<1000) needed for the detector. This makes the cost for the single readout boards low compared to an ASIC development.

An important factor that has to be taken into account is the radiation tolerance of the FPGAs. The total ionization dose (TID) tolerance of commercial SRAM cells increases with the down-scaling of the CMOS process [75] due to dramatically decreased life-time of trapped positive charges in the gate oxide. Therefore the threshold voltage shifts are of little concern while the leakage currents are of increasing importance. For modern SRAM cells, produced in a commercial 90 nm CMOS process, a total ionization dose tolerance of roughly 300 krad can be expected [76]. This makes the usage of modern SRAM-based FPGAs also possible for on-detector readout electronics in high energy physics, which was investigated in this thesis and will be discussed further in Chapter 7. The main drawback of using an SRAM-based FPGA in the detector readout is a frequent reloading of the FPGA firmware, because the configuration registers can flip due to radiation.

5.2 Methods for time measurements with an FPGA

There are different methods to realize a TDC on an FPGA. Most of these methods use the small signal delay from the single logic elements on the FPGA, but it is also possible to use fast inputs (LVDS receivers) or phase-locked loops (PLL). Time resolutions down to a few picoseconds can be achieved by the tapped-delay line method [55]. The advantage of using an FPGA-based TDC is the flexibility, so it is easy to fit the TDC exactly to the detector readout scheme. In the following, the methods using a tapped-delay line, a ring oscillator, a fast sampling with LVDS receivers and fast counters will be described.

5.2.1 Tapped-delay line

One of the first FPGA-based TDCs was developed in 1997 with a time resolution of 200 ps [56]. This TDC used a tapped-delay line. The tapped-delay line exploits the signal propagation time through the logic elements for the time measurement. Although there are different possible implementations, the tapped-delay lines are all based on the same principle. The very fast FPGA-based TDCs use the carry signals between the LBs inside a LAB, because the carry signals have the smallest delay, which results in the smallest TDC bin size. The start signal for the time measurement propagates through a line of delay elements connected in series. After each delay element, the signal is tapped and fed to the input of a flip-flop. The stop signal is connected to the clock inputs of the flip-flops, which triggers the flip-flops to save the status of the delay line. Figure 5.3 shows a schematic of a tapped-delay line. The time is decoded by the position of the start signal in the tapped-delay line. It is important to be sure that the decoder finds a real transition, which is realized by also checking the following flip-flops, if these stay at the new signal value a real transition is found.

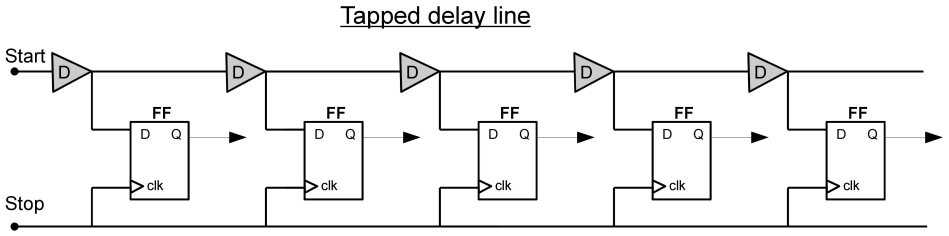


Figure 5.3: Schematic of a tapped-delay line. Architecture: The start signal for the time measurement is wired through a chain of delay elements (gray triangles with label D) and after each delay element the start signal is connected to the input of a single flip-flop. The stop signal is connected with the clock inputs of the flip-flops. The principle: The start signal propagates through the delay line and the stop signal triggers the flip-flops to save the state of the delay line. The time between start and stop signal is calculated from the position of the signal level change in the tapped-delay line.

In a real TDC implemented with this method, the time bin size varies because the delay elements and the signal routing have different propagation time. A cell-by-cell calibration is necessary, which also depends on the temperature. Furthermore, it is not always possible to construct all delay elements with the same size, because of the FPGA architecture. The usage of the fast carry signals between the logic blocks is not for every delay element possible. When all logic

blocks inside a logic array block are used, the next logic element in the neighboring logic array block has to be taken. The delay between two neighboring logic array blocks is much bigger than between for two neighboring logic blocks. This produces so called "ultra wide" TDC bins, which are typically bigger by a factor of three to five with respect to the small bins. One possibility to avoid the "ultra wide" bins is to propagate a multi-transition start signal, instead of a single transition start signal, through the delay line. This method is called wave union. If one transition is in an "ultra wide" time bin, then the other is in a normal time bin. This arrangement effectively subdivides the "ultra-wide" bins using the information of both transitions in the time encoding. A time resolution of below 10 ps is reachable with this method.

The drawback of this design is the requirement of a relatively large amount of logic-elements for a single TDC channel in addition to the bin size calibration and temperature dependence.

5.2.2 Ring oscillator

The ring oscillator is a self oscillating system. It is constructed by connecting a buffer with an inverter, looped back to the buffer input. The frequency of the system is determined through the delay between the two logic elements, which give their result back to the input of the other element. In the example shown in Figure 5.4, the AND gate is the buffer and the NOR gate is the inverter.

The ring oscillator method uses two ring oscillators with a small frequency difference [57]. The two ring oscillators are started with two different signals. The TDC start signal triggers the flip-flop of the slower ring oscillator and the TDC stop signal triggers the start of the faster ring oscillator. The two resulting clocks are used for two separate counters, which start to count at beginning of the oscillations. A phase detector triggers the latching of the two counter values at the moment when the fast clock and the slow clock are in phase. Figure 5.5 shows the waveform for the ring oscillator TDC.

The slow/fast counter value n_1/n_2 and the time period of the corresponding oscillators T_1/T_2 determine the measured time $T_{\mathrm{Start-Stop}}$

$$T_{\mathrm{Start-Stop}} = n_1 \cdot T_1 - n_2 \cdot T_2. \tag{5.1}$$

The fast ring oscillator is built with a flip-flop, an AND gate and a NOR gate. The slow oscillator uses an additional AND gate as delay between the two logic gates. By adding an AND gate to the NOR gate, the frequency of the oscillator decreases. The periods of such a ring oscillator are of the order of 5 ns. The clock period difference of the two ring oscillators represents the time resolution of the TDC.

The ring oscillator TDC represents an event-driven asynchronous TDC, this does not fit to a clock driven synchronous TDC needed for the LHCb Outer Tracker. An additional drawback of this method is that the maximum number

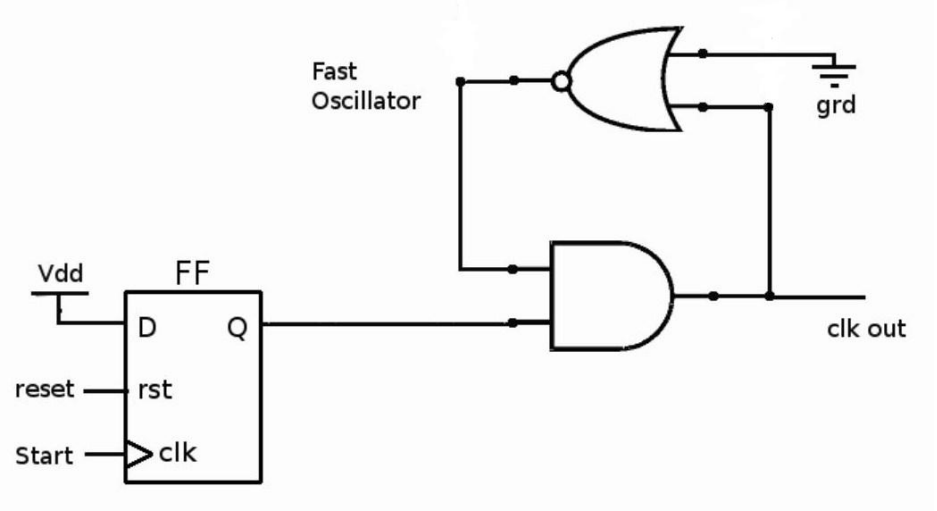


Figure 5.4: Schematic of the ring oscillator. The connected AND gate and the NOR gate result in a self-oscillating system [57].

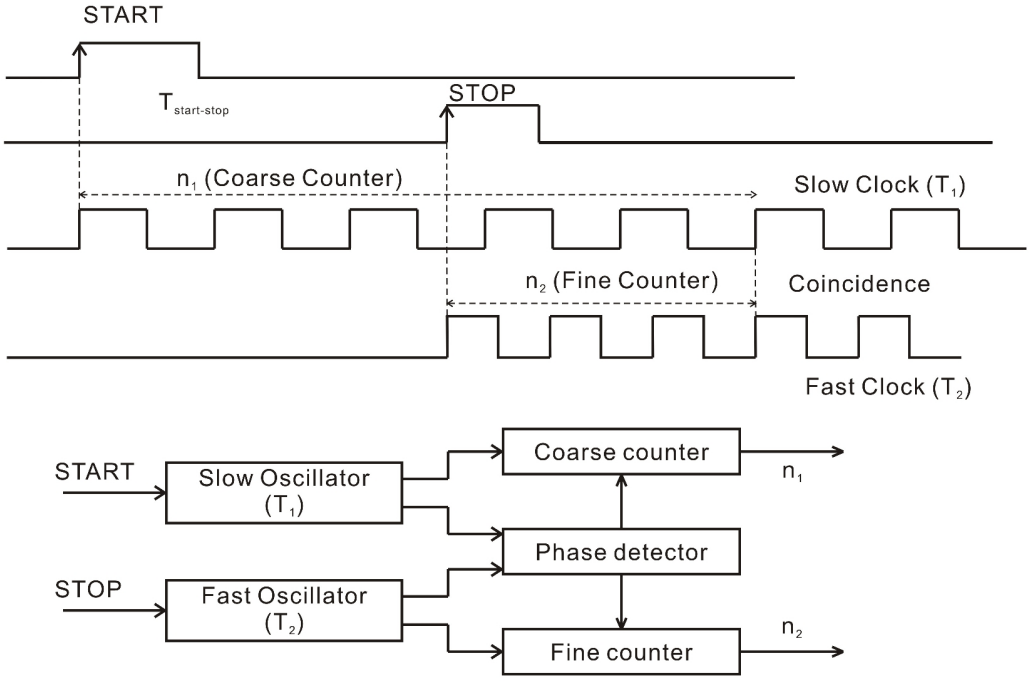


Figure 5.5: Waveform of the ring oscillator method. The Figure was taken from [57] and modified.

of counts for the fast counter until the synchronization is reached is rather high which results in a low maximum hit rate for the TDC channel. This rate is typically in the low MHz region. This makes this method not suitable for the usage in a high occupancy detector. Furthermore, the ring oscillator frequency depends strongly on the temperature.

5.2.3 Fast sampling with LVDS receivers

Modern FPGAs have LVDS (Low-voltage differential signaling) inputs which are used for high speed data transfer from chip to chip. These receivers sample the input with a frequency of about 800 MHz. It is possible to sample the signal of a single detector channel directly with these fast inputs [58]. The deserialized data of the detector channel are analyzed to determine the measured time by searching for signal level transitions in the data. The position of the transitions inside the data stream represents the time of the hit. The time resolution of the TDC depends on the sampling frequency. It is possible to increase the time resolution by using two or four LVDS receivers sampling one detector channel signal. In this case these LVDS receivers use clocks, which are phase shifted to each other. The phase shift between the LVDS receivers represents the time bin size and it is possible to reach time resolutions below the LVDS receiver clock period.

The drawback of this method is that the number of TDC channels depends on the number of LVDS receivers in the FPGA which is usually small.

5.2.4 Fast counter method

This time measurement is realized by latching the value of a counter, running with a high frequency ν, when a start or a stop signal occurs. The difference of the counter value n_1 for the start signal and the counter value n_2 for the stop signal represents the measured time. The time Δt is equal to the counter difference Δn times the counter period T:

$$\begin{aligned} \Delta t &= \Delta n \cdot T, \\ \Delta n &= n_2 - n_1, T = \frac{1}{\nu}. \end{aligned} \tag{5.2}$$

The maximum frequency for logic blocks inside the FPGA is limited to 500 MHz today, which makes it necessary to combine two or four phase-shifted counters to reach time resolutions below 1 ns. The phase-shift between the counter clocks represents the size of the time bin of the TDC. The first counter measures the coarse time and the other three counters sub-divide the clock period by a factor of 4 as shown in Figure 5.6. The division of the counter period is referred as fine timing, which can be achieved also by other techniques.

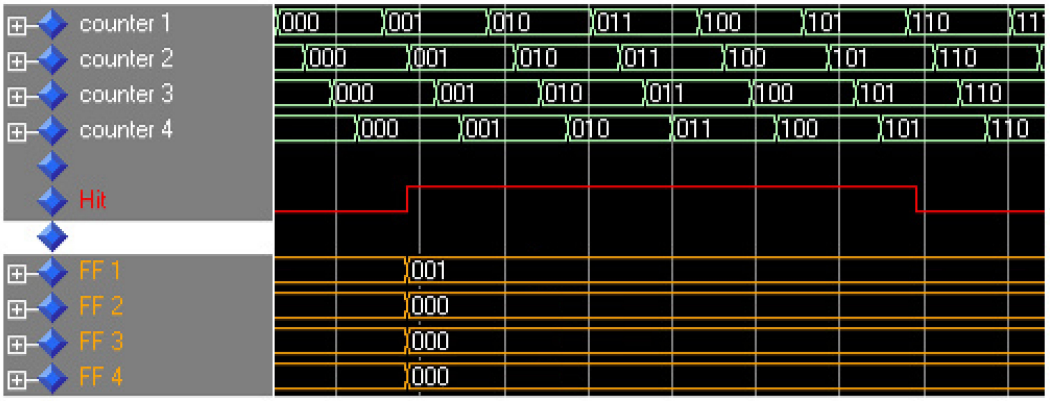


Figure 5.6: Working principle of the fast counter method. To reach a time bin size below the counter period, four counters are used. The counters are running with the same clock frequency and are phase-shifted by 90° with respect to each other. The rising hit signal (red) triggers the latching of the four counter values (green) into the flip-flops (orange). The absolute time of the hit signal can be calculated from these four values.

5.3 Time measurements with the Stratix FPGA

The first FPGA-based TDC for the planned LHCb Outer Tracker upgrade was implemented on a Stratix FPGA[6] development board [59] because no PCB with the chosen Arria GX FPGA was available at the beginning of this study. The largest difference between the two FPGAs is that the Arria GX FPGA provides 3.125 GBit/s transceivers which are foreseen to be used for the readout of the detector data. The Stratix FPGA provides no GBit/s transceivers what makes The fast counter method was selected because with this method no special LVDS inputs are needed, and a clock driven synchronous TDC is possible. In addition, the amount of logic blocks needed is lower than for the tapped-delay line.

Two TDC designs for the Stratix FPGA will be presented in this section, the first design uses four phase-shifted fast counters. It was possible to implement the first working single channel TDC with this straightforward method, but it was not possible to realize a multi channel TDC. This was achieved in the second design using a different layout and spatially hand placed logic elements.

In the following, the technical constraints for the TDC design are given, taking the upgrade of the Outer Tracker readout into account. After this the hardware used for the development and test of the TDC will be presented. Finally, the two firmware implementations of the Stratix designs are shown and their performance are compared.

5.3.1 Technical constraints for the TDC design

The LHCb Outer Tracker drift time is measured with respect to the rising 40 MHz LHC clock. Figure 5.7 shows the waveform for the time measurement. Every first hit in a 25 ns LHC clock period has to be measured for a single TDC channel. Furthermore, a time resolution below 1 ns is required. This can be achieved with an FPGA-based TDC using the fast counter method. Moreover, it should be possible to implement 32 TDC channels on the FPGA, to reduce the amount of FPGAs needed for the readout electronics. In addition, the channel-to-channel variation should be as small as possible without single channel calibration.

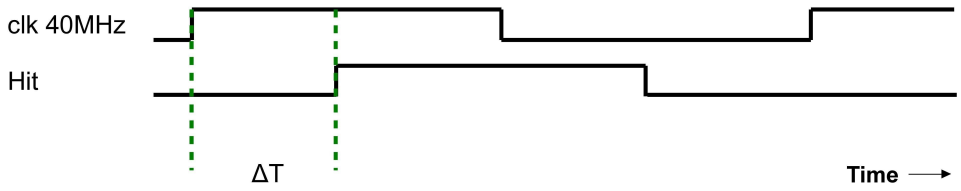


Figure 5.7: Schematic of the drift time measurement (ΔT) with respect to the LHC clock.

[6] EP1S25F1020

5.3.2 Hardware used for the Stratix FPGA-based TDC

At the beginning of the TDC studies, a Stratix development board from Altera was used [59]. The main components of this board are a Stratix FPGA[7], a PCI[8] bus, 256 MByte DDR-SDRAM[9] and flexible clocking with socketed 33 MHz and 100 MHz oscillators. Figure 5.8 shows a picture of the development board. In addition to the development board, a PC with a PCI slot was used. For the communication between the FPGA and the PC, a PCI core inside the firmware of the FPGA was used, and on the PC side, the WinDriver from the company JUNGO for the PCI bus was installed. In the computing language C, routines control the read/write operations from the PC to the PCI registers on the FPGA. Furthermore, several connectors were developed, in order to loop back clock signals from the FPGA back to the FPGA to emulate detector signals. These clock signals can be varied in phase with a NIM delay element[10].

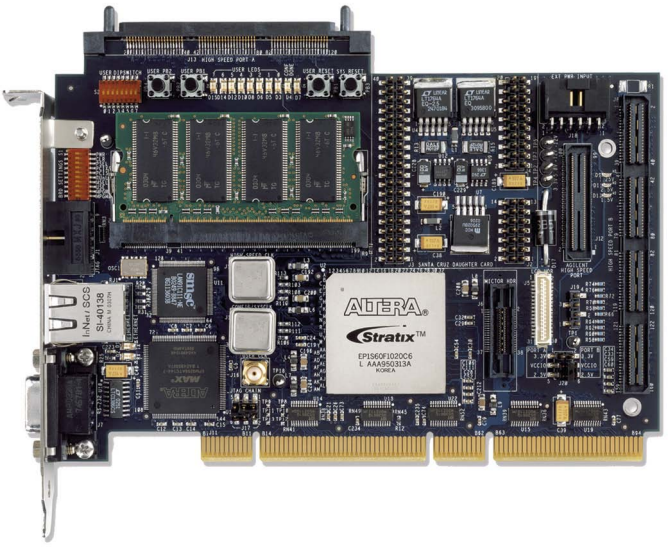


Figure 5.8: Picture of the Stratix development board [59].

5.3.3 First design of the FPGA-based TDC

The following subsection shows the first design of an FPGA-based TDC using the fast counter method, main blocks of the firmware are introduced, including TDC block with encoding, the histogram block, the PCI block and the different

[7] EP1S25F1020C5
[8] Peripheral Component Interconnect
[9] Double data rate synchronous dynamic random-access memory
[10] Delay of 0.5 ns - 63.5 ns in 0.5 ns steps.

control and measurement blocks. Many of them are more general blocks to test the TDC, which were also used by other TDC firmware blocks. Figure 5.9 shows the top level schematic of the first TDC design for the Stratix FPGA. The TDC clocks are generated in a phase-locked loop (PLL). The TDC data are analyzed in two histogram blocks which are read out via a PCI block. The test measurements of the TDC block are controlled via the control block.

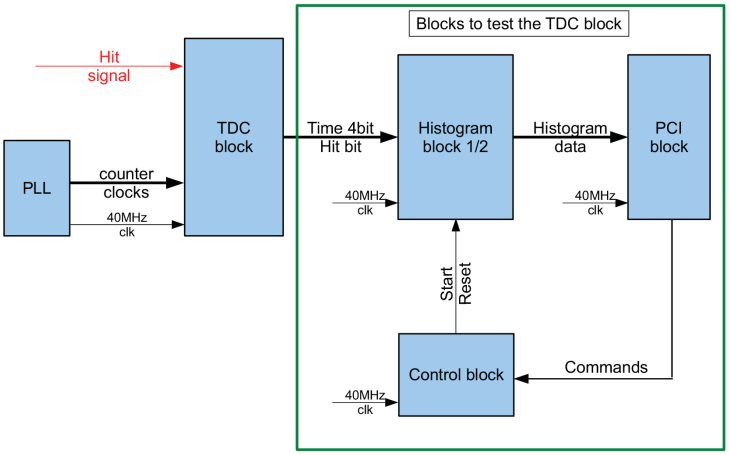


Figure 5.9: Top level schematic of the Stratix FPGA-based TDC.

TDC block

The time measurement is implemented with 4 phase-shifted counters running synchronous to the LHC 40 MHz clock. For a hit the values of all counters are latched and used to determine the point in time inside the 25 ns period. Figure 5.10 shows in a functional diagram how the 4 counters sub-divide the LHC clock cycle. The counter clocks are phase-shifted by 90° to each other.

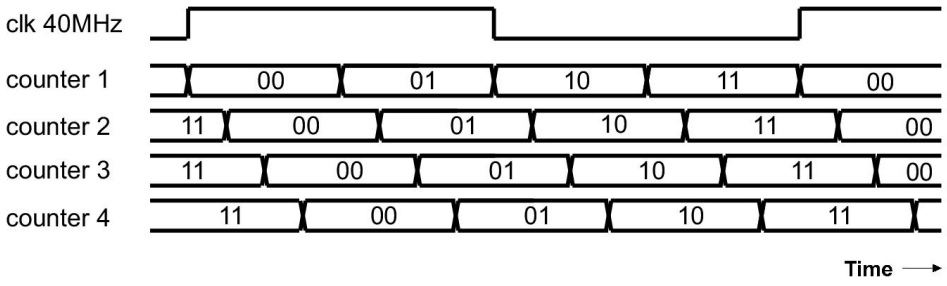


Figure 5.10: Functional diagram of the first TDC design of the Stratix FPGA-based TDC.

	Clk cycle N	Clk cycle N+1	Clk cycle N+2	Clk cycle N+3
TME 1	measuring	encoding	measuring	encoding
TME 2	encoding	measuring	encoding	measuring

Table 5.1: Measurement and encoding scheme of the time measurement elements for the different LHC 40 MHz clock cycles.

The TDC block is built with four 2 bit counters, running at four times the LHC clock (∼160 MHz). See Figure 5.11 for the TDC block schematic. The four counter clocks are generated from the LHC clock by an enhanced Stratix PLL. If the four counter values are fixed for each point in time in the 25 ns LHC clock period an easy time encoding would be possible which correlates to certain counter values always the same point in time in the 25 ns LHC clock period. To achieve this repeating counter value pattern every 25 ns without a counter reset, the number of possible counter values[11] as well as the ratio of counter clock frequency and LHC clock frequency are chosen to be equal.

The counters are connected to two time measurement elements (TME) which are necessary to measure every first hit during an LHC clock period of 25 ns. These time measurement elements measure the time for different LHC clock periods alternately, such that each element has enough time for the time-encoding. The alternating scheme for the measurement and encoding of the time measurement elements for the different LHC 40 MHz clock cycles is shown in Table 5.1. This makes a dead-time free measurement of the first hit in a LHC clock period (bunch crossing Bx) possible.

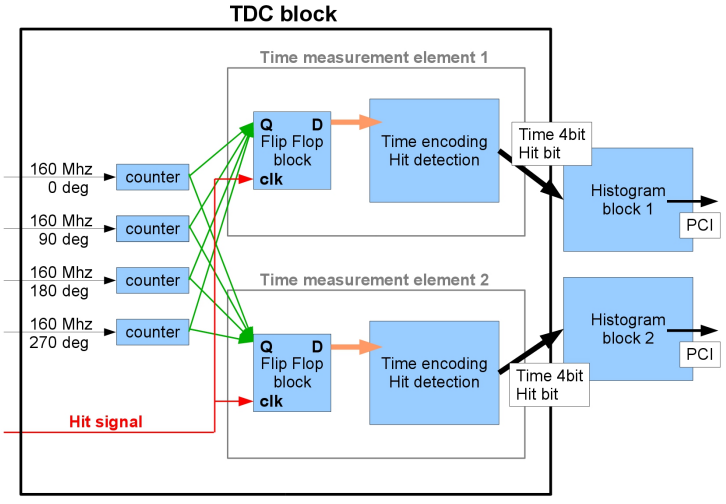


Figure 5.11: Schematic of the TDC block for the first design of the Stratix FPGA-based TDC.

[11] Possible counter values = 2^n, where n is the number of counter bits.

A hit signal triggers the latching of the counter values of the corresponding time measurement element, within the corresponding clock cycle. To avoid setup and hold time violations, the latching signals for the four counters are synchronized to the inverted counter clocks. In addition to the drift time measurement a hit signal triggers the set of a hit register. This hit signal is needed because all 4 bit time values are valid drift times, any possible counter value is a valid time. The hit bit flags valid times. Each time measurement element consists of a flip-flop block for the four counter values and the hit register and its own encoding block.

Encoding block

The outputs of the hit register and counter value flip-flops of a time measurement element are connected to the corresponding encoding block. The time (ΔT) is calculated from the time information in the flip-flops. The counter running with the 320 MHz clock with phase 0 to the 40 MHz reference clock is taken as coarse counter. Furthermore, the coarse counter value is compared to the other three counter values to determine the fine timing inside the coarse count. The procedure is the following: First the latched value of the counter no. 4 is shifted two bits to the left (multiplication with 4) and taken as coarse time value. Second the latched value of counter no. 4 is compared to the other three latched counter values. The result of all the 3 comparisons will be inverted and then added to the coarse time value. Lastly, a constant is subtracted from the time value to set the time value 0 to the beginning of the 25 ns bunch crossing period. The resulting time information has 4 bits. The encoding block is reset after the readout and is ready for the next measurement.

The outputs of the TDC block include 4 bit time information and the corresponding hit bit, both information exist for the two time measurement elements. These lines are connected with following logic blocks which are used to test the TDC design.

Histogram block

The histogram block is used to measure the distribution of the measured times for a TDC channel. Two histogram blocks are included into the TDC firmware. There is one histogram block for each time measurement element of a selectable TDC channel. The histogram block is built with a 4 bit demultiplexer controlling the enable signals of 16 counters (32 bit). For each possible time value exists one counter which counts the number of valid measurements. The measured drift time value controls the demultiplexer which routes the hit signal to the corresponding counter. Their values are saved in PCI bus registers.

PCI block

The PCI bus block is used to control and monitor the firmware. It is only used for the Stratix FPGA. It has two address spaces. One has 1024 words with 32 bit width. All the status, control and measurement registers are placed in this address space. The second address space has a size of 256 MB and is not used for the TDC studies.

Control block

The different measurements are controlled through the PCI command registers. Start and reset commands can be given through these registers to the firmware. The PCI command registers form a single byte which is compared with static bytes corresponding to different actions. If two bytes are equal, the corresponding action is started.

5.3.4 ModelSim simulation of the 4 counter TDC

The TDC firmware was simulated with ModelSim. No timing information was included into this functional simulation. Figure 5.12 shows the simulated waveform of the TDC design. The simulation shows the latching of the counter values after a hit signal, the encoding part is not visible. Three LHC clock cycles (75 ns) are plotted. The 40 MHz clock and the 20 MHz clock are shown in yellow. The counter values are visible in green and running at 160 MHz. The phase-shift between the counter clocks is 90°. The hit signal in this simulation is represented by a 20 MHz clock (red). Whenever the hit signal rises it is synchronized to the inverted counter clocks to avoid the readout of the counters when the count values change. The synchronized signals are used to trigger the latching of the counter values into the corresponding flip-flops (orange). The delay between the hit signal and the change in the flip-flops is caused by the hit signal synchronization.

5.3.5 TDC performance test setups

The general setup for the delay scan and the bin size measurement is shown, which is used to evaluate the performance of the Stratix FPGA-based TDCs.

Setup for the delay scan

One important test of the performance of the TDC is the delay scan, with which the correct function of the encoding block can be verified and the linearity of the TDC channel can be tested. The idea of this measurement is to measure the time for a synchronous hit signal with the TDC. As a synchronous hit signal, the system clock of 20 MHz can be used. The phase of this hit signal can be changed with a delay.

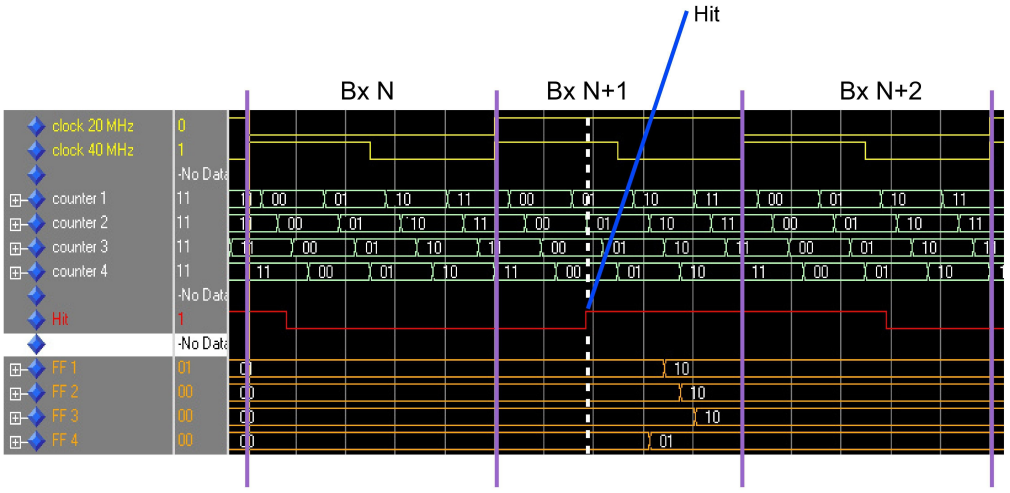


Figure 5.12: ModelSim simulation of the 4 counter TDC. The LHC 40 MHz clock is divided by one counter by four and the other three counters subdivide the counter bin again by four. The point in time within the LHC clock period is defined by the four counter values. Each LHC clock cycle is also referred as bunch crossing Bx.

For the setup, the clock is fed through an SMA[12] connector to a NIM[13] delay box and further to a developed connector board, which was plugged as a mezzanine board to the Stratix development board. It was possible to inject the 20 MHz clock into the corresponding TDC channel pin. The phase-shift of the 20 MHz clock was controlled with the NIM delay element. The step size was 0.5 ns and 128 steps were available. The PCI bus was used to control and readout the measurements. For each delay value the time of 40,000,000 hits is measured.

Setup for the bin size measurement

The time bin size of the TDC can be checked by using a random asynchronous hit signal and counting how often each possible time was measured. The size of the time bins is proportional to how often it was measured.

In the setup a function generator[14] was used to generate a pseudo random hit signal. This is possible, because the function generator and the TDC are using two independent oscillators as reference signal. The resulting hit signal is pseudo random. The function generator was connected to the TDC channel input, and as hit signal a 1.13 MHz clock signal was used. For a time window of 80,000,000 LHC clock cycles, all measured times are written into the two histogram blocks

[12]Coaxial radio frequency connector: SubMiniature version A
[13]Nuclear Instrumentation Module
[14]Hewlett Packard 8116A Pulse/Function Generator 50 MHz

of the two time measurement elements. After this the data in the histograms are read out and analyzed.

The size of each time bin is proportional to the number of hits in this time bin. If the frequency (f_{random}) of the pseudo random hit signal is known, then the bin size (bz) can be calculated using the number of hits in the time bin (n_{hits})

$$bz\,[\text{ns}] = \left(\frac{n_{\text{hits}}}{80,000,000 \cdot 2.5 \cdot 10^{-8}\,\text{s} \cdot f_{\text{random}}\,[\text{Hz}]} \right) \cdot 2 \cdot 25\,\text{ns}. \tag{5.3}$$

To calculate the time bin size the ratio of the number of hits in the time bin and the total number of generated hits is multiplied with the length of one TDC measurement cycle.

5.3.6 Results of the first FPGA-based TDC

The first design with one TDC channel was successfully tested, and the test results will be shown in this subsection.

Delay scan: The delay scan of the TDC channel shows a linear behavior as expected which can be seen in Figure 5.13. The 20 MHz clock was fed through the NIM delay element as described in Subsection 5.3.5. For each data point the mean of 40,000,000 hits was calculated and was plotted against the delay of the NIM delay element. The measurements of the first time measurement element are shown in blue and, the measurements of the second one are shown in red.

To quantify the linearity of the TDC channel the integral nonlinearity (INL) is determined. For this the bin size measurement is used. For each time bin a sum is calculated by adding the bin sizes of all previous time bins. In addition, for each time bin a second sum is calculated by adding the ideal bin size for all previous bins. For each time bin the difference of the two corresponding sums is calculated. The largest difference represents the INL.

The INL for the current TDC of TME 1 is 0.3 bins (0.45 ns) and for TME 2 the INL is 0.2 bins (0.3 ns).

Bin size measurement: The bin size measurement of the first TDC design is shown in Figure 5.14. As hit signal a 1.13 MHz clock from a function generator was used as described in Subsection 5.3.5. The bin size is proportional to the hits in the corresponding bin. An alternating pattern is visible around the expected bin size of 1.6 ns.

To characterize the spread of the bin sizes, usually the differential nonlinearity (DNL) is given which is calculated by adding the maximum bin size difference and the absolute minimum bin size difference. For the bin size difference the bin size of neighboring time bins are compared. This can be expressed with the following formula

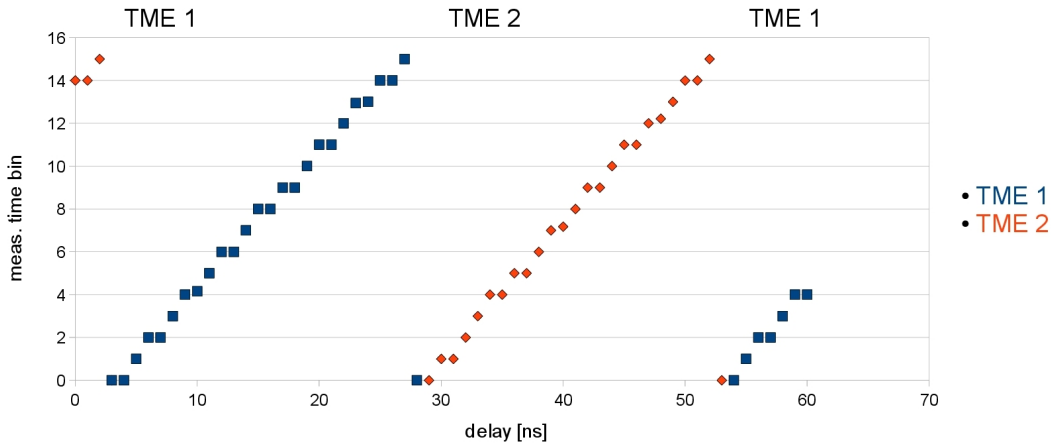


Figure 5.13: Delay scan of the first TDC design.

$$DNL = |max\{\Delta_i\}| + |min\{\Delta_i\}|. \tag{5.4}$$

Δ_i is the bin size difference between bin number i and the neighboring bin number $i-1$. Time bin 1 is compared with time bin 16.

The DNL for the current TDC of TME 1 is 0.5 bins (0.8 ns) and for TME 2 the DNL is 0.6 bins (1 ns).

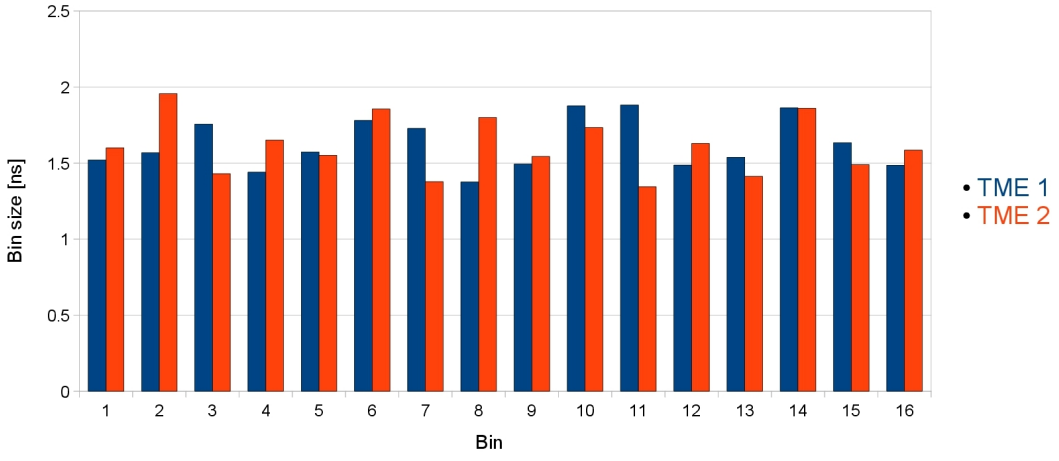


Figure 5.14: Bin size measurement of the first TDC design.

In the following, a summary of the first TDC design is given. The first realized TDC is a 4 bit TDC, with a time bin size of 1.6 ns. The time resolution is in principle good enough for the tracking, nevertheless a 5 bit time information would be desirable.

Furthermore, it was realized during the development that the placement of elements and routing of signals using the compiler software (Quartus II), is not sufficient to realize a multi-channel TDC. The bin sizes of the channels vary strongly and the encoding block for each single TDC channel had to be adjusted individually to have a linear behavior in the delay scan. This problem was solved with the second Stratix TDC design, shown in the next subsection (5.3.7).

5.3.7 FPGA-based TDC with manually placed logic

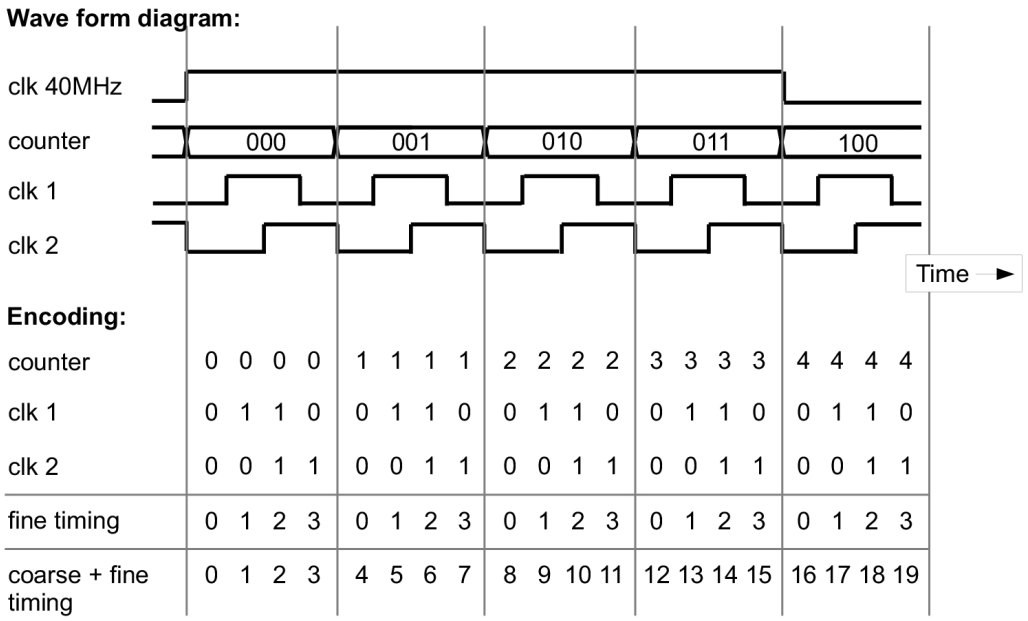
The main difference of the following TDC firmware to the first firmware is the usage of manually placed logic blocks, which is a time consuming task. To make the placement easier, the TDC design was modified to have as little as possible logic in the time critical parts. In addition, the counter frequency was doubled to 320 MHz, so a TDC time bin size of below 1 ns can be reached. First, a reference channel was designed and verified. After this it was possible to move the verified TDC channel to another position on the FPGA, and the resulting channel had largely the same performance as the first channel. Furthermore, it was possible to realize a reliable 16 channel 5 bit TDC with this design. A time bin size of 0.78 ns was reached, a satisfactory size for LHCb Outer Tracker needs.

In the following subsection the second design of an FPGA-based TDC, which also uses the fast counter method, is discussed. The main blocks are the TDC block with encoding, the histogram block, the PCI block and the different control and measurement blocks. Only the new TDC core is shown, all other blocks are identical to the ones of the first design that were already described in Subsection 5.3.3. In addition, the manual placement of the logic elements of the TDC channel is described.

TDC block

The time measurement is implemented with one counter running synchronous to the LHC 40 MHz clock and two additional phase-shifted clocks. All three clock frequencies are 320 MHz. For a hit the value of the counter and the status of the two additional clocks are latched and used to determine the point in time inside the 25 ns period. The top of Figure 5.15 shows in a functional diagram (wave form diagram) how the counter and the two phase-shifted clocks sub-divide the LHC clock cycle. The counter clock and the two additional clocks are phase-shifted by 90° to each other.

Each TDC bock is built with one 3 bit counter, running at 8 times the LHC clock (∼320 MHz). Figure 5.16 shows a block diagram of a single TDC channel. A dead-time free measurement every 25 ns is reached by using two time measurement elements for each TDC channel. Both time measurement elements alternately measure the time to guarantee a proper encoding. The counter clock is generated from the LHC clock with an enhanced Stratix PLL. In addition, two



counter	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3	4	4	4	4
clk 1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
clk 2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
fine timing	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
coarse + fine timing	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

Figure 5.15: Functional diagram (top) and encoding scheme (bottom) for the manually placed TDC design of the Stratix FPGA-based TDC.

320 MHz clocks are generated. The three clocks are phase-shifted by 90° to each other and they are synchronized to the LHC clock. The 3 bit counters subdivide the 25 ns LHC period by a factor of 8. The values of the two additional 320 MHz clocks are used to subdivide each counter period by the factor of 4. Each point in time in the 25 ns period can be identified with a fixed bit pattern of the counter and the clocks.

The hit signal triggers the latching of the counter value and the latching of the actual value of the 2 additional 320 MHz clocks of the flip-flop block in the corresponding time measurement element. To avoid setup and hold time violations during the counter latching, the hit signal is synchronized to the inverted counter clock. In addition to the measured time value the hit signals triggers the setting of a hit bit. Each time measurement element has a single hit register. The outputs of the hit register, the counter flip-flop values and the 320 MHz clock flip-flops are connected to the encoding block.

Encoding block

The drift time (ΔT) is calculated from the time information in the flip-flops. The counter running with the 320 MHz clock is taken as coarse counter. The two flip-flops latching the status of the phase-shifted 320 MHz clocks represent 4

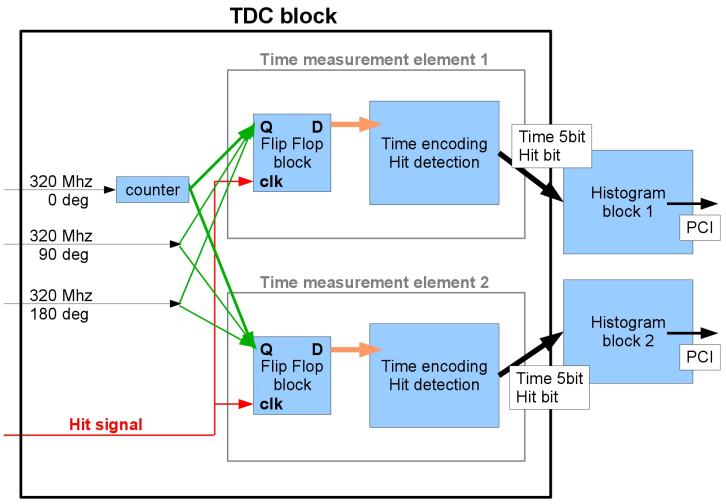


Figure 5.16: Schematic of the TDC block for the second design of the Stratix FPGA-based TDC.

possible values and for each value a fine timing value is defined which is added to the coarse count. The encoding scheme is shown in the bottom of Figure 5.15. The encoding is implemented as follows: The value of the counter is shifted two bits to the left (multiplication by 4) and taken as coarse time value. In addition, the value of the second clock flip-flop is shifted one bit to the left (multiplication by 2) and added to the 5 bit coarse time. Moreover, the two clock flip-flops are compared and the inverted output is added also to the 5 bit TDC time. At the end of the encoding a constant is subtracted from the time value to reach a time value of zero at the beginning of the LHC clock period. The resulting time information has 5 bits. The encoding block is reset after the readout and is ready for the next measurement. For each time measurement element, there exists a single encoding block.

The outputs of the TDC block are the 5 bit time information and the corresponding hit bit, both information exist for the two time measurement elements. These outputs are connected with following logic blocks.

Manually placed TDC reference channel

All the time critical logic blocks were placed manually, using the time information from Quartus II for the signal delays between the different logic elements. These times are not very precise but they show roughly how big the signal delays are on the real chip. This is the reason why it is necessary to validate these numbers with measurements.

During the manual placement, emphasis must be put on equal signal delays for the different logic elements. One of the most important signals is the hit

signal, which triggers the latching of the counter value flip-flops and the clock flip-flops. The placement was chosen to reach a jitter for the hit signal as small as possible at the flip-flop positions. In addition, the delay of the counter outputs to the flip-flops was chosen to be equal for all 3 bits in both time measurement elements. A difficulty is that it is not possible to place all logic elements in a single logic array block, due to input constraints.

After creating one reference channel, this channel was copied to other positions on the FPGA to create more TDC channels. It was achieved to place 16 TDC channels on the left upper corner of the Stratix FPGA. Figure 5.17 shows the chip planner which presents the location of the firmware on the FPGA chip. The chip planner view shows how many logic blocks inside a logic array block are used for the different LAB of the Stratix FPGA. Rectangles with a light blue color are empty, dark blue means that the logic array block is completely occupied. The green rectangles show the RAM blocks and the brown rectangles at the border of the chip are I/O cells. The 16 TDC channels were placed in 16 lines, the time uncritical logic was placed by the Quartus II fitter. 64 channels would also be possible, as there are enough logic blocks available.

Figure 5.18 shows the layout of the reference channel. The TDC channels had to be placed in rows because the input pins for the different TDC channels are placed in neighboring I/O pins. It is not possible to shrink the design more because the amount of reset and clock signals for each logic block array are limited. The difficulty of constructing a reference channel is to place the logic blocks such that the delays between them are equal and in addition to fulfill the filling constraints of each logic array block.

5.3.8 Results of the manually placed FPGA-based TDC

In the following first the functional simulation with ModelSim is shown. Afterwards, the measurements of the real performance are presented.

ModelSim simulation of the one counter TDC design

A simulation of the second TDC design was done with ModelSim. The functional simulation shows a working TDC design. The simulation is shown in Figure 5.19. The latching of the counter value and the latching of the states of the two additional clocks can be seen. The encoding is not shown.

The second design was tested successfully with 16 TDC channels, and the results will be shown in this subsection. The behavior of the 16 channels is uniform, all channels have a good linearity and the bin size distribution is equal within 100 ps. It is possible to use the same type of encoding block for all the different channels.

Delay scan: The delay scan of the 16 TDC channels shows a linear behav-

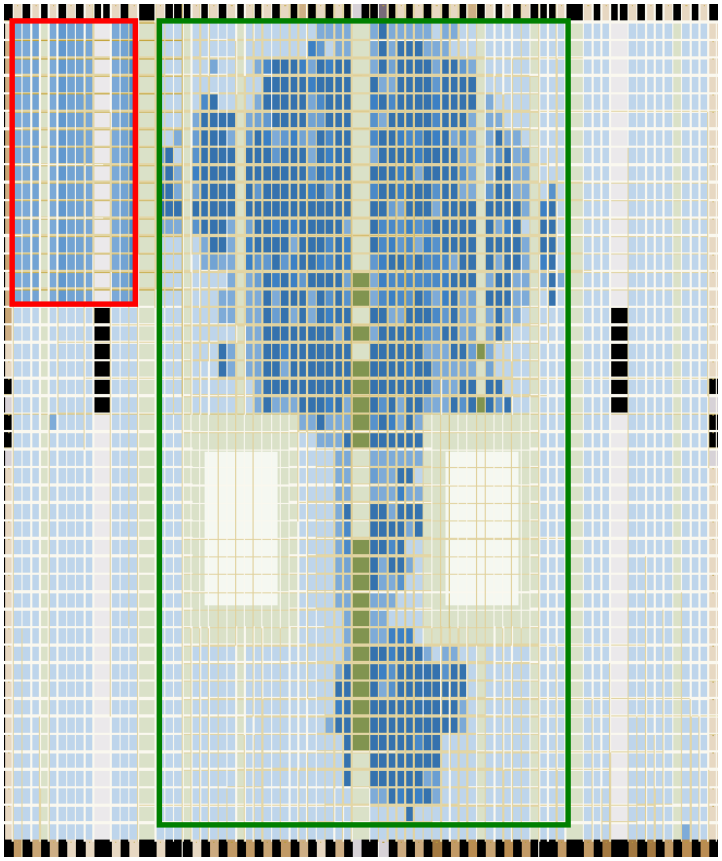


Figure 5.17: Chip planner view of the Stratix chip for the 16 channel 5 bit TDC. The time criticial logic elements of the 16 TDC channels are placed in the red frame and the time uncritical logic blocks, placed by the Quartus II fitter, are shown in the green frame. The TDC channels are placed in rows.

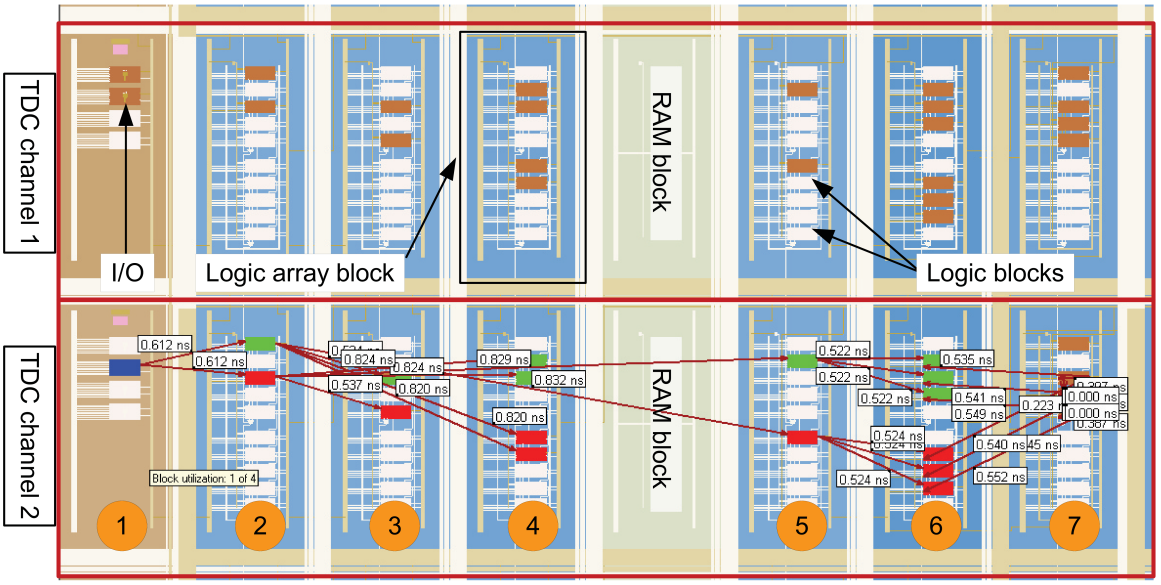


Figure 5.18: Reference channel layout. Two TDC channels are shown arranged in two FPGA rows. The visible part of the TDC channels does not include the encoding blocks, which are located for each TDC channel further to the right in the row. In the firmware used logic blocks are colored brown and not used ones are white. For TDC channel 2 the logic blocks are colored in green for TME 1 and red for TME 2. In addition, the I/O pin is colored blue. The distribution of the hit signal in TDC channel 2 is shown with red arrows including labels with the expected signal delays between the logic blocks. The hit signals enters the chip at position 1. and is distributed to two logic blocks at position 2. used to select the hit signal for the corresponding even or odd LHC clock cycle. From this location the signal is distributed further to the corresponding hit flip-flop at position 3., the two flip-flops latching the status of the two phase-shifted clocks clk 1 and clk 2 at position 4. and to position 5. where the hit signal is synchronized to the inverted counter clock. The synchronized hit signal triggers the flip-flops at position 6. to latch the status of the counter at position 7.

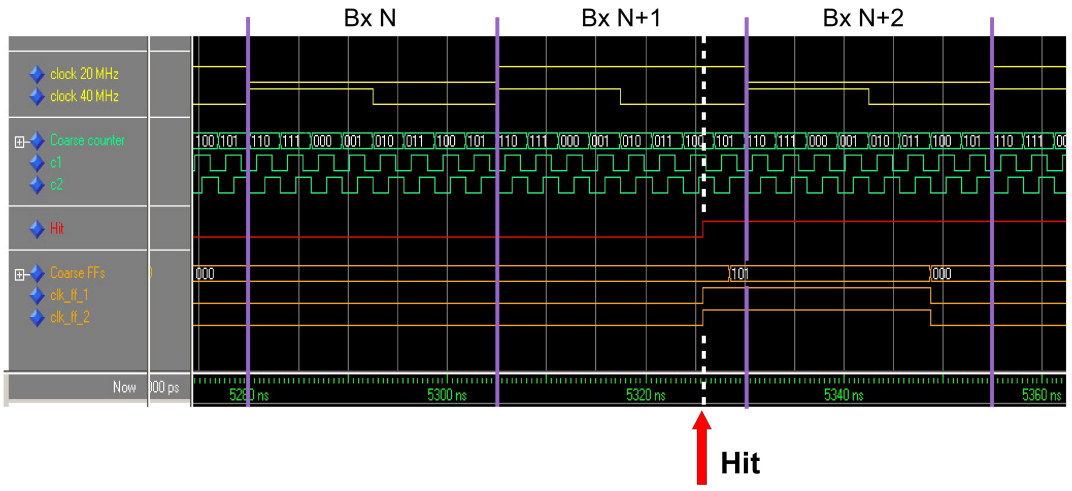


Figure 5.19: ModelSim simulation of the second TDC design. The simulations shows the time period of 3 LHC clock cycles respectively 75 ns. The 40 MHz clock and the 20 MHz clock are shown in yellow. The counter values and the additional two 320 MHz clocks are visible in green. The phase-shift between the 320 MHz clocks is 90°. The hit signal in this simulation is represented by a 20 MHz clock (red). Whenever the hit signal rises the first time during an LHC clock cycle, the hit signal is synchronized to the inverted counter clock to avoid setup and hold time violations. This signal is used to trigger the latching of the counter value into the corresponding three flip-flops (orange). The delay between the hit signal and the change in the flip-flops of the counter is caused by the hit signal synchronization. The latching of the 320 MHz clocks are not synchronized and so not delayed to the hit signal.

ior. Figure 5.20 shows the results for channel 15 as example. The 20 MHz clock was fed through the NIM delay element as described in 5.3.5. For each data point the mean of 40,000,000 hits was calculated and this value is plotted against the delay of the NIM delay element. The measurements of the first time measurement element are shown in blue and the measurements of the second one are shown in red. The linearity is good with a INL of 0.06 bins (0.05 ns) for both TMEs. The result is much smaller as for the 4 counter TDC which was placed by the Quartus II fitter.

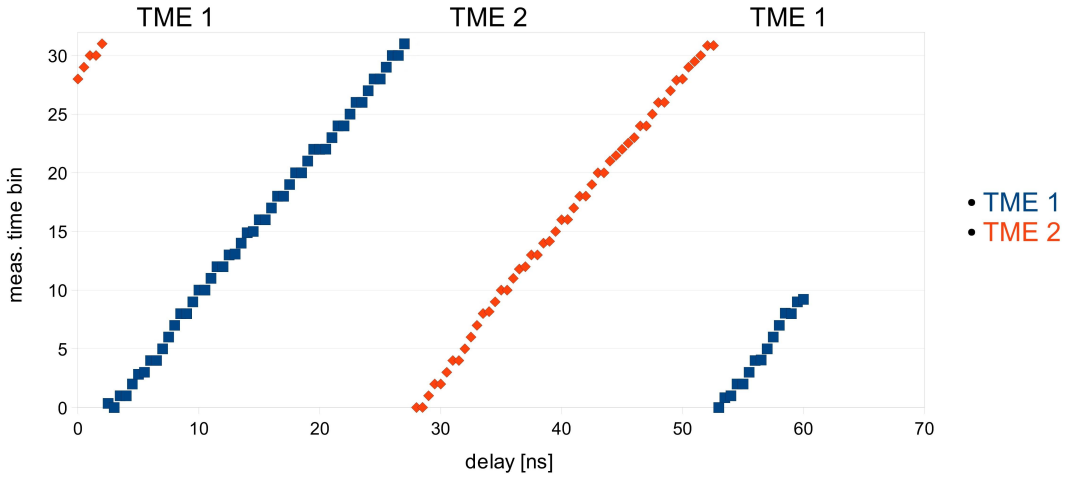


Figure 5.20: Delay scan channel 15 of the manually placed TDC design for the Stratix FPGA.

Bin size measurement: The bin size measurement for the TDC channel 15 is shown in Figure 5.21. As hit signal, a 1.13 MHz clock from a function generator was used as described in Section 5.3.5. The bin size is proportional to the hits in the corresponding bin. An alternating pattern is visible from the large and small bins. This pattern is caused by the real phase-shift of the two additional 320 MHz clocks at the flip-flop inputs which is not exactly 90 °. The DNL for the TDC channel 15 TME 1 is 0.19 bins (0.15 ns) and for TME 2 0.22 bins (0.17 ns). This is much smaller than the DNL of the first TDC design. The manually placed TDC channels have a better performance than the TDC channel placed by the Quartus II fitter. The maximum difference for the bin sizes of all 16 channels is 200 ps. Figure 5.22 shows the bin sizes of the 16 TDC channels. The DNL for the 32 TME variates between 0.17 bins (0.13 ns) and 0.35 bins (0.27 ns). The bin size variation for different TDC channels of all 16 TDC channels is only 100 ps.

5.3.9 Summary for the Stratix FPGA results

The results of the second TDC design show, that a multi-channel TDC with a time resolution below 1 ns can be implemented on an FPGA, using the fast

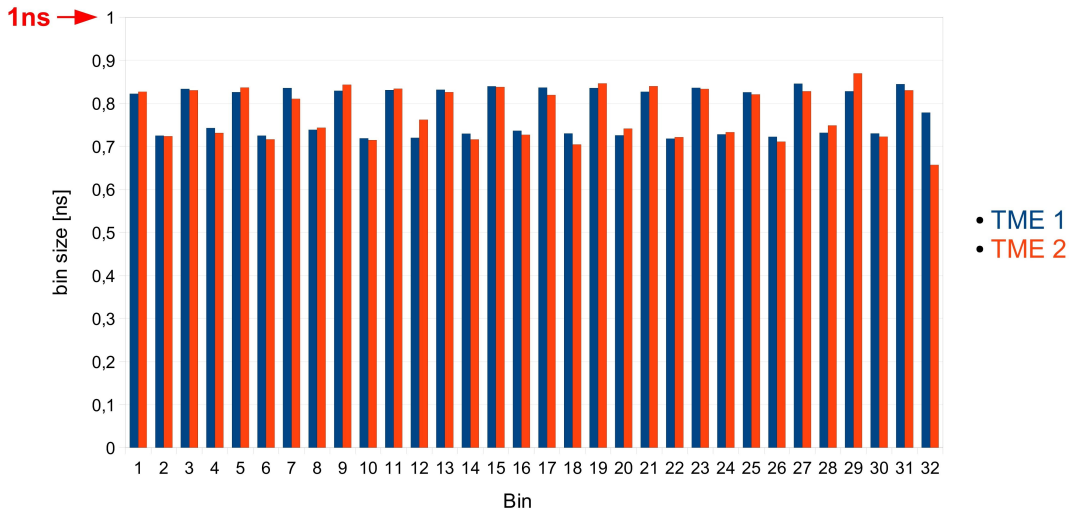


Figure 5.21: Bin size measurement for channel 15 of the manually placed TDC design for the Stratix FPGA.

counter method and manually placed logic elements. The Quartus II fitter can not achieve the same result, including only timing constraints for the different TDC channels. When a reference channel with manually placed logic elements works properly, it is possible to implement a multi-channel TDC by copying the single TDC channel design to different positions on the chip.

5.4 Time measurements with the Arria GX FPGA

The Stratix FPGA used before has no GBit/s transceivers what makes this FPGA not suitable for the LHCb Outer Tracker readout electronics upgrade. The Arria GX FPGA family provides already 3.125 GBit/s transceivers and are not as expansive as the modern Stratix FPGA families which also have GBit/s transceivers. The Arria GX FPGA (EP1AGX35DF780I6) was selected for the development of a prototype board for the LHCb Outer Tracker upgrade. In addition, a TDC design for this FPGA had to be developed which was done during this thesis and is described in the following.

First the first Arria GX TDC design including the different tools and firmware blocks used for the TDC tests are shown. The performance of this TDC was measured and had to be optimized as will be described in the following subsections. Also a C-script developed during this thesis will be introduced which was very useful for the TDC implementation. Finally, the results of the optimized Arria GX TDC are shown, including the investigation of FPGA-to-FPGA variations.

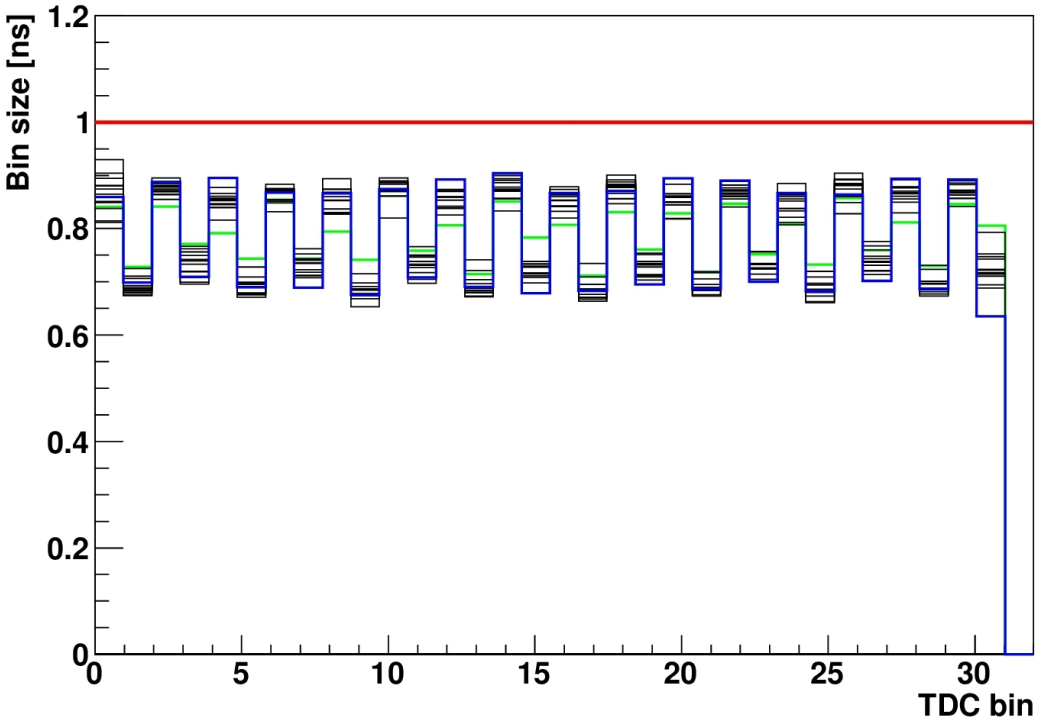


Figure 5.22: Bin size measurement of all 16 channels of the manually placed TDC design for the Stratix FPGA. For each time bin, the bin size of all 32 time measurement elements are plotted. The time measurement element marked with blue has the largest bin size differences and the time measurement element marked with green has the smallest bin size variations.

5.4.1 First TDC design for the Arria GX TDC

For the first Arria GX TDC, the second TDC design of the Stratix FPGA was used as starting point which is described in Subsection 5.3.7. This TDC design is based on the fast counter method. An overview of the firmware gives the top layer schematic of the design in Figure 5.23. The only difference to the Stratix FPGA design is the communication bus block. In the Arria GX TDC an I^2C bus is used, while in the Stratix FPGA a PCI bus was used. For the TDC channel layout it was taken into account that the architecture of the logic elements of the Stratix FPGA and the Arria GX design differ. Furthermore the speed grade of the Stratix, which is five, is faster than the one of the Arria GX FPGA, which is six. The speedgrade quote the delay in nanoseconds through a macrocell in the device [60]. Also the different position of the TDC input pins had to be considered.

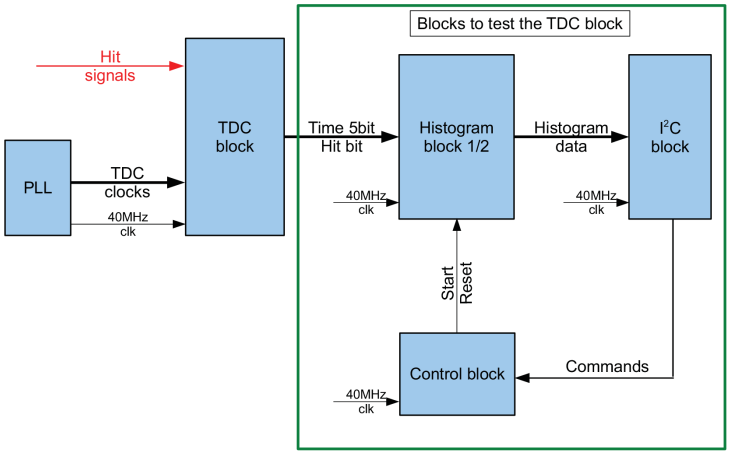


Figure 5.23: Top level schematic of the Arria GX FPGA-based TDC.

These differences made it necessary to change the TDC reference channel layout. The manually placed logic elements were placed anew for the reference channel and a multi channel TDC was realized. The placements and timing constraints were controlled with the TDC channel setter script, which was also developed during this thesis.

The following subsection describes the TDC channel setter script and the I^2C block.

TDC channel setter

During the Arria GX TDC development, more and more placement and timing constraints were included to the design. Changing them developed into a more

and more time consuming task. Including only a single new TDC channel in the FPGA design took more than 30 minutes. Typically around 72 constraints per TDC channel have to be set, most of them are the location assignment, which strongly depends on each other. In order to accelerate the constraint process, a C-script has been written that modify the placement and timing constraints. The C-script accesses all the constraints in two ASCII files: The Quartus Settings File and the Synopsys Design Constraint file, which will be be described in the following.

Quartus Settings File (QSF)
The QSF file controls the pin assignments and location assignments [61]. These assignments are used to tell the Quartus II fitter which I/O is connected to which pin or which register from the design should be placed in which logic element. For a single TDC channel it is necessary to control the location of all logic elements of the time critical parts of the design. For the Arria GX TDC design, 60 location assignments per channel are used. Furthermore, it is possible to constrain clock signals to use the global clock network which reduces the clock arrival skew.

Synopsys Design Constraint file (SDC)
The SDC file is used to specify the design timing and area constraints of the design [62]. This file is used by the TimeQuest tool from Altera, which is a powerful timing analysis tool that validates the timing performance of the logic in a design. The TimeQuest tool checks and optimizes the timing for the final routing of the design. This file was modified for the optimized Arria GX TDC design. It is used to constrain the maximum and minimum signal delays.

TDC channel setter "TDC_Channel_setter_V3.C" is a C-script developed as part of this thesis, which sets all the location assignments and the constraints of the maximum and minimum signal delays for a specific TDC channel in the corresponding files. This is useful if you have to shift several TDC channels to a different position on the FPGA, or if you want to include/exclude more TDC channels. Figure 5.24 shows the visualization of the Arria GX TDC in the Altera Chip Planner. The 32 dark blue surrounded rectangles inside the red rectangle on the top of the FPGA show the position of the 32 TDC channels, which were placed with the TDC channel setter. All the logic inside the green rectangle on the bottom of the FPGA are placed by the Quartus II fitter, as they are not time critical.

In addition to the TDC channel constraint settings, the TDC channel setter can read a file of the bin size measurements and calculates the new maximum and minimum signal delays constraints for the SDC file. This feature was used to optimize the Arria GX TDC design see Section 5.4.5.

During the development of the optimized Arria GX TDC, it appeared that every single TDC channel time measurement element needs its own timing con-

straints. An automatic procedure to modify the timing constraints using measurements became useful. The optimization process for the TDC is very fast using the TDC channel setter.

The work flow for the optimization of a single front-end is the following: First, the TDC channels are only placed with the TDC channel setter on the chip using the standard timing constraints. After this, the design is generated with Quartus II. Second, the FPGA is programmed and the bin sizes of all channels are measured. Finally, the TDC channel setter optimizes the SDC file timing constraints respecting the measurements and the design is generated with Quartus II again. Without this C-script it would not be possible to optimize the Arria GX TDC so fast.

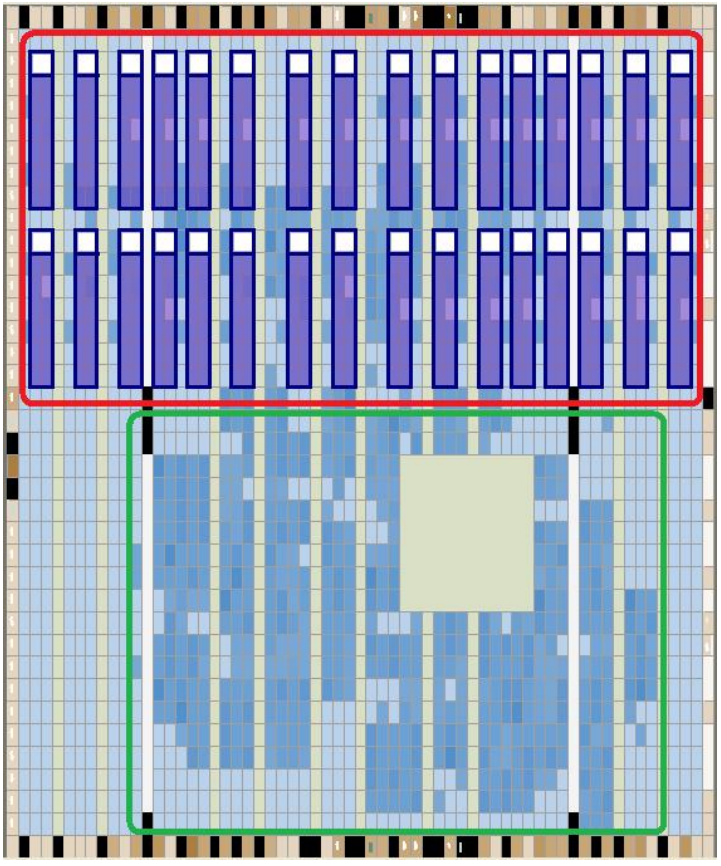


Figure 5.24: Chip planner of the Arria GX TDC design. The 32 dark blue rectangles in the red box represent the 32 manually placed TDC channels. The logic blocks in the green box are placed by the Quartus II fitter, these blocks are not time critical.

I²C block

For the communication with the Arria GX FPGA, an I²C bus was used, which was connected with a USB-to-Serial bridge[15] to a USB port. The USB-to-Serial bridge used, has the capability to establish serial data transfer interfaces like I²C. The I²C bandwidth of 400 kb/s is high enough to control the FPGA and to read out the data in the histograms and counters that were already analyzed on the FPGA.

The FPGA firmware uses an I²C block written in Verilog. On the PC side, a C-program was developed using the libraries from the FTDI company to control the measurements. This program was developed during this thesis.

5.4.2 TDC performance test setups

The general setups for the delay scan and the bin size measurement, which are used to evaluate the performance of the Arria GX TDCs, are shown.

Setup for the delay scan

During the development of the Arria GX TDC, a method similar to the measurements described in the Chapter 5.3.5 was used to perform the delay scan. The 20 MHz clock was routed to a LEMO port on the top of the test board, where it was connected to an adapter for the sensor connector to inject the 20 MHz clock as hit signal to the different TDC channels. Again the NIM delay element was used between the LEMO port and the adapter to change the delay. For each measurement point 40,000,000 consecutive hits were measured.

Automatic delay scan: At the end of the TDC development, a 160 MHz function generator from Rigol[16] was used to perform the delay scan. The delay was changed from the measurement program itself via USB/Ethernet. The function generator and the FPGA were synchronized. The new test setup made it possible to measure the delay scan with 100 ps steps. The I²C script for the control and measurements was modified to control also the Rigol function generator[17]. The second method also measured 40,000,000 consecutive hits from a synchronous 20 MHz signal for each measurement point. This automatic method is much faster than the old method and it is possible to measure many channels over night automatically.

The delay precision of the Rigol function generator was checked with a 1 GHz (5 GS/s) oscilloscope[18], measuring the phase difference of the function generator

[15] UM232H development board from FTDI

[16] DG4162

[17] VISA libraries from National Instruments and general Standard Commands for Programmable Instrument (SCIP) commands

[18] Tektronix oscilloscope DP4104B

channel 1 and the function generator channel 2 at the oscilloscope. A 20 MHz clock with 50/50 duty cycle was used and the step size was 0.5° (69 ps). For each step 100 measuring points were taken. The linearity is perfectly fine for the delay scans.

Setup for the bin size measurement

The bin size measurement used the Hewlett Packard generator or the Rigol function generator with the sensor connector adapter. As hit signal, an asynchronous 1.13 MHz signal was used, see Section 5.3.5.

5.4.3 Results of the first Arria GX FPGA-based TDC

The first results used the same TDC design as the Stratix multi-channel TDC, but with a modified manually placed time measurement element. The modifications were mostly due to the different logic array block architecture in the Arria GX FPGA. Again the signals delays were matched for the different logic element outputs to have the same delay to the following logic element.

First results

The first test was a delay scan of the single TDC channels. Figure 5.25 shows a delay scan of the first Arria GX TDC design channel 9. This channel 9 is representative for all other 32 channels. It is visible that the measured drift time jumps back always after ∼3 ns by three TDC bins. This behavior can be explained by a wrong phase-shift of the 180° 320 MHz clock which is explained in Figure 5.26. The schematic shows in black the ideal situation for the fast counter and the two clocks. The encoding shows a linear behavior as needed. In red, the actual situation for the Arria GX TDC is depicted. In this situation, the phase-shift of the second clock is not exactly 180°. Now the encoding can not distinguish between the beginning and the end of the coarse count with the fine timing information. The result is that always after 3.125 ns (one coarse count step) there is a jump back of three. This is exactly what we can see in the previously described delay scan in Figure 5.25. This behavior was not seen for the Stratix FPGA. As the timing on the Arria GX TDC can not guarantee the perfect phase-shift of 180°, it is necessary to include additional time information into the fine timing to disentangle the beginning and the end of a coarse count. The following subsection describes how this was realized.

5.4.4 Solution for the non-linearity of the first Arria GX TDC

The TDC design had to be optimized because of the non-linearity of the first Arria GX TDC in delay scans. The problem is that for the encoding scheme used

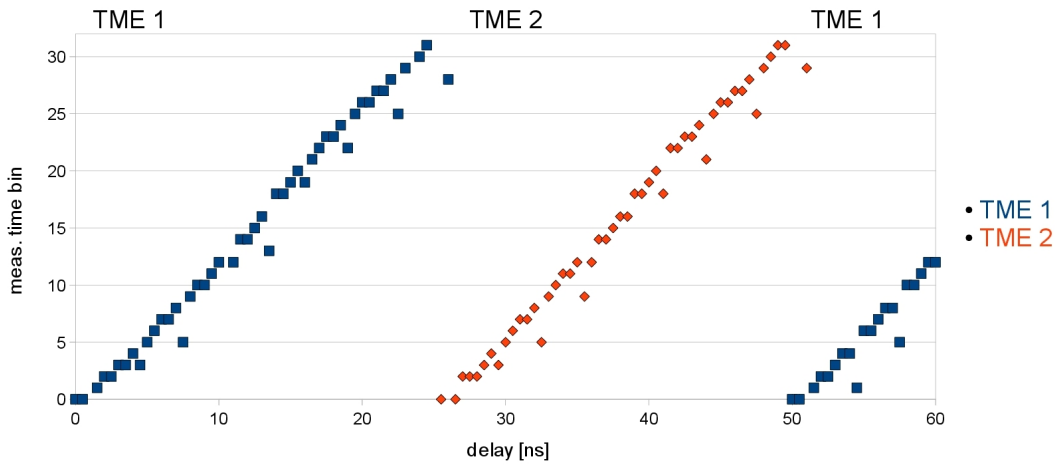


Figure 5.25: Delay scan of the first Arria GX TDC channel 9. A problem with the time encoding is visible once per coarse count (3.125 ns).

so far it was assumed that clock 2 the inverted 320 MHz clock has a phase-shift of 180° what is not correct for the design. The result is that the encoding scheme can not disentangle the beginning and ending of a coarse count. To do this a more redundant time information has to be latched for each hit.

To achieve a more redundant time information, it was decided to add two registers to the fine timing, which measure also the status of counter bit 0. One more early than the normal counter bit 0 flip-flop and one later than the normal counter bit 0 flip-flop. Figure 5.27 shows how these two registers are arranged around the normal counter bit 0 flip-flop. The signal path difference for the hit signal to the three flip-flops makes it possible to check if counter bit 0 changed during the time window, which is defined by the signal path difference of the hit signal (ΔT_2). When the time window is larger than the shift of clock 2, it is possible to disentangle the beginning and end of a coarse count with a modified encoding scheme described in the following. The values of the three flip-flops represent the state of counter bit 0 over time. Flip-flop 3 shows the state of counter bit 0 later in time than flip-flop 2 and flip-flop 2 shows the state of counter bit 0 later in time than flip-flop 1. The three flip-flops show a sequence of the counter bit 0. If counter bit 0 changed during the sequence the point in time is around the end or beginning of a coarse count. If flip-flop 2 is equal to flip-flop 1 the point in time is still at the end of the coarse count. Then the fine timing is set to 3. The other opportunity is that flip-flop 2 is equal to flip-flop 3. Then the point in time is already at the beginning of the coarse count and the fine timing is set to 0. Table 5.2 shows the modified encoding scheme. The drawback of this solution is, that the bin size of the fine time bin 0 and 3 are related to the signal path delays of the hit signal. These delays can be controlled

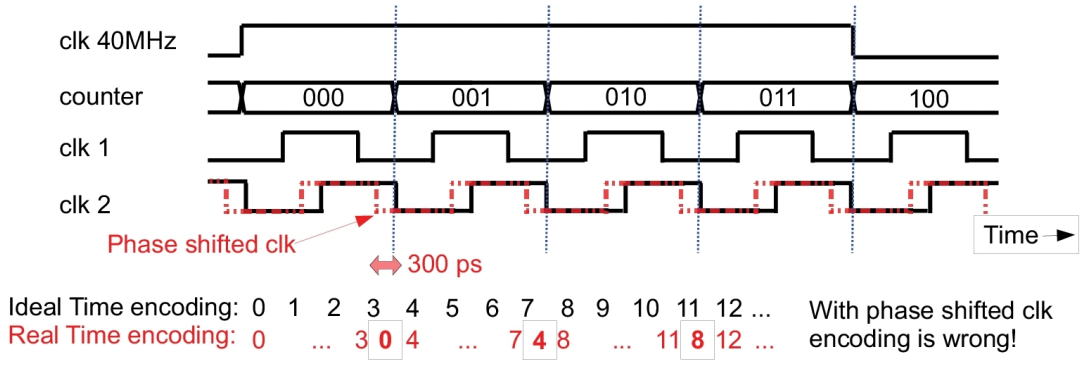


Figure 5.26: Signal diagram of the first Arria GX TDC. A wrong phase-shift of clock 2 can explain the results of the delay scan shown in Figure 5.25.

via the SDC file with maximum and minimum delay constraints for the hit signal to the three flip-flops.

The second optimization was the measurement of the bin size distribution for every TDC channel and to use these with the TDC channel setter to optimize the maximum and minimum delay assignments for each of the 64 time measurement elements of the 32 TDC channels.

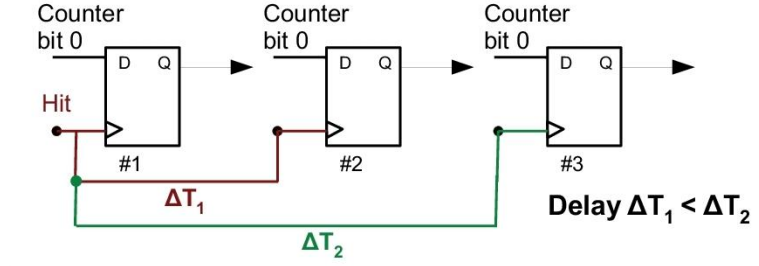


Figure 5.27: Schematic for the fine timing with 3 flip-flops latching counter bit 0. Flip-flop 1 latches counter bit 0 more early than the normal counter bit 0 flip-flop 2. Flip-flop 3 latches counter bit 0 later than the normal counter bit 0 flip-flop 2. The signal delay ΔT_2 defines the time window which has to be larger than the wrong phase shift of clock 2 to disentangle the beginning and the end of the coarse count. ΔT_2 is set to 800 ps.

5.4.5 Results of the modified Arria GX FPGA-based TDC

The delay scan for channel 9 after the modification is seen in Figure 5.28. It shows a linear dependency similar to the TDC on the Stratix FPGA. The jumps

Value of flip-flop 1	Value of flip-flop 2	Value of flip-flop 3	Used fine timing
1	1	0	3
0	0	1	3
1	0	0	0
0	1	1	0
All other possibilities			Fine timing with normal encoding

Table 5.2: Encoding scheme for the modified fine timing.

every 3.125 ns are not visible anymore. This result is also representative for the other 31 TDC channels. The INL for all TMEs varies between 0.3 bins (0.21 ns) and 0.7 bins (0.53 ns). The bin sizes are smaller than 1 ns for the most TDC time measurement elements, but for some TDC channels the bin sizes are larger than the required 1 ns. Figure 5.29 shows the bin size for all 64 time measurement elements of the modified Arria GX TDC. The DNL vary for the 64 TME between 0.2 bins (0.15 ns) and 0.9 bins (0.7 ns). This is worse than the result for the TDC design on the Stratix FPGA. The DNL of the Stratix FPGA-based TDC for the 32 TME variates between 0.17 bins (0.13 ns) and 0.35 bins (0.27 ns). The bin size variation for different TDC channels of all 16 TDC channels is only 100 ps. .

As already mentioned, it is necessary to optimize the delay constants with the TDC channel setter using the bin size measurements. This is shown in the following.

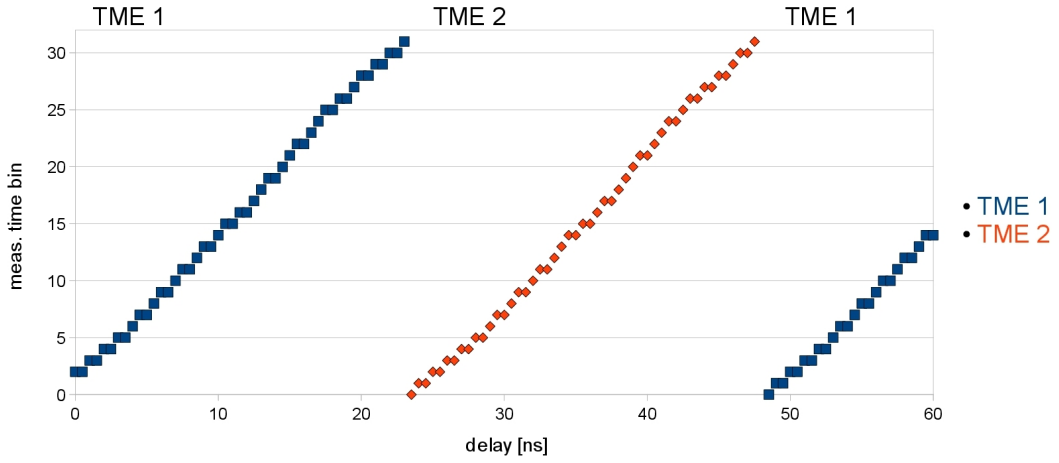


Figure 5.28: Delay scan of the modified Arria GX TDC channel 9.

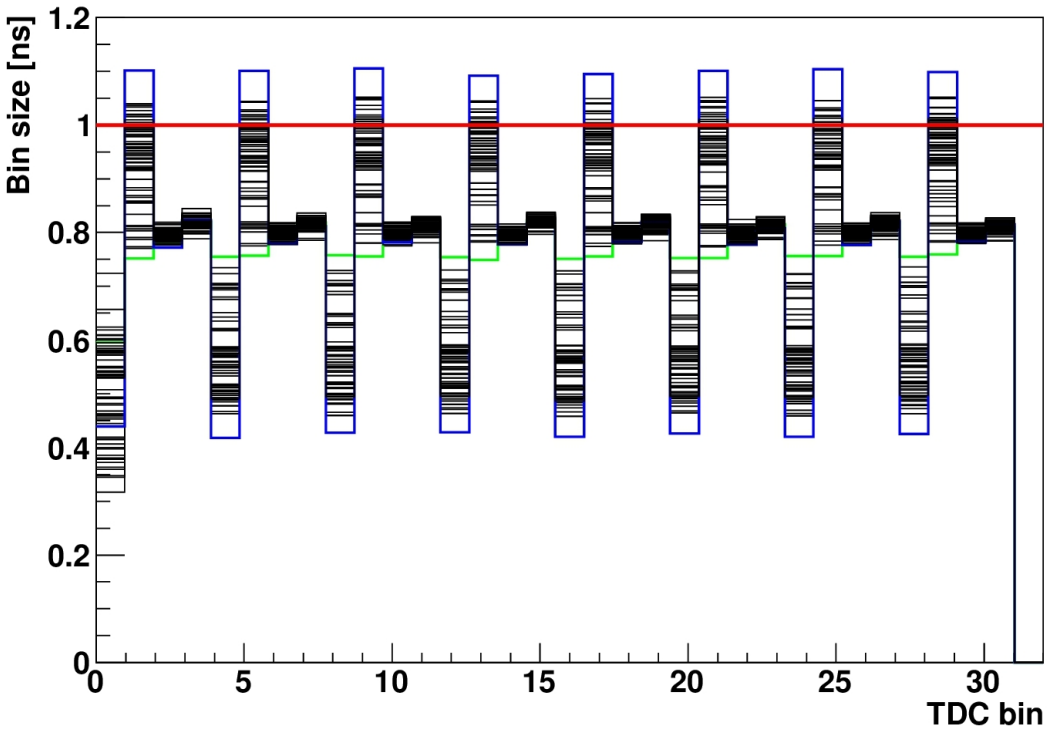


Figure 5.29: Bin size measurement of all 32 channels first optimized Arria GX TDC design. For each time bin the bin size of all 64 time measurement elements are plotted. The time measurement element marked with blue has the largest bin size difference and the time measurement element marked with green has the smallest bin size variation.

Using the TDC channel setter to optimize the timing constraints

The TDC channel setter constrains the hit signal delay to the three flip-flops, which latch the counter bit 0. The latching of counter bit 0 is shown in Figure 5.27. Minimum and maximum delay constraints are used to construct a 50 ps time window for the hit signal to the flip-flops. The constraints for flip-flop one and three are fixed and span a window of 800 ps, which guarantees a linear behavior of the TDC channels. The constraints for the second flip-flop are set in the standard version to the center of the time window, which is later optimized, using bin size measurements of the TDC channel TMEs.

Figure 5.30 shows the bin size distribution of the TDC channel 31 with the standard delay constraints. Both TME of the TDC channel show the same bin size structure, which recur every fourth time bin. This represents the division of the coarse counter. The first time bin is a small bin with a size of roughly 550 ps. This bin is related to the size of the forth bin through the encoding of the additional time information in the three flip-flops for the counter bit 0. The

second and third time bin have roughly the theoretical bin size of 781 ps.

For Figure 5.31, the size of the forth bin TME 2 was taken and compared to the theoretical bin size (781 ps). The difference of these two values was now added to the delay constraints of the second flip-flop for the fine time information from the counter bit 0. The result shows a larger bin 4 for the TME 2 and a bin 1 with the ideal bin size.

The Figure 5.32 shows the result with the delay constraints optimized for both TMEs. The bin size distribution is more balanced for both TMEs. It is not possible to optimize all TDC channel at the same time because the available routing is not free as for an ASIC. It is only possible to use the already existing routing resources. But it is possible to reach a satisfying bin size distribution for all TDC TMEs.

The result is shown in Figure 5.33, all TDC time bins are below 1 ns. The DNL vary for the 64 TME between 0.1 bins (0.08 ns) and 0.6 bins (0.5 ns). The INL vary for all 64 TME between 0.04 bins (0.03 ns) and 0.6 bins (0.43 ns). The changes of the TDC fine timing bin 0 and 3 depend on each other, when the one bin gets larger by a certain amount the other bin gets smaller by the same amount. It is also visible if two neighboring time bins are combined to a single time bin which results in a 4 bit time information. The distribution of the large and small bins for the 4 bit time bins spread over a much smaller time range from channel to channel as for the 5 bit TDC. This can be seen in Figure 5.36.

The TDC linearity has not changed with the delay optimization step, which was tested with an additional delay scan using the new function generator method with 0.1 ns step size. Figure 5.34 shows the result of the delay scan for channel 10, which shows a linear behavior as before.

FPGA to FPGA TDC variations.

The variation of the TDC design between different FPGA test boards was tested, using four completely identical test boards and measuring the bin sizes of the same TDC channel. In Figure 5.35, the bin sizes of the TDC channel 6 of four FPGA test boards with the corresponding 2 time measuring elements is shown. Each FPGA used the same firmware and by that the same delay constants for the second fine timing flip-flop of clock 2.

The TDC bin variation from FPGA to FPGA is up to 200 ps and small compared to the channel to channel variation. This means that the same firmware can be used for all front-ends.

5.4.6 Summary of the Arria GX TDC results

At the beginning of the development of the Arria GX TDC, the successful design of the Stratix FPGA was used to implement a 32 channel 5 bit TDC. To this end, the hand placed logic elements had to be rearranged because the architecture of

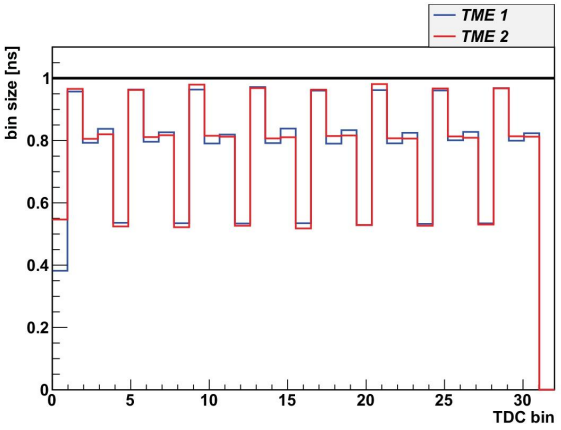


Figure 5.30: Bin sizes of TDC channel 31 with standard delay settings.

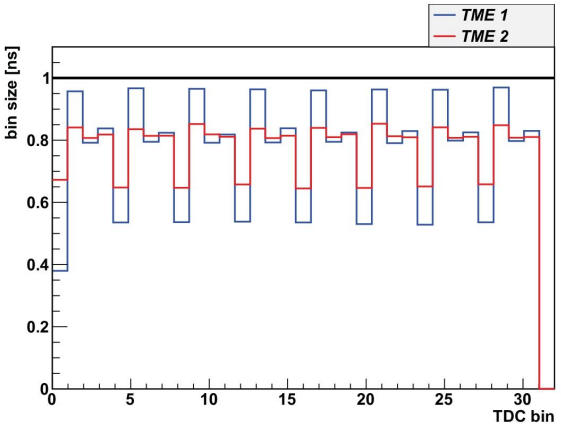


Figure 5.31: Bin sizes of TDC channel 31 with optimized delays of TME 2.

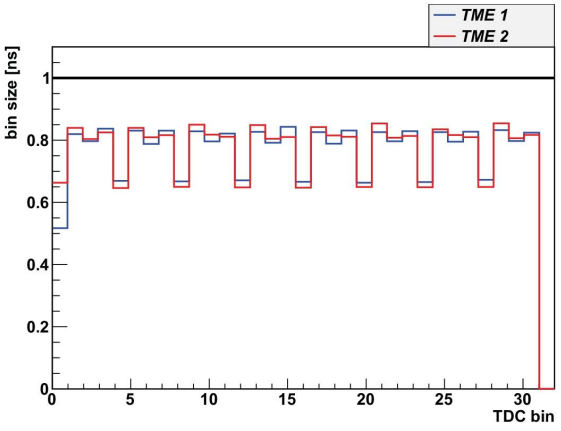


Figure 5.32: Bin sizes of TDC channel 31 with optimized delays of both TMEs.

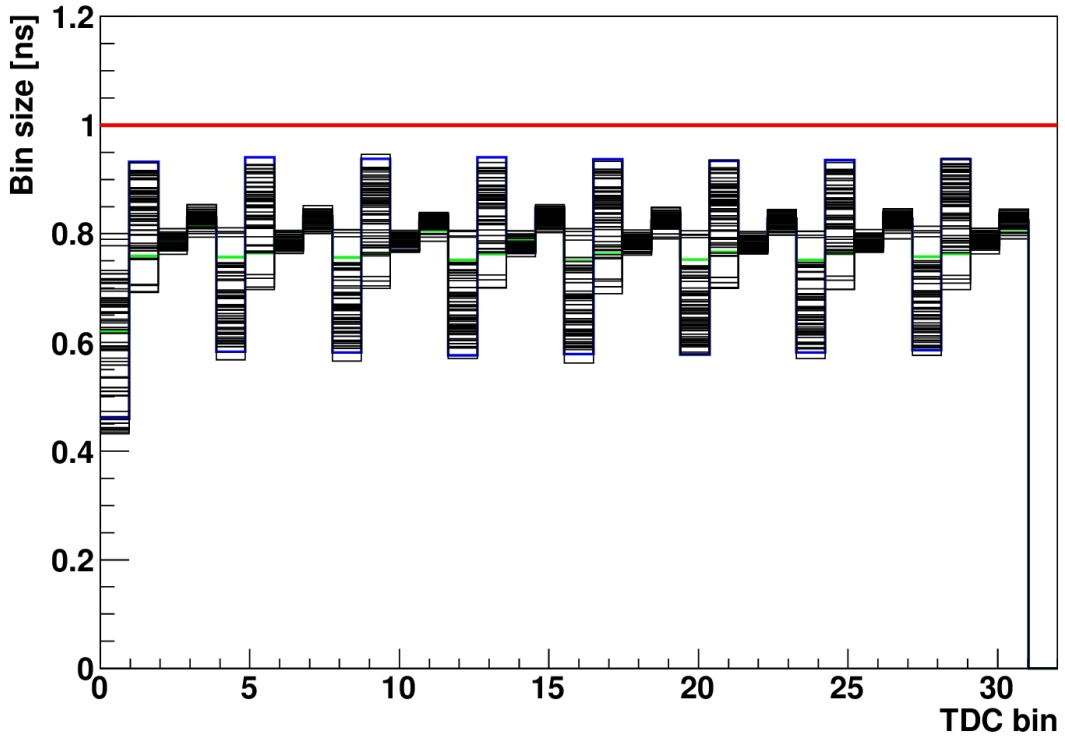


Figure 5.33: Bin size measurement of all 32 channels delay optimized Arria GX TDC design. For each time bin the bin size of all 64 time measurement elements are plotted. The time measurement element marked with blue has the largest bin size differences and the time measurement element marked with green has the smallest bin size variations.

the Stratix and Arrix GX FPGA differ. The results identified a weak point in the TDC design, namely that the phase-shift of the 2nd clock for the fine timing differed from the ideal case. This was not observed during the tests of the Stratix FPGA. The encoding could not disentangle the beginning and the end of a coarse count. The TDC design was modified with additional fine timing information to make an encoding possible which can discriminate the beginning and the end of a coarse count. This solved the fine timing ambiguity. Furthermore, performing bin size measurements of all 32 TDC channels showed that some time bins were larger than 1 ns, which was solved by using a newly developed C-script, the TDC channel setter, which optimizes the delay constants of every TDC channel with measurements. In addition, the design was tested with a more precise and completely automatic delay scan using a RIGOL function generator. Furthermore, the variation between different FPGA chips was measured, which is up to 200 ps and small enough to use the same firmware for all front-ends. The result of this TDC design fulfills the needs of a TDC for the Outer Tracker upgrade.

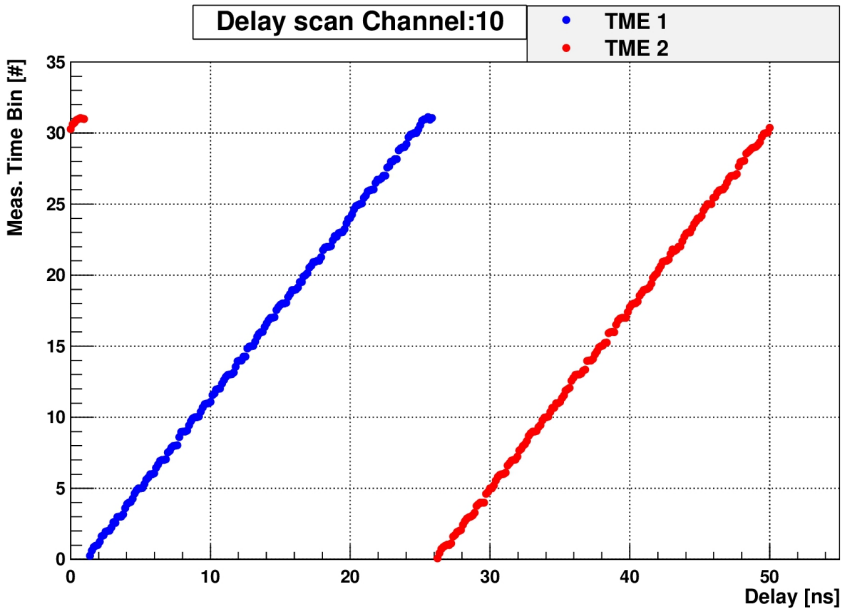


Figure 5.34: Delay scan of the timing constraint optimized Arria GX TDC channel 10.

The Table 5.3 summarizes the four presented TDC designs. The number of channels per design and the amount of logic elements used for one complete TDC channel can be seen, including the logic elements for the encoding blocks. Only results for the Arria GX design with the solved linearity problem are shown, where the design Arria GX V.2 is the design before the delay optimization with the TDC channel setter and the design Arria GX V.3 is the one after the delay optimization. The best performance is seen with the Stratix V.2 design. The results for the Arria GX V.3 design satisfy the needs for the LHCb Outer Tracker, too.

Design	Number of channels	Logic elements per TDC ch.	Bin size [ns]	DNL [LSB]	INL [LSB]
Stratix V.1	1	146	1.56	0.5/0.6	0.3/0.2
Stratix V.2	16	42	0.78	0.17 - 0.35	0.03 - 0.23
Arria GX V.2	32	55	0.78	0.2 - 0.9	0.3 - 0.7
Arria GX V.3	32	55	0.78	0.1 - 0.6	0.04 - 0.6

Table 5.3: Summary of the four TDC designs.

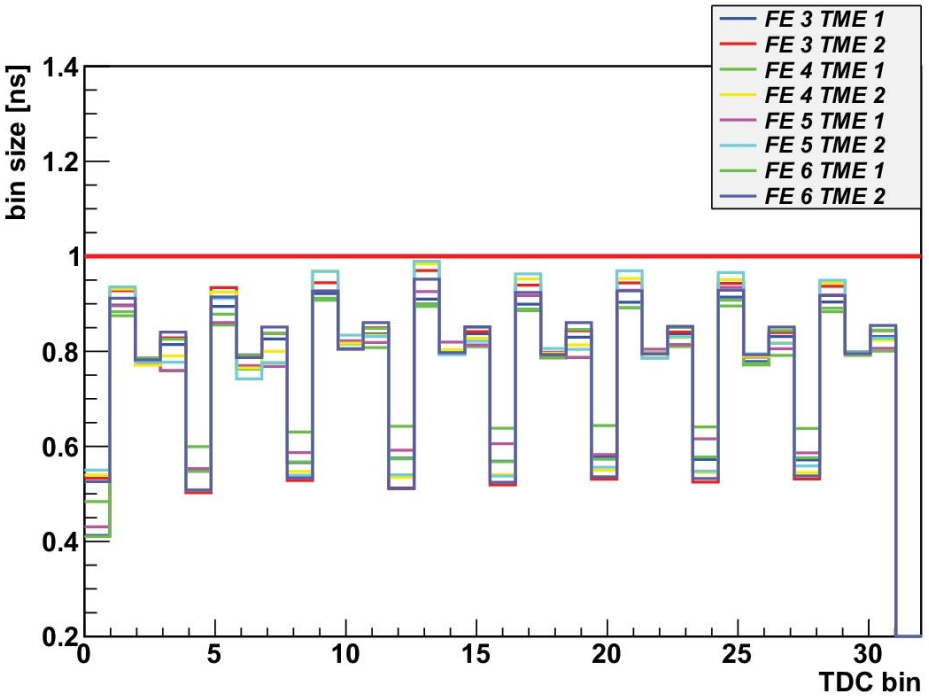


Figure 5.35: FPGA to FPGA bin size variations of TDC channel 6.

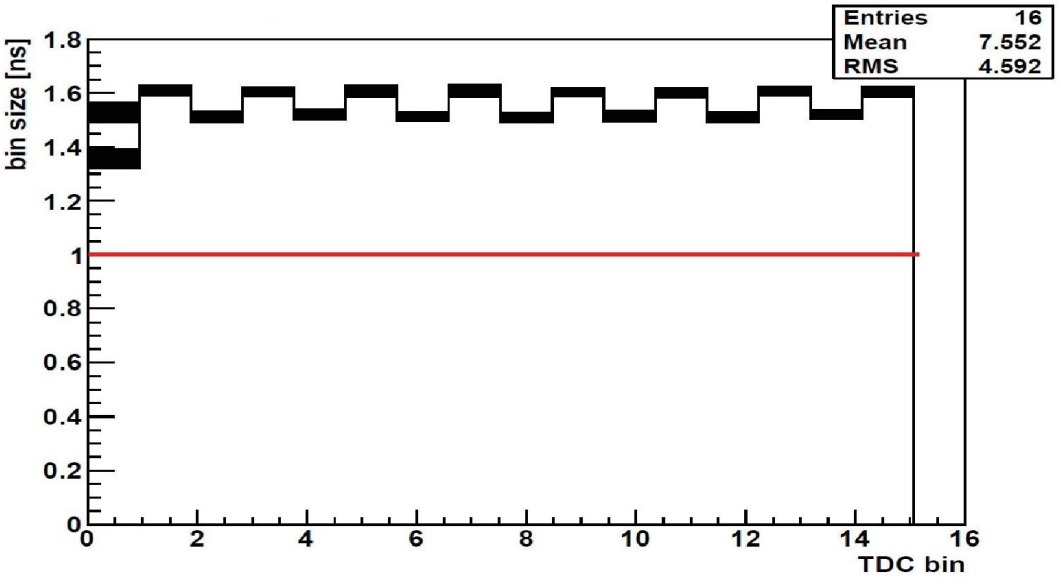


Figure 5.36: Bin size measurement of all 32 channels using only 4 bit time information.

CHAPTER 6

Functionality test: Outer Tracker module readout

In this chapter a functional test is described which was performed to validate the usage of the Arria GX FPGA and the developed TDC firmware in a real detector readout. It was decided to perform the functional test with a short LHCb Outer Tracker straw-tube prototype module in a cosmic setup to measure the LHCb Outer Tracker drift time spectrum. As described in Chapter 4.3.1 only the pre-amplifier board (ASDBLR board) will be reused for the upgrade of the LHCb Outer Tracker readout electronics. Two prototype boards were developed during this thesis to replace the OTIS board and the GOL/AUX board. These two boards are called connection board and FPGA test board and the designs are shown. The hardware and software of the cosmic setup and the determination of the drift time spectrum is described. At the end of this chapter a design proposal for the upgraded LHCb Outer Tracker front-end box will be shown.

6.1 Prototype boards

For the upgrade of the Outer Tracker front-end electronics the TDC board (OTIS board) and the GOL/AUX board will be replaced, while the pre-amplifier board (ASDBLR board) will be reused. To replace the GOL/AUX board an FPGA test board has been developed first. The board was also used for the FPGA

irradiation test which will be described in Chapter 7.

In addition, to replace the OTIS board the connection board has been developed. This second board connects the ASDBLR board with the FPGA test board. It is a test board to investigate how the ASDBLR can be connected to the Arria GX FPGA. The design of both boards will be shown in the following subsections.

6.1.1 FPGA test board

The FPGA test board uses a SRAM-based FPGA to measure the LHCb Outer Tracker drift times, to serialize the data and send the data with GBit/s transceivers to the back-end electronics. All components used except the SRAM-based FPGA are qualified for the usage in radiation areas. The FPGA test board measures the drift time of 32 detector channels with the FPGA-based TDC developed in this thesis. The TDC design is shown in Section 5.4. The data can be sent with two 3.125 GBit/s optical transceivers to the back-end electronics. The pre-amplifier ASDBLR boards will be connected via a second board, the connection board.

The main component of the board is the Arria GX FPGA from Altera. Two 3.125 GBit/s transceivers of the FPGA are connected with two SFP[1] modules to convert the electric signals to optical signals. Figure 6.1 shows the schematic of the FPGA test board. The board is powered with +5 V and -5 V supply voltages and used two types of power regulators from CERN. These are the LHC4913 and LHC7931, which are qualified as radiation hard. The output voltages of the power regulator are: +3.3 V,+3.0 V,+2.5 V,+1.2 V,-3.0 V. Three clock signals are used on the board: a 125 MHz clock from a crystal as possible input for the FPGA phase-looked loops (PLLs), a 40 MHz clock from a QPLL generating a low jitter and phase stable clock from the LHC clock and a 62.5 MHz clock from a crystal used as reference clock for the fast GBit transceiver PLLs. The QPLL is an ASIC developed in the CERN Microelectronics group which uses a PLL and a quartz crystal to generate a low jitter LHC reference clock throughout the whole LHC [63]. The LHC clock can be connected via the front connector to the QPLL and further to one FPGA PLL. Moreover, all slow control signals are connected to the FPGA via the front connector (50 pins). Testpules from the front connector are routed to the FPGA which drives these test pulses to the sensor connectors. These test pulses can be used to inject pulses into the pre-amplifier to test the whole readout chain.

It is possible to set a board address with three hex switches, which are connected to the FPGA, which means the addressing scheme of the old GOL/AUX board could be reused. Furthermore, SMD switches and status LEDs are available. The FPGA can be programmed directly by a PC via JTAG, or by a 16 MBit flash memory (EPCS16). Power cycling the FPGA causes an automatic programing of the FPGA from the flash memory. The 32 channel detector hit signals are

[1]Small form-factor pluggable transceiver

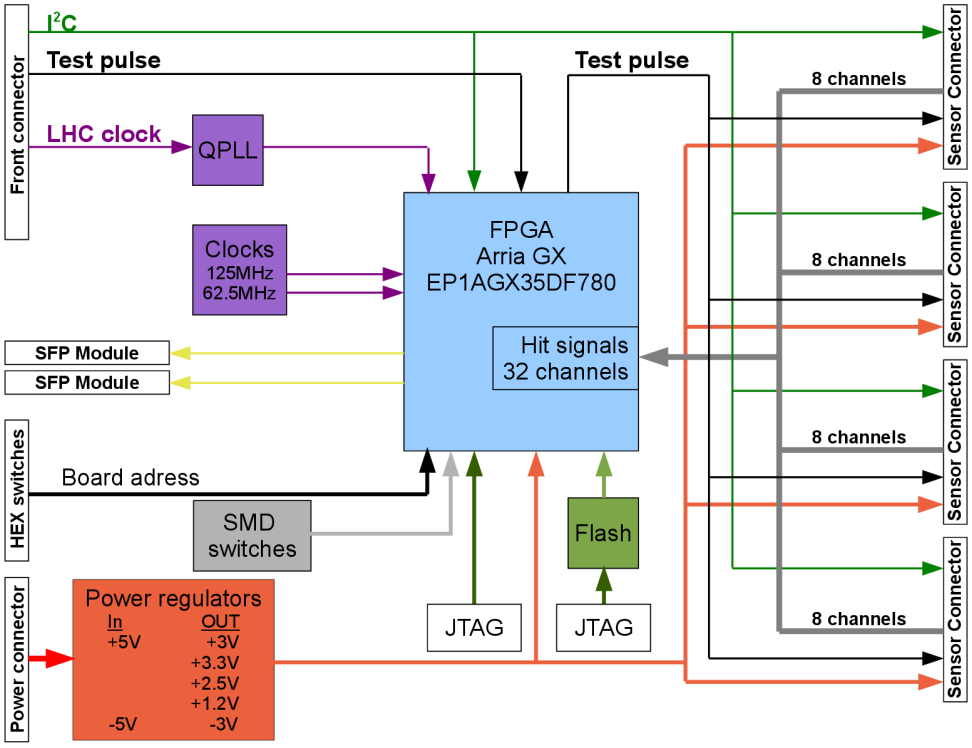


Figure 6.1: FPGA test board schematic. The main components of the FPGA test boards are depicted: the Arria GX FPGA in blue, the supply power lines in red, the communication and programming of the FPGA in green, the clock signals in violet, the GBit/s transceiver lines in yellow, test pulse and board address in black, and the 32 detector channels in grey.

connected through four sensor connectors (80 pins), which also provide power, control signals and test pulses to the connected boards. For further details see the full schematic of the IF13-6 in Appendix C. The FPGA test board is completely pin compatible to the existing readout electronics of the Outer Tracker. Figure 6.2 shows a picture of the FPGA test board.

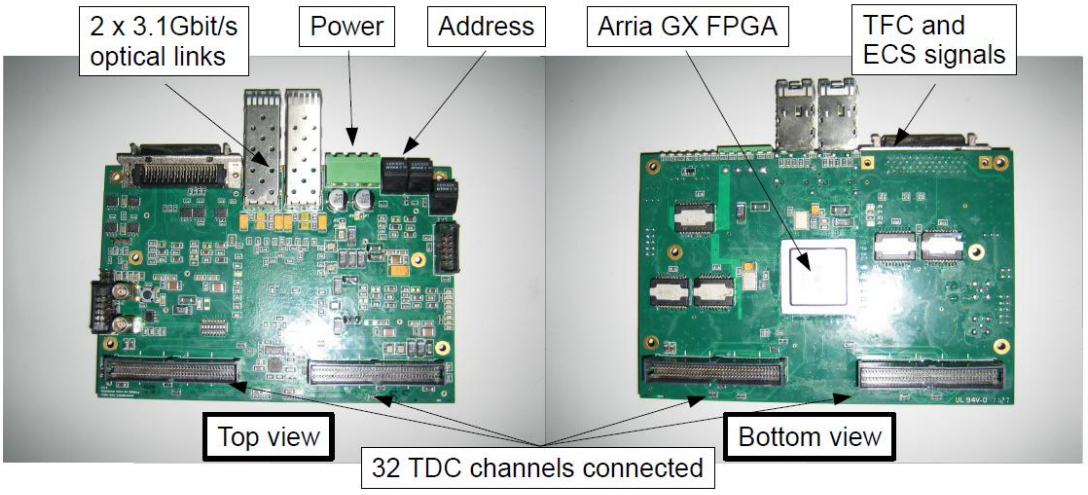


Figure 6.2: Picture of the FPGA test board.

6.1.2 Connection board

The connection board provides the signal connection between the pre-amplifier boards and the FPGA test board. It replaces the current OTIS board. Figure 6.3 shows the functional schematics of the connection board and Figure 6.4 shows the placement plan for the top and the bottom. The main task of this PCB is to convert the differential LVDS ASDBLR signals to single ended CMOS, to connect them to the TDC input pins of the FPGA test board and to set the ASDBLR thresholds. The hit signals are converted with fast LVDS receivers[2] to single ended CMOS signals and the ASDBLR thresholds are controlled with a four channel 10 bit DAC[3] via the I^2C bus. Furthermore, it is possible to read the temperature from a temperature sensor[4] which is also connected to the I^2C bus. It is foreseen to test the readout chain by sending test pulses to the ASDBLR chip. These test pulses can be generated in the FPGA and are connected to high-speed differential line driver/receivers[5] on the connection board, where a LVDS/CMOS conversion is done.

[2]TI DS90LV048A
[3]DAC-AD5306
[4]ADT7410
[5]TI SN65LVDS2

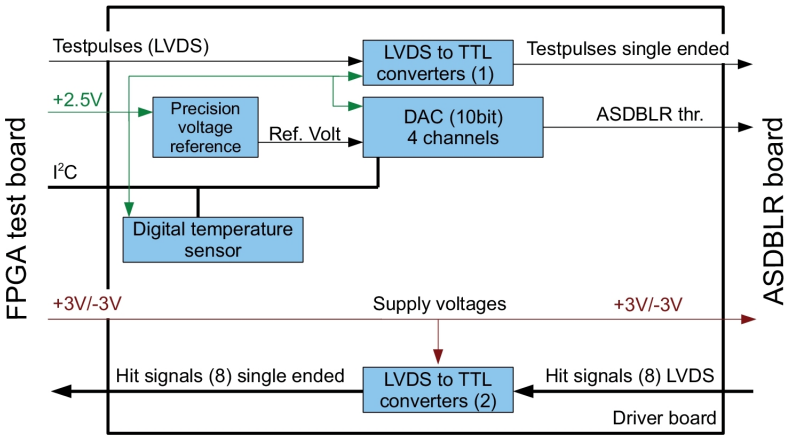


Figure 6.3: Connection board functional schematic.

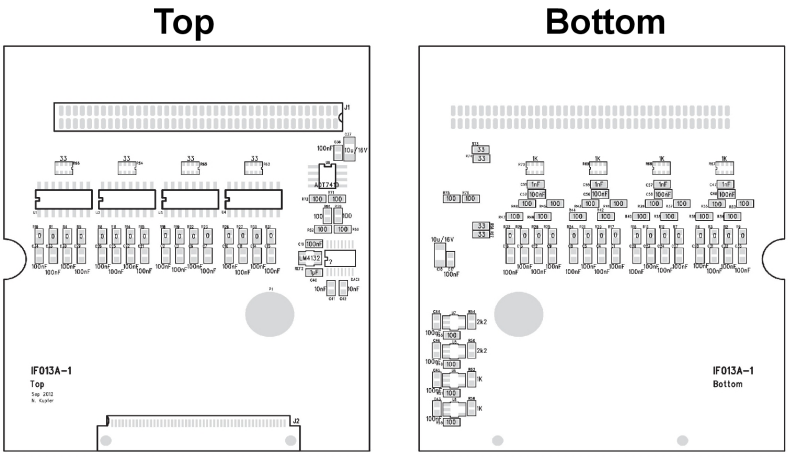


Figure 6.4: Driver board placement plan, left: top layer and right: bottom layer.

Digital to analog converter test

To provide the ASDBLR threshold voltage the digital to analog converter on the connection board is used. The DAC linearity was tested with an oscilloscope. The result of this measurement can be seen in Figure 6.6 and satisfy the need for the ASDBLR.

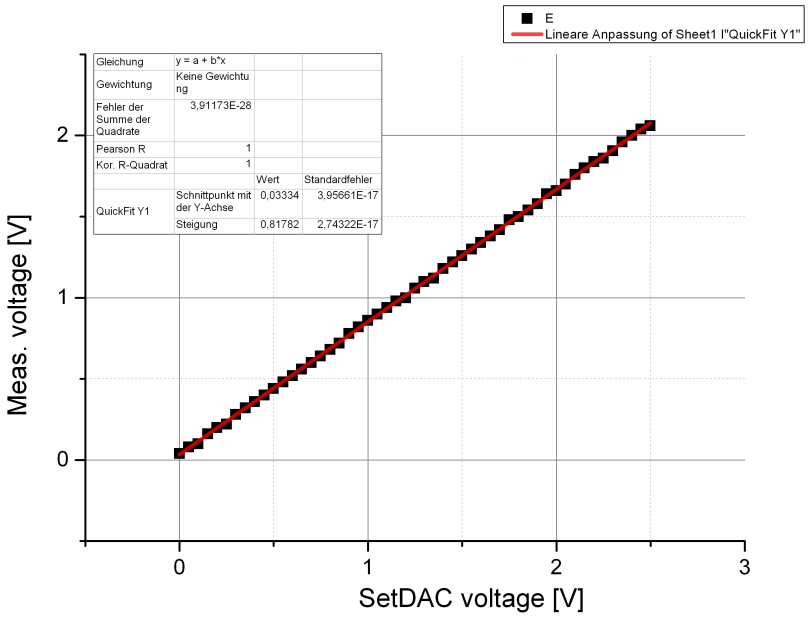


Figure 6.5: The DAC linearity test results satisfy the need for the ASDBLR.

6.2 Cosmic test

In the LHCb Outer Tracker detector the readout electronics measures the drift time of the ionizing particles traversing the straw-tube modules. The drift time is the time difference between the point in time when a particle passes the straw-tube generating ionization clusters along the track and the point in time the hit signal is detected. The readout electronics in the LHCb detector is synchronized to the LHC clock. This makes it possible to measure the drift time with respect to the rising LHC clock. For the test of the developed readout electronics cosmic muons were used. The muons traversed the detector asynchronously. The drift time measurement in a cosmic setup is only possible with a reference signal. A coincidence signals of two scintillators was used as reference signal for a muon traversing the detector. In addition to the two scintillators a short LHCb Outer Tracker straw-tube prototype module was used. The muon rate at sea level is 110 muons $\mathrm{m}^{-2}\,\mathrm{s}^{-1}\,\mathrm{sr}^{-1}$ [64], so the measurements take several hours to several days to reach reasonable statistics.

In the following the hardware and software used for the cosmic test are described. Afterwards, the noise reduction will be discussed and the determination of the time resolution of the whole system will be presented. At the end of this section the measurement of the LHCb Outer Tracker drift time spectrum with the Arria GX FPGA is shown and compared to the results of the current readout electronics used by the current detector.

6.2.1 Hardware

The muons traverses the module asynchronously to the clock of the readout electronics. To calculate the drift time for a particle, two scintillators were used to generate a coincidence signal if both scintillators are hit by the same muon. The time difference between the coincidence signal and the hit signals in the straw-tubes represent the drift time including a offset. The offset is caused by the signal latency differences of the time reference signal and the straw-tube hit signals. The maximum drift time for the LHCb Outer Tracker straw-tubes at nominal voltage of 1550 V is 45 ns [66, 67].

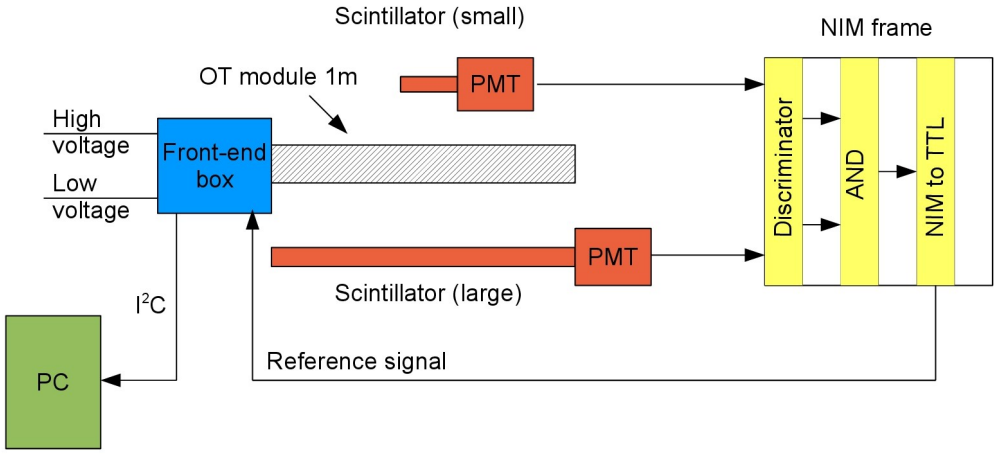


Figure 6.6: Cosmic setup for the drift time measurement. The Front-end box hosts one ASDBLR pre-amplifier board, the connector board and the FPGA test board. Two scintillators are used to generate a reference signal for the drift time measurement of the cosmic muons.

The setup for the cosmic test used a 1 m straw-tube detector which was operated at 1550 V and with a gas mixture of Ar / CO_2 (70% / 30%). The straw-tube module is an Outer Tracker prototype module. In addition, one large scintillator was placed below the straw-tube module and a small scintillatorone on the top of the module. The large scintillator covered the whole acceptance of the straw-tube module and the small scintillator covered only a rectangular area of

5 cm × 15 cm. Both scintillators were connected to photo multiplier tubes (PMT). The PMT signals were discriminated and combined to the coincidence signal. To measure the time of the coincidence signal the signal level had to be converted from NIM[6] to TTL[7] before it was connected to one TTL input of the FPGA test board. The corresponding input pin of the Arria GX FPGA was connected to TDC channel 1.

For the readout an Outer Tracker front-end box was used which contained the FPGA test board, the connection board and the pre-amplifier board (ASDBLR board). For the slow control and the data acquisition the I^2C bus was used. This was possible because of the low coincidence rate.

6.2.2 Software and firmware

The main parts of this design are the TDC which is described in Chapter 5.4, a I^2C slave and a FIFO (96 bit wide and 512 words deep). Figure 6.7 shows a block schematic of the cosmic firmware. The TDC data of 8 channels and the value of a 32 bit counter running with 40 MHz are written to the FIFO in parallel. The 32 bit counter is used as coarse time information in addition to the fine time of the TDC. The data at the output of the FIFO are grouped into 12 bytes which are connected to the I^2C slave. These 12 bytes represent a so called event. Zero suppression has been implemented and was used during the test. In the following the I^2C slave and the zero suppression are described.

I^2C block

For the communication with the Arria GX FPGA, an I^2C bus was used which was connected with a USB-to-Serial bridge[8] to a USB port. The USB-to-Serial bridge used, has the capability to establish several serial data transfer interfaces. One is the I^2C bus with a bandwidth of 400 kb/s which is high enough to control the FPGA and to read out the data in the histograms and counters already analyzed on the FPGA.

The FPGA firmware uses a I^2C block written in Verilog. On the PC side, a C program was developed using libraries from the FTDI company, to control the measurements. This program was developed during this thesis.

To achieve an as high as possible bandwidth the I^2C package read mode was used. This mode needs only one register address at the beginning of a read cycle. After the first byte is read, the byte of the next register address is read, this continues till the defined package length is reached. The FTDI USB-to-Serial bridge has a 1024 byte deep buffer, which defines the maximum length of the package readout mode. A read cycle starts with the read of the first byte of the

[6] Nuclear Instrumentation Module
[7] Transistor transistor logic
[8] UM232H development board from FTDI

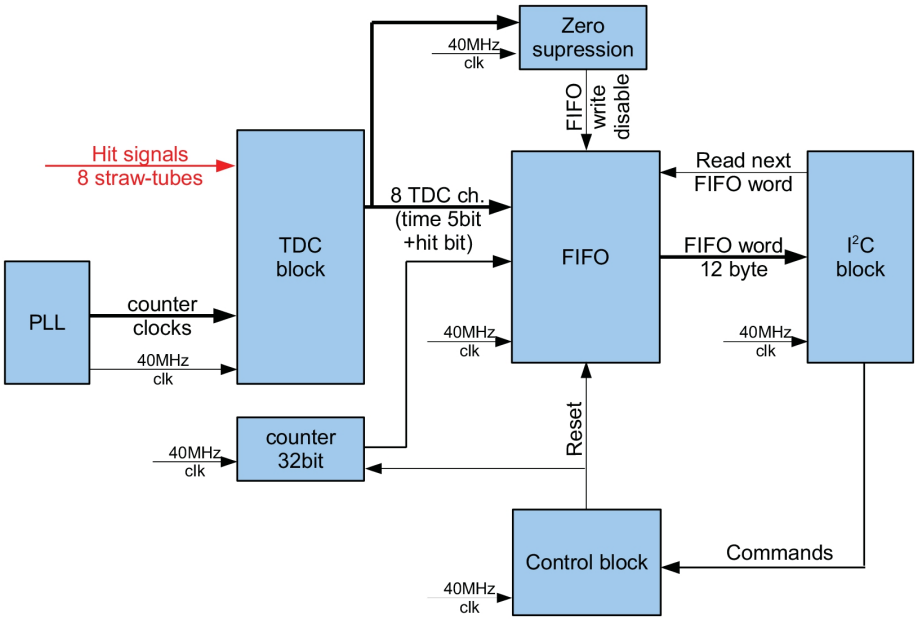


Figure 6.7: Block schematic of the cosmic firmware.

12 byte wide FIFO word and after the 12th byte was read the I^2C slave triggers the next FIFO read to make the next FIFO word available in the I^2C registers.

The readout of the FIFO is controlled by a PC, a C-script checks how deep the FIFO is filled. If the FIFO is filled more than half the half FIFO is readout via the scheme described above. The data are written into an ASCII file.

Zero suppression

The zero suppression checks the hit registers of the TDC channels. If for a data-set all of them are zero the FIFO write will be disabled and the data-set is not accepted.

6.2.3 Noise reduction

At the beginning it was not possible to measure any detector signals with the new electronics, due to strong noise. Even with a high ASDBLR thresholds of 1800 mV nearly every 25 ns period showed a hit. This was also seen on the 1 GHz oscilloscope at the ASDBLR outputs and the outputs of the fast LVDS receivers.

The problem was caused by the +3 V supply voltage for the ASDBLR. The +3 V was used on the connector PCB also to power the fast LVDS receivers. The time for a redesign of the connection board was too short. This is why a quick solution was implemented. The power pins of one ASDBLR board connector were

cut and the board was powered via a cable from the connection board including a filter with two capacitors and a coil. The noise came down to an acceptable level of a few Hz with this solution. An ASDBLR threshold of 1400 mV was selected. The modified board was used for all the following measurements.

6.2.4 Time resolution measurement of the readout

The time resolution for the reference signal was measured with the FPGA-based TDC by connecting the two scintillator PMT signals after discrimination and NIM → TTL conversion to two TDC channel inputs of the FPGA test board. The signal path for the large scintillator to the FPGA test board was longer by 15 ns than the signal path for the small scintillator. The raw data of this measurement was analyzed with a c-script. For every 12 byte event in which the two scintillator PMTs showed a hit the time difference between these two signals was calculated and written into an histogram. The histogram can be seen in Figure 6.8. The time distribution was fitted with a Gaussian function. It is

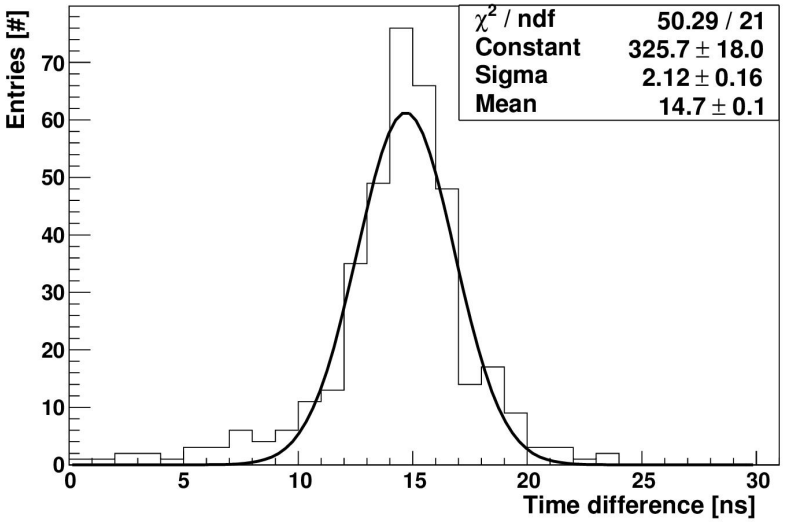


Figure 6.8: Time difference between both scintillators. One additional 15 ns delay element was used for the large scintillator.

possible to measure the cable delay between the two scintillators. The width of the time difference distribution is 2.1 ns. That is large but still good enough to measure the drift time of the 1 m straw-tube module.

6.2.5 Drift time spectrum measurement

The task of the LHCb Outer Tracker readout electronics is to measure drift times in the straw-tubes. The following test was performed to demonstrate that it is

possible to use the Arria GX FPGA firmware and the two developed PCBs to measure proper drift times of an Outer Tracker module.

Drift time spectrum with the Arria GX FPGA

The drift time is the time difference between the point in time when a particle passes the straw-tube generating ionization clusters along the track and the point in time the electrons reach the anode. To measure the drift time the time difference between hit signals from the straws in event N and the time of the reference signal in event N+1 was calculated with a c-script. The difference in the event number is caused by the longer signal path for the reference signal to the TDC than for the straw-tube hit signals to the TDC. Bunch crossing counter values and TDC values were combined. The data taking period was 5 days. Figure 6.9 shows the measured drift time spectrum for the eight connected straw-tubes, which is in agreement with the expected maximal drift time of roughly 45 ns [66, 67].

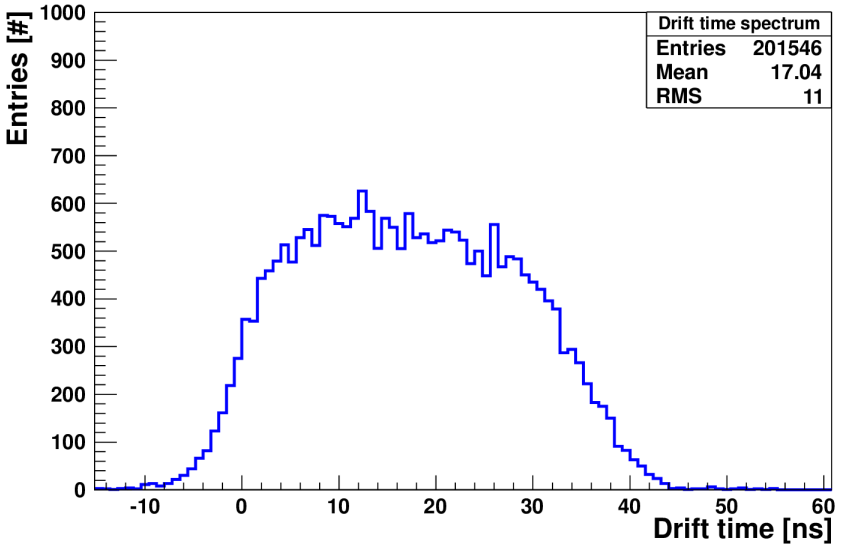


Figure 6.9: Measured drift time spectrum with the Arria GX TDC using cosmic muons. The data of all eight available channels are included. Data taking period was 5 days.

Conclusion

The result of this test shows that it is possible to use the Arria GX FPGA and the developed FPGA-based TDC for the readout of LHCb Outer Tracker modules. In addition, the two developed prototype boards demonstrated that these can be used with the ASDBLR board to determine drift times of Outer Tracker modules. But before the prototype boards can be extended to a real upgrade design the

radiation tolerance of the Arria GX FPGA has to be determined. This test will be shown in Chapter 7.

6.3 Design proposal for the FPGA front-end board

The current FPGA test board has only the possibility to readout 32 straws of an Outer Tracker module. For the upgraded front-end board 128 TDC channels have to be available. In addition, it is a big advantage to use faster GBit/s transceivers like the one from the Arria II family from Altera. These transceivers have a bandwidth of 6.375 GBit/s.

The Figure 6.10 shows a proposal for an upgraded front-end board. Two small Arria II GX FPGAs are foreseen. The amount of available logic elements in these FPGAs is a factor 2 higher than on the Arria GX FPGA used currently, so it would be easily possible to implement the 128 TDC channels. The speed grade of this FPGA is the same as for the Arria GX FPGA, which means that the TDC will have at least the same performance.

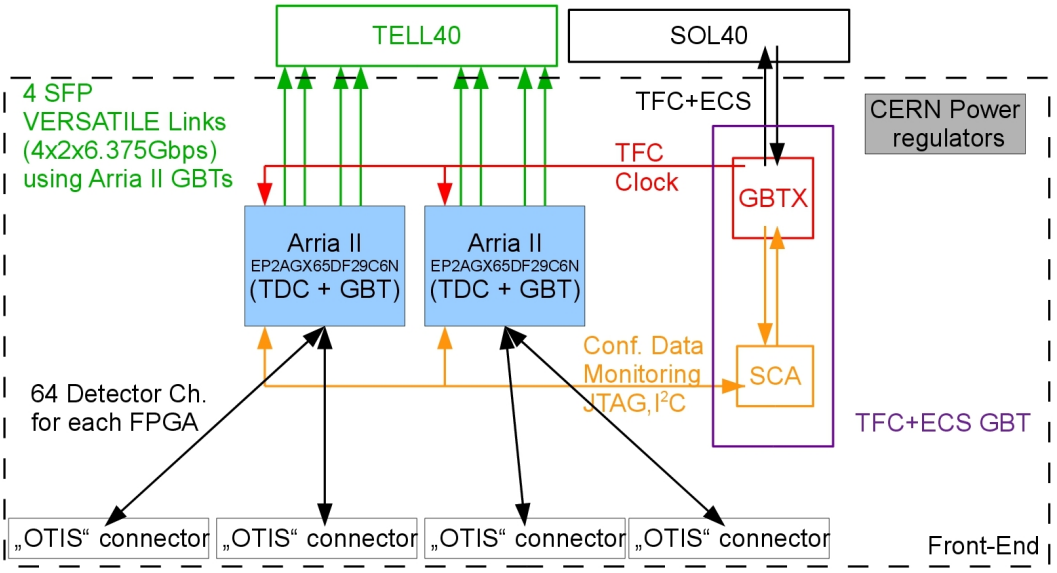


Figure 6.10: Schematic of the front-end board proposal. The front-end would also include a connection board like the connection board which is depicted in Figure 6.3. The connection board is used to connect the ASDBLR board with the "OTIS" connectors.

Dual port optical modules from the CERN Versatile link projects [69] could be used as SFP[9] modules. They are qualified by the Versatile link group for

[9]Small form-factor pluggable transceiver

radiation environments like the LHC. Four GBit/s transceiver links from each FPGA would be connected to the back-end board (TELL40). The board would be powered with the CERN standard power regulators[10] also used for the FPGA test board. The trigger and fast control signals (TFC), experiment control signals (ECS) and clock signals for the FPGAs would be provided by one GBTX chip [70] which received these signals over an optical GBit/s transceiver from the SOL40 board [71]. The task of the SOL40 board is to distribute the timing and readout control information to the front-end electronics and the TELL40 boards. In addition, the GBT SCA chip (Slow Control Adapter ASIC) [70] would be necessary to distribute the slow control and monitoring. The GBT SCA chip would also provide a JTAG[11] bus with which it would be possible to load the firmware of the Arria II FPGAs.

[10] LHC4913 and LHC7931
[11] Joint Test Action Group

CHAPTER 7

Irradiation test of the Arria GX FPGA

The crucial test for the front-end prototype for the LHCb Outer Tracker upgrade described here, is the radiation hardness of the commercial SRAM-based FPGA. To examine this, an irradiation campaign was performed at the Max-Planck-Institute for Nuclear Physics in Heidelberg, using the Tandem-van-de-Graaff-Accelerator. First, radiation effects with FPGAs will be discussed and the expected dose for the Outer Tracker readout electronics in the upgrade environment will be estimated. Next, the setup for the measurements and the preparations of the test boards are described. To interpret the results, the radiation dose was simulated and measured. This will be shown before the measurements of the FPGA are discussed. To classify the radiation tolerance of the FPGA, the following parameters of the FPGA were measured before, during and after the irradiation: temperature, electrical currents, stability of firmware, PLL stability, and TDC behavior of the FPGA.

7.1 Radiation effects of FPGAs

There are three different types of FPGAs: Anti-fuse, flash based and SRAM-based FPGAs. The anti-fuse FPGAs are programmed by using a programing voltage, which melts fuses for routing. A result of this is that the firmware cannot be changed any more. This is an advantage in radiation areas, the firmware of the FPGA does not change. For anti-fuse based FPGAs standard and radiation

tolerant chips exist. The total ionization dose (TID) hardness for the radiation-tolerant anti-fuse FPGAs is stated from the producer to be 300 krad [72].

The second type of FPGAs are flash-based FPGAs. The flash cell is built of a isolated floating gate between the control gate and the source-drain. The floating gate controls the current between source and drain and the control gate controls the charge on the floating gate. The flash cell can be programmed by setting a high positive voltage (10 V) to the control gate. Electrons tunnel through the isolating oxide to the floating gate which stops the source drain current. To reset the transistor a high negative voltage is set to the control gate. A bit is stored in the flash cell by the charge on the floating gate. The flash cells used make it possible to re-program the firmware and in addition, the FPGA does not lose the firmware by switching the supply voltage off. These FPGAs do not lose their firmware by configuration register flips during irradiation. But if the tunnel oxide between floating gate and substrate for a flash cell gets damaged, it is not possible to program this cell any more. An additional weak part is the charge-pump for the programming [73]. For flash based FPGAs, standard and radiation tolerant chips exist. Irradiation tests of a standard flash-based FPGA, the ProASIC3 from Actel/Microsemi, performed by the LHCb Syracuse group, have shown that this chip is programmable until 17 krad and then shows high currents and malfunction after 30krad [48]. The more expensive radiation tolerant version is quoted to sustain a higher total ionization dose of up to 100 krad [74].

The third type of FPGAs are the SRAM-based FPGAs which use CMOS SRAM cells as configuration registers. These FPGAs are more advanced in the technology level than the other two FPGA types. It is possible to use higher clock frequencies in the logic elements and more advanced functionality. One example are GBit/s transceivers which are provided by modern SRAM-based FPGAs. The drawback of SRAM-based FPGAs is that these chips lose the configuration during irradiation mainly by high-energy hadrons (E>20MeV). The SEU cross sections for protons depends on the proton energy and rises with higher kinetic energy until 30 MeV where it reaches a plateau [89, 90, 91]. At 22 MeV the SEU cross section is roughly one third of the plateau value.

Figure 7.1 shows a schematic of a CMOS SRAM cell. It uses two CMOS inverters to store a single bit. Ionizing particles generated by nuclear reactions in the silicon create electron-hole pairs. These charge carriers drift in the pn-junction field of a switched off transistor. In the schematic shown for the left NMOS and for the right PMOS the source-drain current is disabled. If the left NMOS transistor is hit by an ionizing particle and a critical amount of electrons during a short time is created, this can change the potential for the gates of the right transistors. The result is a flip of the SRAM cell value.

Another point is the TID hardness for SRAM cells which depends mostly on the gate oxide thickness of the SRAM MOSFETs. Modern SRAM cells with gate length below 100 nm are radiation hard up to the level of 300 krad [76].

Taking only the radiation tolerance of the FPGA firmware into account, the

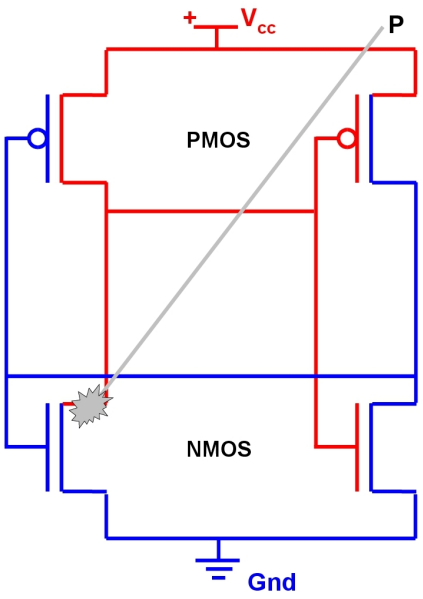


Figure 7.1: Schematic of a CMOS SRAM cell [73].

flash-based FPGA would be the right choice because the firmware does not change during irradiation and it is possible to change the firmware. But these FPGAs does not sustain as high of ionization doses as the SRAM-based FPGAs. The right choice depends on two parameters: the expected TID and the particle flux which corresponds to the expected firmware error rate for the SRAM-based FPGAs. If the TID is too high and the expected firmware error rate for SRAM-FPGAs is not acceptable, only the anti-fuse FPGAs remain.

In general, FPGAs also suffer from the same radiation effects as ASICs. In the following, these effects will be shortly introduced.

Total ionization dose effects

Ionizing particles create electron-hole pairs along their path. In the MOSFET gate oxide, the positive charges can be trapped while the electrons leave the oxide. This charge build-up results in a threshold voltage shift, leakage currents due to charge build-up in the lateral oxide, or the creation of defects at the interface between silicon and silicon dioxide. With the decreasing CMOS technology size the gate oxide thickness decreased which results in a higher radiation hardness [75]. If the gate oxide thickness is below 10 nm electrons are able to tunnel to the positive charge inside the gate oxide with high probability [77]. The main problem remaining is the leakage currents, because the lateral oxide is not decreasing in the same order as the gate oxide. For ASICs, there are design techniques like

enclosed gate structures and guarding rings to minimize these leakage currents. With these techniques it is possible to reach TID hardnesses of 10 Mrad and above [79].

Single event upsets

Single event upsets (SEUs) are bit flips in semiconductor memories. The configuration of the FPGA is not the only part affected by SEUs. All flip-flops, latches, registers and other RAM cells can be flipped by radiation, too.

7.2 Expected radiation levels for the LHCb Outer Tracker upgrade

The expected radiation levels were estimated with a FLUKA simulation [78]. The following parameters were extracted from this simulation: The total ionization dose, 1 MeV equivalent neutron fluence[1] and charged hadron fluence. For each sub-detector and parameter a map was generated with which it is possible to determine the fluences per proton-proton collision or dose per proton-proton collision.

A map of the total ionization dose normalized to a single proton-proton collision for the Outer Tracker T3 station is shown in the Figure 7.2. The Outer Tracker front-end position is exposed to a maximum dose of $2{\cdot}10^{-14}$ Gy per collision.

The total ionization dose is determined from the number of proton-proton collisions $N_{\text{collisions}}$ calculation using the Formula 7.1. The inelastic proton-proton cross section at 7 TeV [80] σ=72 mb, the forseen LHCb upgrade instant luminosity $\mathcal{L}$=$2 \cdot 10^{33}$ cm^{-2}s^{-1} and the typical amount of seconds running during one year Δt=$1 \cdot 10^{7}$ s are included. The higher proton-proton cross section (+14 %) at $\sqrt{s} = 14$ TeV compared to $\sqrt{s} = 7$ TeV is neglected.

$$N_{\text{collisions}} = \sigma \cdot \mathcal{L} \cdot \Delta t \tag{7.1}$$

From this an total ionization dose for the upgraded LHCb Outer Tracker electronics of 28.8 Gy per year is expected after the upgrade. This corresponds to 29 krad for 10 years running.

Table 7.1 summarizes the results for the FLUKA simulation. Throughout this chapter no safety factors are included, which will be only included during the interpretation of the results.

[1] Fluence of 1 MeV neutrons causing the same damage in a material as induced by the simulated particle fluence with the specific energy distribution.

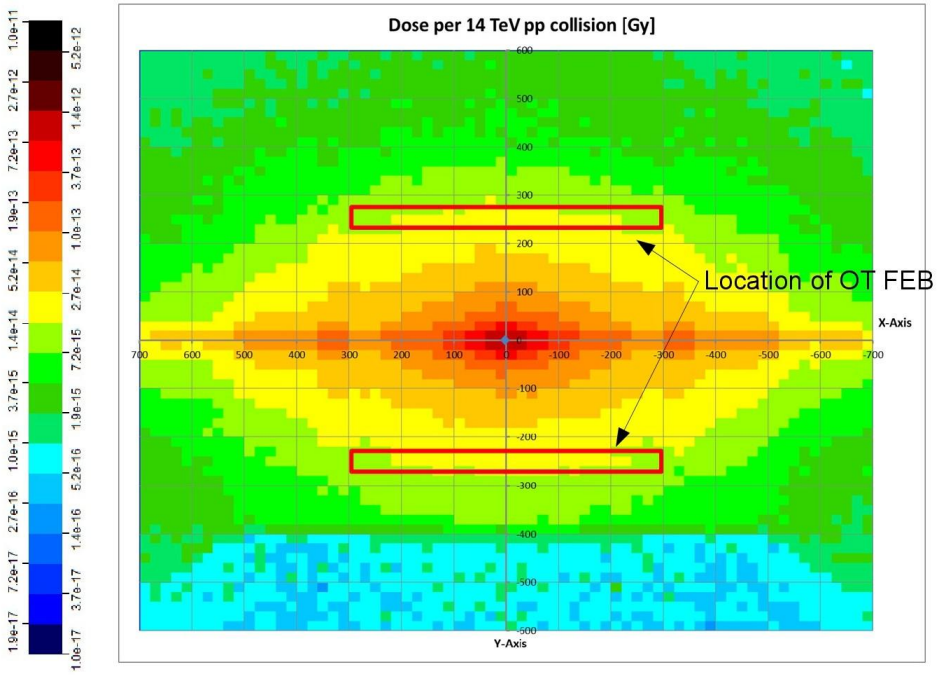


Figure 7.2: Fluka simulation for the LHCb upgrade dose of the Outer Tracker T3 station. The total ionization dose in Gray is shown per proton proton interaction. The two red rectangles indicate the position of the Outer Tracker readout electronics [86].

	Current situation	Upgrade situation
Luminosity	$2{\times}10^{32}$ cm^{-2}s^{-1}	$2{\times}10^{33}$ cm^{-2}s^{-1}
Total ionization dose	3 krad	29 krad
1 MeV neutrons	$4{\cdot}10^{11}$ cm^{-2}	$4{\cdot}10^{12}$ cm^{-2}
Charged hadron fluence	290 particle $\cdot$ Hz / cm^2	2900 particle $\cdot$ Hz / cm^2

Table 7.1: Radiation environment for the current and upgraded LHCb OT readout electronics. For both situations a running time of 10 years is assumed. No safety factors are included.

7.3 General setup

The main focus of this irradiation campaign was the investigation of total ionization effects. In addition, cross sections for configuration bit flips, GBit/s transceiver errors and single event upsets of the flip-flops were measured. These cross sections depend on the proton energy as already mentioned.

The irradiation test was performed at the Max-Planck-Institute for Nuclear Physics in Heidelberg which provides the possibility to conduct irradiation tests with different ions. The 12 MV Tandem-van-de-Graaff-Accelerator accelerates protons up to a kinetic energy of 24 MeV with beam currents from 23 pA up to 1 μA. The FPGA irradiation test was performed with two FPGA test boards, which were developed during this thesis and already introduced in Section 6.1.1. Both boards were irradiated with 22 MeV protons. The FPGA test boards were mounted to a flange outside a vacuum tank in the single pass target area for biological irradiation experiments. The proton beam exited the flange through a 100 μm stainless steel window. Figure 7.3 shows the mounting frame of the FPGA test board. Between the flange and the FPGA, two additional layers were located. The shutter layer hosts a movable collimator for the beam profile measurements and the fiber layer was used as mounting frame for an irradiation test of fibers running in parallel. For safety reason an additional radiation shield around the whole setup was constructed with 5 mm steel plates. In addition, a Faraday cup could be place into the proton beam upstream the vacuum tank. This was used to measure the proton beam current.

7.4 Total ionization dose determination

For the irradiation test, the total ionization dose (TID) for the FPGA is the crucial reason why the energy deposition in the FPGA silicon was calculated. The total ionization dose is later also referred as integrated dose. In addition, passive dosimeters (alanine [82]) were used to crosscheck the calculation. First, the calculation with the different steps is introduced. After this, the measurements with alanine dosimeters are shown and compared to the calculation.

7.4.1 Total ionization dose calculation

The TID of the FPGA was calculated using the measured proton beam profile and was cross checked with passive dosimeters. The TID determination is possible because the beam optics was constant during the whole irradiation campaign. Only the beam intensity (proton beam current) was changed between the different irradiation periods.

The dose, D, for an object at a certain point in time of the irradiation test

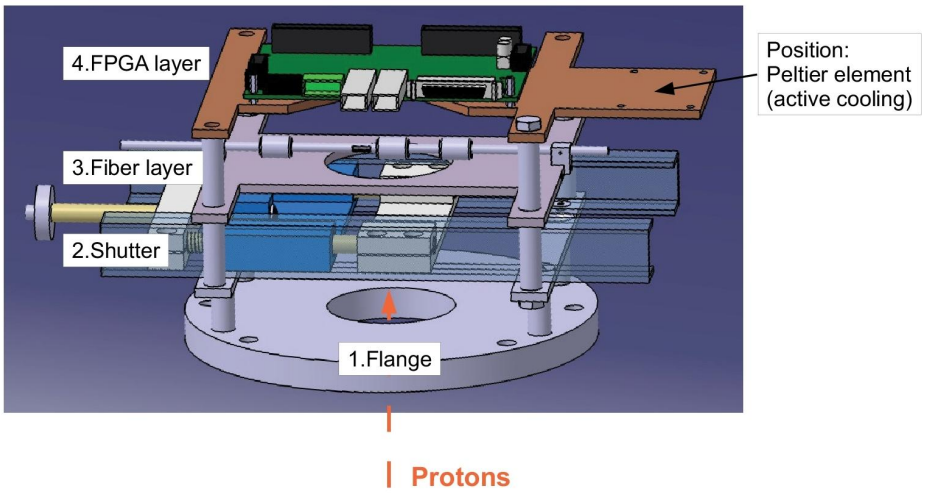


Figure 7.3: Schematic of the FPGA test board mounting frame. To irradiate the FPGA with protons, the FPGA test board is mounted to a frame which is screwed to a flange of a vacuum tank. The protons come out of the vacuum tank through a stainless steel window in the flange. The vacuum tank is placed at the end of the proton beam line of the area for biological irradiation experiments. The shutter layer is used as collimator for the beam profile measurement. The third layer, the so-called fiber layer, is used for an additional irradiation test of fibers. The fourth layer is made of copper and used as support structure and cooling with a Peltier element.

can be determined using the following formula:

$$D = C_{\text{fraq}} \cdot \frac{N_{\text{proton}} \cdot \Delta E}{M_{\text{object}}}, \tag{7.2}$$

$$N_{\text{proton}} = I_{\text{beam}} \cdot t_{\text{irr}}. \tag{7.3}$$

C_{fraq} is the fraction of the proton beam which passed the object which is calculated by the profile. N_{proton} is the integrated number of beam protons and can be determined with the beam current measurements, I_{beam}, of the Faraday cup and the irradiation duration, t_{irr}. ΔE is the energy loss of a single proton when it passes through the object and the mass of the object is M_{object}.

Beam profile measurement

The knowledge of the proton fluence through the FPGA is necessary to determine the exact total ionization dose deposited in the silicon of the chip. The proton fluence can be calculated with the relative proton beam profile and the proton beam current.

The proton beam profile was measured by collimating the beam perpendicular to the direction of the straw-tubes of an Outer Tracker test module and counting the number of protons passing each straw-tube of the test module.

The Outer Tracker straw-tube test module was placed in front of the flange with the electronics removed by mounting it to the radiation shielding box. In addition, the collimator was inserted in the shutter layer of the flange. Figure 7.4 illustrates the setup for the beam profile measurement. The collimator slit was perpendicular to the straw-tube direction and had a size of 50 μm. The length of the slit covered the whole circular flange window. The straw-tube module is 16 cm wide (32 straw-tubes) and 1 m long. Each straw-tube corresponds to a single detector channel. The readout board of the straw-tube module uses two VV50 pre-amplifier boards to amplify the signals of the 32 detector channels which are multiplexed with a relay to a single readout channel. The relay is controlled via a RS232 bus. In addition, this board provides the high voltage for the straw-tubes. The readout board output was connected to a discriminator of the LogicBox. The LogicBox is an universal, FPGA-based control & DAQ system, developed at the electronics department of the Physikalische Institut University Heidelberg [81]. The discriminated signals were used to count the number of protons passing a single straw-tube for time periods of 4 s. The counting was done inside the FPGA. The control of the readout board, LogicBox and also the measurement itself was realized with LabView 8.0.

During the profile measurement the collimator was moved in 0.5 cm steps in the y direction and for each collimator position the rate in each of the 32 straw-tubes was measured. Figure 7.5 shows the measurement result with the marked positions of the FPGA itself. The measured beam profile has an elliptic shape with the semi-major axis parallel to the X axis and the semi-minor axis parallel to

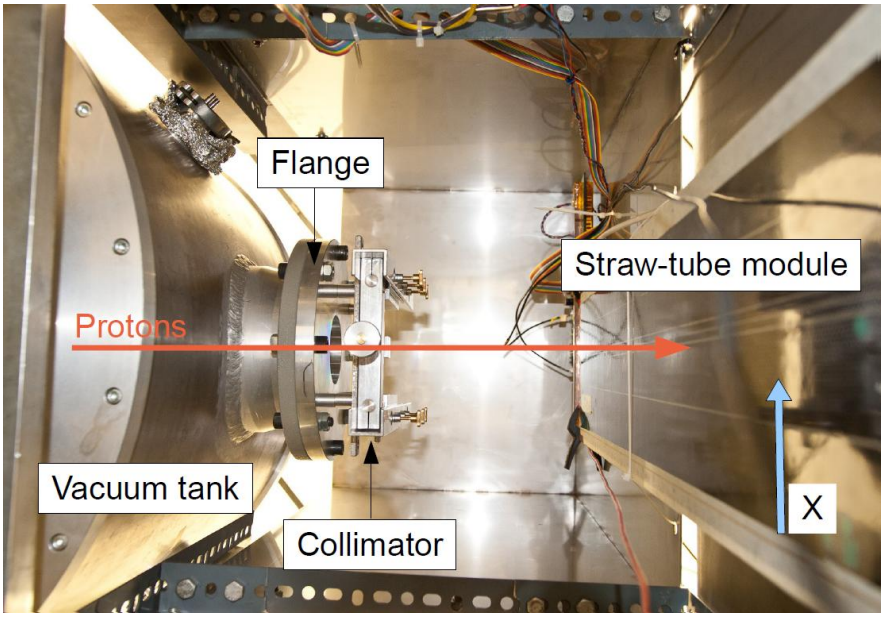


Figure 7.4: Beam profile measurement setup: the protons pass the 100 μm thick stainless steel window in the flange and the collimator before they hit the straw-tube module.

the Y-axis of the defined coordinate system. The center of the ellipse is roughly X=8.5 cm Y=0 cm. This flat shape in the middle is seen because for the center of the beam the measurement was in saturation. The FPGA was located in the center of the proton beam profile.

Fitting the proton beam profile

For the proton beam profile a 2 dimensional Gaussian was assumed. The parameters were determined by fitting a single Gaussian to the beam profile measurements in slices of the X and Y coordinates. Figure 7.6(a) and 7.6(b) show the beam profile data and the fitted single Gaussian for the X and Y slices around the center of the FPGA. The data in the center are excluded, because the measurement setup was in saturation.

These fits were done for all slices in X and Y coordinates. All show comparable results for the Gaussian mean and Gaussian width. The beam profile is crucial to determine the dose as it is needed to calculate the fraction of the beam current which crosses the object.

Furthermore, the measured beam profile has to be scaled down, because the beam width at the straw-tube module (the measurement layer) differs from the beam width at the FPGA layer. The proton beam was focused to the Faraday cup, see Figure 7.7. The scaling factor c_s can be calculated using the intercept theorem which results in $c_s = 0.9$.

Figure 7.8 shows the beam profile simulation which was used to determine the

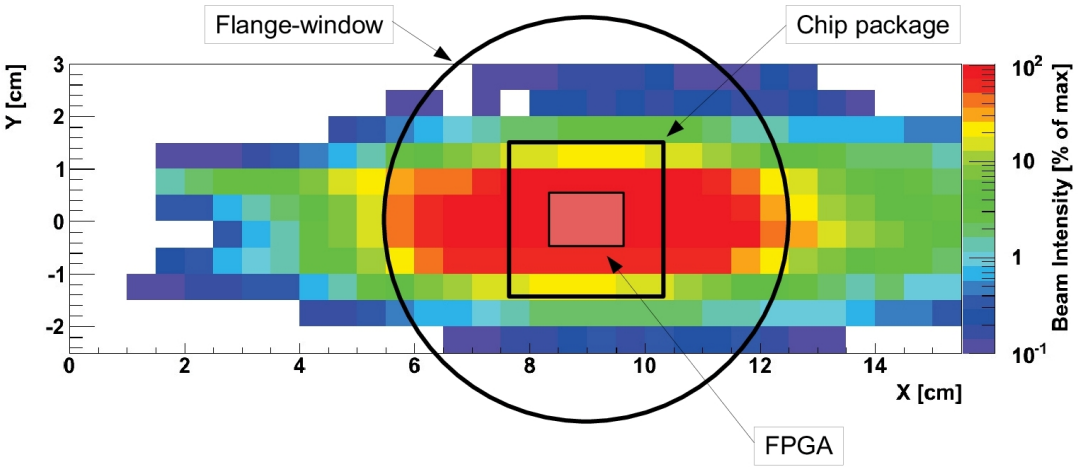
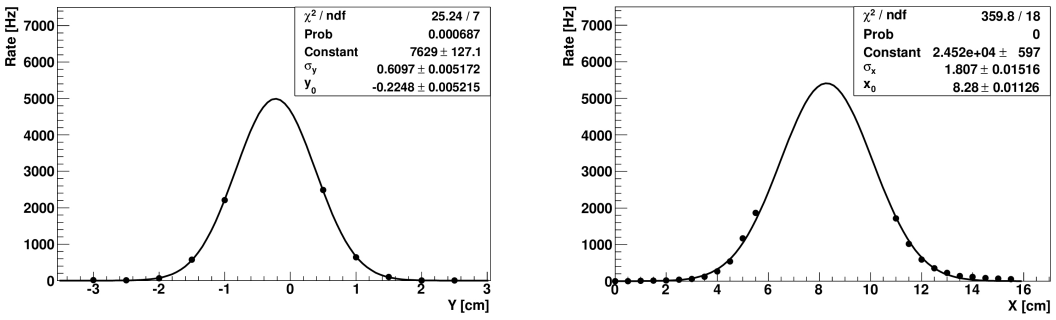


Figure 7.5: Beam profile measurement, the position of the FPGA and the flange window are shown. The FPGA was placed in the center of the flange window.



(a) Beam profile data and a single Gaussian fit in y direction for X=9 cm.

(b) Beam profile data and a single Gaussian fit in x direction for Y=0 cm.

Figure 7.6: Fits of single X and Y slices of the beam profile measurements at the position of the FPGA.

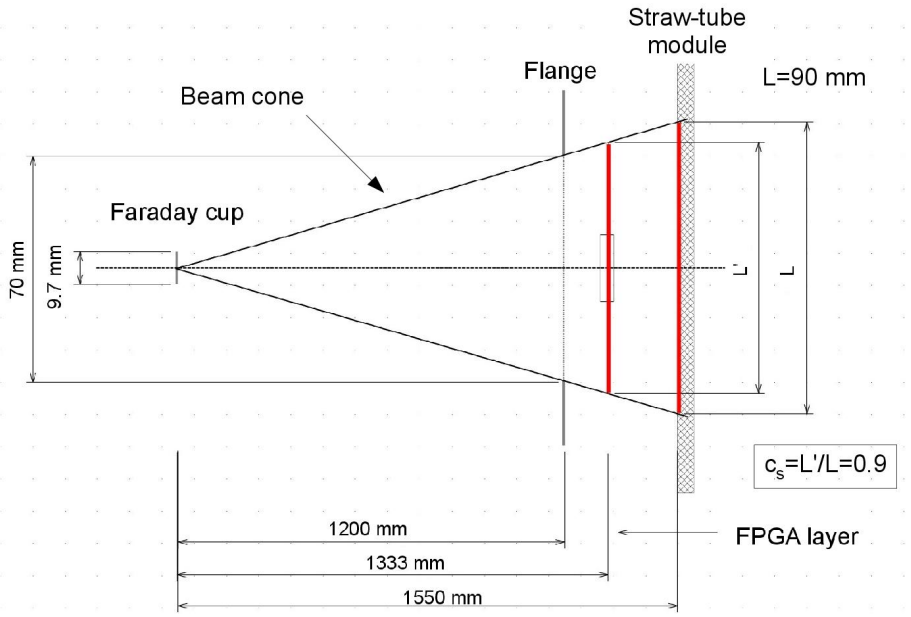


Figure 7.7: Beam cone schematic. The beam widens from its focus towards the FPGA and straw-tube module. This results in a scaling factor of 0.9 for the measured beam profile to get the the beam profile at the FPGA layer.

fraction of the beam received by the different objects. The profile P is parameterized using the following function:

$$P(x,y) = A \cdot e^{-\left(\frac{(x-x_0)^2}{2\cdot\sigma_x^2\cdot c_s^2}+\frac{(y-y_0)^2}{2\cdot\sigma_y^2\cdot c_s^2}\right)} \tag{7.4}$$

Where A is a constant, c_s is the scaling factor, x_0 is the mean of the beam profile in x direction (y=0 cm), σ_x is the width of the beam profile in x direction (y=0 cm), y_0 is the mean of the beam profile in y direction (x=9 cm), σ_y is the width of the beam profile in y direction (x=9 cm). The mean and width parameters are the fit results of the single Gaussian fits shown in Figure 7.6. The constant A is irrelevant for this study because only the fraction of the proton beam for a certain object is calculated with the beam profile. The constant A was set to 100.

The proton fluence accross the chip varies between -50% and $+40\%$ of the average proton fluence which is show in Figure 7.9. The beam variation over the chip has to be taken into account for the different irradiation measurements, when the internal FPGA structures are located only in a certain corner of the chip. 70% of the chip area was irradiated with at least the average proton fluence.

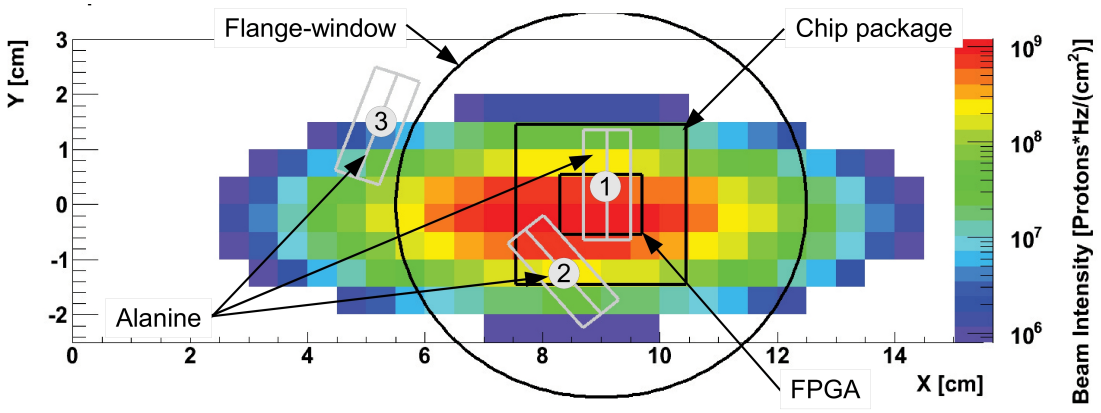


Figure 7.8: Beam profile simulation for 1 nA of proton beam current. The FPGA inside the package and the stainless steel window in the flange is depicted. In gray the position of the dosimeter pairs are visible. The FPGA received 21% of the proton beam.

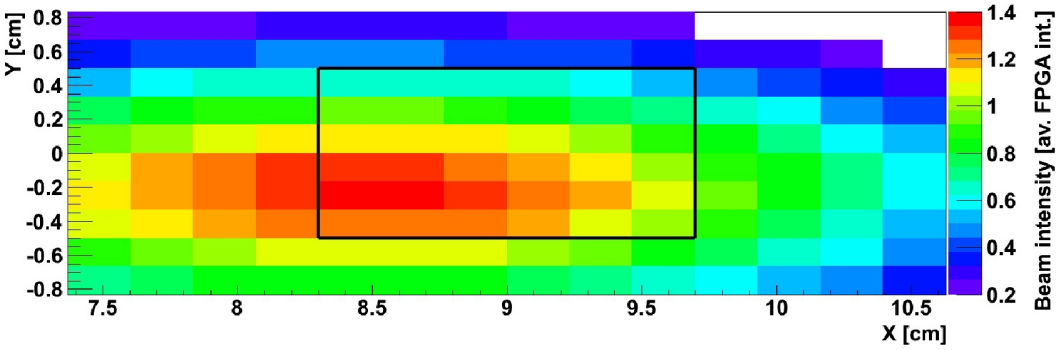


Figure 7.9: Chip irradiation homogeneity from simulation. The chip position is marked with the black rectangle. The variation is between -50% and +40% from the average proton fluence.

Object	Material	Object depth [mm]	Energy loss [MeV]	Proton energy after the object [MeV]
Flange window	Steel	0.1	1.2	20.8
Air	N_2 + O_2	133.3	0.4	20.4
FPGA package	Cu	0.5	9.6	10.8
FPGA chip	Si	0.5	4.7	6.1
Alanine stick	α-amino acid Paraffin wax	3.1	15.7	4.7

Table 7.2: Calculated proton energy loss in the different objects.

Energy loss calculations

The energy loss of the protons for the different objects of the irradiation setup was calculated using the ATIMA program[2] from GSI. The energy loss of the protons inside the alanine sticks has been determined with the help of the stopping power from the PSTAR data base of the National Institute of Standards and Technology's USA. The maximum energy of the protons at the Tandem-van-de-Graaff-Accelerator in Heidelberg is 22 MeV. In the Table 7.2 the energy loss inside the objects from the flange window to the FPGA chip or alanine stick are shown.

The largest energy loss stems from the FPGA package which is made of copper for cooling purpose. Nearly 50% of the proton energy is lost in the copper. The flange window and the air between the window and the alanine stick or FPGA package cause only a minor drop of the proton energy. The proton energy deposition in the alanine sticks and the FPGA are calculated as follows.

Alanine stick

The alanine stick has a cylindric shape of r=4 mm radius and l=20 mm length. The protons therefore traverse different amounts of alanine depending on the proton impact parameter with respect to the cylinder axis. A simplified shape is assumed with only one material thickness for the computation of the energy loss. This shape is cuboid with the same volume and width as the cylinder, its depth d_{eff} is given by

$$d_{\text{eff}} = \frac{r \cdot \pi}{2} = 3.14\,\text{mm}. \tag{7.5}$$

The protons enter the alanine stick with an energy of 20.4 MeV. For the energy loss ΔE calculation the rectangular alanine stick was cut into five equidistant slices and the energy loss in every slice was calculated individually using the formula

[2] ATIMA is a tool developed at GSI, which is used to calculate the slowing-down of protons or heavy ions in matter for specific kinetic energies [84]. The possible energies range from 1 keV/u to 500 GeV/u.

$$\Delta E = MSP \cdot \rho \cdot d. \tag{7.6}$$

There MSP is the mass stopping power which is the energy loss per length divided by the density of the object. The density is ρ and the thickness of the object is d. The energy loss inside the alanine stick amounts to ΔE=15.69 MeV. The results of the energy loss calculation can be seen in Figure 7.10.

The mass stopping power of water was used from the PSTAR data base [85] because the mass stopping power ratio of alanine and water are equal[3]. The corresponding mass stopping power for water and proton energies between 20 MeV and 8.5 MeV range from 26.07 MeV cm^2 g^{-1} to 52.02 MeV cm^2 g^{-1}. The density of alanine is 1.42 g cm^{-3}. A finer granularity than five slices is not improving the calculation due to the coarse granularity of the PSTAR data.

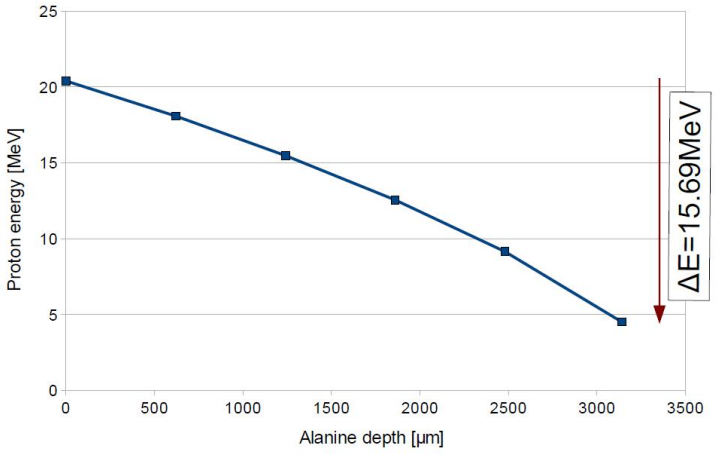


Figure 7.10: Calculation of the proton energy loss inside the alanine stick. The protons enter with a kinetic energy of 20.4 MeV. The stopping power from the PSTAR data base was used. Each proton loses roughly 15.7 MeV inside the alanine stick.

FPGA chip

The protons enter the FPGA chip with an energy of 10.8 MeV. The energy loss in the FPGA was calculated with the ATIMA tool and amounts to ΔE=4.7 MeV, see Figure 7.11. For this calculation the chip was approximated as a block of 14 mm×11 mm×0.5 mm of silicon. The energy loss was calculated in 250 slices of equal thickness. The mass of the silicon is 0.18 g with a density of 2.34 g cm^{-3}.

[3]Stopping power ratio alanine/water: 1 ± 0.03 [83, 86]

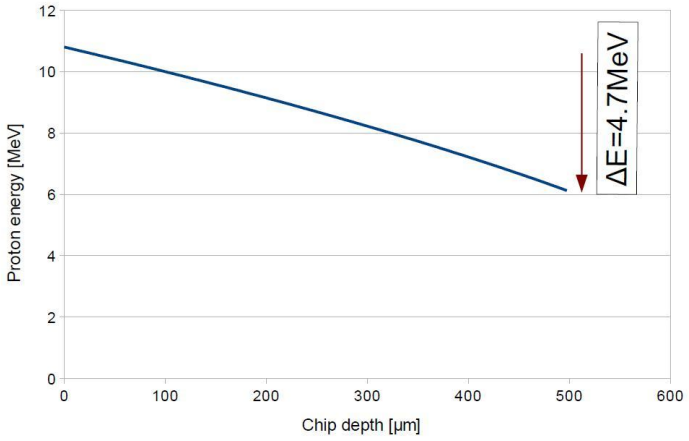


Figure 7.11: Calculation of the energy loss in the FPGA for 10.8 MeV protons. The ATIMA tool of GSI was used. Each proton loses roughly 4.7 MeV inside the FPGA.

7.4.2 Dose measurement

The previously mentioned alanine sticks were used as passive dosimeters and have a sensitivity from 10 Gy up to 122 kGy [82, 86]. The Figure 7.12 shows the schematic of one alanine stick. The sticks consists of α-amino acid and paraffin wax. One effect of ionizing particles in organic substances like α-amino acid is the generation of free radicals. The concentration of the radicals can be measured with electron paramagnetic resonance (EPR) spectroscopy. The total ionization dose measurement is done by comparing the EPR signal of the alanine stick before and after the irradiation.

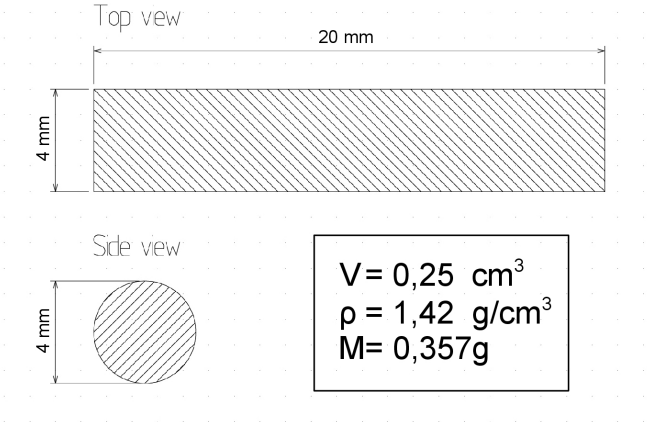


Figure 7.12: Schematic alanine stick passive dosimeter.

Six alanine probes were grouped in pairs and placed at three different positions

	Measured dose Probe 1 / Probe 2 [Mrad]	Simulated alanine dose Probe 1 / Probe 2 [Mrad]
Position 1	∼0 / 0.07	0.06 / 0.06
Position 2	0.15 / 0.25	0.12 / 0.32
Position 3	8.2 / 12.2(max)	7.9 / 14.0

Table 7.3: Comparison of measured and calculated total alanine dose. Relative uncertainty of the alanine measurements is ∼20% [86].

in the beam, see Figure 7.8. The first alanine stick pair was used only for the first irradiation period in front of the FPGA. The two other alanine stick pairs were placed next to the FPGA of the FPGA test board. The dosimeters collected the dose of the whole irradiation.

The measured total dose of all three pairs of alanine sticks are shown in Table 7.3. The relative measurement error for the alanine sticks is around 20% [86]. The expected doses of the simulation are compared with the measurements, in addition. The values are in very good agreement apart from the one in Position 1, there the alanine stick was not fixed well during the irradiation and moved out of the beam. For Probe 2 in Position 3 the maximum limit of 12.2 Mrad was reached. The alanine measurements confirms the calculated doses. From the good agreement for the alanine sticks it is concluded that the TID calculation of the FPGA is correct within errors.

7.5 FPGA firmware

In this section the firmware of the Arria GX FPGA for the irradiation test is presented. The firmware was designed to perform several tests in parallel. The stability of the time measurement, the data transmission with the GBit/s transceivers and the number of single event upsets were tested, controlled and monitored via an I^2C bus. The stability of the configuration registers was checked with a predefined block from Altera which was activated in the Quartus II compiling options (CRC option). This block is completely independent from the user firmware.

A block diagram of the user firmware is shown in Figure 7.13. The firmware consists of five main parts:

- The 32 channel 5 bit TDC developed for the LHCb Outer Tracker upgrade as described in Chapter 5.4.
- The bit error probability tester, see Subsection 7.6.6.
- A single event upset (SEU) tester, see Subsection 7.6.7.

- An I²C bus slave.
- TDC transmitter block to readout four TDC channels to a second FPGA, see Subsection 7.6.6.

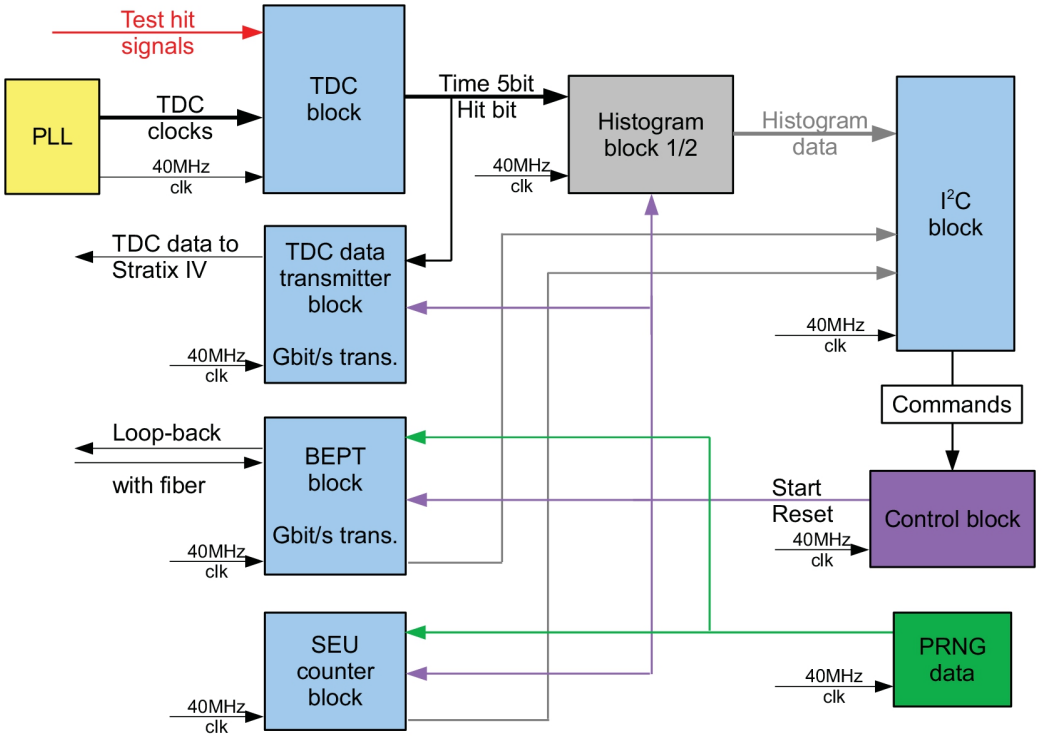


Figure 7.13: Block diagram Arria GX FPGA firmware for irradiation test

The whole firmware takes roughly 80% of the FPGA resources, which is visible in the Figure 7.14.

Only the I²C slave is be described here, all the other firmware blocks will be described in detail in the corresponding measurement subsection.

7.5.1 I²C bus slave

The I²C bus slave finite state machine (FSM) has been modified with Hamming encoding to detect and correct single bit errors in the FSM states. In addition, the state registers were realized with triple modular redundancy (TMR). This effort was necessary to ensure a reliable communication during irradiation.

To test the proper implementation of the Hamming encoding it is possible to invert the fifth state bit, using the user dip switch on the PCB. When Hamming encoding is used, the I²C bus slave continues to work even with an inverted fifth

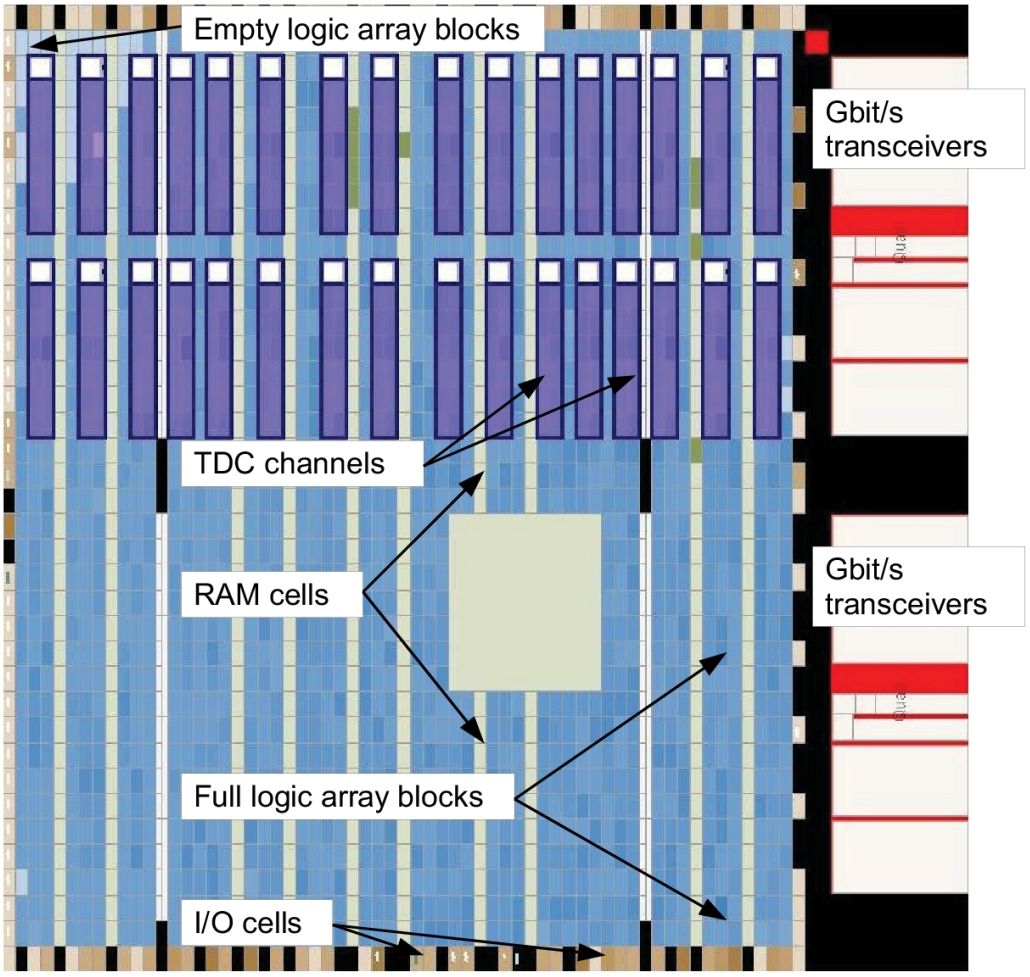


Figure 7.14: The chip planner of the FPGA firmware for the irradiation test. Roughly 80% of all logic array blocks are used, the small blue rectangles show full logic array blocks and the small light blue rectangles show empty ones. The 32 TDC channels are surrounded by the dark blue rectangles.

state bit. With normal encoding the I^2C bus slave crashes after triggering the state bit inversion.

7.6 FPGA irradiation measurements

The 22 MeV proton beam was used to irradiate two Arria GX FPGAs and an integrated dose of 7Mrad (31Mrad) for the first (second) FPGA was reached. The corresponding integrated proton flux is $1.2 \cdot 10^{13}$ protons/cm^2 ($5.3 \cdot 10^{13}$ protons/cm^2). The irradiation was split in several irradiation periods of different length varying from 1 to 45 minutes and different radiation levels. The proton beam currents varied from 22 pA to 7.5 nA for the different irradiation periods in which the FPGAs received integrated doses between 4.5 krad to 5 Mrad. The FPGA was controlled and monitored over the I^2C bus. When the communication stopped due to finite state machine failures caused by the irradiation, it was re-established after the irradiation periods, using a power cycle of the FPGA test board. The finite state machine failure can be caused by a changed firmware. During the breaks between the irradiation periods the following tests were done at least once: stability test of 8 channels of the implemented 32 channel TDC, reliability test of the data transmission with two 3.125 GBit/s optical transceivers and single event upset tests of user flip-flops.

7.6.1 Temperature

It is important to measure and control the temperature to interpret the TDC results because a change of the chip temperature can influence the timing of the chip. The FPGA board was actively cooled with a Peltier element, and the temperature was stable during the irradiation. This was checked using a digital multimeter and a K-type thermocouple, which was placed at the edge of the package. The temperature measurement was done only for the FPGA test board I, because the cooling plate was radioactive afterwards and a safe handling was impossible. The multimeter was connected via USB to the control and measurement PC. A program read the temperature every 3 s and wrote the measurements with a time stamp to an ASCII file. The precision of this measurement is 1 °C.

Results

The temperature of the FPGA package was stable. Figure 7.15 shows the temperature as function of time. Three periods are indicated. The first was a testing phase without irradiation (a so called "dry test") marked with a green arrow. The second period was the irradiation period marked with a red arrow and the last period after irradiation is marked with a blue arrow. During the irradiation the FPGA package temperature was stable at (30 ± 1) °C. Only at the end of the red marked period, at the time point of 01:30 AM, the power of the board was off

for seven minutes. A temperature drop is visible as well as a rise back to 30 °C once the power was restored. During the last period the FPGA and the FPGA test board I were switched off.

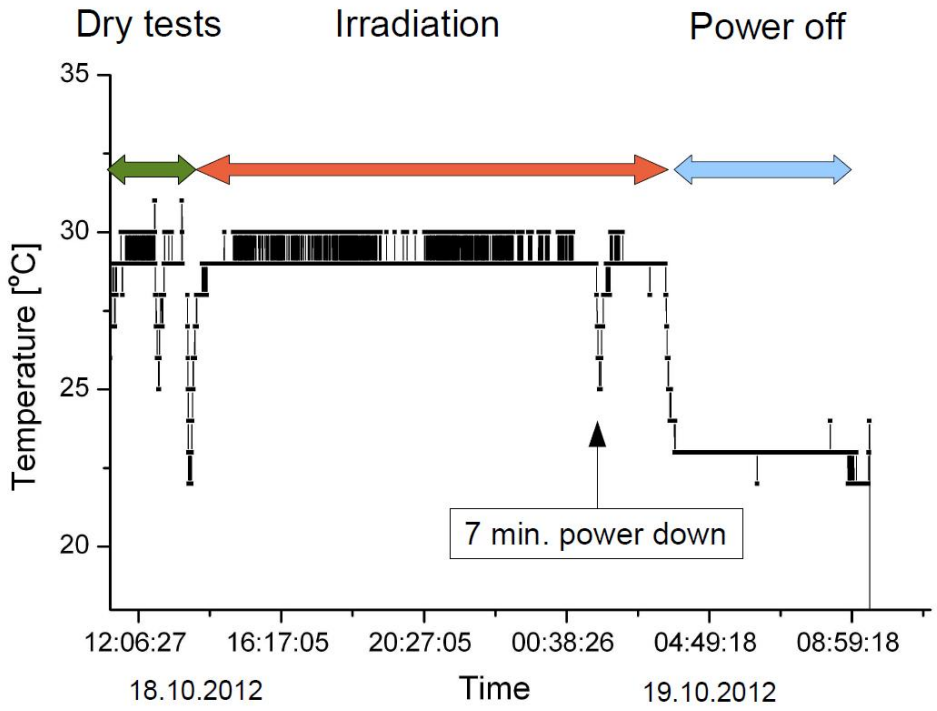


Figure 7.15: Monitoring of the FPGA package temperature of the FPGA test board I during the irradiation.

7.6.2 Electric currents

The monitoring of the electric current during the irradiation is important to detect first signs of irradiation effects in the FPGA. The currents can rise due to increasing leakage currents which can disturb the functionality of the chip. The current monitoring was done by two methods. The first method reads the HAMEG HMP4040 power supply to measure the currents of the ±5 V supply voltages. The second method uses an indirect current measurement with shunt resistors on the test board. The voltage drop over these resistors was measured with a 8 channel 14 bit ADC of the LogicBox. The parasitic resistors were chosen to be as small as possible to avoid malfunctions of the FPGA test board. The chosen resistors had values between 0.15 Ω and 6.2 Ω.

Currents of different parts of the FPGA were monitored. These parts are the internal logic arrays (core current), the six I/O banks (I/O current), the phase-looked loops (PLL current) and the GBit transceivers (analog currents and digital

current). Furthermore, the current of the 100 MHz oscillator was monitored which provided the clock for the FPGA PLLs.

Results

All currents were observed to be stable up to doses of 150 krad. Above this the first permanent increase from leakage currents becomes visible in the FPGA core current. The FPGA core current of the test board I is shown in Figure 7.16. The level of the default core current rises in total by 6.5% after an integrated dose of 7 Mrad. The core current of the second FPGA shows a similar rise after 31 Mrad.

During runs with high irradiation intensities, larger than $2 \cdot 10^5$ times the intensity expected for the LHCb upgrade, drops and spikes of the current are observed which are explained by partial loss of the firmware configuration. This disappears directly after a power cycle and a re-programming of the FPGA.

The current of the +5 V supply voltage gives the same results as the FPGA core current. The current of the digital part of the GBit transceivers rises by 5% after a dose of 7 Mrad. The same rise is visible for the FPGA test board II after 31 Mrad. All these changed could be explained with rising leakages currents.

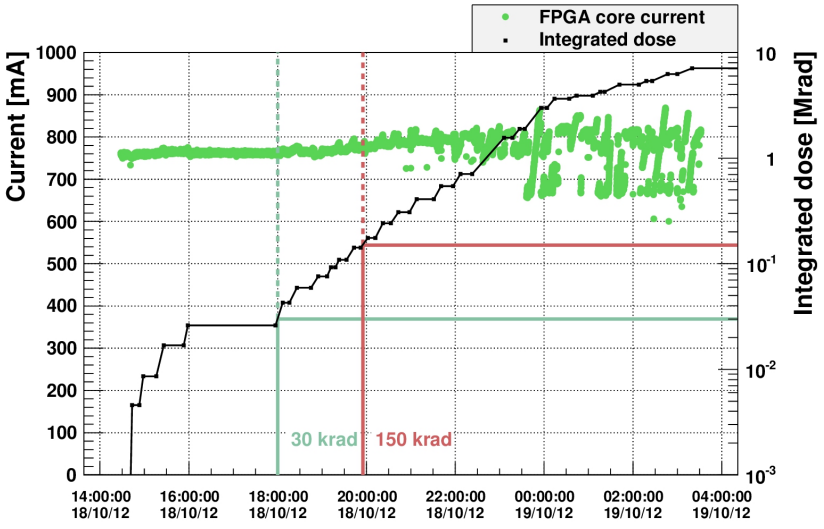


Figure 7.16: FPGA core current (green) of the FPGA test board I as a function of time. Also shown is the accumulated dose (black). In total the current rises by 6.5% after a integrated dose of 7 Mrad. The large current variations during the high intentsity irradiation are caused by radiation induced changes of the FPGA firmware configuration.

After 400 krad, the I/O current starts to decrease and, by the end of the irradiation, has decreased by 6%, which can be seen in Figure 7.17. The FPGA test board II shows a drop in the I/O current of 20% after an integrated dose of 31 Mrad. The decrease of a current was not expected and is difficult to explain. One possibility to interpret the decrease is the loss of I/O cells which reduces the I/O current [87].

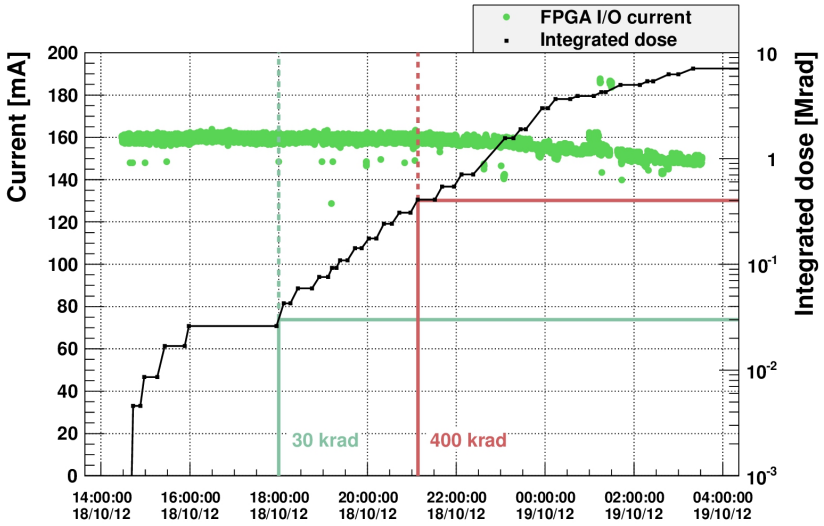


Figure 7.17: FPGA I/O current (green) of the FPGA test board I as function of time. Also shown is the accumulated dose (black). In total the current drops by 6% after an integrated dose of 7 Mrad.

The PLL current and the transceiver analog currents did not show permanent irradiation effects. The current of the −5 V supply voltage is stable at all times.

All permanent current changes of the different FPGA parts are between 5 % - 20 %. From the current measurements, the TID hardness of the chip appears to be high enough for the expected total ionization dose at the upgraded LHCb Outer Tracker.

7.6.3 Firmware errors

Since the Arria GX FPGA is an SRAM-based FPGA, measuring radiation induced modifications of the configuration firmware in the irradiation test is crucial. The function of the FPGA depends on the correct firmware stored in the configuration registers. The different configuration registers have different tasks, like routing, lookup table function or, even more critical PLL configurations. This

means it is important to measure the cross section for irradiation induced configuration flips which depends on different parameters like particle type and energy or the design of the SRAM cell itself.

The Arria GX FPGA has the possibility to test the current firmware, using a cyclic redundancy check (CRC)[4]. If the CRC test block finds a single error inside the configuration registers it sets the CRC pin high. This test is running in an endless loop and it takes 2 μs to test the entire configuration.

During the irradiation test this pin of the FPGA was monitored. It was possible to inject a test CRC error for debugging purpose. When a firmware error was detected the firmware was reloaded from a flash memory which is located on the FPGA test board behind the cooling plate and hence shielded against the radiation. The CRC pin is set to low after the firmware has been reloaded. The reload of the firmware takes about 1 s.

Results

The firmware error rate was measured at the beginning of the irradiation of the FPGA test board I. Every time a configuration bit flip was detected, the FPGA was power cycled to reload the correct firmware and to restart the measurement. Figure 7.18 shows the measurement results. The number of firmware errors (CRC counter) N_{errors} increased during irradiation and reached 10 at the end. The proton flux during the test corresponds to an irradiation intensity of 54,000 times the expected LHCb upgrade intensity. The effective measurement time Δt is 279 s. The average time between a power cycle and a configuration bit flip is (27.9 ± 3.2) s. The proton cross section for a configuration register flip σ_{CRC} is calculated with the following formula

$$\sigma_{\text{CRC}} = \frac{N_{\text{errors}}}{\Delta t \cdot F_{\text{proton}} \cdot N_{\text{conf.cells}}}. \tag{7.7}$$

Where the number of configuration SRAM cells $N_{\text{conf.cells}}$ for the used Arria GX FPGA is 9,640,672 [92] and the average proton flux F_{proton} during the test was $2.3{\cdot}10^7$ protons Hz/cm^2. The proton cross section for a configuration register flip results to $1.6 \cdot 10^{-16}$ cm^2/ per bit.

Comparision with other measurements.

The 22 MeV proton cross section for configuration bit flips is a factor 5-50 smaller than for cross section measurements of older SRAM-based FPGAs from Xilinx and Altera[89, 90, 91]. It must be taken into account that the older measurements

[4]The CRC is an error-detecting code used to check for changes in stored data. A check value is calculated from the data and stored with them. The calculation is a polynomial division and the check value is the rest of the polynomial division. The data are checked by redoing the polynomial division including the check value. If the result is not equal to zero the stored data have changed. For more details see [88]

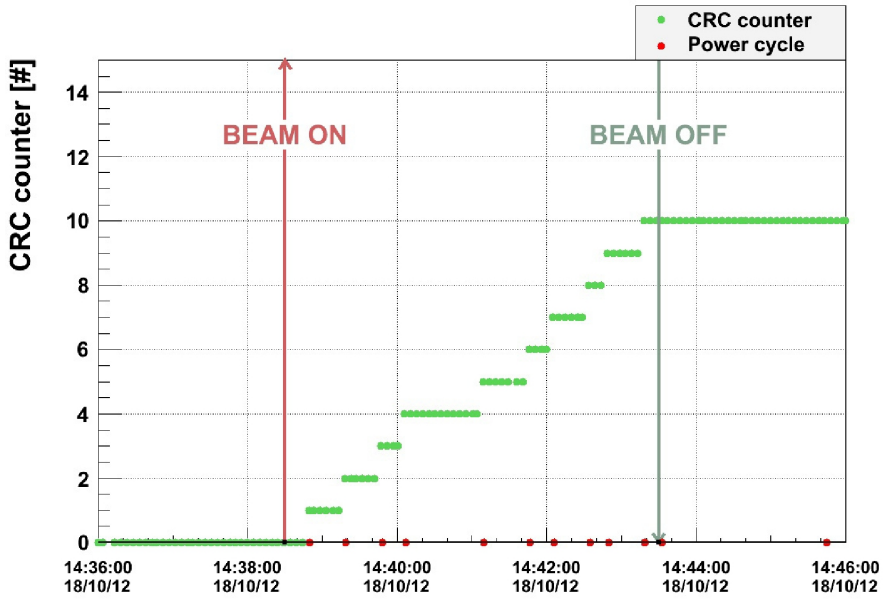


Figure 7.18: Increase of the number of configuration register flips (green) as function of time. The test was performed with an average proton flux inside the FPGA of $2.3{\cdot}10^7$ protons Hz/(cm^2). Power cycles to reload the firmware are shown in red.

were taken with FPGAs using transistor gate lengths larger than 100 nm which can explain the deviation of the measurements by the technology size of the older SRAM cells.

Consequences on operation in the LHCb upgrade

The expected rate of firmware errors for the LHCb upgrade intensity can be calculated, scaling the time for a configuration flips of 27.9 s during the irradiation test to the expected LHCb upgrade irradiation environment. The result would correspond to a firmware error rate of $6.6{\cdot}10^{-7}$ Hz/FPGA. However the measurement was performed with 22 MeV protons for which the configuration bit flip probability is about a factor 3 smaller than for higher energy protons. Nevertheless the error rate seems manageable for the LHCb upgrade. A further test is recommended to confirm this indication with an irradiation test using 60 MeV protons.

7.6.4 TDC stability

The TDC developed for the Arria GX FPGA was tested during and after the irradiation. The TDC design is described in Chapter 5.4. Here, the stability of the time measurement was checked, using a hard-wired timing signal: The

20 MHz system clock was looped back with a cable from one LEMO output to 4 TDC channels. The readout of the TDC data was via the modified I^2C bus slave.

Results

The two tested FPGAs show different behaviors, which will be described in the following. In both cases the time measurement remained stable up to integrated doses much higher than the expected 30 krad for the LHCb Outer Tracker upgrade.

Test of the FPGA test board I

All 4 tested TDC channels (2,3,4,5) show the same behavior. The results for channel 2 are shown in Figure 7.19. The time measurement is stable until the dose reaches 400 krad. Afterwards, the measurement shows a drift. Every time the radiation was switched off, the measured time value goes back rapidly to the expected level of 13. This could possibly be related to a loading effect which changes the threshold voltages and thereby the time behavior.

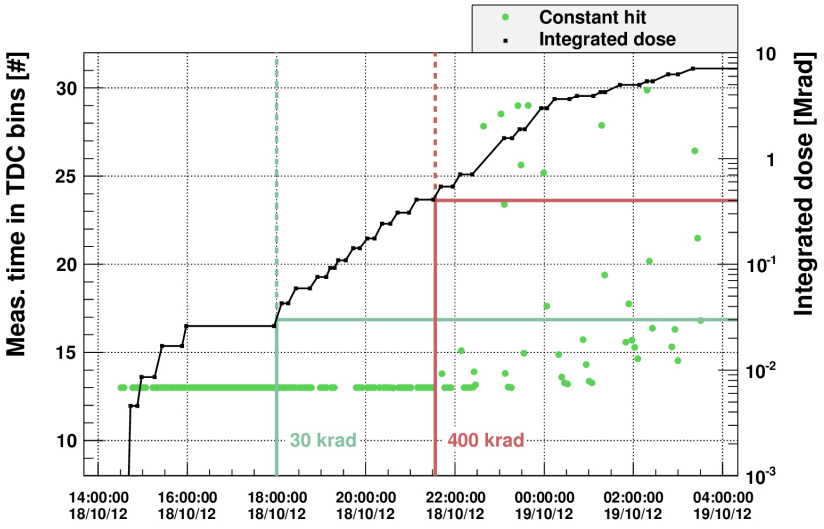


Figure 7.19: Measured time value for a constant timing signal (green) for TDC channel 2 on the FPGA test board I as function of time. Also shown is the accumulated dose (black). The times are stable until 400 krad.

Test of the FPGA test board II

All 4 tested TDC channels (2,3,4,5) show again the same behavior. The results for channel 2 are shown in Figure 7.20. The time measurement remained stable until 4 Mrad. After this, the measurement shows a shift from 13 to 15. The

shift is permanent. Even 25 days after the irradiation campaign, in the lab, the measurement showed a constant value of 15. The shift corresponds to 1.6 ns.

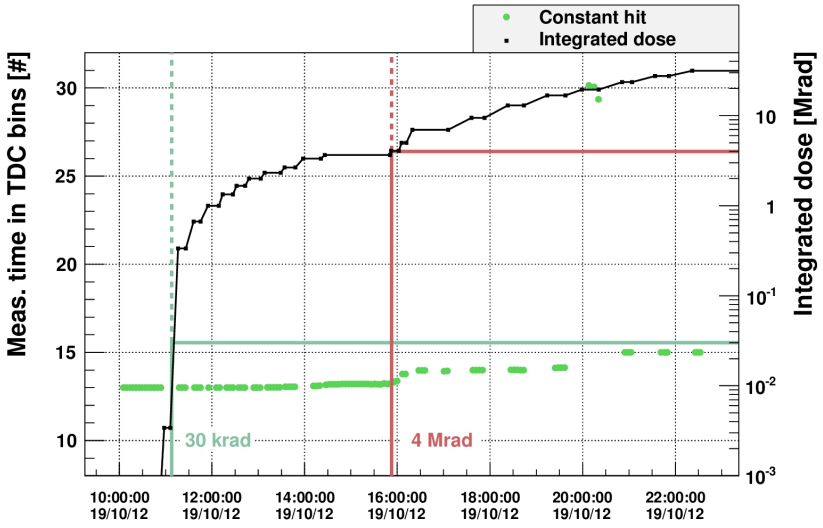


Figure 7.20: Measured time value for a constant timing signal (green) for TDC channel 2 on the FPGA test board II as function of time. Also shown is the accumulated dose (black). The drift time starts to drift after roughly 4 Mrad and reaches TDC bin 15 after 20 Mrad.

7.6.5 Phase-locked loop stability

The stability of the FPGA phase-locked loops (PLLs) are crucial for the stability of the time measurement of the TDC and the data transmission with the GBit/s transceivers. Therefore, it was important to monitor the behavior of the PLLs before, during and after the irradiation. Two types of PLLs were tested. The stabilities of one PLL for the internal clock signals and one fast PLL for the GBit transceivers were monitored with a 1 GHz oscilloscope[5] using a custom LabView 8.0 program. The program writes measurements with a time stamp to an ASCII file every 3 s.

For the internal clock signal PLL the frequencies of the fast TDC clock (312.5 MHz) and the system clock (19.8 MHz) were monitored. In addition, the phase between the two clocks was measured.

The fast PLL of the GBit transceivers was tested by monitoring the clock frequency of the Arria GX transceiver serializer (156.25 MHz). The test setup

[5]TEK DPO4104B with 5 GS/s

used the FPGA test board connected with one SFP[6] module and an optical fiber to a Stratix IV development board [93]. The TDC data of four channels were transmitted with 3.125 GBit/s to this second FPGA, which was placed outside the radiation shielding. The receiver of the Stratix IV FPGA recovered the transmitter clock from the bit stream. The de-serialized transmitter clock was routed to an SMA output and connected to the 1 GHz oscilloscope to monitor the clock frequency of the Arria GX transceiver serializer, which uses the fast PLL.

Results

The three clock frequencies measured with the oscilloscope are stable over the entire test reaching up to 7 Mrad. The FPGA test board II showed the same result reaching an integrated dose of 30 Mrad.

The phase between the fast counter clock and the system clock was stable at -150° up to 3 Mrad. Afterwards the phase became unstable and was shifted to higher values, this can be seen in Figure 7.21. The PLL is a analog circuit with three blocks: the phase detector, the charge pump and the voltage controlled oscillator. These blocks are used to generate an output signal whose phase is related to the reference signal. The phase of the output signal and the reference signal is compared by the phase detector which controls the charge pump. The charge pump controls the phase and frequency of the voltage controlled oscillator. A malfunction of the phase detector could explain the measurement of the clock phase.

The monitored PLLs sustained the TID of the expected upgrade environment with large safety factors.

7.6.6 GBit/s transceiver tests

The FPGA test boards host two GBit/s optical SFP modules which are connected to the GBit/s transceivers of the Arria GX FPGA. They were tested during and between the different irradiation periods. Two different methods were used. The first method used a bit error probability (BEP) test of a looped back data transmission on the same board. For this, the transmitter port was connected with the receiver port of the same SFP module with an optical fiber. The second method checks if it is possible to send valid TDC data to a second FPGA. In the following, the setup and the results of these two methods are shown.

First method: Bit error probability measurement

To measure the bit error probability (BEP) a loop-back is realized using a 20 m optical fiber[7] and a SFP transceivers module from Avago (AFBR-57D7APZ).

[6] Small form-factor pluggable transceiver

[7] LEONI GigaLine I-V(ZN)H 2X 1G50/125 STB900 2,8

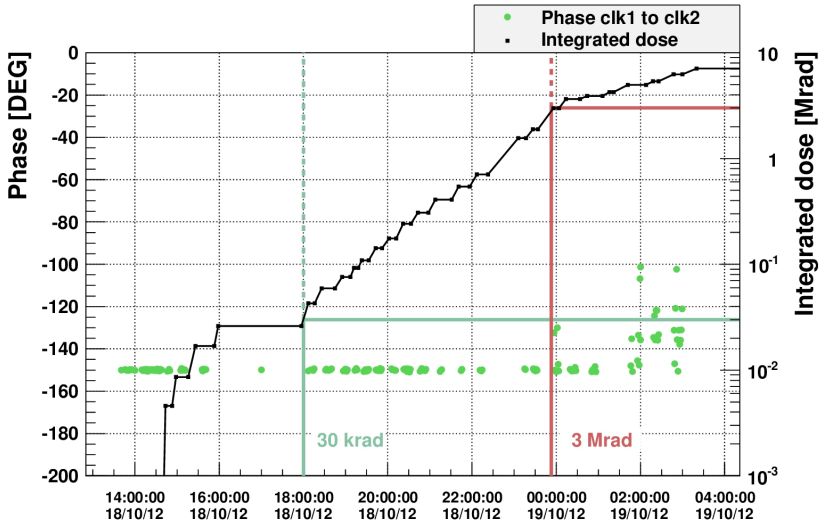


Figure 7.21: PLL phase value during irradiation. The monitored phase between the fast counter clock and the system clock is visible (green) and stays stable until a dose of 3 Mrad. After 3 Mrad the phase is not stable anymore and tends to shift. The data shown is taken between irradiations. The integrated dose is plotted in black.

These modules are multi-rate 850 nm SFP transceiver which are specified up to 8.5 GBit/s. The GBit/s transceiver transmits **p**seudo **r**andom **n**umber **g**enerated (PRNG) data with a data rate of 3.125 GBit/s, the maximum speed of the FPGA transceivers. The bit error probability is calculated by comparing every transmitted byte with the corresponding received byte and counting the number of differing bits. The number of errors is divided by the total number of tested bits.

In the following, the block diagram of the bit error probability measurement is described, see also Figure 7.22. The test data are generated with a PRNG block or, alternatively, with a counter. The PRNG data bits change homogeneously independent of their significance which is not the case for the counter generated data. The counter data was used for debugging purpose. The selection between counter and PRNG data is done with a multiplexer.

The transceiver control block manages the initialization process for the GBit/s transceiver, the bit alignment every 2.5 million clock cycles, and a write request inhibit for the delay FIFO (first in first out memory) for all data before the finished start sequence. For the initialization the analog and digital parts of the transceiver are reset in a cycle defined by Altera [94].

In addition, if a BEP measurement is started, a start pattern is sent through the loop-back before the counter or PRNG data are sent. This enables the receiver part of the BERT block to identify the start of the transmitted data package. The transceiver control block is controlled via the I^2C bus. After the transceiver control block, the data is written to the transceiver FIFO to change the clock domain. Three different clocks are used in the BEPT block, all running with the same frequency of 156.25 MHz. The Altera transmitter data input block and the receiver data output block are running with the internal transmitter and receiver clocks, which makes changing the clock domain before transmitting and after receiving the data necessary.

The FIFO control blocks are used to request writing and reading of the FIFO memories. The depth of the FIFOs are 256 words and the fill state of the FIFOs were monitored via I^2C.

After passing through the Altera transmitter/receiver block the data is synchronized to the system clock domain with the receiver FIFO. The start pattern detect block searches for the start pattern and enables the readout of the delay FIFO on the transmitter side. The received data is delayed by one additional clock cycle with a delay register. The start pattern triggers the comparison of transmitted and received data.

A bit flip between the two data words increments the bit error counter. The BEPT control block starts the BEP measurement and counts the number of tested bits. The amount of bits to test is programmed into the BEPT control registers.

Effects related to TID: Before the irradiation, the BEP was found to be smaller than 10^{-15} errors per bit, testing one link for one week at 3.125 GBit/s without a single bit error.

In the breaks between the irradiation periods, the bit error rate test ran only

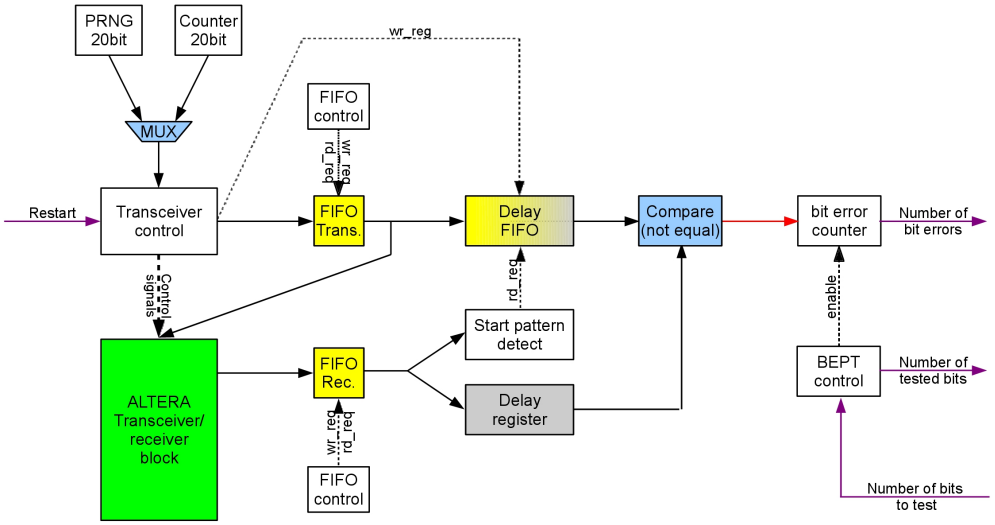


Figure 7.22: Block diagram of the bit error tester.

periods of up to 10 minutes. No bit error was found for the FPGA test board I in the breaks. The BEP can only be constrained to be below the level of 10^{-11} errors per bit. This value did not change during the irradiation campaign of the FPGA test board I. The same test was performed 25 days after the irradiation campaign and the BEP was determined to be smaller than 10^{-14} errors per bit. The GBit/s transceiver obtained an integrated dose of 7 Mrad and is still functional.

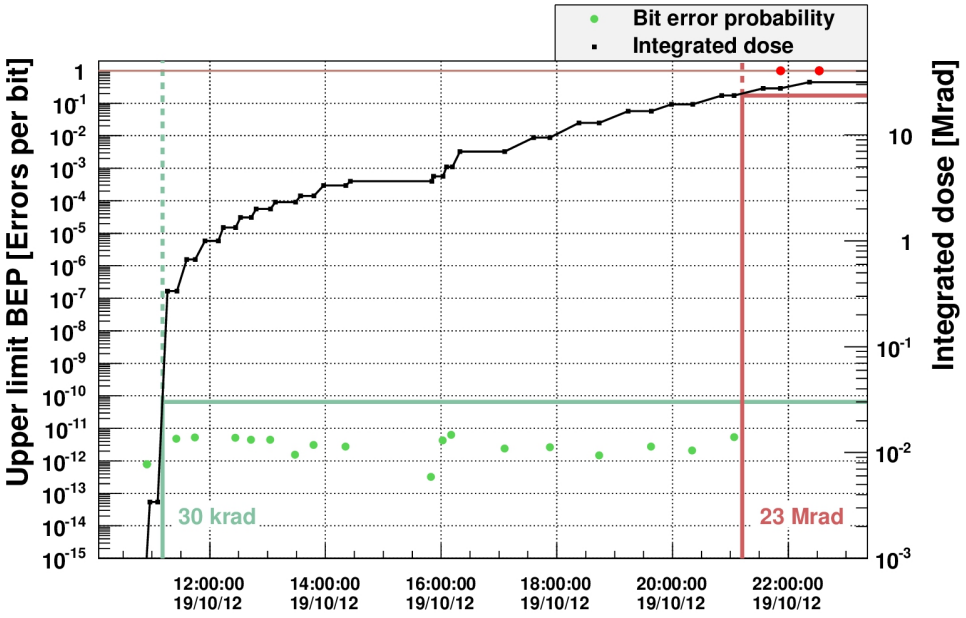


Figure 7.23: Upper limit for BEP (green) FPGA test board II during irradiation periods. After 23 Mrad the transceiver stopped working, a BEP of 1 per bit is visible. The integrated dose is plotted in black.

The BEP of the FPGA test board II is shown is Figure 7.23. For almost the whole irradiation campaign of the FPGA test board II, the result is the same as for the FPGA test board I. The BEP is found to be smaller than 10^{-11} errors per bit. After 23 Mrad, the transceiver stopped working. From this point in time onwards the encoded data of the GBit/s transceivers showed permanent bit alignment errors which makes a data transmission not possible any more.

Effects related to single event upsets: During the irradiation periods three types of errors were detected when operating the GBit/s transceivers. The single bit flip of a transmitted bit is by far the error with the lowest probability. Only one bit flip was detected during an irradiation period of the FPGA test board I 1 minute with an intensity of 167,000 times the expected LHCb upgrade

intensity. All other irradiation periods showed no single bit flip for a transmitted bit.

The second effect, occurring at a much higher rate, is the loss of the bit alignment. This loss is recovered by the transceiver control block automatically by sending a bit alignment pattern, a so called comma word. This was done every 2.5 million transmitted words. It is possible to optimize the transceiver control block, so an alignment bit loss is always detected automatically and an alignment word is send directly after.

The third effect observed is the loss of synchronization between the transceiver and the receiver. The transceiver control block could not recover this problem. In these cases the error counter continued to increase even without irradiation until the next FPGA power cycle. A power cycle of the FPGA was necessary with a new initialization of the transceiver block.

Figure 7.24(a) and Figure 7.24(b) show the frequency of the loss of bit alignments and the loss of synchronizations between transmitter and the receiver as a function of the proton fluence. Both data samples were fitted with a linear function constrained to no error without irradiation.

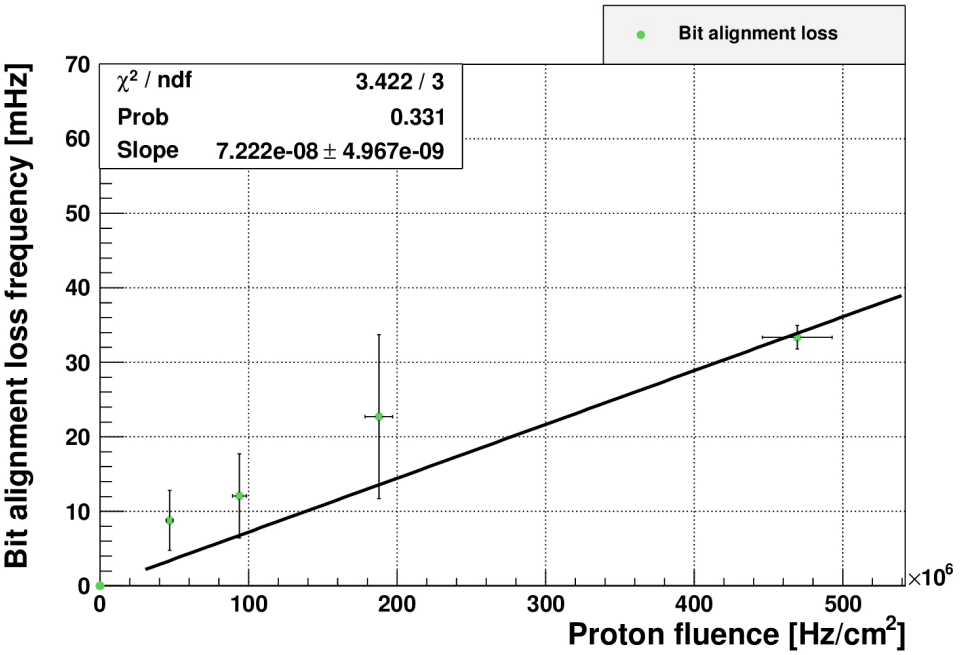
The 22 MeV proton cross section for the bit alignment loss is $(1.3\pm0.5)\cdot10^{-10}\text{cm}^2$ per transceiver.

The 22 MeV proton cross section for the loss of synchronization between transmitter and receiver was determined to be $(8\pm4)\cdot10^{-11}\text{cm}^2$ per transceiver. For the upgrade of the LHCb Outer Tracker a manual reset of a single GBit/s transceiver is expected every $3 \cdot 10^7$ s by scaling this to the LHCb Outer Tracker readout electronics upgrade radiation environment of $2.8 \cdot 10^{-7}$ krad/s. However the measurement was performed with 22 MeV protons for which the bit flip probability is smaller than for higher energy protons. Nevertheless the error rate seems manageable for the LHCb upgrade. A further test is recommended to confirm this indication with an irradiation test using 60 MeV protons.

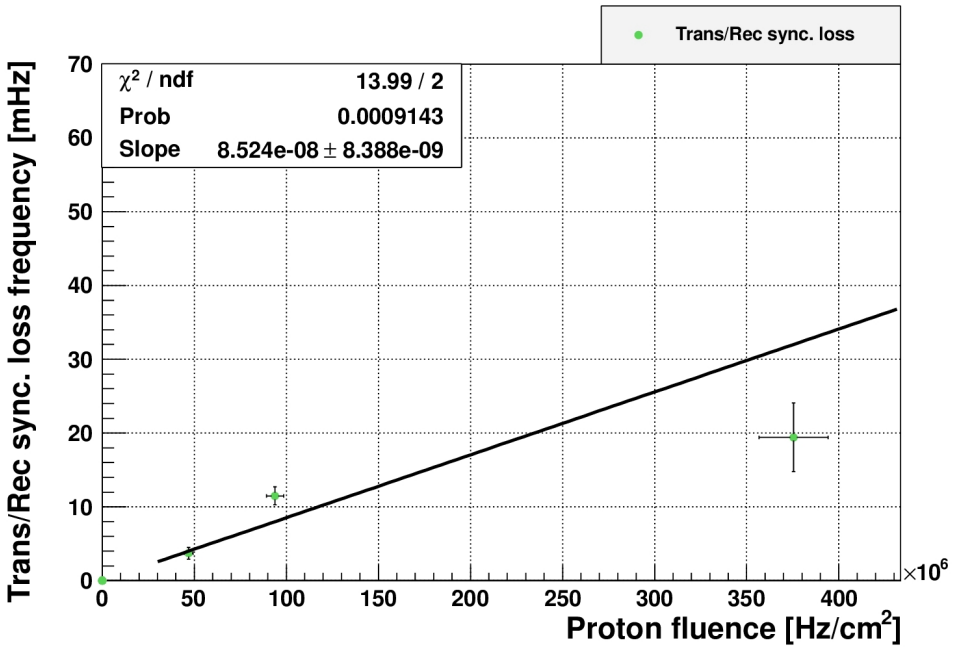
Second method: Data transmission to the Stratix IV development board

The second method confirmed the results of the BERT. The GBit/s transceiver of the FPGA test board I sustained the 7 Mrad TID and is still working, the GBit/s transceiver of the FPGA test board II stopped working after 23 Mrad.

For this method, the data of 4 TDC channels were transmitted with the second optical 3.125 GBit/s transceiver to a second FPGA board (Stratix IV development board). The data were analyzed on the Stratix IV and written into histograms. It was checked if valid TDC data were transmitted. The Stratix IV development board was placed behind the radiation shield and was readout via the I^2C bus. Between the FPGA test board and the Stratix IV development board a mezzanine board for the Stratix IV board was placed, to convert the optical signals from the fiber into electrical signals for the Stratix IV GBit/s receivers.



(a) Bit alignment loss frequency as function of the proton fluence.



(b) Transceiver de-synchronization frequency as function of the proton fluence.

Figure 7.24: Frequency of the two detected effects during the bit error measurements as function of the proton fluence.

This 8 SFP transmitter/receiver mezzanine board for the Stratix IV board was developed by the LHCb group at the Technische Universität Dortmund.

7.6.7 Single event upsets

The single event upset (SEU) rate for the flip-flops was measured using triplets of flip-flops where a bit flip can be detected using a majority logic. PRNG data had been written to 4608 flip-flops in total. If a single flip-flop of a triplet showed a flip the single event upset counter was incremented by one.

Results of the SEU measurement

No SEU was detected with the 4608 flip-flops during the irradiation campaigns of both FPGA test boards. The highest proton flux F_{proton} tested was $1.9 \cdot 10^8$ protons $\cdot$ Hz/cm^2 ($\Delta t = 55$ s). The 22 MeV proton cross section for the user flip-flops σ_{SEU} can be constrained to be below $2{\cdot}10^{-14}$ cm^2 per flip-flop using the formula

$$\sigma_{\text{SEU}} = \frac{1}{\Delta t \cdot F_{\text{proton}} \cdot N_{\text{FF}}}. \tag{7.8}$$

Where the number of flip-flops is N_{FF}.

The measurement was performed with 22 MeV protons for which the SEU probability is about a factor 3 smaller than for higher energy protons.

7.7 Conclusions

Both tested FPGAs sustained the TID expected for the upgraded LHCb Outer Tracker electronics. The first irradiation induced effects are observed after an integrated dose of 150 krad, a change of the first tested FPGA core current. All monitored permanent current changes are between 5% and 20% and rather small. A real malfunction of the chip was detected after 400 krad. The TDC time measurement stopped working reliable. The PLL clock frequencies were not affected by the irradiation but the phase between two clocks changed after 3 Mrad. The tested 3.125 GBit/s transceivers sustained orders of magnitude more than 30 krad, they stopped working after 23 Mrad.

Different cross sections for single event effects (SEE) such as configuration bit flips have been measured with 22 MeV protons. Scaled to the irradiation condition at LHCb one expects transceiver re-initalization resets every $3 \cdot 10^7$ s per transceiver and one CRC error every $1.5 \cdot 10^6$ s per chip. The scaling does not take into account that the effects for SEE of high energy protons is up to a factor 3 larger than for the 22 MeV protons used in the irradiation test described here. Taking the larger damage of the protons at the LHC into account a usage of the FPGA seems nevertheless feasible.

CHAPTER 8

Summary

The LHCb collaboration is planning to upgrade the detector in 2018 to a 40 MHz readout for a much more flexible software-based triggering system that will increase the data rate as well as the efficiency, especially in channels with hadronic final states. In this thesis a feasibility study to use the SRAM-based Arria GX FPGA from Altera for the readout electronics upgrade of the LHCb Outer Tracker has been performed.

First, to measure the Outer Tracker straw-tube drift times a 32 channel FPGA-based TDC has been developed. To reach the desired drift coordinate resolution of $<$200 μm a time resolution of $<$1 ns has to be achieved. Furthermore, the TDC has to be able to measure every first hit in a channel during each 25 ns LHC clock period. The time bin size of the TDC is 780 ps with a differential non-linearity variation between 0.1 bins (0.08 ns) and 0.6 bins (0.5 ns) for all channels. The TDC bins have a size well below 1 ns. This was achieved by manually placing the TDC channels in the FPGA manually and using timing constraints for the Quartus II routing algorithm. In addition, the DNL variation was minimized by using bin size measurements of the single TDC channels and recalculating the timing constraints for every individual TDC channel. The TDC fulfills all the requirements of the LHCb Outer Tracker detector.

A test board with the Arria GX FPGA as the main component was developed which is pin compatible to the existing LHCb Outer Tracker readout electronics. With this board, 32 of the 128 straw-tubes can be read out. An additional interface board was constructed which connects the existing pre-amplifier board

with the FPGA test board. Both boards were successfully tested with a cosmic ray setup to measure the drift times for 8 channels of an LHCb Outer Tracker module. The measured drift time spectrum has a width of 45 ns, similar to measurements in the current LHCb Outer Tracker. This test shows that it is possible to use the FPGA test board with the TDC firmware to read out an Outer Tracker module.

The Arria GX FPGA is one of two chips considered for the upgrade of the LHCb Outer Tracker readout electronics. An important question was the radiation tolerance of the commercial SRAM-based FPGA. An irradiation test was performed with two Arria GX FPGAs at the Max-Planck-Institute for Nuclear Physics in Heidelberg in October 2012 with a 22 MeV proton beam up to a total ionization dose (TID) of 30 Mrad, 1000 times more than the expected dose of 30 krad for the upgraded LHCb Outer Tracker electronics. At the beginning of the irradiation campaign the proton beam profile was measured with a straw-tube module to calibrate the TID in the chips. The intensity beam profile was checked with 3 pairs of passive dosimeters. The dose extrapolation from the beam profile and the dosimeter measurements are in good agreement. The following parameters of the FPGAs were monitored during the irradiation campaign: the different supply currents of the FPGA, the stability of the clock filters (PLLs), the stability of the 32 channel TDC on the FPGA, the bit flips in the data transmission with two 3.125 GBit/s optical transceivers and single event upsets rate of user flip-flops. After an integrated dose of 150 krad the first impairment is observed, which is a change of the core current of the first tested FPGA. All monitored permanent current changes are between 5% and 20%. A malfunction of the time measurement with the TDC was detected after 400 krad. The PLL clock frequencies were not affected by the irradiation but the phase between two clocks changed after 3 Mrad. The tested 3.125 GBit/s transceivers stopped working after 23 Mrad.

The BEP was small enough to operate the transceivers in the upgraded LHCb Outer Tracker readout electronics. Furthermore, transceiver re-initalization resets are necessary every $3 \cdot 10^7$ s per transceiver, which would be acceptable for efficient data taking. The 22 MeV proton cross section for SEUs of the user flip-flops was determined to be smaller than $2 \cdot 10^{-14}$ cm^2. The 22 MeV proton cross section for the configuration registers was measured to be $1.6 \cdot 10^{-16}$ cm^2 per bit. The error rate in the FPGA configuration registers scaled to the upgraded LHCb Outer Tracker radiation environment seems to be manageable at one firmware error every $1.5 \cdot 10^6$ s per chip. For the measurements of cross sections related to proton induced single event effects the energy of the proton beam was too low. The results therefore underestimate the flip probability by roughly a factor 3. To determine these numbers with higher reliability it is recommended to measure the flip probabilities with 60 MeV protons.

The results of the irradiation campaign show that the Arria GX FPGA can sustain the total ionization dose expected for the upgrade of the LHCb Outer Tracker.

It has been successfully shown that the readout electronics and firmware developed in this thesis fulfill the requirements for the LHCb Outer Tracker upgrade. Furthermore, it is confirmed that it is possible to use modern SRAM-based FPGAs as a component of detector readout electronics in radiation environments expecting total ionization doses of 30 krad.

The measured firmware error rate per chip indicates that these flips can be rare enough to operate a detector readout with modern SRAM-based FPGAs. This needs to be confirmed with irradiation tests with 60 MeV protons or higher. The usage of SRAM-based FPGAs is also considered for the readout electronics of the planned LHCb Fiber Tracker.

The usage of SRAM-based FPGAs in the readout electronics of high energy physics detectors in moderate radiation environments is of great interest for the High Energy Physics community. The usage brings many advantages for the development of the detector readout electronics, as SRAM-based FPGAs are technologically the most advanced FPGAs. Most technology requirements of a high energy physics detector readout chip can be fulfilled with these modern FPGAs, and their usage will reduce the time consuming and expensive ASIC development for the readout electronics.

APPENDIX A

List of Acronyms

ADC	Analog to Digital Converter
ALICE	A Large Ion Collider Experiment
ASDBLR	Amplifier, Shaper, Discriminator with ion-tail cancellation and Base Line Restoration
ASIC	Application-Specific Integrated Circuit
ATLAS	A Toroidal LHC AparatuS
BEP	Bit error probability
BEPT	Bit error probability test
BER	Bit error rate
BERT	Bit error rate test
BX	Bunch crossing
BZ	bin size
CERN	Conseil Européen pour la Recherche Nucléaire
CLK	Clock
CMOS	Complementary Metal Oxide Semiconductor
CMS	Compact Muon Solenoid
DAC	Digital to Analogue Converter
DAQ	Data Acquisition
DLL	Delay locked loop
DNL	Differential Non Linearity
ECS	Experiment Control System
EPR	Electron paramagnetic resonance

FE	Front-end
FE-Box	Front-end box
FF	Flip-flop
FIFO	First in, first out
FPGA	Field Programmable Gatter Array
GOL	Gigabit Optical Link
HDL	Hardware description language
I/O	Input/output
LAB	Logic array block
LB	Logic block
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LUT	Lookup table
LVDS	Low Voltage Differential Signaling
MUX	Multiplexer
NIM	Nuclear Instrumentation Module
OT	Outer Tracker
OTIS	Outer tracker Time Information System
PCB	Printed circuit board
PCI	Peripheral Component Interconnect
PLL	Phase-locked loop
PRNG	Pseudorandom number generator
QPLL	Quartz Crystal phase-looked loop
RAM	Random-access memory
RST	Reset
SEE	Single Event Effect
SEU	Single event upset
SMA	Coaxial radio frequency connector: SubMiniature version A
SRAM	Static random-access memory
TFC	Timing and Fast Control
TDC	Time to Digital Converter
TID	Total ionization dose
TLD	Thermoluminescent dosimeter
TME	Time measurement element
TMR	Triple modular redundancy
VHDL	Very High Speed Integrated Circuit Hardware Description Language

APPENDIX B

Appendix : Outer Tracker gas monitoring

The LHCb Outer Tracker uses a gas mixture of $Ar/CO_2/O_2$ (70%/28.5%/1.5%). The amount of oxygen and humidity of this mixture is measured in a gas anlysis rack. The concentration of oxygen is stable at 1.5% and the amount of H_2O is at 5 ppm. It is difficult to decide from these values alone if the gas mixture is still within the range to operate the detector. The gas amplification, which is effected most by the gas mixture should stay constant. If the gas amplification is too low the detector loses detection efficiency. If the gas amplification is too high, space charge effects can lead to inefficiencies or for much to high gas amplifications the strong current could damage the wire inside the straw-tubes. The monitoring of the gas amplification is very important for longterm detector operation.

B.1 Method

The relative gas amplification is monitored with the following method. A small amount of the input gas mixture for the LHCb Outer Tracker as well as some of the output gas is used to run test modules. The test modules are irradiated with ^{55}Fe sources and pulse spectra are taken. The 5.9 keV peak position[1] is proportional to the gas amplification. Figure B.1 shows a pulse spectrum of a ^{55}Fe source. The K-α and the K-β peak is fitted with the following function

[1]Fe-55 decays via electron capture to Mn-55 at a half-life of 2.7 years followed by emitting Auger electrons of 5.19 keV, K-α photons of 5.9 keV or K-β photons of 6.5 keV.

$$\frac{N}{\sigma_1 \cdot \sqrt{2 \cdot \pi}} \cdot e^{-\frac{1}{2} \cdot \left(\frac{x-\mu}{\sigma_1}\right)^2} + \frac{0.14 \cdot N}{\sigma_2 \cdot \sqrt{2 \cdot \pi}} \cdot e^{-\frac{1}{2} \cdot \left(\frac{x-\mu \cdot 1.1}{\sigma_2}\right)^2}. \tag{B.1}$$

For each of the two spectral lines a Gaussian functions is used. The relative peak positions and the relative intensities are fixed [96]. The spectral line widths are not constrained for either line. N is a constant, the mean is the Gaussian mean of the 5.9 keV peak position, σ_1 is the width of the 5.9 keV peak and σ_2 is the width of the 6.5 keV peak.

The small peak at roughly half the pulse height is the escape peak which is cause by ionizing a K-shell electron of the argon. The electron loses its energy in the gas and the primary ionized argon atom emits a K-photon which can leave the detector. This reduces the energy deposited in the detector.

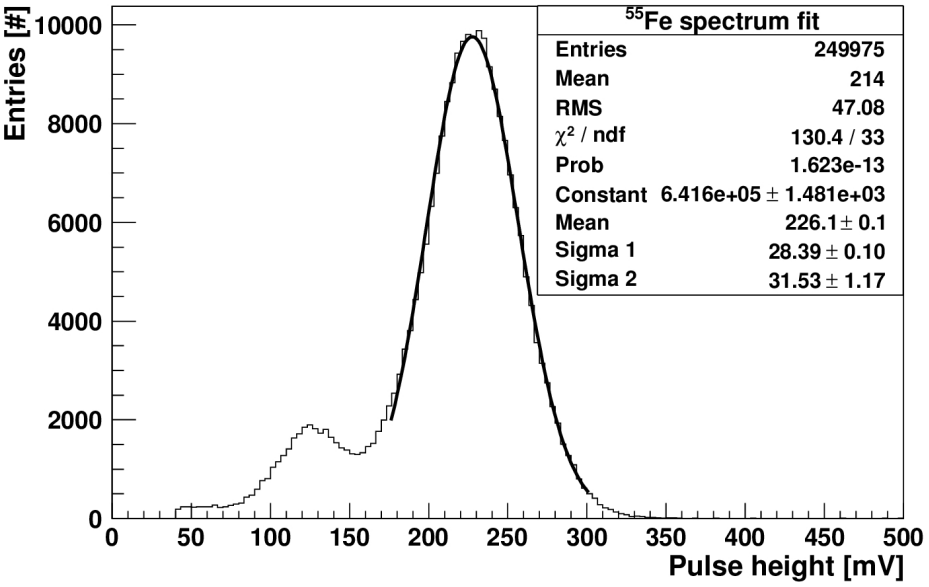


Figure B.1: ^{55}Fe pulse height spectrum. The data is fitted with Equation B.1. The variables are: Constant N, Mean of the 5.9 keV line position μ , Sigma 1 σ_1, Sigma 2 σ_2. The variable Mean is monitored for the gas stability.

In the following sections the system for the monitoring of the gas amplification of the Outer Tracker is introduced. First the hardware is described, followed by the gas pressure correction necessary. Afterwards the software, which has been integrated in the LHCb control system will be shown.

B.2 Hardware

The LHCb Outer Tracker gas is monitored both before it enters (input gas) as well as after passing through the detector (output gas) each with a single test module. Both modules were built at NIKHEF[2] using neither glue nor rubber to make the module gas tight. Due to the absence of glue and rubber no aging is expected which is crucial for a monitoring system.

B.2.1 Electronics

The readout boards of the test modules use VV50 pre-amplifier and were developed in the electronic department of the Physikalische Institut University Heidelberg. These consist of a high voltage board which distributes the high voltage to the straw-tubes and a readout board. It is possible to choose one of the 64 straw-tubes via a RS232 programmable relay for readout.

The amplified detector pulses are measured with 100 MHz 12 bit ADCs of a LogicBox [81]. In addition, the LogicBox is used to measure the output voltages of two barometers with two slow 12 bit ADCs. The two barometers were used to measure the gas pressure of the modules to correct the monitored gas amplification. This is described in the next section. The LogicBox itself is controlled and readout via an USB interface using LabView 8.0.

For each test module the high voltage of 1550 V is provided by a two channel HV supply[3]. The high voltages are monitored and controlled via a RS232 bus.

Figure B.2 shows a photo of the gas monitoring electronics excluding the readout board.

B.3 Gas pressure correction

For proportional counter detectors the gas amplification is anti-proportional to the pressure of the counting gas [97]. This will be explained in the following. Electrons created along the path of an ionizing particle drift in the electric field towards the anode wire. These electrons gain kinetic energy from the electric field between collisions with gas atoms or molecules. The energy gain depends on the mean free path of the electrons and the electric field. When the electrons drift towards the central anode wire the mean free path is constant but the electric field changes with $\frac{1}{r^2}$. At a certain distance from the wire the kinetic energy gain of the electrons is high enough to ionize the atom or molecule in the following collision. This distance describes the starting point for the gas amplification process.

The mean free path for drifting electrons rises anti-proportional to the gas pressure. So for lower gas pressure the electrons gain more kinetic energy from

[2]National Institute for Nuclear and High energy physics in Amsterdam
[3]ISEG NHO 226L

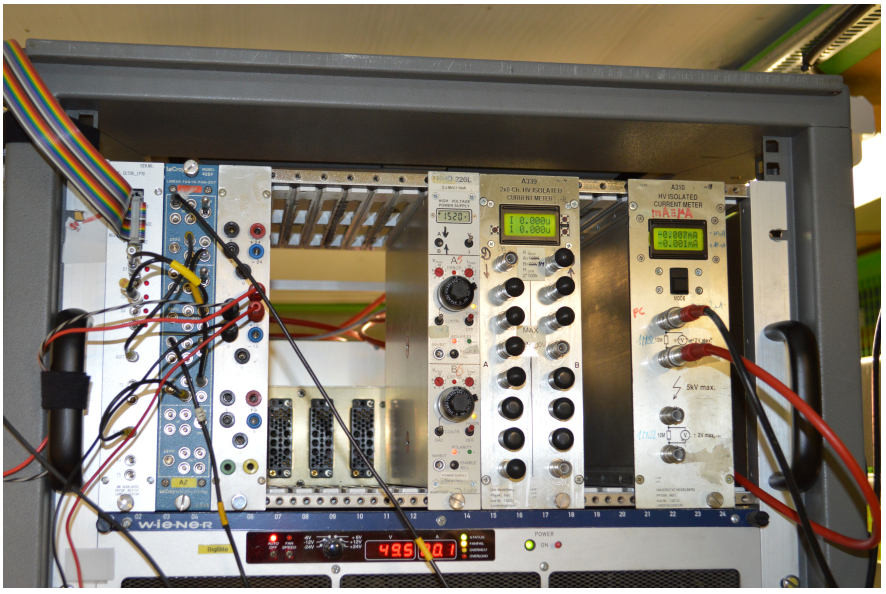


Figure B.2: Photo of the gas monitoring electronics excluding the readout board, from left to right: the LogicBox with two fast ADCs, low voltage supply, high voltage supply and current meters (not used).

the electric field between two collisions with the gas atoms or molecules. The result is that the distance at which the gas amplification starts, increases and more amplification stages can occur until the electrons reach the anode wire. The gas amplification increases.

This effect has to be disentangled from gas amplification changes due to the gas mixture variations. The pressure inside the test modules depends on the air pressure outside the modules. So the gas pressure is not constant over time. The current system uses one pressure sensor[4] connected to a 1 l buffer volume in-front of each test module to measure the counting gas pressure.

Figure B.3 shows the calibration curve which is used to correct the gas amplification of the input module. This calibration curve is taken on data half a day with a fast change in air pressure. For calibration, a gas bottle with $Ar/CO_2/O_2$ (70%/28.5%/1.5%) has been used as counting gas to guarantee a stable gas mixture.

Figure B.4 shows a monitoring chart of the LHCb Outer Tracker control software for the gas gain at the Outer Tracker output. The gas pressure corrected data in green and uncorrected data in blue (upper) are shown for a time period of 10 days. The bottom blue chart is the gas pressure. A monitoring of gas mixture changes without gas pressure correction is not possible.

[4]Honeywell FP2000 FPA1BJ,2P,5A,60,9E

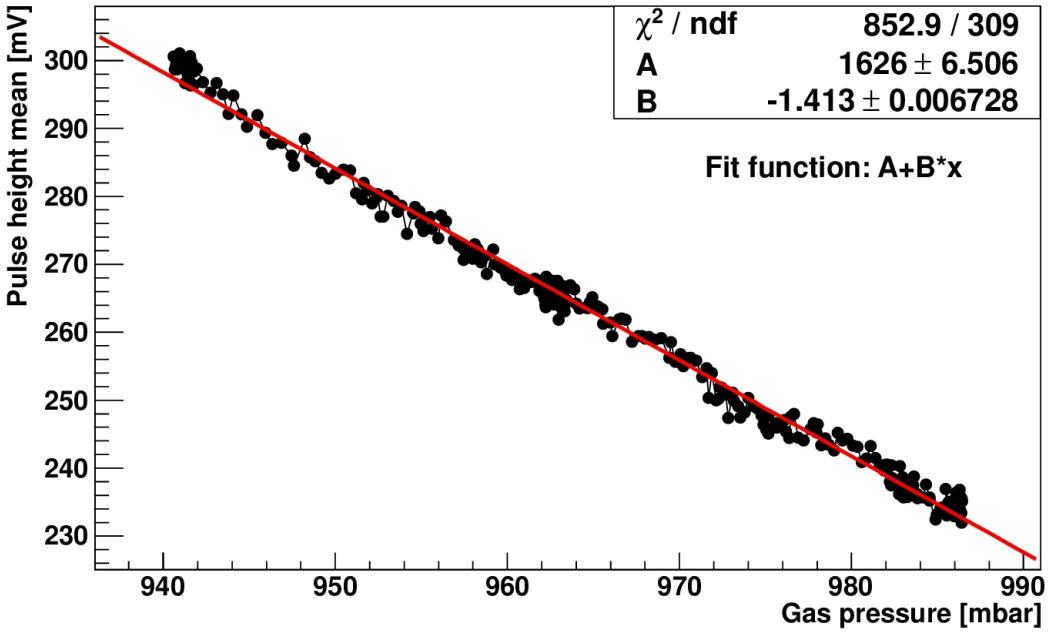


Figure B.3: Pulse height mean as function of the gas pressure. The fit function is a 1st order polynominal.

B.4 Software

The software of the gas monitoring is divided into three parts. The data acquisition (DAQ), the data analysis and the control system. In the following all three parts will be shortly introduced.

B.4.1 Data acquisition

The data acquisition is done with a LabView project which controls and monitors the readout board relays, the high voltage supply and the LogicBox. It provides the possibility to monitor the current meter as well which is currently not the case. The LabView project takes a pulse spectrum for each module and measures the air pressure and high voltage every 10 minutes. All data for a given time interval are written into ASCII files.

B.4.2 Analysis software

The ASCII files are analyzed by a script using the programming language C. This script fits each pulse height spectrum and adds the results to the corresponding file. Furthermore, the script corrects the measured peak position for the air

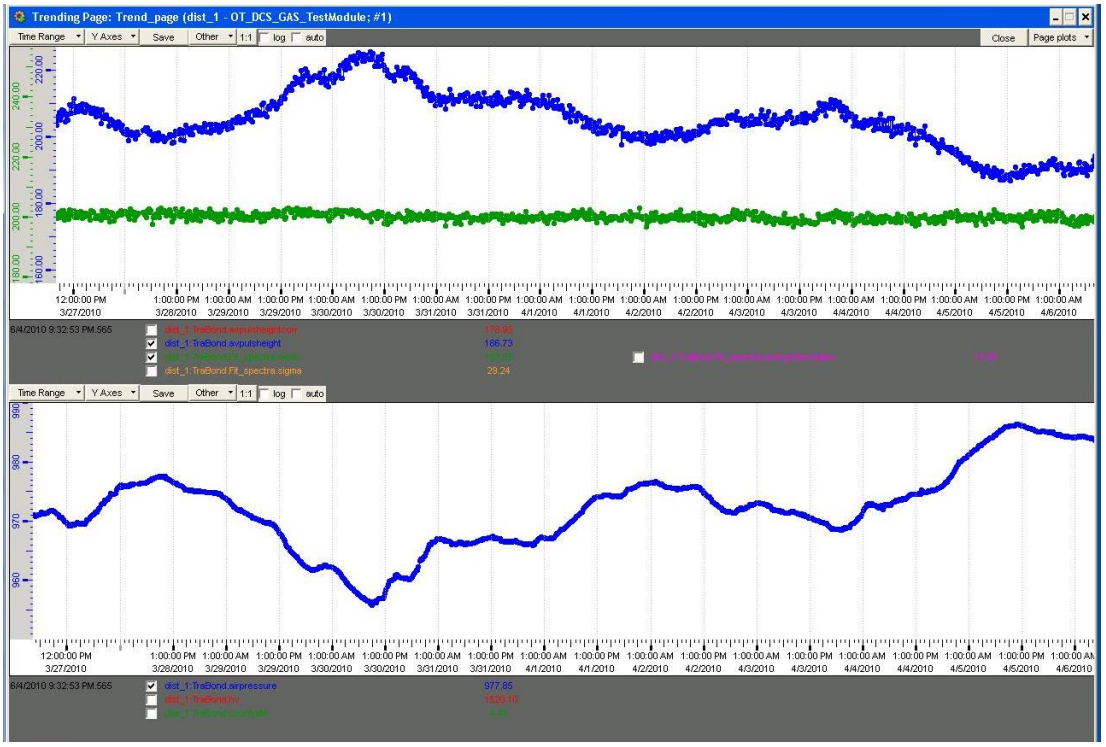


Figure B.4: Gas monitoring panel of the LHCb Outer Tracker control software for the gas at the Outer Tracker output. The time scale is ten days. The upper blue chart shows the pulse spectrum mean without air pressure correction, the green charts depicts the one with air pressure correction. The air pressure is shown in the blue chart on the bottom. The anti-proportional behavior of the gas amplification vs. the air pressure is very well visible.

pressure. A cron job[5] starts this C-script periodically.

B.4.3 Piquet script

When running the LHCb detector one person is responsible for the Outer Tracker, referred to as piquet. This OT-person will be called if a problem arises which the LHCb shift crew can not solve. Every morning at 08:50 AM a cron job summarizes the last 30 hours for the input gas and the output gas of the Outer Tracker. Figure B.5 shows a summary for the output gas. This system is independent of the global LHCb control system to ensure operation in cases of power cuts where the control system is unavailable. This is crucial to investigate the stability of the gas mixture especially in case of a power cuts.

B.4.4 Emergency script

Often during gas alarms after power cuts the global LHCb control system is not available. The LabView project continues to take data on a PC with an independent power line. Hence a script accessing these data remains operational when the global LHCb control system is unavailable. A script similar to the piquet script with the possibility to choose the time period has been included. The script searches for all pulse spectra files during the specified period, analyses the spectra and plots the results. It is possible to investigate all monitored parameters: average pulse height gas pressure corrected, pulse height mean corrected for the gas pressure, average pulse height raw data, gas pressure and high voltage.

B.4.5 Integration into the global LHCb control system

The LHCb global control system uses the PVSSII control software [98]. The Outer Tracker gas monitoring PVSSII project collects data from the ASCII files produced by the local LabView project and writes them into an Oracle data base. Various PVSSII panels were designed during this thesis to present the data and to make an analysis of the Outer Tracker gas status available to the OT piquet. A malfunctions can be identified with the help of the gas amplification value. It was decided to trigger an alarm if at least one of the two modules shows a pressure corrected peak position which deviates by more than 5% from the nominal position. The Outer Tracker piquet is called automatically to have a look at the gas system in these cases.

[5]Cron is a program for Linux which starts jobs after a pre-defined schedule. It is often used to control jobs which are used periodically.

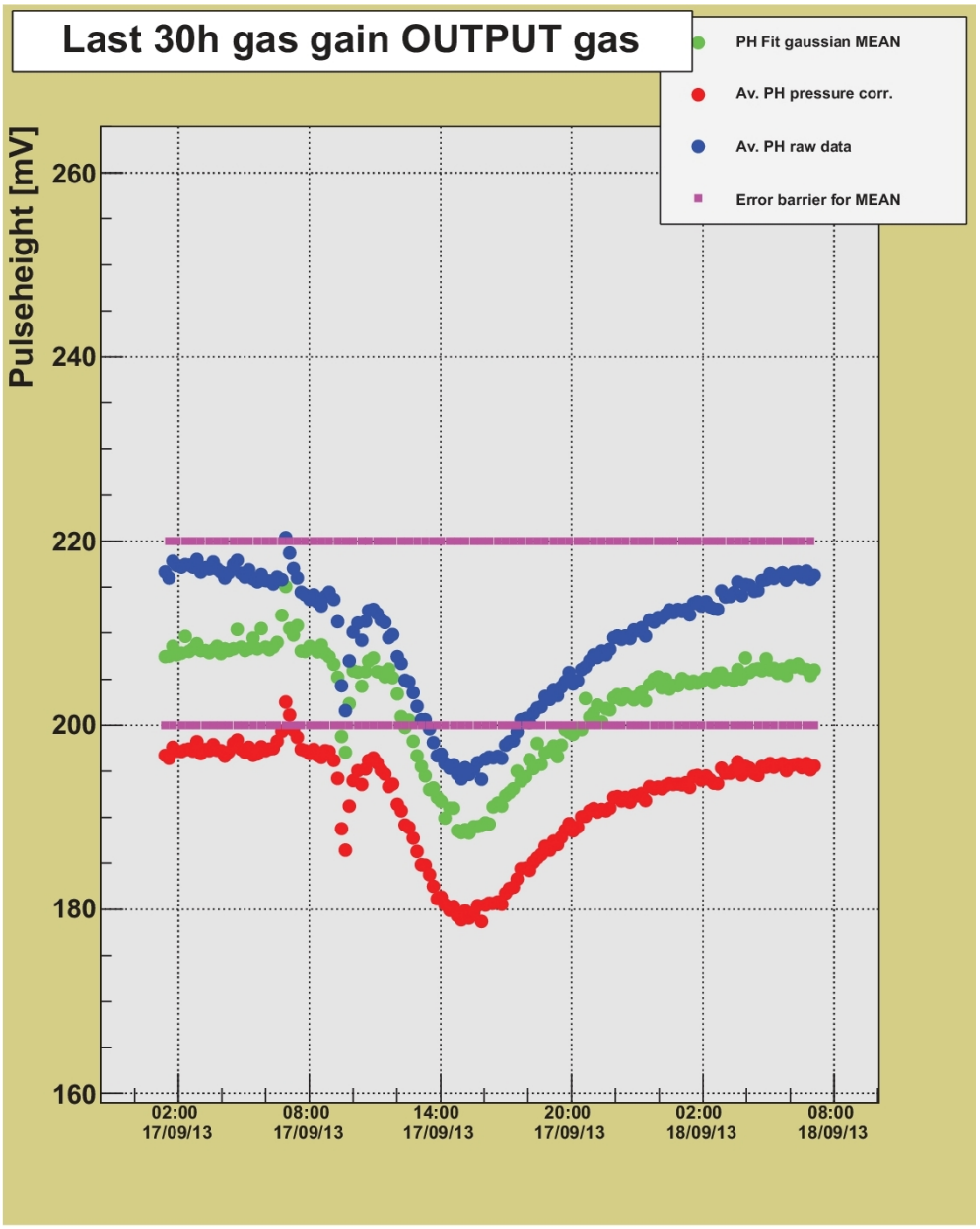


Figure B.5: Last 30 hours gas gain OUTPUT gas. Blue is the average pulse height without correction for gas pressure changes. The red curve shows the average pulse height with gas pressure correction. The green curve is the Gaussian mean also corrected for gas pressure. The green chart is used for the alarm. The alarm levels are shown in purple. During the shown 30 hours an alarm was triggered, which usually happens after a change of the gas system from the mixed gas to the pre-mixed gas from the battery after a power cut.

B.5 Outer Tracker gas stability

The LHCb Outer Tracker gas was stable throughout the entire run period of 2009-2013. The PVSSII panel for the pressure corrected mean of the input gas and output gas can be seen in Figure B.6. A three month interval is presented. Only minor gas amplification changes were detected which were mostly related to power cuts. The gas monitoring system was used to decide after power cuts and related gas mixture changes, at which time the high voltage for the entire Outer Tracker could be switched on again. The rule of thumb is to wait another 6 hours after the gas amplification for input gas and output gas is stable to switch on high voltage. The stability of the gas amplification is $\pm 2\%$. The LHCb Outer Tracker gas monitoring was running reliably since 2009.

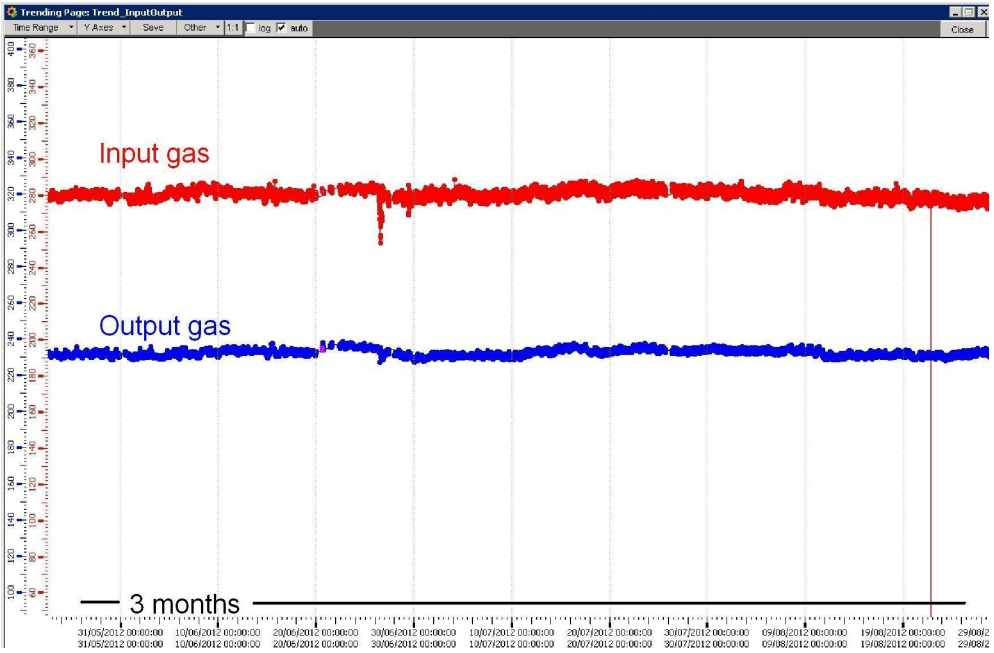


Figure B.6: The PVSSII panel for the pressure corrected mean of the input gas and output gas of the LHCb Outer Tracker is shown. Both are corrected for gas pressure changes. The gas amplification of the input gas and output gas of the LHCb Outer Tracker is stable within $\pm$ 2%. All visible changes are related to known events like power cuts or planned gas system interventions.

APPENDIX C

Appendix : Schematic IF13-6

The FPGA test board uses a SRAM-based FPGA to measure the LHCb Outer Tracker drift times of 32 straw-tube channels, to serialize the data and send the data with GBit/s transceivers to the back-end electronics.

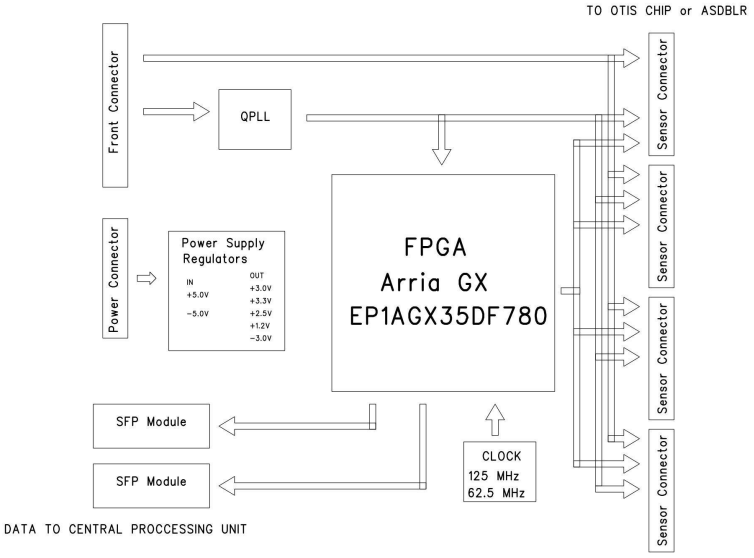


Figure C.1: Schematic IF13-6 block diagram [99].

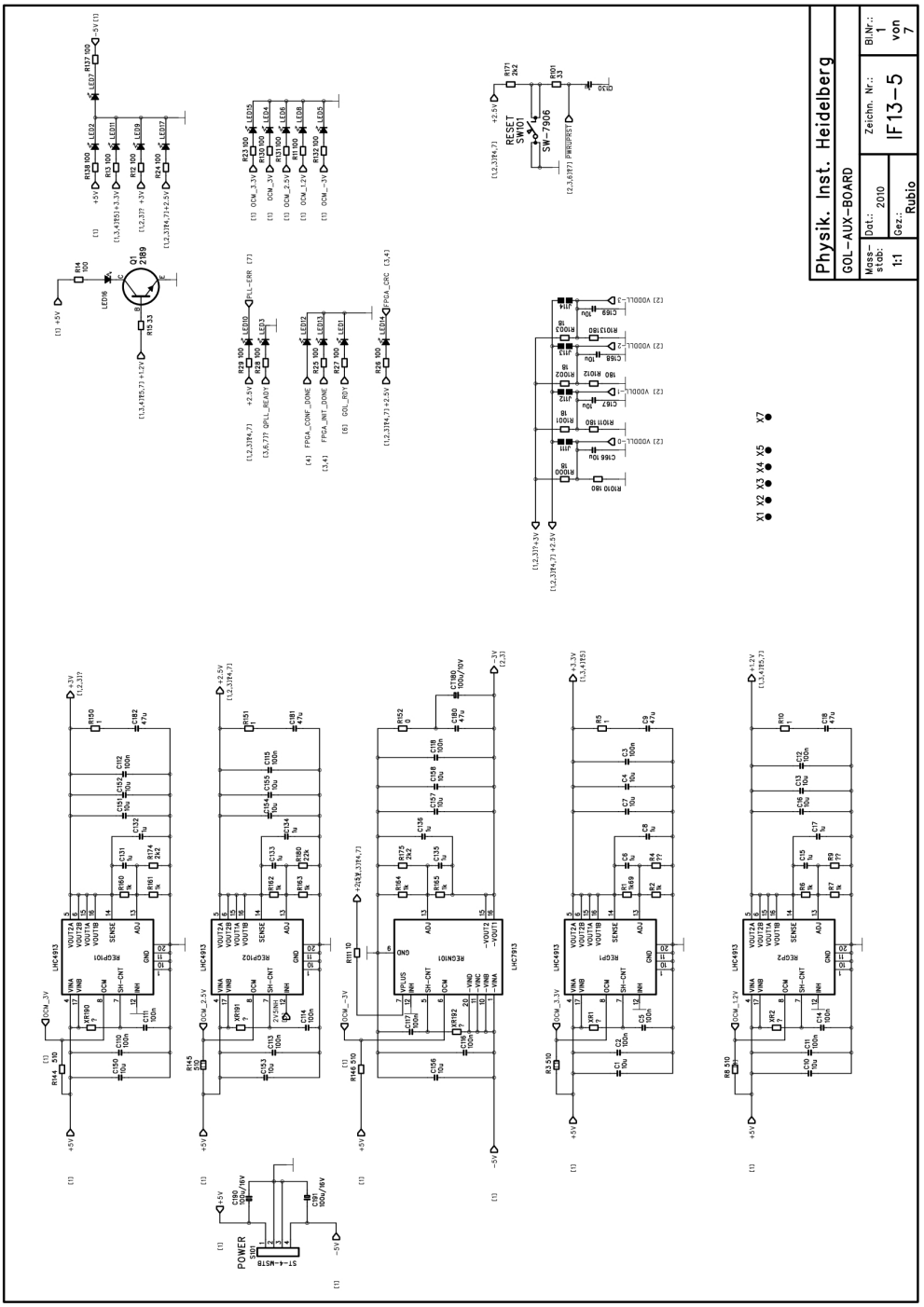


Figure C.2: Schematic IF13-6 page 1 [99].

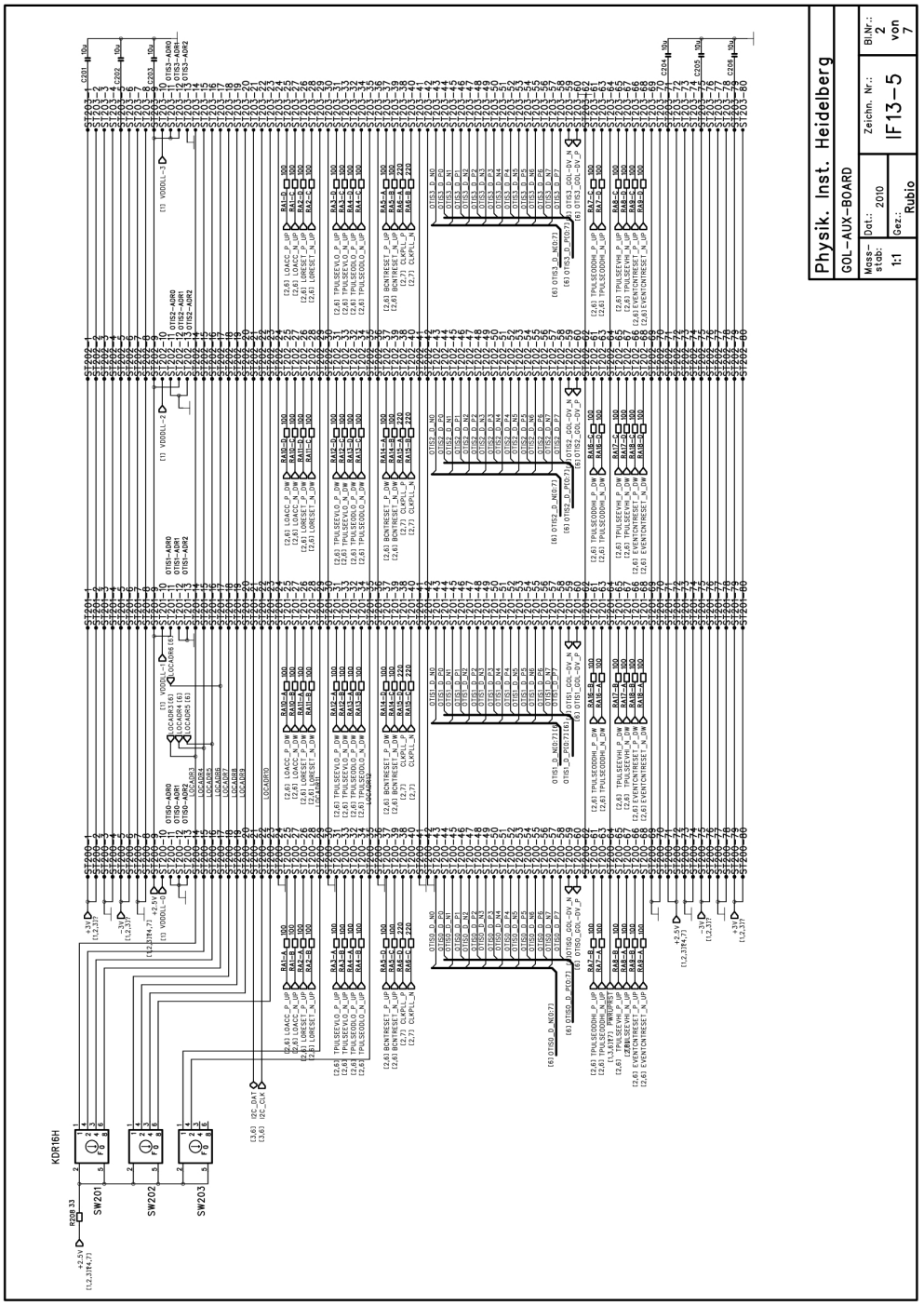


Figure C.3: Schematic IF13-6 page 2 [99].

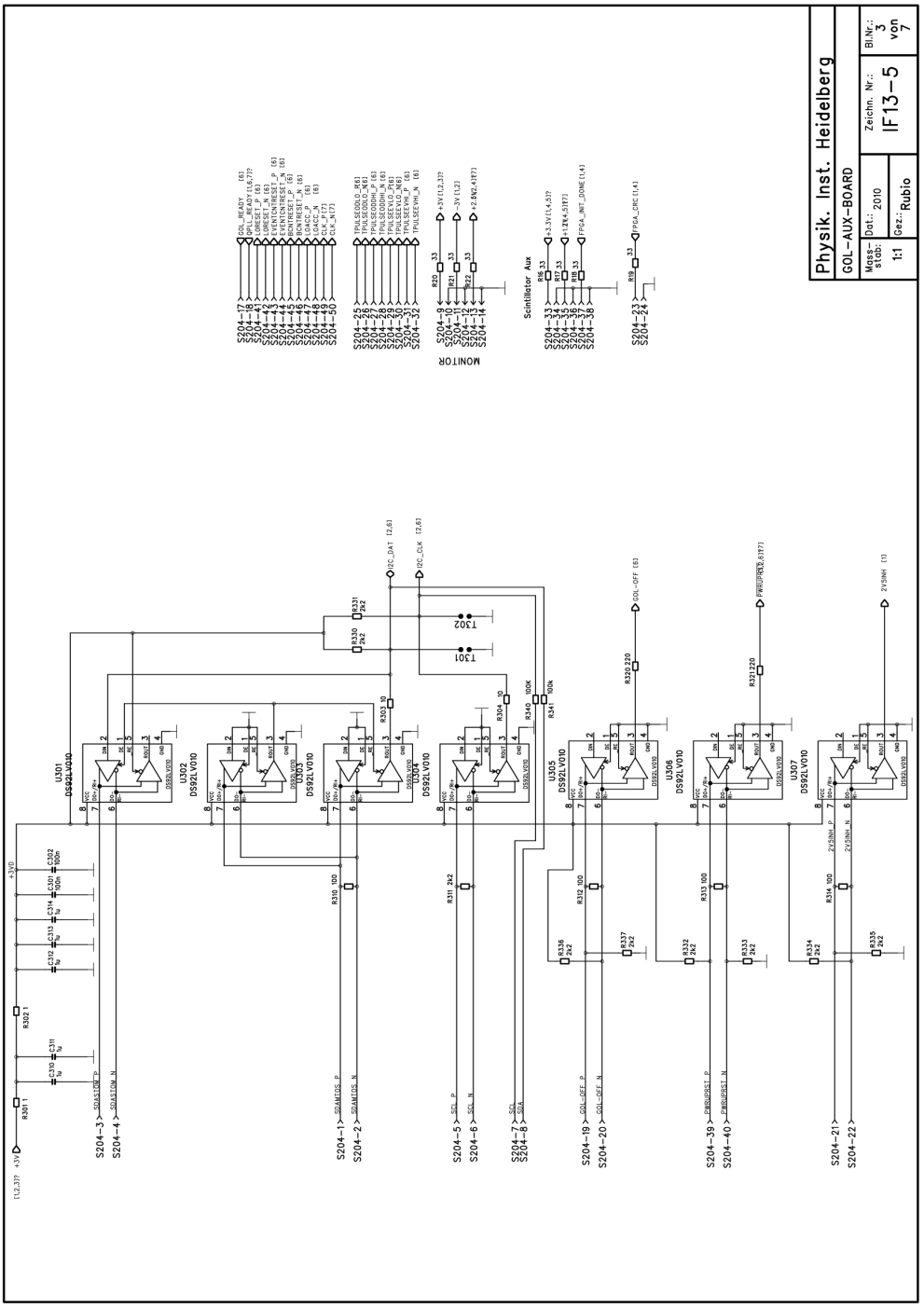


Figure C.4: Schematic IF13-6 page 3 [99].

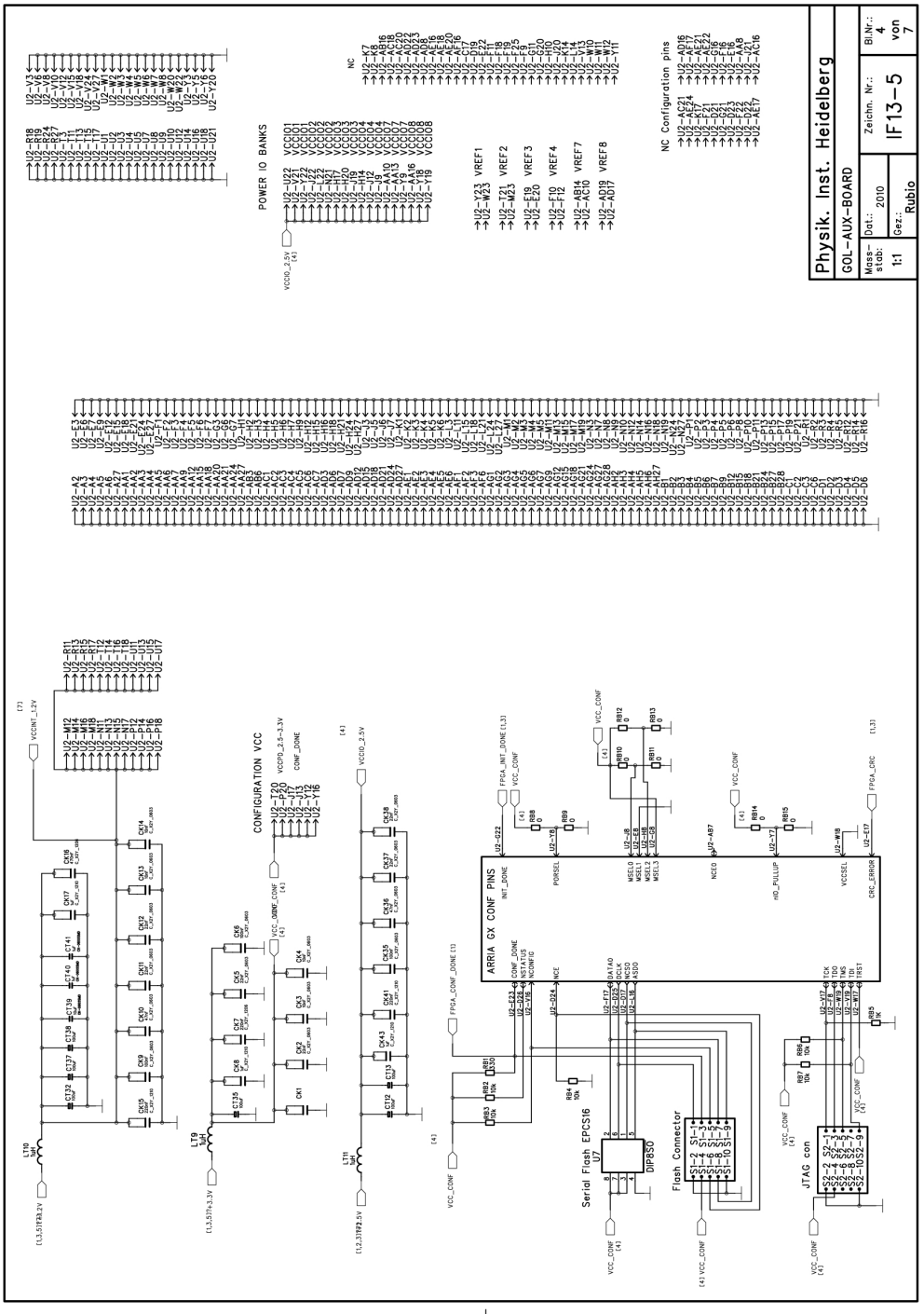


Figure C.5: Schematic IF13-6 page 4 [99].

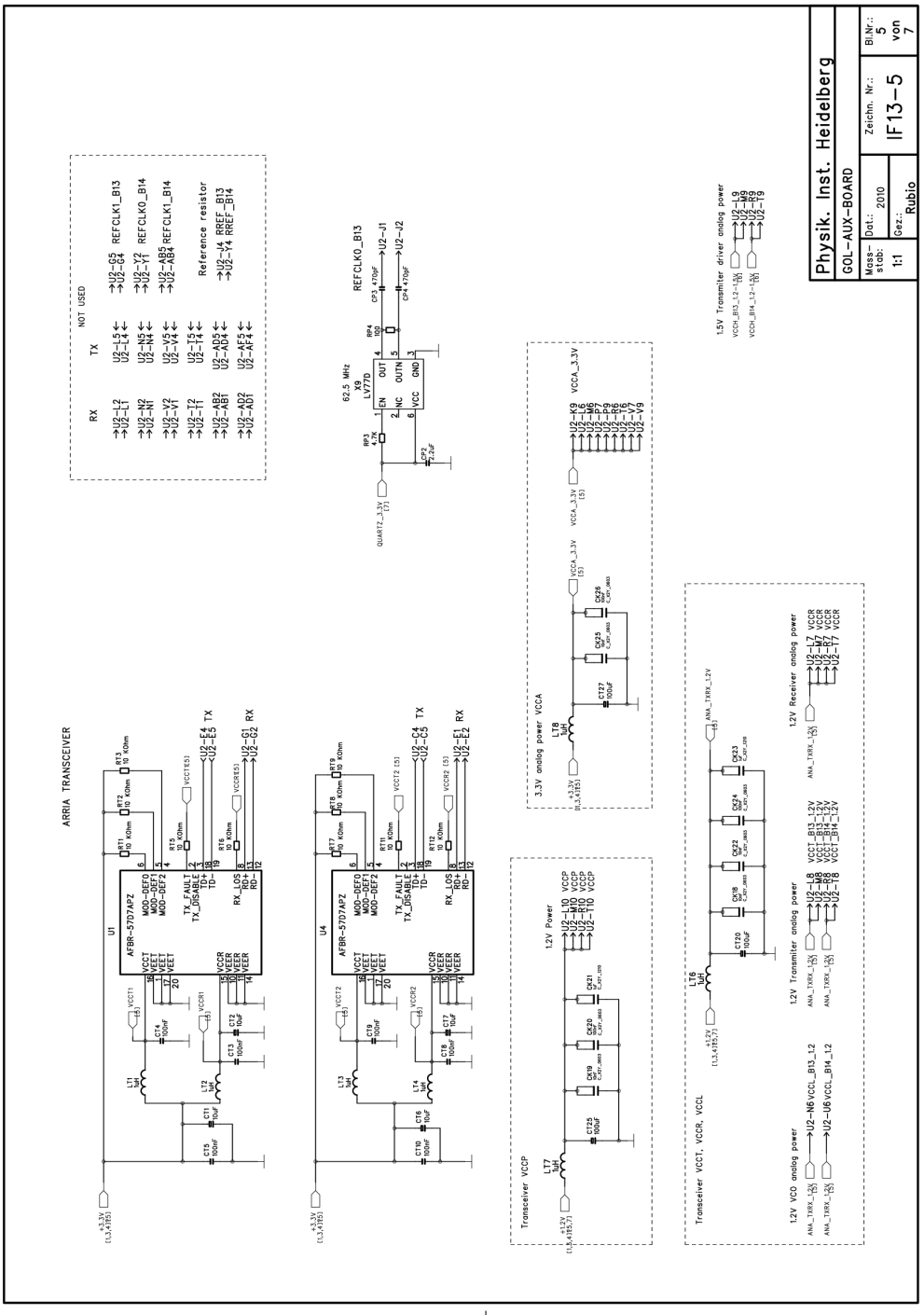


Figure C.6: Schematic IF13-6 page 5 [99].

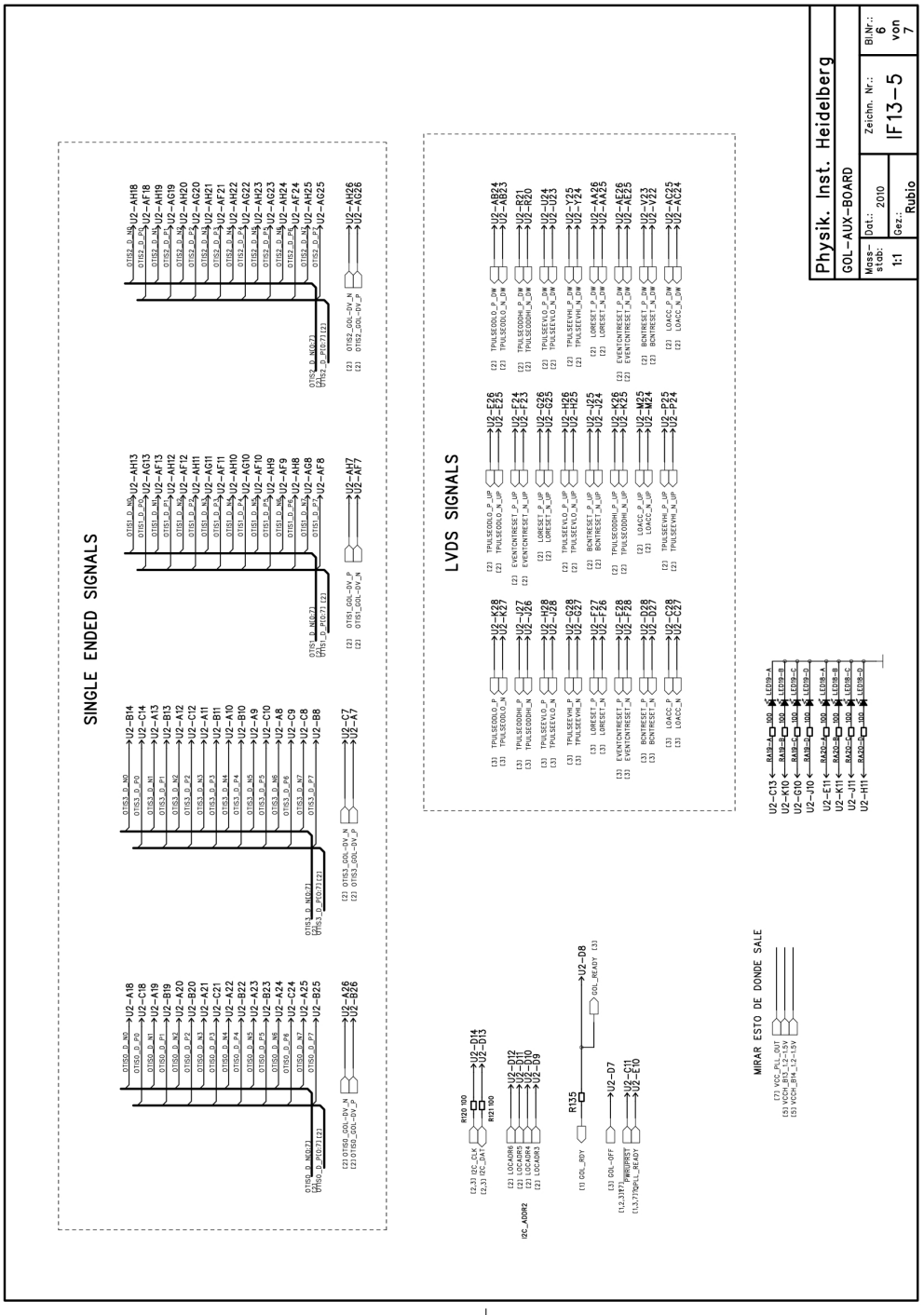


Figure C.7: Schematic IF13-6 page 6 [99].

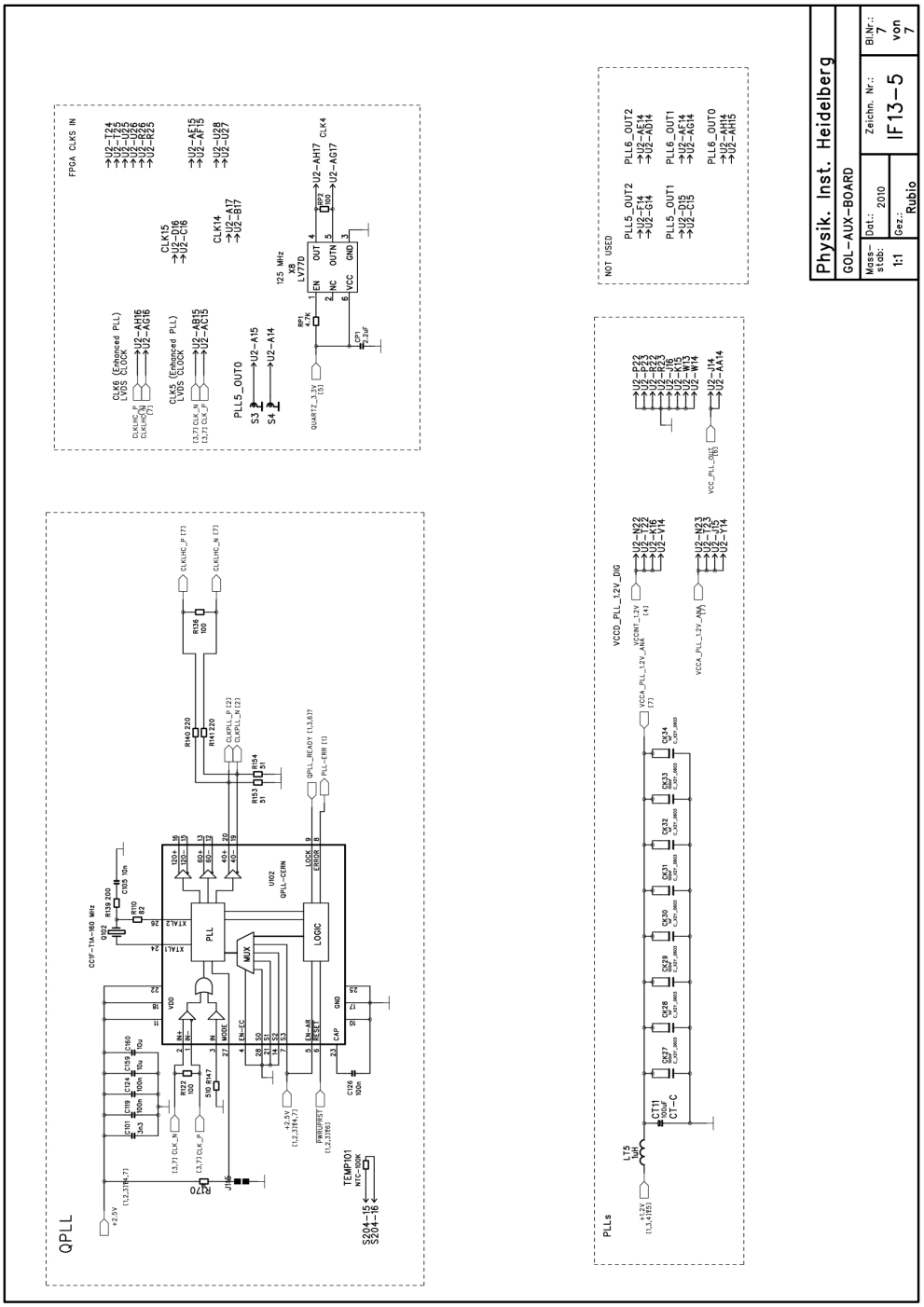


Figure C.8: Schematic IF13-6 page 7 [99].

APPENDIX D

Appendix : Schematic IF013A

The connection board provides the signal connection between the pre-amplifier boards and the FPGA test board. The main task of this PCB is to convert the differential LVDS ASDBLR signals to single ended CMOS, to connect them to the TDC input pins of the FPGA test board and to set the ASDBLR thresholds.

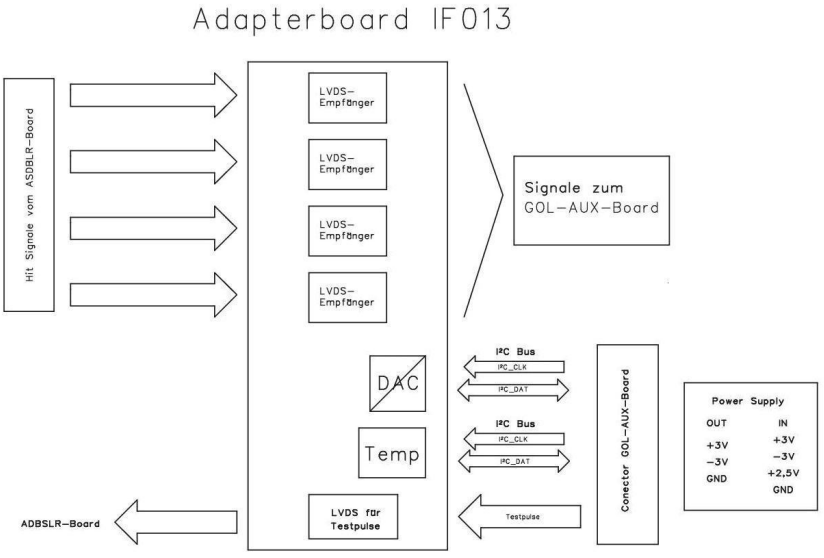


Figure D.1: Schematic IF013A block diagram [100].

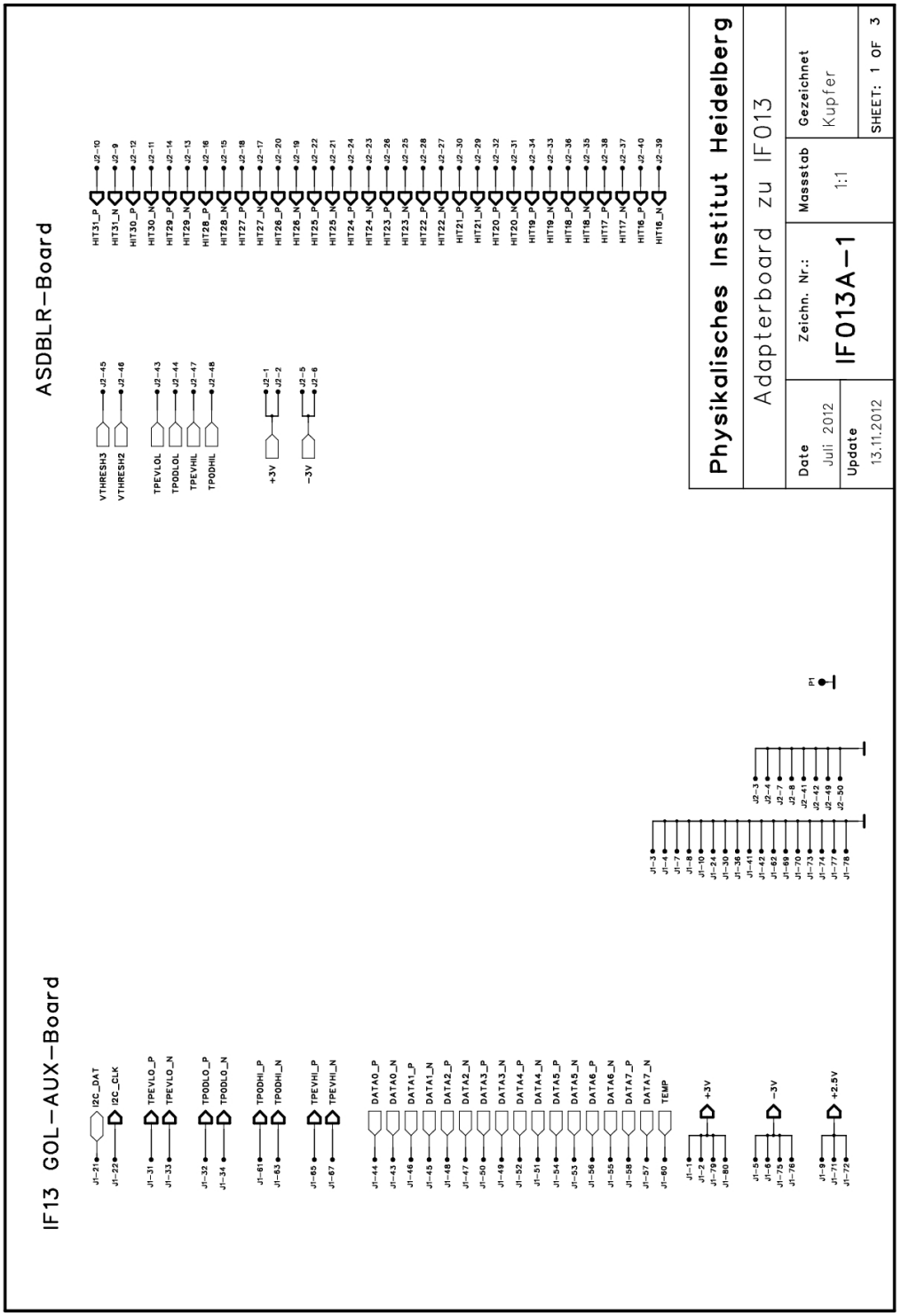


Figure D.2: Schematic IF013A page 1 [100].

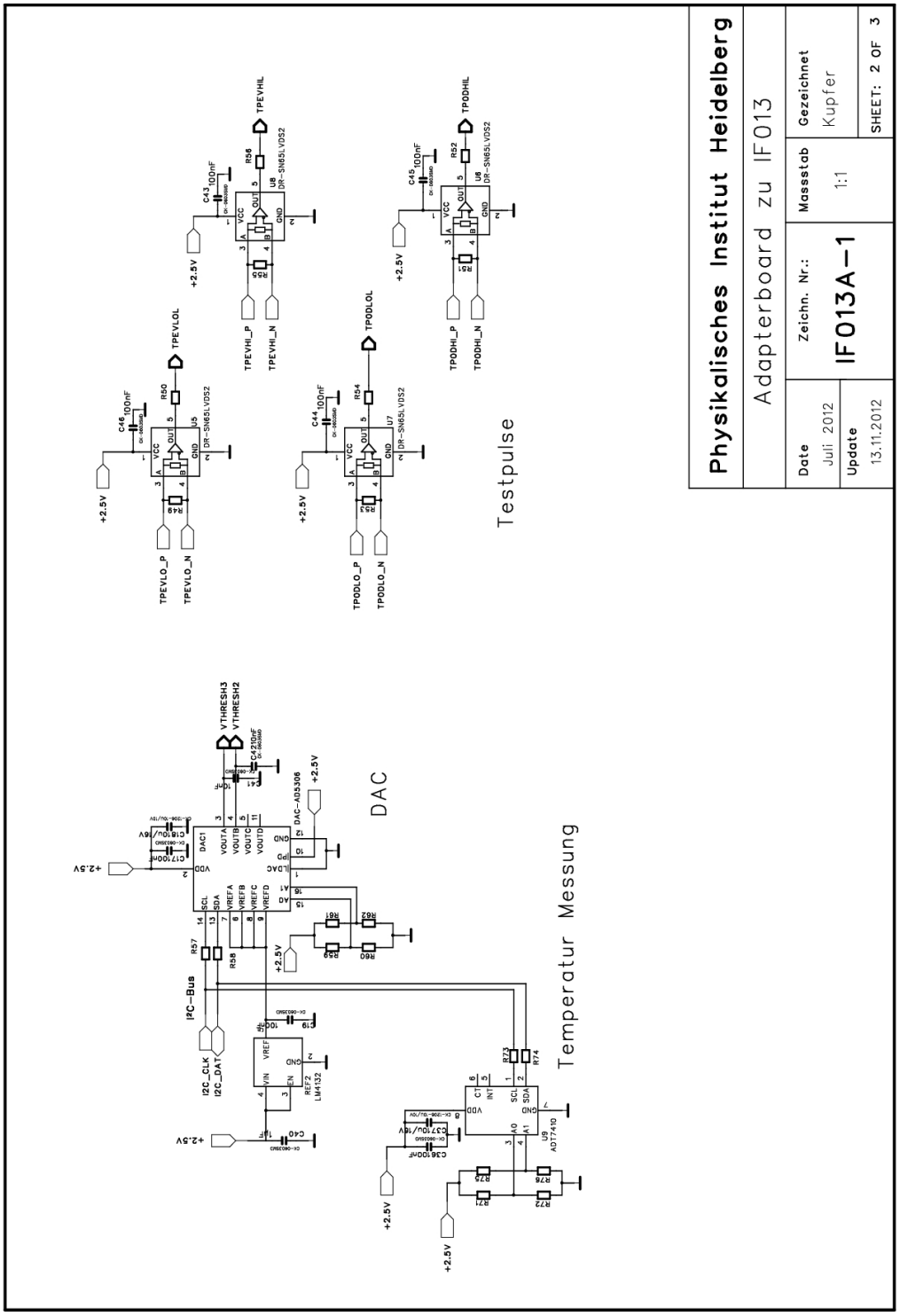


Figure D.3: Schematic IF013A page 2 [100].

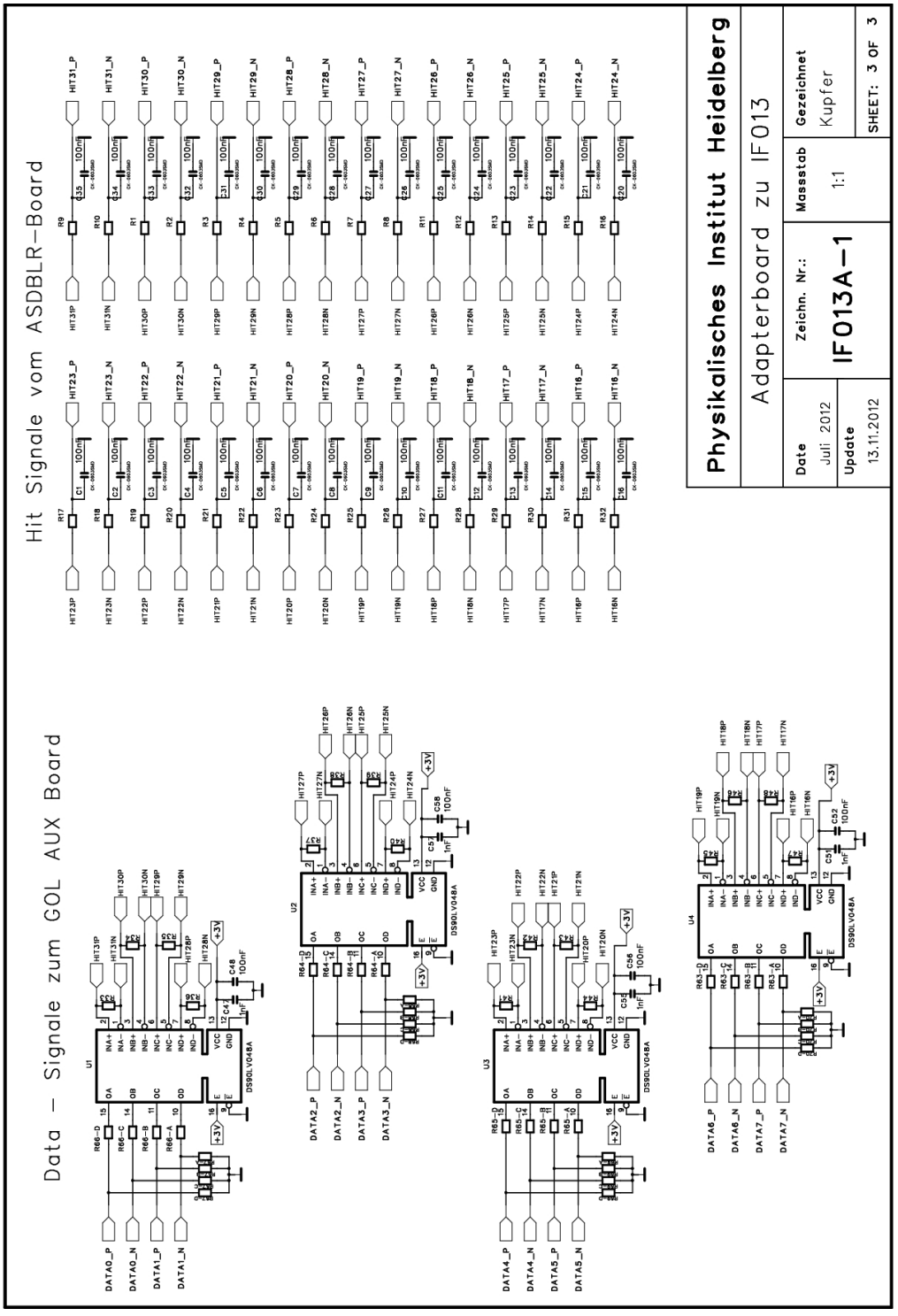


Figure D.4: Schematic IF013A page 3 [100].

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Bibliography

[1] S. Berryman, *Ancient Atomism*, The Stanford Encyclopedia of Philosophy, Fall 2008 Edition, http://plato.stanford.edu/archives/fall2008/entries/atomism-ancient/.

[2] The LHCb collaboration, *Updated sensitivity projections for the LHCb Upgrade*, LHCb-PUB-2013-015, October 2013.

[3] F. Halzen and A. D. Martin, *Quarks and Leptons: An Introductory Course in Modern Particle Physics.*, John Wiley & Sons Inc., (1984).

[4] O. Nachtmann, *Phänomene und Konzepte der Elementarteilchenphysik.*, Friedr. Vieweg & Sohn, (1986).

[5] D. H. Perkins, *Introduction to High Energy Physics.*, Cambridge University Press, 4th edition, (2000).

[6] K. Nakamura et al., *Particle Data Group*, J. Phys. G 37, 075021 (2010) and 2011 partial update for the 2012 edition.

[7] S. Chatrchyan et al. *Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC.*, Physics Letters B 716.1 (2012), pp. 30 Ű61. http://www.sciencedirect.com/science/article/pii/S0370269312008581.

[8] G. Aad et al., *Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC.*, Physics Letters B 716.1 (2012), pp. 1 Ű29. http://www.sciencedirect.com/science/article/pii/S037026931200857X.

[9] M. Kobayashi and T. Maskawa, *CP Violation In The Renormalizable Theory Of Weak Interaction*, Prog. Theor. Phys. 49 652 (1973).

[10] L. Wolfenstein, *Parametrization of the Kobayashi-Maskawa Matrix*, Phys. Rev. Lett. 51 (1983) 1945.

[11] CKMfitter Group (J. Charles et al.), Eur. Phys. J. C41, 1-131 (2005),[hep-ph/0406184], updated results and plots available at: `http://ckmfitter.in2p3.fr`.

[12] The LHCb collaboration, *Letter of Intent for the LHCb Upgrade*, CERN-LHCC-2011-001, March 2011.

[13] LHCb collaboration, R. Aaij et al., *Measurement of the $B_s^0 \tilde{U} \bar{B}_s^0$ oscillation frequency Δm_s in the decay $B_s^0 \to D_s^+ \pi^-$*, New J. Phys. 15 (2013), p. 053021. DOI:10.1088/1367-2630/15/5/053021. arXiv:1304.4741 [hep-ex].

[14] J. Charles et al., *Predictions of selected flavour observables within the Standard Model*, Phys. Rev. D84 (2011) 033005, arXiv:1106.4041 with updated results and plots available at http://ckmfitter.in2p3.fr.

[15] LHCb collaboration, R. Aaij et al., *Measurement of CP-violation and the B_s^0-meson decay width difference with $B_s^0 \to J/\psi K^+ K^-$ and $B_s^0 \to J/\psi \pi^+ \pi^-$ decays*, Phys. Rev. D87 (2013) 112010, arXiv:1304.2600.

[16] A. J. Buras, J. Girrbach, D. Guadagnoli, G. Isidori, *On the Standard Model prediction for $B(B_{s,d} \to \mu^+ \mu^-)$*, CERN-PH-TH/2012-210, arXiv:1208.0934v3 [hep-ph] October 2012.

[17] M.O. Bettler., *The LHCb analysis for $B_s^0 \to \mu^+ \mu^-$*, LHCb-CONF-2009-022, (2009).

[18] E. L. Berger, B. W. Harris, D. E. Kaplan, Z. Sullivan, T. M. P. Tait, C. E. M. Wagner, *Low-energy supersymmetry and the tevatron bottom-quark cross section.*, Phys. Rev. Lett., 86(19):4231Ũ4234, May 2001.

[19] LHCb collaboration, R. Aaij et al., *First evidence for the decay $B_s^0 \to \mu^+ \mu^-$*, Phys. Rev. Lett. 110 (2013) 021801, arXiv:1211.2674.

[20] LHCb collaboration, R. Aaij et al., *Measurement of the $B_s^0 \to \mu^+ \mu^-$ branching fraction and search for $B^0 \to \mu^+ \mu^-$ decays at the LHCb experiment*, Phys. Rev. Lett. 111 (2013) 101805, arXiv:1307.5024.

[21] CMS collaboration, S. Chatrchyan et al., *Measurement of the $B_s^0 \to \mu^+ \mu^-$ branching fraction and search for $B^0 \to \mu^+ \mu^-$ with the CMS experiment*, Phys. Rev. Lett. 111 (2013) 101804, arXiv:1307.5025.

[22] University Tokyo ICEPP ATLAS Home Page, `http://www.icepp.s.u-tokyo.ac.jp/atlas/public/lhc/`.

[23] *LHCb Reoptimized Detector Design and Performance: Technical Design Report*, CERN.LHCC 2003-030

[24] The LHCb collaboration, *The LHCb detector at the LHC.*, J. Instrum., 3:S08005, 2008.

[25] *LHCb Velo: Technical Design Report*, CERN/LHCC 2001-011.

[26] *LHCb Inner Tracker Technical Design Report*, CERN/LHCC 2002-29.

[27] *LHCb Outer Tracker Technical Design Report*, CERN/LHCC 2001-024.

[28] LHCb Silicon TrackerWebsite, `http://lhcb.physik.uzh.ch/ST/public/material/index.php`.

[29] *LHCb RICH Technical Design Report*, CERN/LHCC 2000-037, September 2000.

[30] LHCb HLT trigger web page, `http://lhcb-trig.web.cern.ch/lhcb-trig/HLT/HltDescription.html`.

[31] *LHCb magnet: Technical Design Report*, CERN/LHCC 2001-007.

[32] *LHCb Calorimeters: Technical Design Report*, CERN/LHCC 2000-036.

[33] *LHCb muon system: Technical Design Report*, CERN/LHCC 2001-010.

[34] N. Tuning et al., *Ageing in the LHCb outer tracker: Aromatic hydrocarbons and wire cleaning*, Nuclear Instruments and Methods A 656 (2011) 45.

[35] J.P.Koutchouk, *Luminosity Optimization and Leveling*, Proceedings of Chamonix 2010 workshop on LHC Performance.

[36] G. W. van Apeldoorn, S. Bachmann, T. H. Bauer, E. Bos, Y. Guz, T. Haas, J. Knopf, J. Nardulli, T. Ketel, A. Pellegrino, T. Sluijk, N. Tuning, U. Uwer, P. Vankov, D. Wiedner, *Beam Tests of Final Modules and Electronics of the LHCb Outer Tracker in 2005*, LHCb-2005-076 ; CERN-LHCb-2005-076, October 2005.

[37] R. Ruschmann, *Entwicklung und Untersuchung von Straw Tubes fuer den LHCb Detektor*, Januar 2002, available under `http://www.physi.uni-heidelberg.de/Publications/`.

[38] LHCB Outer Tracker Home Page, `http://www.nikhef.nl/pub/experiments/bfys/lhcb/outerTracker/`.

[39] D. van Eijk, *Ageing and the Decay of Beauty*, Phd thesis, CERN-THESIS-2012-137, NIKHEF Amsterdam 2012.

[40] N. Dressnandt, N. Lam, R. Van Berg, H. H. Williams, *Implementation of the ASDBLR Straw Tube Readout ASIC in DMILL*, volume 2. Nuclear Science Symposium Conference Record, 2000.

[41] H. Deppe,U. Stange, U. Trunk, U. Uwer, *The OTIS Reference Manual*, Physikalisches Institut Heidelberg University, 2004.

[42] U. Stange, *Development and Characterisation of a Radiation Hard Readout Chip for the LHCb Outer Tracker Detector*, Phd thesis, Heidelberg 2005.

[43] M. Nedos, *Entwicklung, Implementierung und Test eines FPGA-Designs für die Level-1-Frontend-Elektronik des Äußeren Spurkammersystems im LHCb-Detektor*, PhD thesis, Dortmund 2008.

[44] Fabio Sauli, *Principles of operation of multiwire proportional and drift chambers*, CERN 77-09.

[45] LHCb collaboration, *Framework TDR for the LHCb Upgrade : Technical Design Report*, CERN-LHCC-2012-007, LHCb-TDR-12.

[46] A. Federico, on behalf of the LHCb Collaboration, *The LHCb Upgrade*, LHCb-PROC-2013-054, arXiv:1310.0183, CERN-LHCb-PROC-2013-054, DPF2013-49.

[47] E. Simioni, *Front End Electronics Production Status*, Talk Outer Tracker session, 2006, `https://indico.cern.ch/conferenceDisplay.py?confId=8973`.

[48] A. Pellegrino, NIKHEF (NL), Mini-review OT FE electronics architecture March 2013, private communication.

[49] Bob Zeidman, *Designing with FPGAs and CPLDs.*, 2002.

[50] Altera Arria GX web page, `http://www.altera.com/devices/fpga/arria-fpgas/arria-gx/overview/architecture/agx-architecture.html`.

[51] M.Wannemacher, *Das FPGA-Kochbuch*, International Thomson Publishing GmbH 1998.

[52] HDL Designer web page Mentor Graphics, `http://www.mentor.com/products/fpga/hdl_design/hdl_designer_series/`.

[53] ModelSim web page Mentor Graphics, `http://www.mentor.com/products/fv/modelsim/`.

[54] Quartus II web page Altera, `http://www.altera.com/products/software/quartus-ii/subscription-edition/qts-se-index.html`.

[55] J. Wu, Z. Shi, *The lO-ps Wave Union TDC: Improving FPGA TDC Resolution beyond Its Cell Delay*, DOI:10.1109/NSSMIC.2009.5401738, Proceedings of the Nuclear Science Symposium Conference Record (NSS/MIC), 2009.

[56] J. Kalisz, R. Szplet, A. Poniecki, *Field programmable gate array based time-to-digital converter with 200 ps resolution*, IEEE Trans. Instrum. Meas., vol. 46, no. 1, pp. 51Ű55, Feb. 1997.

[57] K. Hari Prasad1, V. B. Chandratre, P. Saxena, C. K. Pithawa, *FPGA based Time-to-Digital Converter*, Proceedings of the DAE Symp. on Nucl. Phys. 56, 2011.

[58] A. Villar Villanueva, *Design and implementation of the Multiple Time to Digital Converter system with sub ns resolution in a low cost FPGA for the NA62 experiment at CERN*, Master thesis, University Vigo, 2012.

[59] Altera Corporation, *Stratix PCI Development Board*, September 2003 `http://www.altera.com/literature/ds/ds_stratix_pci_bd.pdf`.

[60] Altera Device Part Number Format web page, `http://www.altera.com/products/devices/dev-format.html`.

[61] Quartus Setting File Reference Manual, `http://www.altera.com/literature/manual/mnl_qsf_reference.pdf`.

[62] SDC and TimeQuest API Reference Manual, `http://www.altera.com/literature/manual/mnl_sdctmq.pdf`.

[63] QPLL web page, `http://proj-qpll.web.cern.ch/proj-qpll/`.

[64] Particle Data Group, *Particle Physics Booklet*, July 2012.

[65] LHCb Outer Tracker group, *Performance of the LHCb Outer Tracker*, arXiv:1311.3893,2013.

[66] Tanja Haas, *Alterungsstudien und Studium der Betriebseigenschaften des Outer Trackers des LHCb Detektors* PhD thesis, Heidelberg 2007, `http://www.physi.uni-heidelberg.de//Publications/HaasDiss07.pdf`.

[67] *Beam Test of the final modules and Electronics of the LHCb Outer Tracker in 2005*, noteLHCb2005-076.

[68] V. Coco, A. Kolinskiy, LHCb Outer Tracker group, private communication, 2013.

[69] The Versatile Link Application Note, `https://espace.cern.ch/project-versatile-link/public/VersatileLinkPublicDocuments/ApplicationNote/ApplicationNoteV2.2.pdf`.

[70] GBT Project web page, `https://espace.cern.ch/GBT-Project/default.aspx`.

[71] K. Wyllie, F. Alessio, C. Gaspar, R. Jacobsson, R. Le Gac, N. Neufeld, R. Schwemmer, *Electronics Architecture of the LHCb Upgrade*, `http://cds.cern.ch/record/1340939?ln=en`.

[72] RTAX-S/SL FPGAs Microsemi web page, `http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rtax-s-sl`.

[73] K. Bunkowski, I. Kassamakov,J. Królikowski,K. Kierzkowski,M. Kudla, et al., *Radiation tests of cms rpc muon trigger electronic components.*, Nuclear Inst. and Methods in Physics Research, a, 538(1), 708-717. 2005.

[74] RT ProASIC3 FPGAs Microsemi web page, `http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rt-proasic3`.

[75] R. Lacoe, *CMOS scaling design principles and Hardening-By-Design methodologies*, presented at the Short Course Nuclear and Space Radiation Effects Conf., Monterey, CA, Jul. 2003.

[76] Y. Boulghassoul, M. Bajura, S. Stansberry, J. Draper, R. Naseer and J. Sondeen, *TID Damage and Annealing Response of 90nm Commercial-Density SRAMs*, RADECS 2008.

[77] J. M. Benedetto, H. E. Boesch, Jr. F. B. McLean, and J. P. Mize, *Hole removal in thin gate MOSFETŠs by tunneling*, IEEE Trans. Nucl. Sci., vol. NS-32, p. 3916, 1985.

[78] G. Corti, L. Shekhtman, *Radiation background in the LHCb experiment*, LHCb-2003-083, October 2003.

[79] F. FACCIO, *RADIATION ISSUES IN THE NEW GENERATION OF HIGH ENERGY PHYSICS EXPERIMENTS*, Int. J. Hi. Spe. Ele. Syst., 14, 379 (2004). DOI: 10.1142/S0129156404002429.

[80] TOTEM Collaboration, *First measurement of the total proton-proton cross section at the LHC energy of 7 TeV*, EPL, 96 (2011), p. 21002.

[81] LogicBox web page, `http://ew-dev.physi.uni-heidelberg.de/~rubio/LogicBox/index.php/Main_Page`.

[82] Coninckx F., Schönbacher H., Bartolotta A., Onori S. and Rosati A., *Alanine Dosimetry as the Reference Dosimetric System in Accelerator Radiation Environments*, Appl. Radiat. Isot. Vol. 40, No. 10-12, pp. 977-983, 1989.

[83] S. Onori, F. d'Errico, C. De Angelis, E. Egger, P. Fattibene, I. Janovsky, *Alanine dosimetry of proton therapy beams*, Med. Phys. 24 (3), March 1997.

[84] ATIMA web page, `http://web-docs.gsi.de/~weick/atima/`.

[85] PSTAR web page, National Institute of Standards and Technology, `http://physics.nist.gov/PhysRefData/Star/Text/PSTAR.html`.

[86] M. Karacson, LHCb radiation safety group, private communication, 2012.

[87] L. Zhang, Field Application Engineer EBV Elektronik for Altera FPGAs, private communication, 2013.

[88] W. Press, S. Teukolsky,W. Vetterling, B. Flannery, *Numerical Recipes: The Art of Scientific Computing*, 3rd ed. New York: Cambridge University Press, 2007.

[89] P. Antonioli, A. Alici, A. Mati, S. Meneghini, M. Pieracci, M. Rizzi, C. Tintori, *Radiation tolerance tests for key components of the ALICE TOF TDC Readout Module*, 10th Workshop on Electronics for LHC and Future Experiments, Boston, MA, USA, 13 - 17 Sep 2004, pp.184-188.

[90] N. J. Buchanan, D. M. Gingrich, *Proton Induced Radiation Effects on a Xilinx FPGA and Estimates of SEE in the ATLAS Environment*, ATLAS note, ATL-LARG-2001-011, April 2001.

[91] E. Fuller, M. Caffrey, A. Salazar, C. Carmichael, J. Fabula, *Radiation Testing Update, SEU Mitigation, and Availability Analysis of the Virtex FPGA for Space Reconfigurable Computing*, Proceeding of the MAPLD, September 2000.

[92] Altera Corporation, *Altera Configuration Devices*, `http://www.altera.com/literature/hb/cfg/cfg_ch1_vol_2.pdf`.

[93] Altera Corporation, *Stratix IV GX FPGA Development Board Reference Manual*, August 2012.

[94] Altera Corporation, *AN 553: Debugging Transceivers*, December 2009.

[95] Altera Cororation, *High Speed Mezzanine Card (HSMC) Specification*, June 2009.

[96] Laboratoire National Henri Becquerel web page, `http://www.nucleide.org/DDEP_WG/Nuclides/Fe-55_tables.pdf`.

[97] W. Blum, L. Rolandi, *Particle Detection with Drift Chambers*, Springer, Berlin (1993).

[98] CERN Engineering Department web page, `http://j2eeps.cern.ch/wikis/display/EN/PVSS+Service`.

[99] E. Rubio, Engineer Physikalische Institut Heidelberg University, private communication, 2010.

[100] N. Kupfer, Electronic technician Physikalische Institut Heidelberg University, private communication, 2013.

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