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Development of Integrated Circuits and Smart Sensors for Particle Detection in Physics Experiments and Particle Therapy

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Abstract

Future particle physics experiments have to cope with increasing demands on particle detection concerning resolution and high rates. Particle detection is the key task of tracking detectors in particle physics experiments and in medical physics in the field of particle therapy. These detectors determine the trajectory of the particles, which allows the reconstruction of the vertices and the identification of the particles. Particle detection is also important for monitoring the particle beam used for medical applications in particle therapy centres. For this purpose, particle detectors are used to ensure safe and accurate treatment.

High Voltage Monolithic Active Pixel Sensors (HV-MAPS) are a new promising technology for smart particle detection sensors. They offer promising time and vertex resolution, are cost-effective to produce, are radiation hard and can be thinned down to 50 µm.

The focus of the thesis is to investigate the suitability of HV-MAPS sensors for tracking detectors and beam monitoring and to develop smart sensor chips for these applications. In the course of this thesis, two HV-MAPS sensor families with multiple generations, the MuPix and HitPix, were developed in HV-CMOS technology. The MuPix is a large HV-CMOS sensor, which is suitable as a tracking sensor and will be used in the Mu3e experiment. It offers a time resolution of less than 10 ns and an efficiency of more than 99.8 %. The HitPix implements in-pixel counting and fast projection readout. It can handle high rates and radiation levels. This makes it suitable as a beam monitor, especially for particle therapy centres.

With the MuPix and the HitPix, two HV-MAPS chips have been successfully designed for particle detection with the advantages of HV-CMOS technology. Therefore, this thesis provides an important contribution to the application and further development of a promising new technology, both in the field of medical and particle physics.

Zusammenfassung

Zukünftige Teilchenphysikexperimente müssen steigenden Anforderungen an die Teilchendetektion hinsichtlich Auflösung und hohen Raten gerecht werden. Der Teilchennachweis ist die Hauptaufgabe von Spurdetektoren in Teilchenphysikexperimenten und in der medizinischen Physik auf dem Gebiet der Ionenstrahltherapie. Mit Hilfe dieser Detektoren werden die Spuren von Teilchen bestimmt, wodurch der Ursprung und die Art der einzelnen Teilchen rekonstruiert werden können. Auch zur Überwachung des medizinisch genutzten Teilchenstrahls in Ionenstrahltherapiezentren ist die Teilchendetektion wichtig. Hierfür werden Teilchendetektoren eingesetzt, um eine sichere und genaue Behandlung zu gewährleisten.

Ein neues vielversprechendes Konzept für intelligente Sensoren zur Teilchendetektion sind High Voltage Monolithic Active Pixel Sensors (HV-MAPS). Sie bieten eine vielversprechende Zeit- und Ortsauflösung, sind kostengünstig in der Herstellung, strahlenhart und können auf 50 µm gedünnt werden.

Der Schwerpunkt der Arbeit liegt auf der Untersuchung der Eignung von HV-MAPS Sensoren für Spurdetektoren und Strahlüberwachung sowie auf der Entwicklung von Sensorchips für diese Anwendungen. Im Rahmen dieser Arbeit wurden zwei HV-MAPS Sensorfamilien mit mehreren Generationen, der MuPix und der HitPix, in HV-CMOS Technologie entwickelt. Der MuPix ist ein großer HV-CMOS Sensor, der sich als Spursensor eignet und im Mu3e Experiment eingesetzt werden wird. Er zeichnet sich durch eine Zeitauflösung unter 10 ns und eine Effizienz von über 99,8 % aus. Der HitPix ermöglicht eine pixelinterne Zählfunktion und eine schnelle Projektionsauslese. Er kann hohe Teilchenraten verarbeiten und hält einer hohen Strahlungsbelastung stand. Dadurch eignet er sich als Strahlmonitor, insbesondere für Ionenstrahltherapiezentren.

Mit dem MuPix und dem HitPix wurden erfolgreich zwei HV-MAPS Chips für die Teilchendetektion mit den Vorteilen der HV-CMOS Technologie entwickelt. Damit leistet diese Arbeit einen wichtigen Beitrag zur Anwendung und Weiterentwicklung einer vielversprechenden neuen Technologie, sowohl im Bereich der Medizin- als auch der Teilchenphysik.

Contents

Part I

Introduction

Chapter 1

Motivation, outline and contributions

This section presents the motivation of this thesis, describes the outline and explains the author's contributions.

Motivation

Particle detectors for future particle physics experiments have to meet increasingly high requirements in terms of resolution and high rates.

In order to discover new physics beyond the standard model of particle physics, increasingly sensitive experiments are being built. An important part of these experiments are tracking detectors that record the trajectories of particles. This requires high time and vertex resolution as well as high detection efficiency and radiation hardness. Another application is particle therapy. Here, particle beams are used for tumour treatment. Beam monitoring is necessary to observe and verify the beam in order to guarantee an effective treatment as well as to prevent damage to healthy tissue. The smart sensors for this monitoring must be radiation hard, able to handle the high rates in the beam and display it accurately.

High Voltage Monolithic Active Pixel Sensors (HV-MAPS) are a new promising smart sensor technology for particle detection. HV-MAPS collect the signal charge in the sensor by drift and not by diffusion. Charge collection by drift is fast and allows for better time resolution in comparison to standard MAPS using mainly diffusion. The achieved time resolution of HV-MAPS is less than 10 ns. Furthermore, the HV-MAPS technology enables the development of robust, thin and cost-efficient sensors. With HV-MAPS it is possible to realise a fill factor of 100 % and high efficiency. The developed HV-MAPS are realised as application specific integrated circuits (ASICs) in a standard 180 nm HV-CMOS technology. This enables the implementation of complex circuits in CMOS logic.

The focus of the thesis is to investigate the suitability of HV-MAPS sensors for tracking detectors and beam monitoring and to develop sensor chips for these applications. Two HV-MAPS sensor families have been developed for two different applications. One is a large sensor specifically for particle tracking (MuPix) while the other is a radiation hard sensor that can handle high rates and is therefore suitable as a beam monitor (HitPix).

The Mu3e experiment is a particle physics experiment at the Paul Scherrer Institute in Switzerland that searches for the lepton flavour violating decay of $\mu^+ \rightarrow e^+e^-e^+$. A new, highly sensitive detector system is being built for the Mu3e experiment. The requirements for the Mu3e tracking detector are challenging: the sensors for the tracking detector have to be thinned to 50 µm to reduce multiple scattering and the time resolution has to be better than 20 ns. In addition, a high efficiency with 100 % fill factor is required. The developed full reticle size tracking sensor MuPix meets these requirements of Mu3e with an efficiency of more than 99 % and a time resolution better than 10 ns. The designs described in this thesis are the final designs that will be used for the upcoming final submission of MuPix, the final sensor for detector construction.

The Heidelberg Ion Beam Therapy Centre (HIT) is a centre for tumour treatment with particle therapy. A beam monitor is needed to guarantee safe and effective treatments.

The sensors are placed directly in the beam, meaning that they must be radiation hard and able to cope with the high rates in the beam focus. With the HitPix, a new sensor family was developed from scratch which will be used to investigate whether HV-MAPS implemented in HV-CMOS can meet the necessary requirements for beam monitoring. The HitPix was successfully put into operation and tested in several beam tests.

With the developed sensor chips, this thesis makes an important contribution to the application and further development of HV-CMOS pixel sensors for the field of medical and particle physics.

Outline of the thesis

This work focuses on the development of integrated circuits and smart sensors (HV-MAPS) for particle detection in physics experiments in the field of tracking detectors and in particle therapy in the context of beam monitoring. The work is divided into four parts. It starts with the introduction, the second part focuses on the development of integrated circuits for HV-MAPS, while in the third part, the chip development and characterisation is presented. The last part summarises and concludes the thesis.

The first part gives an introduction to the thesis. Firstly, the motivation, outline and the author's contributions are presented (chapter 1), followed by an introduction to the physics of semiconductor sensors (chapter 2) and to sensors for particle detection and tracking (chapter 3). Two different applications of HV-MAPS as sensors for particle detection are presented: Mu3e's tracking detector and a beam monitoring sensor in the context of particle therapy at HIT (chapter 4).

The second part focuses on the development of integrated circuits for HV-MAPS carried out in the scope of this thesis. The two main circuits for signal generation are presented, starting with the amplifier (chapter 5) followed by the comparator (chapter 6). Then a special library for minimising the leakage current caused by radiation is presented (chapter 7). The last chapter of section 2 is dedicated to the explanation of a counter and adder for beam monitoring and handling of high rates (chapter 8).

The third part describes the development of smart sensor chips and their characterisation: the MuPix and the HitPix, which the author conducted as part of this work. The design of the MuPix with its readout architecture and various measurements is presented (chapter 9). Next, the architecture of the HitPix and its characterisation in laboratory and beam tests is explained (chapter 10).

In the fourth part, the entire work is summarised and a brief outlook is given.

Contributions from the author

The development of several smart sensors for particle detection conducted in this work is an extensive task and is partly based on existing developments. The characterisations,

in-beam measurements and data analyses involves contribution from many people. The structure of the report of the author's contributions follows the structure of the thesis.

The charge sensitive amplifier used in the designed sensors is relying on the charge sensitive amplifiers developed by the working group for many years. Its behaviour was verified by the author with simulations. The comparator is based on a standard design. The transistor sizes were optimised by the author and the circuit was transferred into a radiation hard design with closed transistors for the HitPix project. The 180 nm HV-CMOS radiation hard library for minimal leakage currents has been developed entirely by the author. It is the first library within the designer group with a focus on minimal leakage current. The presented counter is based on the ripple counter principle and was realised by the author in the 180 nm HV-CMOS process using the library she designed. The adder was implemented by the author in the 180 nm HV-CMOS process.

Before this work began, there were already small prototypes of the MuPix, up to the MuPix7. The MuPix8 is the first larger prototype (8 mm × 19.5 mm). The author started to work on the readout buffers in a column-drain architecture already during her master thesis, and continued working on this chip in the frame of this work. The author designed the pixel and readout buffer matrices, the top level analogue design and parts of the top level digital design of the MuPix9. The MuPix10 is the first full-size MuPix ASIC (20.66 mm × 23.18 mm). Here the author further developed the readout buffer and all its sub-circuits. The developed readout buffer is the design for the final MuPix. The entire readout buffer matrix has an optimised layout to minimise space requirements. In addition, the author has carried out simulations of the individual parts, at column level and at matrix level of the MuPix10 to verify the design.

The author performed the threshold tuning measurements of the MuPix8 and their analysis with the support of a group member from the Karlsruhe Institute of Technology (KIT). The adapter boards for the existing GECCO system for the MuPix9 and MuPix10 were designed by the author. She also modified the firmware and software of the GECCO system for these two chips with a developer of the GECCO system.

HitPix, HitPixISO and HitPix2 are completely developed and implemented by the author herself. They are not based on predecessor sensor chips. The author developed the HitPix, HitPixISO and HitPix2 architectures. She designed the pixels including amplifier, comparator, in-pixel counter and adder. She developed the row control and the readout shift register to realise an address-based readout architecture. In addition, the author realised the complete top level design. Most of the circuits were designed using the radiation hard library developed by her.

An adapter board for the HitPix and its variants was designed by the author for the GECCO system. The firmware and software were adapted for the HitPix by the author and

a developer of the GECCO system. The measurements of the unirradiated and irradiated samples in the laboratory were carried out by the author. The testbeam measurements at the Heidelberg Ion Therapy Centre (HIT) were also carried out by the author together with two other members of the group from the KIT, who took care of the data transmission and beam settings. With the support of a KIT group member the data from the HitPix was analysed by the author.

Chapter 2

Physics of semiconductor sensors

The smart sensors developed and later presented in this thesis are HV-CMOS sensors. They are based on transistors implemented on silicon wafers. In this chapter, the special properties of a semiconductor, the structure and the characteristics of MOSFET transistors are presented. Then the types of noise are introduced and the radiation damage in CMOS transistors is described.

2.1 Basics of semiconductors

The ASICs developed are based on silicon and MOSFET transistors. To understand how the ASICs work, it is first necessary to have a clear comprehension of the properties of silicon as a semiconductor and how MOSFET transistors work. The two subsections first explain the different types of semiconductors and then the pn-junction.

2.1.1 Different types of semiconductors

The different types of semiconductors are presented in this section with focus on silicon. Silicon is the most often used semiconductor [1] mainly for consumer electronics [2]. This leads to a high availability and a low price.

In the periodic table of elements, silicon is located in the fourth main group due its four valence electrons, see figure 2.1.

III	IV	V
B	C	N
Al	Si	P
Ga	Ge	As

Figure 2.1: A section of the fourth group of the chemical periodic system of elements to show the position of silicon. For doping elements from the neighbouring groups like boron or arsenic are used.

The silicon atoms are arranged in a diamond cubic latter structure, see figure 2.2. The atoms are connected by covalent bonds. Each valence electron is shared with another silicon atom, so each atom is connected with four covalent bonds to four other atoms. Because all the valance electrons are involved in these bonds, pure silicon has a low conductivity [3].

The allowed states of an electron in solid state materials, like in a silicon crystal, for a time-independent potential are described by the time-independent Schrödinger equation:

$$\left(-\frac{\hbar^2}{2m}\nabla^2 + V(\vec{r})\right)\Psi(\vec{r}) = E\Psi(\vec{r}) \tag{2.1}$$

$\hbar = \frac{h}{2\pi}$ is the reduced Planck constant.

$V(\vec{r})$ is the periodic potential by the crystal lattice containing the link to the crystal lattice defining $\vec{R}$:

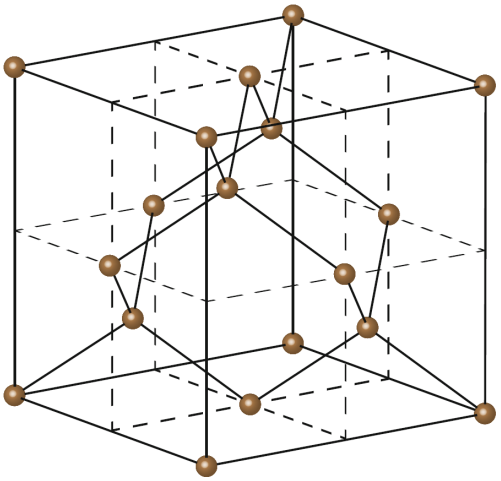

Figure 2.2: The silicon atoms are arranged in a diamond lattice repeating a pattern including 8 atoms. (From [4])

$$V(\vec{r}) = V(\vec{r} + \vec{R}) \tag{2.2}$$

In case of periodic potentials the time-independent Schrödinger equation is solved by Bloch-waves [5]

$$\Psi(\vec{r}) = e^{i\vec{k}\vec{r}} u_{\vec{k}}(\vec{r}) \tag{2.3}$$

where

$$u_{\vec{k}}(\vec{r}) = u_{\vec{k}}(\vec{r} + \vec{R}) \tag{2.4}$$

describes the periodicity of the lattice.

This leads to possible energy states for electrons. The quasi-continuous electron states are called band. Two bands have a particularly important significance as they define the electrical conductivity of insulators, semiconductors and conductors: the band with the lowest energy not fully occupied in ground state (conduction band) and the next lower band (valence band). Electrons in the valence band are not available for current flow, whereas electrons in the conduction band (and holes in the valence band) are free to move and lead to current flow if an electric field is applied. At $\mathrm{T} = 0\,\mathrm{K}$ the fermi energy is defined in the middle between the occupied states and the unoccupied states.

The different energy band structures for insulator, semiconductor and metal are shown in figure 2.3. In an insulator and a semiconductor, the valence band is separated from the

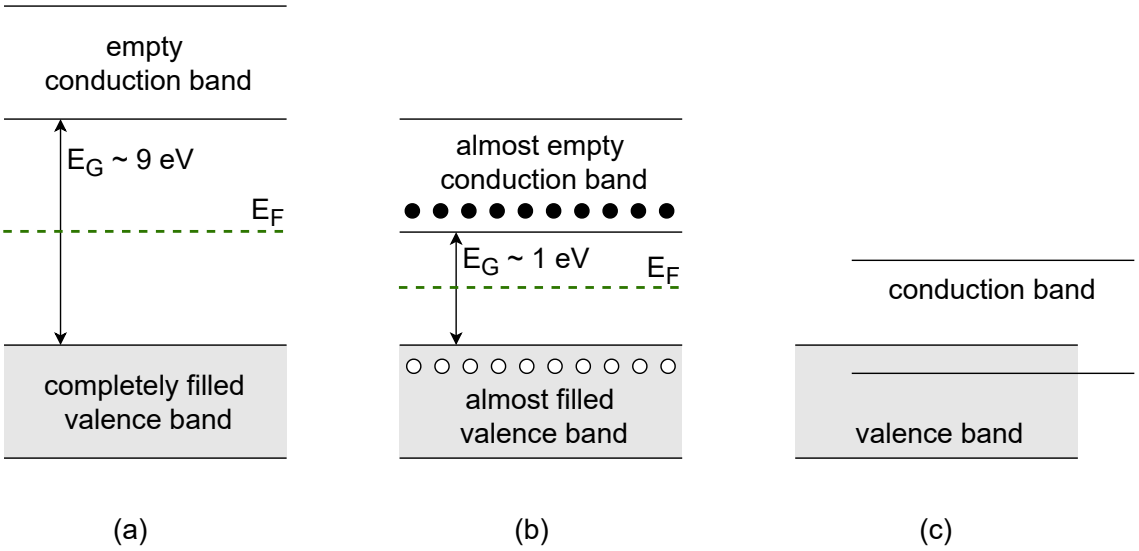

Figure 2.3: Schematic energy bands for insulator (a), semiconductor (b) and metal (c) and the fermi energy E_F. In an insulator (a) and a semiconductor (b), the valence band is separated from the conduction band by the so-called band gap. In an insulator (a) the conduction band is empty and the valence band is filled, whereas in a semiconductor (b) they are almost empty and almost full. The band gap is smaller in semiconductors than in insulators. In a conductor (c) the two bands overlap. (Modified from [4] and [6])

conduction band by the so called band gap (figure 2.3 (a)). For insulators and semiconductors the fermi level is located inside the band gap. The band gap of insulators is larger than 4 eV, for semiconductors less than 4 eV (figure 2.3 (b)). For silicon the band gap is 1.12 eV at room temperature and for silicon dioxide 9 eV. With increasing pressure and temperature, the band gap of semiconductors is decreasing. At $T = 0\,K$ in a semiconductor all electrons are in the valence band and none in the conduction band. In the case of semiconductors, small additional energy (for example thermal energy or external fields) make it possible to bring electrons from the valence band to the conduction band where they can contribute to a current flow.

The band structure of semiconductors leads to a division into direct and indirect semiconductors. Figure 2.4 shows the simplified band structure of silicon as an example of an indirect semiconductor and gallium arsenide as an example of a direct semiconductor. The indices on the x-axes are the miller indices which describe the crystal orientation. In the case of a direct semiconductor, the maximum of the valence band and the minimum of the conduction band are at the same reciprocal lattice vector (miller indices). The needed band gap energy E_G to bring an electron from the valence band with the energy E_V to the conduction band with E_C is

$$E_G = E_C - E_V. \tag{2.5}$$

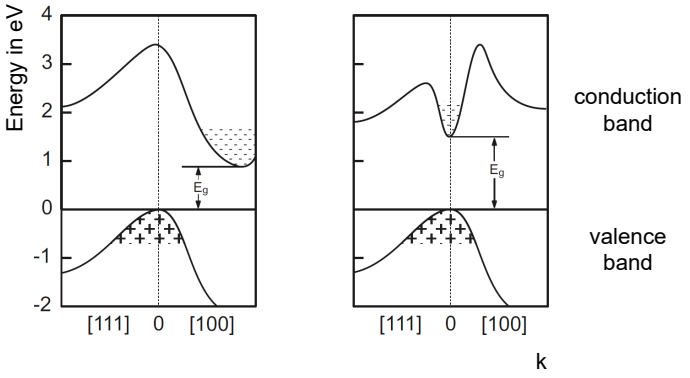

Figure 2.4: Simplified band structures of silicon (indirect semiconductor) on the left and gallium arsenide (direct semiconductor) on the right. Silicon is an indirect semiconductor because the maximum of the valence band and the minimum of the conduction band are not at the same Miller indices. In direct semiconductors such as gallium arsenide, they are at the same Miller indices. (From [4] after [8])

In an indirect semiconductor the maximum of the valence band and the minimum of the conductive band are not at the same miller indices, the band gap is indirect. Because of the indirect band gap it is not enough to bring an electron from the valence to the conductive band with the band gap energy E_G.

The detailed band structure of silicon is shown in figrue 2.5. The band gap is approximately 1.12 eV.

To move an electron from the valence band up to the conduction band, more energy is necessary or an additional impulse has to be transferred to the crystal lattice via a phonon. In the case of a direct semiconductor the maximum of the valence and the minimum of the conductive band are directly above each other, leading to a direct band gap [4]. Direct semiconductors are more efficient for light generation and absorption, therefore gallium arsenide is often used for LEDs [7].

Pure semiconductors (intrinsic semiconductors) have a high resistivity at room temperature, because thermal excitation only generates a small amount of free electrons and holes. The conductivity of intrinsic silicon is described by:

$$\sigma_i = n_i e(\mu_e + \mu_h) \simeq 2.8 \cdot 10^{-4} (\Omega\mathrm{m})^{-1} \tag{2.6}$$

with the intrinsic charge carrier density n_i, the elementary charge e and the charge carrier mobility of the electrons μ_e and holes μ_h. The given approximate value is at room temperature. To be able to put the conductivity of silicon into perspective, the conductivity of copper is 12 orders of magnitude larger with: $\sigma_{Cu} \simeq 10^8 (\Omega\mathrm{m})^{-1}$ [4].

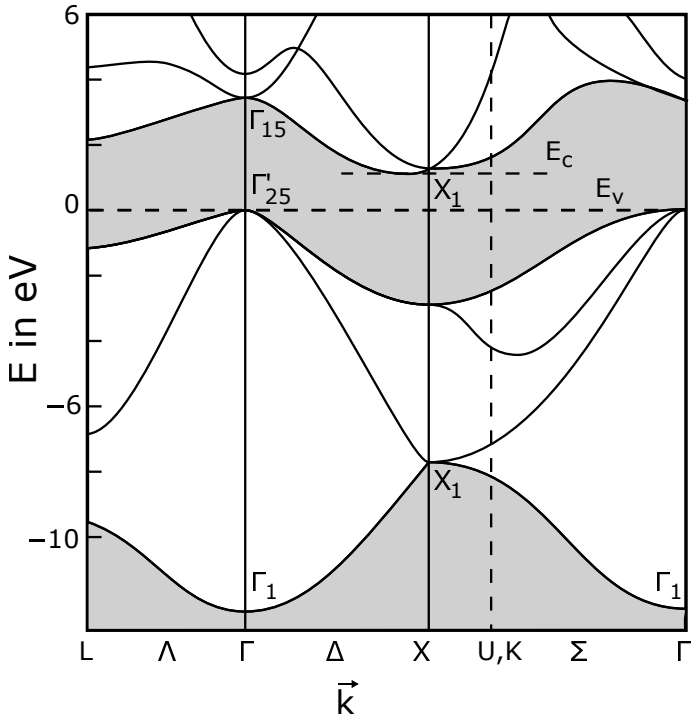

Figure 2.5: Detailed band structure of silicon. The minimum of the valence band E_V and conduction band E_C are not at the same miller indice, therefore silicon is an indifferent semiconductor. (From [9] after [10])

The resistivity of a semiconductor can be manipulated with a process called doping: impurity atoms are built into the crystal structure, the semiconductor is now called extrinsic. In the case of silicon typically elements of the III or the V group of the periodic system of elements are used. Elements of the III group have one electron less, the ones of the group V one electron more than silicon.

With elements from the III group, like boron, a vacancy in a covalent bond is added, see figure 2.6 (a). Simplified, this adds a mobile hole (electron acceptor) to the valence band. Impurity addition of electron acceptors to a semiconductor is called p-doping. In a p-doped (also p-type) semiconductor holes are majority carriers and electrons minority carriers.

If, instead of atoms of the group III, atoms of the group V are used for doping, each atom brings an additional electron into the lattice. Now electrons are majority carriers and the holes are minority carriers, the semiconductor is called n-doped (n-type), see figure 2.6 (b) [11].

Doping changes the fermi level of semiconductors: with p-doping the fermi level is decreased, with n-doping increased.

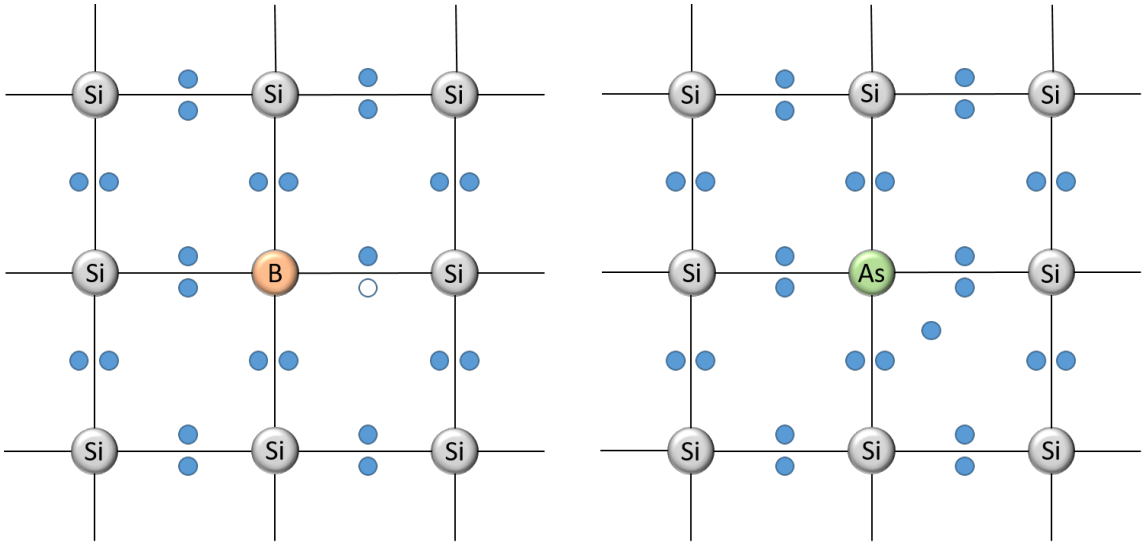

Figure 2.6: Schematic of doped silicon lattice: on the right p-doping with boron generating a hole and on the left n-doping with arsenic leading to an unpaired electron.

2.1.2 PN-junction

An n- and a p-doped semiconductor in contact with each other, is called a pn-junction. This represents one of the simplest semiconductor devices: the diode. The behaviour of this interface is important to understand the characteristics of transistors in section 2.2. The n-doped and p-doped parts show a strong concentration gradient of charge carriers. This leads to a diffusion current i_{diff}, bringing electrons from the n-doped to the p-doped region and holes from the p-doped to the n-doped region [12]:

$$\vec{i}_{\text{diff}} = -eD\nabla n \tag{2.7}$$

D is the diffusion constant, e the elementary charge and n the charge carrier density. At the interface, recombination of charge carriers leads to a zone without free charge carriers: the depletion zone. The fixed leftover ionized atoms in the n-doped and p-doped interface build a space charge region with an intrinsic electric field. The electric field leads to a drift of electrons and holes in the opposite direction of the diffusion. Figure 2.7 shows the drift and diffusion current directions of the charge carriers at a pn-junction.

In figure 2.8 the evolution of the charge concentrations and the forming of the depletion region is shown. At time $t = 0$ the p- and n-doped semiconductors build a pn-junction. Then at $t = t_1$ the free charge carriers move, due to diffusion, and recombine with each other in the area around the doping transition forming the depletion region. Here, the immobile ionized atoms form an electric field. At time $t = \infty$ the pn-junction reaches equilibrium, the driving gradients of drift and diffusion currents compensate [3].

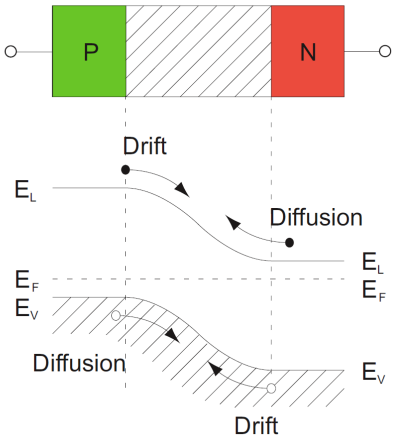

Figure 2.7: The directions of the drift and diffusion currents for electrons in the conduction band and holes in the valence band at a pn-interface. On the left, the semiconductor is p-doped and on the right n-doped. (From [4])

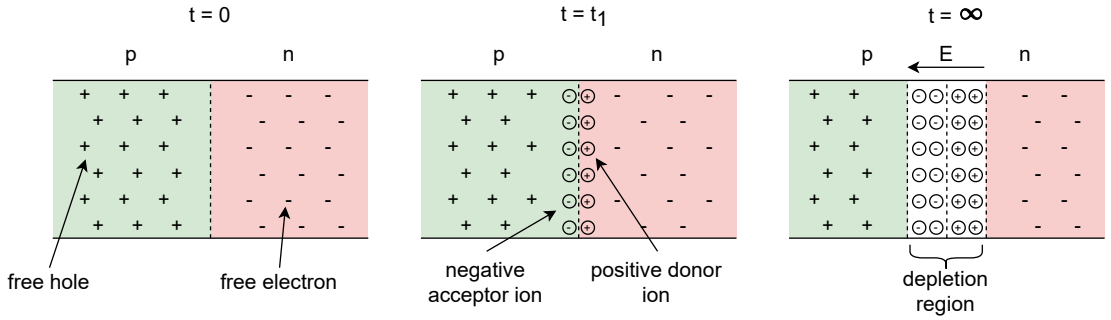

Figure 2.8: Evolution of the equilibrium of the pn-junction over time after a sudden contact. In the first figure, the two semiconductors form a pn-junction at $t = t_1$. The next figure shows at $t = t_1$ the movement due to diffusion of the free charge carriers. Around the doping transition they recombine and create a depletion zone. The immobile ionised atoms form an electric field. At the time $t = \infty$, the pn-transition reaches its equilibrium. (After [3], modified)

In equilibrium, the space charge region depends only on the doping of both semiconductors. The charge density using the Schottky approximation is [4]:

$$\rho(x) = \begin{cases} 0 & \text{for } x \leq -x_p \\ -eN_A & \text{for } -x_p < x \leq 0 \\ +eN_D & \text{for } 0 < x \leq x_n \\ 0 & \text{for } -x_p < x \end{cases} \tag{2.8}$$

The charge carrier amounts in the space charge region have to be the same for both parts of the junction:

$$N_A x_p = N_D x_n \tag{2.9}$$

Therefore the space charge region is larger in the lower doped side.

With the one-dimensional Maxwell equation for the electrical field and the boundary conditions in equations 2.1.2 and 2.1.2 the electrical field E can be calculated [4]:

$$E = \begin{cases} \frac{-eN_A}{\epsilon\epsilon_0}(x + x_p) & \text{for } -x_p < x < 0 \\ \\ \frac{+eN_D}{\epsilon\epsilon_0}(x - x_n) & \text{for } 0 < x < x_n \end{cases} \tag{2.10}$$

The maximum of the field is at $x = 0$ leading to

$$E_{max} = -\frac{eN_A}{\epsilon\epsilon_0}x_p = -\frac{eN_D}{\epsilon\epsilon_0}(-x_n) \tag{2.11}$$

The differences of the potentials ϕ in the n- and p-doped area outside the space charge region lead to a voltage drop across the depletion region, the so called built-in voltage U_{bi}:

$$U_{bi} = \phi_p - \phi_n \tag{2.12}$$

With the intrinsic (E_f) and extrinsic (E_F) fermi energies the needed potentials are calculated:

$$E_f - E_F^p = -e\phi_p = kT\ln\left(\frac{N_A}{n_i}\right) \tag{2.13}$$

$$E_F^n - E_f = -e\phi_n = kT\ln\left(\frac{N_D}{n_i}\right) \tag{2.14}$$

This leads to:

$$U_{bi} = kT\ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{2.15}$$

For silicon U_{bi} is typically between 0.6 V and 0.8 V [4]. The detailed derivation of the potentials and energies can be found in [4] and [8].

So far, the pn-junction has been considered without external voltage. Now the description is extended by an external voltage U_{ext}. The external voltage changes the width of the depletion zone. In figure 2.9 the two different cases and their effect on the depletion region are shown. If an external voltage is applied with higher potential to the p-doped and negative potential to the n-doped region, it is called forward bias, if it is applied in the other direction it is called reverse bias.

Forward bias

- U_{bi} decreases with U_{ext}: $U_{bi,\,\text{reverse bias}} = U_{bi} - |U_{ext}|$.
- The drift current is reduced compared to the diffusion current.
- In comparison to the equilibrium more electrons diffuse from the n- to the p-part while more holes diffuse from the p- to the n-part.
- The depletion region is shortened.

Reverse bias

- U_{bi} increases: $U_{bi,\,\text{reverse bias}} = U_{bi} + |U_{ext}|$.
- The diffusion current is reduced compared to the drift current.
- The depletion region gets wider.

The current of a diode as a function of the applied voltage is described with the Shockley equation:

$$I_D = I_0(e^{\frac{eU_{ext}}{kT}} - 1) \tag{2.16}$$

The ideal I/V characteristic of a diode is shown in figure 2.10. For the forward bias the current increases exponentially while for the reverse bias the current is approximately $I = I_0$, because the exponential part of the Shockley equation is negligible [8].

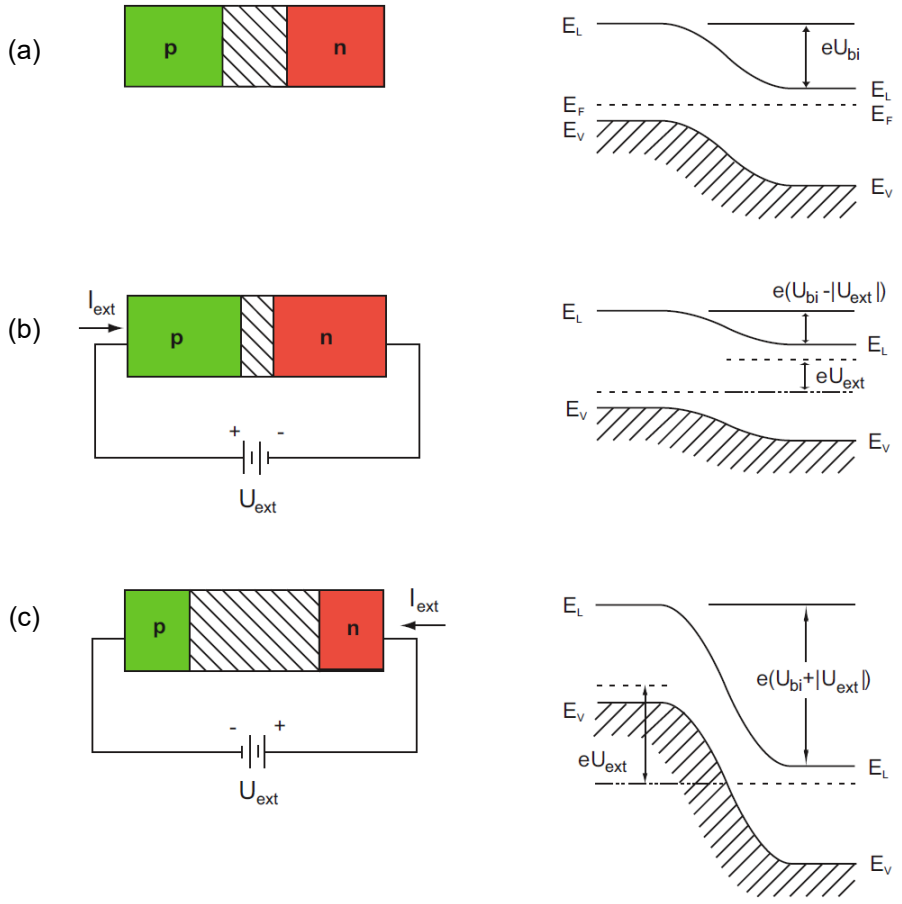

Figure 2.9: Diode without external voltage (top), with external voltage as forward bias (middle) and as reverse bias (bottom). Without external voltage, the diode is in equilibrium. If an external voltage is applied in the forward direction (higher potential for the p-doped region and negative potential for the n-doped region), the junction region shrinks: U_{bi} decreases and the drift current is reduced. With reverse bias, the junction region becomes wider because U_{bi} increases and the diffusion current is reduced. (From [4])

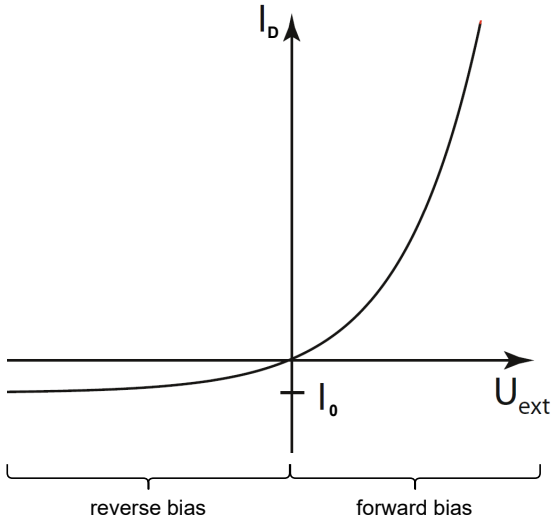

Figure 2.10: Ideal I/V characteristic of a diode. For the forward bias the current increases exponentially while for the reverse bias the current is approximately $I = I_0$.

2.2 Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

The basic elements for sensor electronics are transistors. They are used for signal amplification and readout electronics. For the HV-CMOS sensors in this thesis, metal-oxide-semiconductor field-effect transistors (MOSFET) are used exclusively. The next sections present their structure and characteristics.

2.2.1 Structure and working principle of MOSFETs

A MOSFET has four different pins: source, drain, gate and bulk. The basic idea of a MOSFET is that with a control voltage between gate and source, the conductivity between drain and source can be changed. Therefore, the MOSFET is often called a voltage-controlled resistor or a voltage-controlled current source. MOSFETs consist of differently doped areas of silicon, silicon-oxide as an insulator and poly-silicon as a conductor [13]. Depending on the source and drain doping there is a distinction between n-channel (NMOS) and p-channel (PMOS) transistors. The bulk is the substrate contact.

Figure 2.11 (a) shows the structure of an n-channel MOSFET. The source and drain are n-doped and placed in p-doped silicon substrate. For a p-channel MOSFET, the doping types are inverted. The poly-silicon gate is isolated from the substrate with a thin SiO_2 layer. The source-substrate and drain-substrate interfaces form two pn-junctions (i.e. diodes). In NMOS transistors the substrate potential has to be at a lower potential than source and drain, in which case the diodes are reverse biased.

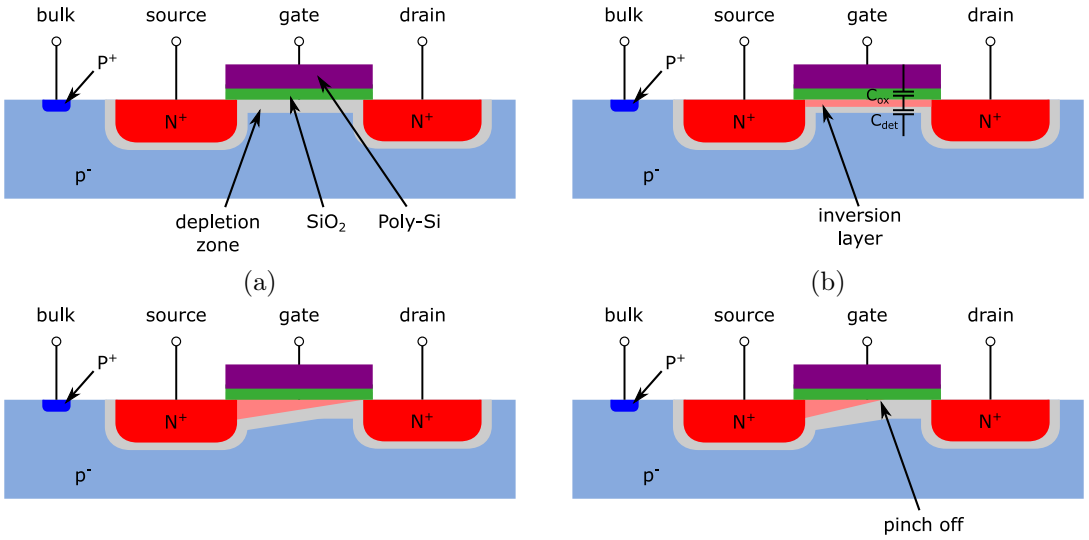

Figure 2.11: Schematic structure of an NMOS transistor without applied voltages (a). In (b) $U_{GS} > U_{Th}$ is applied, an inversion layer is formed and the transistor is operated in linear mode. (c) shows the transition between linear mode to saturation and in (d) the transistor is operated in saturation. (Modified from [6] after [14])

When the control voltage between gate and source is 0 V, no current can flow between source and drain.Without applied voltages a depletion zone is formed around the source and drain regions. The gate has a metal-oxide-semiconductor (MOS) structure, which also leads to a depletion zone below the gate. Instead of metal, poly-silicon is often used, due to manufacturing reasons, with the same behaviour [13] [11].

If a voltage higher than the threshold voltage U_{Th} is applied between gate and source (U_{GS}), a conduction channel is created between drain and source. In this case, the majority carriers are no longer available for recombination. This leads to an accumulation of minority carriers in the substrate under the gate, the inversion layer. In the case of a p-doped substrate (NMOS transistor), the inversion layer is an n-conduction channel connecting source and drain, see figure 2.11 (b). In this operation mode, the drain-source current I_{DS} increases linearly as a function of U_{DS} and the transistor behaves like a voltage-controlled resistor [13] [14] [6].

When U_{DS} reaches the value $U_{DS,\,sat}$, free electrons migrate to the source, narrowing the channel near the drain (channel pinch-off) (see figure 2.11c). The narrowed channel limits the increase in current. At higher U_{DS}, the pinch-off point shifts towards source (see figure 2.11d). In this mode the current does not change with increasing U_{DS}. The drain-source current depends on U_{GS}, this operation mode is called saturation and the transistor behaves like a voltage-controlled current source [13] [14] [6].

2.2.2 IV characteristics

After explaining the structure and the basic functionality of a transistor, the IV characteristic is now derived for an NMOS transistor. The derivation follows the example of [3].

The charge density in the channel near the source is described with the gate capacitance per unit area C_{Ox}, the width of the transistor W and the voltage difference between gate and channel. Because no mobile charge carriers exist in the channel for $V_{GS} < V_{Th}$, the charge density can be described by:

$$Q = WC_{Ox}(V_{GS} - V_{Th}) \tag{2.17}$$

Because the charge density varies over the channel due to the variation of the voltage between gate and channel, equation 2.17 has to be modified to

$$Q(x) = WC_{Ox}(V_{GS} - V(x) - V_{Th}) \tag{2.18}$$

$V(x)$ can take values between 0 and V_D if the channel is not pinched off. The current is given by the passing charge per unit length and its velocity

$$I = Q \cdot v \tag{2.19}$$

with

$$v = -\mu_n E = +\mu_n \frac{dV(X)}{dx} \tag{2.20}$$

Now equations 2.18 and 2.20 are inserted in 2.19:

$$I_D = WC_{Ox}(V_{GS} - V(x) - V_{Th})\mu_n \frac{dV(x)}{dx} \tag{2.21}$$

x describes the channel length, therefore I_D has to be integrated over the channel:

$$\int_{x=0}^{x=L} I_D dx = \int_{V(x)=0}^{V(x)=V_{DS}} \mu_n WC_{Ox}(V_{GS} - V(x) - V_{Th})\, dV \tag{2.22}$$

$$I_D = \mu_n C_{Ox} \frac{W}{L} \left[(V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{2.23}$$

For a constant V_{GS} I_D is rising until the maximum $I_{D,\,Sat}$ at $V_{DS} = V_{GS} - V_{Th}$, here the current saturates due to the channel pinch off:

$$I_{D,\,Sat} = \frac{1}{2}\mu_n C_{Ox}\frac{W}{L}\left(V_{GS} - V_{Th}\right)^2 \tag{2.24}$$

In the case $V_{DS} \ll 2(V_{GS} - V_{Th})$, equation 2.23 can be simplified to:

$$I_D \approx \mu_n C_{Ox}\frac{W}{L}(V_{GS} - V_{Th})V_{DS} \tag{2.25}$$

Here, for a constant V_{GS} I_D as a function of V_{DS} is linear corresponding to the resistor-like behaviour of the transistor. The equivalent resistance is therefore:

$$R = \frac{V_{DS}}{I_D} \approx \frac{1}{\mu_n C_{Ox}\frac{W}{L}(V_{GS} - V_{Th})} \tag{2.26}$$

The value of the resistance can be controlled by V_{GS}, according to equation 2.26. In the case $V_{GS} = V_{Th}$, R becomes infinite, the transistor is turned off. Therefore, the transistor can be seen as a voltage-controlled switch.

After the saturation point the channel shrinks (pinch off) as explained in section 2.2.1. After $V_{DS} = V_{GS} - V_{Th}$ further increase of V_{DS} shifts the pinch off point towards the source contact. Therefore, the integral borders in equation 2.22 have to be changed to contain only the channel:

$$\int_{x=0}^{x=L_P} I_D dx = \int_{V(x)=0}^{V(x)=V_{GS}-V_{Th}} \mu_n W C_{Ox}(V_{GS} - V(x) - V_{Th})\, dV \tag{2.27}$$

This leads to an equation independent of V_{DS}

$$I_D = \mu_n C_{Ox}\frac{W}{L_P}\left[(V_{GS} - V_{Th})^2\right] \tag{2.28}$$

This is under the assumption that $L_P \approx L$ is identical to the saturation current from equation 2.24. So for $V_{DS} > V_{GS} - V_{Th}$ the current saturates and the transistor behaves like a current source controlled by V_{GS}.

Figure 2.12 shows I_D as a function of U_{DS} for different U_{GS} values. In the first half (white background), the transistor behaves like a voltage controlled resistor (linear region). Later the transistor is in saturation (blue background). I_{DS} stops rising and the transistor behaves like a voltage-controlled current source.

In this analysis it is assumed that the current remains constant in the saturation range. However, this is an approximation. Actually the current increases slightly, inversely proportional to the length of the transistor. This behaviour is described by the channel length modulation and a correction factor λ is added to the equation 2.28. For more information on channel length modelling, see [16] [11] [15].

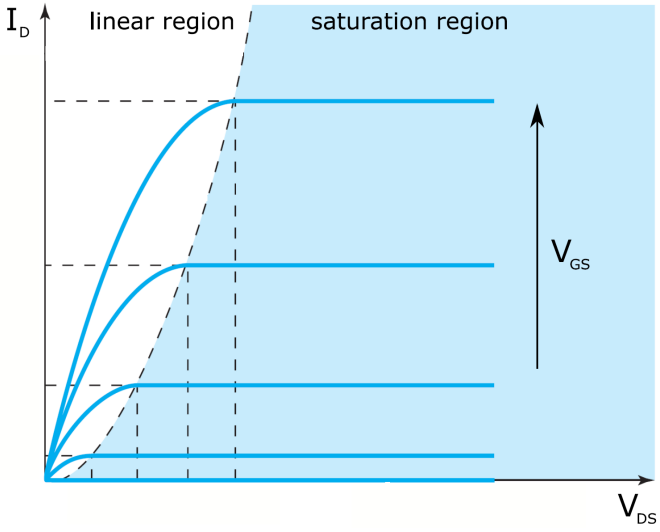

Figure 2.12: IV characteristics of a MOSFET for different U_{GS} values, from bottom to top the U_{GS} voltage increases. (Modified from [15])

2.3 Noise types

Statistical fluctuations in all circuits cause variations in voltages or currents, these are called noise [4]. First, the current I through a sample with a length l is considered. Assuming n carriers with a defined charge of e and a velocity v are moving through the sample, the introduced current is

$$I = \frac{nev}{l} \tag{2.29}$$

The fluctuations of this current are given by

$$\langle di \rangle^2 = \left(\frac{ne}{l}\langle dv \rangle\right)^2 + \left(\frac{ev}{l}\langle dn \rangle\right)^2 \tag{2.30}$$

It can be seen that there are two mechanisms that contribute to the total noise. The fluctuations of velocity are leading to the so called thermal noise (also called Johnson's noise) while the number fluctuations are the reason for shot noise and flicker noise (also called $1/f$ noise) [17].

Thermal noise

The charge carriers move within a conductor and semiconductor due to their kinetic or thermal energy. This is called Brownian movement. Considering the thermal noise of a resistor, the expected values are given by the Nyquist formulas with the Boltzmann constant k_B:

$$d\langle i^2 \rangle_{thermal} = \frac{1}{R}\frac{dP_n}{df}df = \frac{1}{R}4k_BTdf \tag{2.31}$$

$$d\langle u^2\rangle_{thermal} = R\frac{dP_n}{df}df = R4k_BTdf \tag{2.32}$$

From these formulas it follows that the noise is not dependent on the current flowing through the resistor. The thermal noise is dependent on the bandwidth, the absolute temperature and the resistance value. The frequency spectrum of thermal noise is white (constant power spectral density) [18] [4].
The thermal noise has to be taken into account, especially for the channel of the input transistor of the charge sensitive amplifier. This channel behaves like a resistor with non-uniform resistance. The thermal noise leads to current fluctuation of the current flowing through the resistor.

Shot noise

Shot noise occurs during the transport of charge carriers across a potential barrier, for example, at the pn-junction. The spectral noise current density is described by the Schottky relation [4]

$$d\langle i^2\rangle_{shot} = 2eI_0df \tag{2.33}$$

with the electronic charge e and the average current I_0. The shot noise is directly proportional to the current [18] [4].

Flicker noise

The Flicker noise is, unlike the noise types mentioned before, not white. The noise spectrum becomes "non-white" or non-uniform whenever the fluctuations are not purely random in time.

In transistors, charge carriers can be trapped in the gate insulator. This leads to fluctuations in the transistor current. The number of charge carriers and their mobility are influenced by the oxide/bulk charge. This current varies with the trapping of the charge carriers. Charge capture is described by two time constants, the capture time and the emission time [16].

A pure $1/f$ distribution of the spectral power density occurs with an infinite number of uniformly distributed time constants. Already 3 trapping processes with different time constants can result in a $1/f$ spectrum for a wide range [17] [4]. In the case of an amplifier the charge trapping in the gate insulator causes fluctuation of the oxide and bulk charge. The spectral density of this trapping process has the typical dependency of 1/f [17] [4].

2.4 Radiation damage

For many years the radiation hardness of CMOS transistors has been studied due to many application fields of semiconductor devices in radiation environments, such as in space or high energy physics [19] [20].

Radiation damage in metal oxide semiconductors (MOS) changes the basic electro-physical characteristics of transistors [21]. The damages can be separated into two different groups: bulk damage and surface damage. The bulk damage influences the signal generation in the silicon sensor part. The surface damage, on the other hand, influences the behaviour of the CMOS electronics.

Bulk damage

Bulk damage is caused by defects in the crystal structure of silicon due to non-ionizing energy loss of particles [6]. The transferred energy from particles can be large enough to lead to point and cluster defects by removing atoms from the lattice leaving a vacancy. The removed atom can stop somewhere else in the lattice and is called interstitial. In the case that vacancy and interstitial are locally close they form a so called Frenkel defect (see figure 2.13).

These defects lead to macroscopic effects in the band structure as shown in figure 2.14:

- **Donor and acceptor generation**
  States close to the conduction and valance band change the effective doping concentration. They lead to a change of the depletion zone and can lead to type inversion of n-type to p-type substrate. The depletion voltage can drop first and then start to rise later with higher radiation [22].
- **Charge trapping**
  Charge generated by particles can be trapped by defects leading to a lower signal due to less available charge. The trapping reduces the charge collection efficiency of the sensor.
- **Increase of leakage current**
  If the states are close to the middle of the band structure, they lead to a higher leakage current due to more generation centres. More leakage current leads to more shot noise. If the sensor is cooled during operation, the leakage current is smaller.

Parts of these damages can heal over time. This is called annealing. Most likely Frenkel effects "repair themselves" with time. The annealing effect accelerates at moderately higher temperatures. Therefore, the irradiated sensors measured in section 10.3.2 were cooled down to -40°C to prevent annealing processes [22].

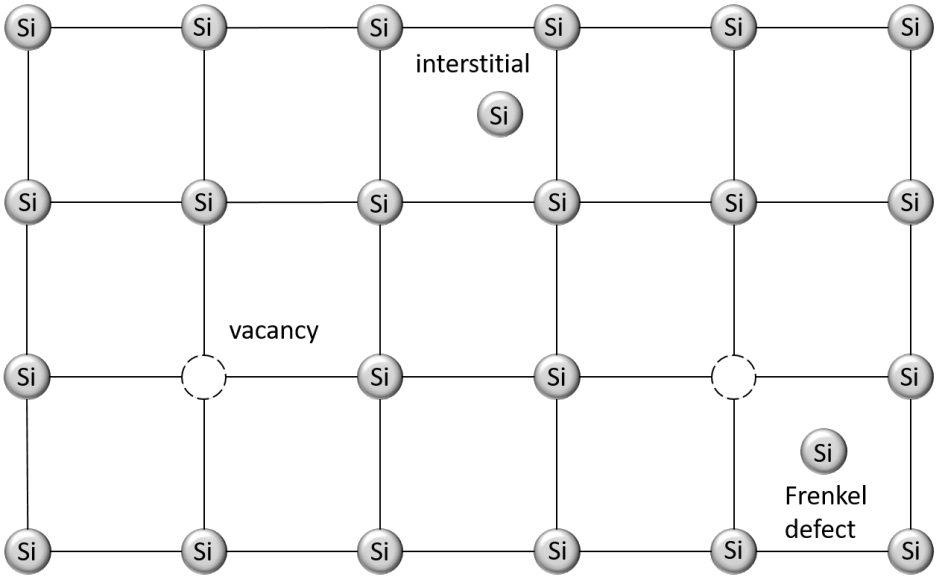

Figure 2.13: Defects in the silicon lattice: vacancy if an atom is removed, interstitial where the removed atom rests. In the case that vacancy and interstitial are locally close, they form a Frenkel defect.

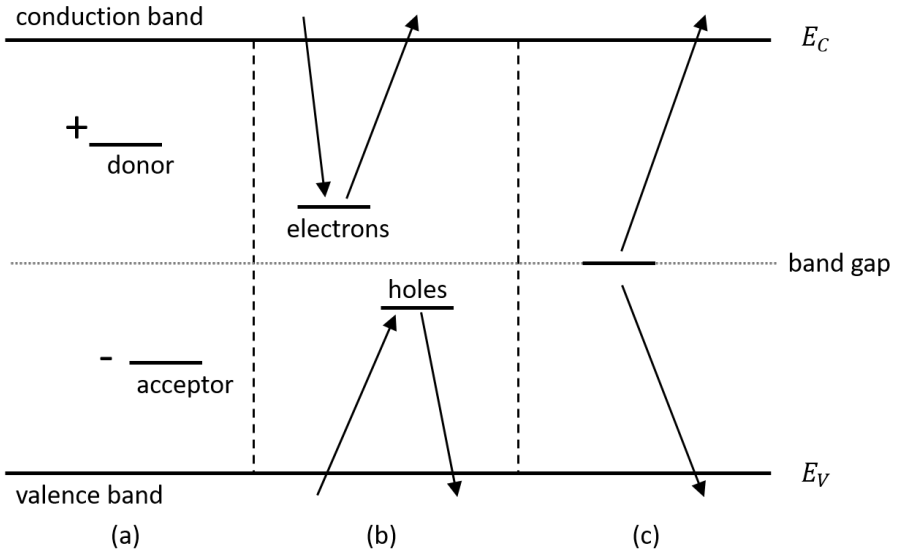

Figure 2.14: Additional states in the band structure of silicon due to lattice defects. There are 3 different types: donor and acceptor generation (a), charge trapping (b) and increase of leakage current (c). First the donor and acceptor generation (a), these are states close to the conduction and valance band. They change the effective doping concentration and lead to a change of the depletion zone. Charge generated by particles can be trapped (b) by defects leading to a lower signal due to less available charge. If the states are close to the middle of the band structure (c), they lead to a higher leakage current due to more generation centres. (After [4] [22])

Surface damage

Surface damage due to ionizing damage changes the electrical behaviour of CMOS electronics. Electron hole pairs generated by the charged particles in the silicon oxide are quite immobile. Nevertheless, the electrons are more mobile than the holes and can sometimes leave the oxide through the gate contact. But the holes will most likely remain in the oxide, leading to a positive charge accumulation there.

In the past the total dose tolerance was limited by the radiation damage in the gate oxide [19]. In the deep sub-micron technologies, like the used 180 nm HV-CMOS process, the gate oxide is thinner and the tunnelling gets easier, therefore these technologies are inherently more radiation tolerant [19]. Nevertheless, special layouts for NMOS transistors have to be used to reduce the leakage current flow.

Trapping centers are built and space charge is accumulated in the silicon oxide leading to a shift in threshold voltages [21] [23]. Furthermore, the mobility of charge carriers in the near surface semiconductor region is decreasing [21]. The charge trapped in the oxide leads to a negative threshold voltage shift for NMOS and PMOS transistors [24] [25] [23]. The charge trapped in the interface shifts the threshold voltage for NMOS in a negative direction and a positive one for PMOS [24] [25] [23]. The threshold shift due to irradiation depends on the thickness of the oxide [23].

In the p-well and p-substrate underneath the field oxide an inversion layer is generated. This layer is formed by the accumulation of positive charge in the silicon oxide after irradiation. The inversion layer allows for a leakage between source and drain and also for inter transistor leakage between neighbouring n^+ implants. The leakage between source and drain can be avoided by forcing all source to drain current to flow only underneath the gate oxide by using a closed gate. With the closed gate, no current path is available underneath the field oxide or along the edges of the active area [26] [20]. The inter transistor leakage between n^+ implants, also caused by the inversion layer, can be prevented by the use of separating guard rings. These isolate the n^+ implants wherever it is necessary [26].

An enclosed transistor design together with guard rings where needed are a common and successful approach to reduce the leakage current [23] [20] [26] [27] [19]. Different papers have studied the radiation effects on enclosed NMOS transistors in different commercial CMOS technologies, like in standard commercial 0.6 µm [23], 0.5 µm [26], 0.35 µm CMOS [20] or 0.25 µm [19] CMOS processes.

The calculation of (W/L) for enclosed transistors, as used for the radiation hard library, is explained in detail in [19]. The enclosed transistors have a non-symmetrical geometry because the source and drain contacts can be chosen inside and outside or the other way around. This leads to an asymmetric behaviour of the device [19].

Chapter 3

Sensors for particle detection and tracking

First, the differences between hybrid and monolithic pixel sensors are shown. Then monolithic active sensors (MAPS) are explained, followed by monolithic active pixel sensors (HV-MAPS). The smart sensors developed in this thesis are HV-MAPS.

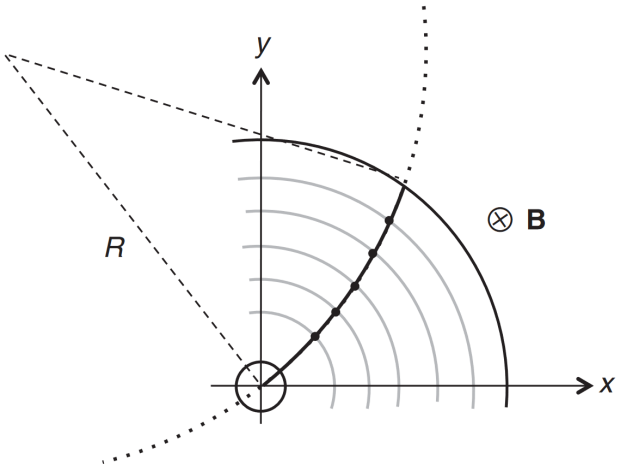

Figure 3.1: The tracking detector consists of several layers, charged particles leave bent trajectories in the detector due to the magnetic field. (From [28])

In many particle physics experiments particle beams are brought to collision at high energies. Other experiments, like Mu3e, collide particles with fixed targets. In both cases the elapsing particle reactions are observed. Many particles decay before they reach the detector. In this case the decay products with sufficient lifetime are observed. In the analysis of the detector's information, the original interaction process with the following decay processes are reconstructed. For this, the involved particle types, their energy and their origin are necessary.

The task of the so-called tracking detectors is to resolve the location and time of the particle hit as precisely as reasonable for the following reconstruction. By this, the particle trajectories and their momenta can be calculated. To get the necessary information, most tracking detectors have a similar structure: several cylindrically arranged layers of particle tracking sensors are built around the interaction point, with the beam axis as symmetry line. A magnetic field parallel to the beam axis leads to bended trajectories of charged particles, see figure 3.1. The magnetic field is usually provided by a solenoid magnet around the detector. On the path of a particle through the tracking detector, it is scattered at the detector itself. To reach a high spatial resolution, the deflection should be small which leads to the requirement for minimal material budget.

3.1 Hybrid and monolithic pixel sensors

The goal of pixel sensors is a two dimensional information on the particle-sensor interaction point. This is achieved by a segmentation of the sensor in two directions leading to a pixel matrix [17].

There are two major approaches to realising this: hybrid and monolithic pixel sensors.

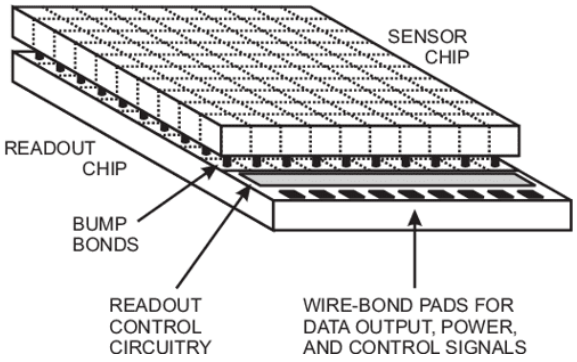

Figure 3.2: A hybrid pixel detector consists of a sensor and a readout chip connected by bump bonds. (From [17])

Hybrid pixel sensors consist of two application-specific integrated circuits (ASIC): the sensor and the readout ASIC (front-end chip). Sensor and readout ASIC are connected in every pixel by bump bonds (figure 3.2) [4]. Particles flying through the sensor generate charge. The signal processing is then done on the readout ASIC. As the pixel has to match the corresponding part of the readout ASIC, the pixel size is limited by the bump bond size. An advantage of hybrid pixel sensors is that both chips can be developed individually and both parts do not need to have the same development cycle. For example the sensor ASIC can be used for several generations of readout ASICs. Also the sensor chips can be used with different front-end chips for different applications and for both ASICs different fabrication technologies can be used. A disadvantage is that the assembling of the connecting bonding is complex as well as time and cost intensive. Furthermore, the sensor ASIC can often not be produced in standard processes leading to an expensive fabrication that is only offered by a few manufacturers. Another disadvantage is the detector thickness due to two ASICs causing multiple scattering [29].

The other common approach is monolithic pixel sensors. In the case of implementations with electronics inside the pixels, these sensors are referred to as monolithic active pixel sensors (MAPS). Here, the sensor and readout are realised on one chip: signal generation, amplification and signal processing are done on the same die.

3.2 High Voltage Monolithic Active Pixel Sensors (HV-MAPS)

The idea of using commercial technologies to develop a monolithic active pixel chip was published first in 1989 [30]. In 2001, monolithic active pixel sensors produced in a standard CMOS technology (MAPS) were presented for charged particle tracking in [31]. In contrast to passive pixel sensors, in which the photo-diode used as the sensor is directly connected to the output line, in active pixel sensors the pixel itself contains an amplifier.

For the first prototype, the minimum ionising particle MOS active pixel (MIMOSA), a standard 0.6 µm CMOS technology was chosen. The used CMOS technology provides a twin-well implanted in a p-type epitaxial layer. A photo-diode already available in CMOS technology was chosen as sensor with the partially depleted thin epitaxial silicon layer as sensitive sensor volume. The charge collection in these MAPS is efficient and on the order of 100 ns [31].

At that time, CMOS sensors were already used for visible light detection, as the standard VLSI technology makes the sensors cheap. Furthermore, the concept is power-saving as the in-pixel are only active during readout and no clock signal has to be distributed. The pixels are easy accessible by addresses for readout. Another advantage is that complex circuits can be realised with CMOS to implement a variety of functionalities [31].

However, MAPS in CMOS technology are also interesting for particle tracking. For particle physics experiments, high efficiency and spatial resolution of detected minimum ionizing particles (MIPs) is necessary. Pixel sizes are usually between 10 and 20 times the minimum feature size of the fabrication process, which means that small pixels are possible. The substrate can be thinned down to a few tens of microns, so that multiple scattering is low. Another advantage is that sub-micron VLSI technologies are less sensitive to radiation damage. In addition, a signal-to-noise ratio of over 100 can be achieved. The n-well and the p-type epitaxial layer form the photo diode. As the charged particles pass through the diode, they generate electrons in the epitaxial layer that move to the n-well diode contact mainly by diffusion. A relativistic charged particle typically generates 80 pairs of electrons and holes per micrometre of silicon. The most important technology parameter for MAPS is therefore the thickness of the epitaxial layer, as this defines the number of electron-hole pairs generated. An epitaxial layer between 12 and 16 µm leads to about 1000 electron-hole pairs per MIP [31].

In 2006, a realisation of MAPS in a triple-well CMOS process was proposed by [32]. The triple-well process makes it possible to implement more complex signal processing circuits at pixel level and to increase the size of the charge-collecting electrode. The deep n-well available in the triple-well technology is used as sensor electrode and part of the readout electronics are placed in the same physical area. The chosen 0.13 µm technology has a thin oxide of about 2 nm, resulting in a high radiation tolerance [32].

The charge in MAPS is collected by diffusion causing a slow collection time of about 100 ns [4] [17] and small amplitudes [33]. To solve these problems, a MAPS using high voltage (HV-MAPS) realised with high voltage CMOS (HV-CMOS) technology was presented in 2007 [34]. HV-CMOS technologies provide standard submicron CMOS transistors (which operate at less than 3.3 V) and high voltage transistors (operating at for example up to 60 V) in a triple-well process. The low-voltage transistors are used for the internal electronics

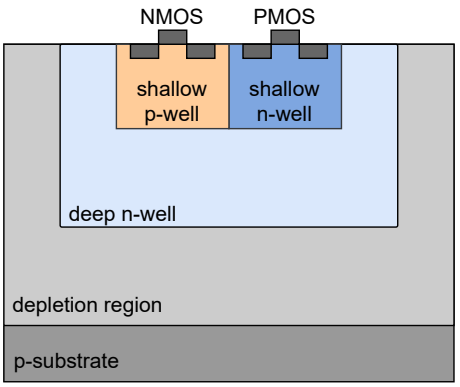

Figure 3.3: In a triple-well structure electronics can be placed in shallow n- and p-wells. A high voltage is applied at the substrate leading to a large depleted area.

(signal amplification, signal processing and readout). The high voltage transistors are used in the output driver [34].

Many HV-CMOS processes offer so-called floating logic. Floating logic allows the implementation of low-voltage electronic blocks in which the ground node is electrically isolated from the substrate. If a p-substrate is used, all transistors of a floating block are placed in a single, low-doped deep n-well. The triple-well structure allows the use of a p-substrate with a deep n-well and a shallow n- and p-well, as seen in figure 3.3. The transistors are placed in these shallow wells with PMOS transistors located in the n-well and NMOS transistors in the p-well [34]. Small standard low-voltage transistors can be used, although a high reverse bias voltage with respect to the p-substrate is applied to the deep n-well. This is possible because the transistors inside the n-well are shielded from the large voltage and are driven with low voltage between their electrodes. In a 0.35 µm process, the depletion area between the deep n-well and the substrate is about 10 µm for a reverse bias of 60 V. This leads to about 780 electrons generated by a MIP. The depleted area can be larger than the depleted area of a typical pn-junction in a MAPS.

For a pixel, the deep n-well has two functions: on one hand it is used to isolate the shallow wells and on the other hand it is used as charge collecting electrode. Complex electronics can therefore be placed inside the n-well. The deep n-well is connected to a highly-resistive circuit based on PMOS transistors between the analogue positive supply voltage (vdda) of 1.8 V and the n-well [34]. The charge generated by a particle in the depleted region is separated by the strong electric field and the negative charge is collected by the n-well [35]. To detect the charge, the n-well is floating, which means that it is acting like a capacitance. The collected charge leads to a small potential drop in the n-well. This small potential drop is amplified by a charge sensitive amplifier also located in the pixel. This is an important property of the pixel: the electronics in the pixel is floating so it can measure the potential change in its own substrate [36] [37].

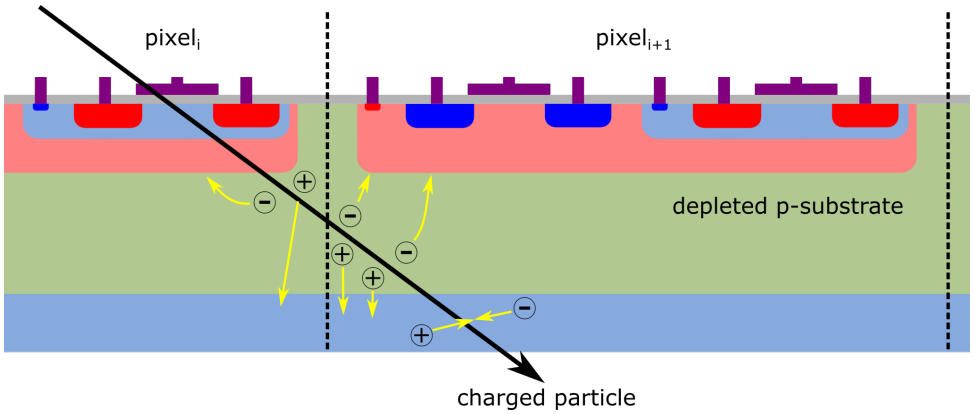

Figure 3.4: A particle generates electron-hole pairs inside a HV-CMOS sensor. The electrons are collected by the collecting electrode, the deep n-well. Here the charge is collected by two pixel electrodes (charge sharing). (From [6])

Due to the strong field, charge is collected by drift, resulting in a fast charge collection process with a time resolution on the order of 15 ns [35] [38] [39]. Figure 3.4 shows a charged particle moving through the HV-CMOS sensor. The electrons are collected by drift in the charge collection electrode (deep n-well). The holes are collected by the substrate contact and do not contribute to the signal charge. If an electron-hole pair is generated outside the depletion region, it is not collected in time to contribute to the signal. In the figure, the generated charge is collected by two neighbouring pixels, which is called charge sharing. If all generated charge is collected by the same pixel, there is no charge sharing and only this pixel generates a hit signal [34] [6].

HV-MAPS offers 100 % fill factor as the pixels are fully sensitive. In addition to the advantages of MAPS, HV-MAPS enable a fast signal response as charge collection is mainly done by drift. This makes HV-MAPS suitable for particle detection, for example in tracking detectors.

Chapter 4

Application for particle physics experiments and particle therapy

In this work, sensors for particle detection were developed for two applications: for particle tracking in the Mu3e experiment (MuPix) and for beam monitoring in particle therapy for HIT (HitPix). In this chapter first the Mu3e experiment will be presented to illustrate the environment and requirements of MuPix. The motivation for the Mu3e experiment is explained in 4.1.1 and in 4.1.2 the detector system with the different sub-detectors is described. Section 4.1.3 focuses on the impact of the MuPix for Mu3e.

The second application of a particle detection sensor is beam monitoring in cancer treatment centres that offer particle therapy, such as the Heidelberg Ion Therapy Centre (HIT). In section 4.2.1 particle therapy is explained, followed by a short introduction to beam monitoring at HIT. In section 4.2.3 the idea of a HV-MAPS beam monitoring chip is discussed.

4.1 Application for the Mu3e experiment

4.1.1 Motivation of the Mu3e experiment

The Mu3e experiment aims to search for the lepton flavour violating decay $\mu^+ \to e^+e^-e^+$ with a sensitivity of one in 10^{16} muon-decays in the second phase [40]. In the first phase, the existing muon beam line πE5 at the Paul Scherrer Institute (PSI) will be used to reach a single event sensitivity of $2 \cdot 10^{-15}$, representing 10^8 muon decays per second. In the second phase, it is planned to use a new muon beam line studied in the high intensity muon beam HiMB project at PSI with a higher intensity [41] [42].

In the Standard Model of particle physics the $\mu^+ \to e^+e^-e^+$ decay is strongly suppressed because lepton flavour violation is suppressed at tree level. Models beyond the Standard Model allow an experimentally accessible amount of lepton flavour violating processes like the $\mu^+ \to e^+e^-e^+$ decay. Observing this process would new physics could be discovered [40] [42].

In phase I the detector has to provide a single event sensitivity of $2 \cdot 10^{-15}$ on the branching fraction which requires more than $2.5 \cdot 10^{15}$ stopped muons, leading to a run time of 400 days [42].

For Mu3e two types of background are particularly important. One is the muon decay with internal conversion $\mu^+ \to e^+e^-e^+\bar{\nu}_\mu\nu_e$. This requires precise momentum resolution for suppression. This is achieved by an ultra-thin detector to minimise multiple scattering. In addition, there is combinatorial background, for example, due to Michel decays and Bhabha scattering. Here, an excellent momentum, vertex and time reconstruction are necessary for the suppression [40] [42] [41].

4.1.2 Concept of the Mu3e detector system

The Mu3e detector consists of different sub-detector systems to fulfil the requirements in efficiency and momentum resolution, timing and track measurements [43]:

- Ultra thin pixel tracking detector
- Scintillating fibre detector
- Scintillating tile detector

The muons are stopped at a target, such that the decaying muon is at rest and emits all decay products at the same time. Figure 4.1 shows an open 3D view of the detector [42].

A magnetic field of 1 T is provided by a solenoid around the whole Mu3e detector. The silicon pixel tracker is used to measure the momenta of the particles. The dominant factor

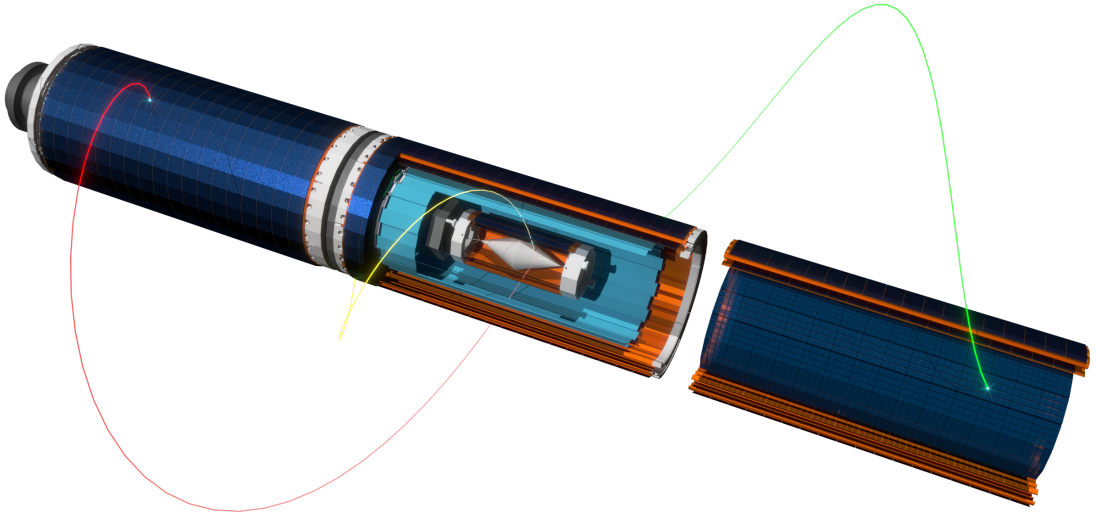

Figure 4.1: Open view of the Mu3e detector with the stopping target in light gray, the pixel tracker in orange and the scintillating fibre detector in light blue. (From [42])

for the momentum resolution is multiple Coulomb scattering in the pixel detector material. Therefore, the detector has to be as thin as possible. This is achieved with thinned silicon High Voltage Monolithic Active Pixel chips [44] [45] (see chapter 3.2).

In the following, the different parts forming the Mu3e detector system are introduced.

The task of the **magnet** is to provide a homogeneous solenoidal magnetic field of $B = 1\,\mathrm{T}$ for the tracking detector to allow a precise momentum determination of the muon decay products. The magnetic field has to be homogeneous. The requirements only allow field inhomogeneities along the beam line below relative deviation of 10^{-3} within $\pm 60\,\mathrm{cm}$ around the center of the magnet. Furthermore, the magnet has to be stable and operation has to stay at reasonable costs. To fulfil the requirements a superconducting magnet design with a closed cooling system has been chosen. The magnet has been delivered in 2020 and performs as expected [46] [42].

The muons ($p = 28\,\mathrm{MeV/c}$) are stopped at a **target**. The stopping target is optimised for stopping power, for keeping its impact on the track measurement low and for wide spreading of the µ-stops. A target similar to the one used for SINDRUM [47] shaped like a double cone made out of Mylar is chosen for Mu3e. The dimensions of the stopping target are shown in figure 4.2. The target has a mass of $0.671\,\mathrm{g}$ and a total area of $6\,386\,\mathrm{mm}^2$ [42].

The **pixel tracker** has to provide precise hit information of the electrons for track reconstruction. To allow for high vertex and momentum resolution the multiple scattering needs

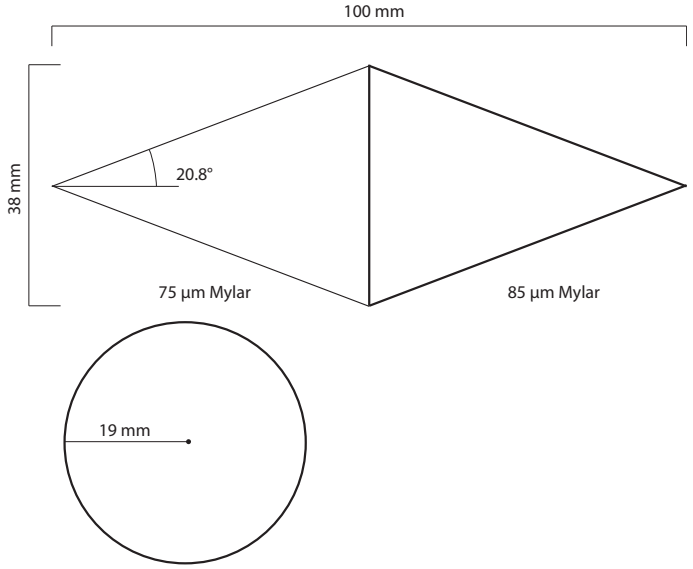

Figure 4.2: Dimensions of the stopping target for Mu3e. The target is shaped like a double cone and made out of Mylar. (From [42])

to be minimized leading to the task of material minimization in the active area. Therefore, High Voltage Monolithic Active Pixel Sensors (HV-MAPS) thinned to 50 µm were chosen to build the pixel tracker. The HV-MAPS are mounted on thin flexible High Density Interconnect (HDI) circuits which provide the power, signal and data lines. The HV-MAPS developed for the Mu3e experiment are called MuPix. The data are read out by three differential lines per chip at a bandwidth of 1.25 Gbit/s per line [42]. The MuPix chips are bonded to the HDI using Singlepoint Tape Automated Bonding (SpTAB), so no additional bonding material is necessary [48] [49]. Thin polyimide foils provide the mechanical stability. Due to the requirement of minimal material no further support structure is allowed. Therefore, the pixel modules consist only of the sensor, the HDI and the polyimide foil. The cooling system is based on a dry helium atmosphere for minimum additional multiple scattering [49] [42].

Figure 4.3 shows the three parts of the Mu3e pixel tracker: in the middle, close to the target, the central pixel tracker is located and on the sides two recurl trackers are placed. The central pixel detector detects the hits for track and decay vertex reconstruction. Reconstruction of hits with higher purity and improved momentum resolution is possible with the hits measured by the recurl trackers. All three parts of the pixel tracker are built out of the same HV-MAPS chip, the MuPix. The central pixel tracker consists of four layers while the recurl trackers are made up of two layers each [42]. Figure 4.4 shows the central tracker with the different layers from two different perspectives.

Besides the pixel tracker the Mu3e detector contains two timing detectors, the scintillating fibre and scintillating tile detector. Their location is shown in figure 4.1 [43].

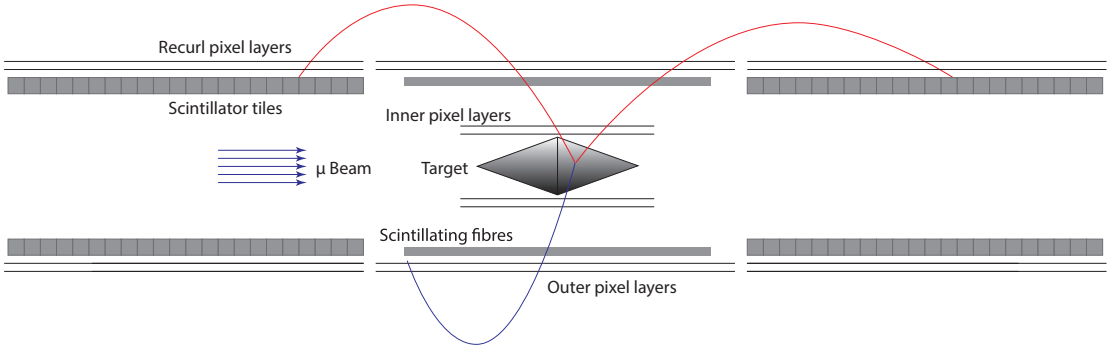

Figure 4.3: The Mu3e pixel tracker consists of the central tracker and two recurl trackers. It is complemented by two timing detectors, the scintillating fibre and tile detectors. (From [42])

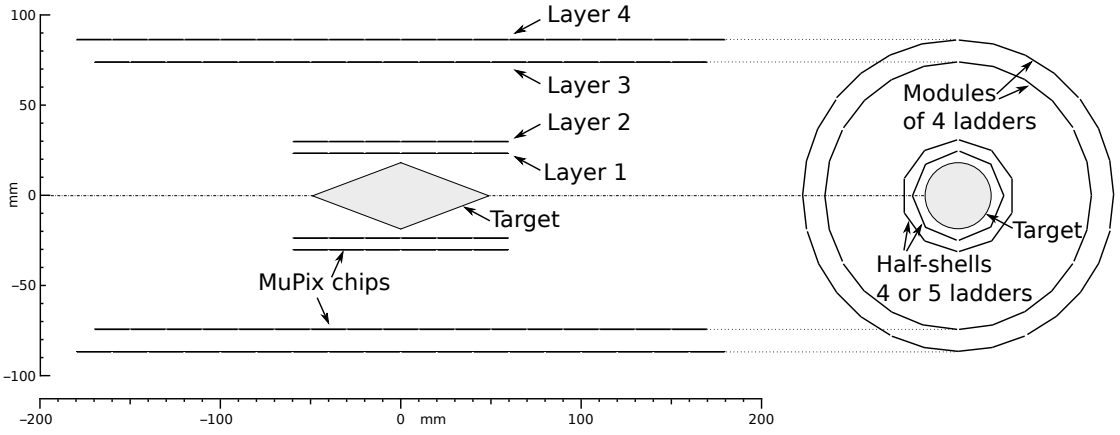

Figure 4.4: The central pixel tracker is formed by four layers of MuPix chips. The layers are built up from modules consisting of 4 or 5 ladders. (From [42])

The purpose of the **scintillating fibre detector** (SciFi detector) is mainly to suppress accidental combinatorial background from tracks with different timing. This leads to challenging specifications of the SciFi detector: time resolution of 250 ps, efficiency of more than 95 %, spatial resolution around 100 µm. Because the SciFi detector is located in the central region of the experiment (see figure 4.1 in light blue), it has to be as thin as possible and compact, similar to the pixel tracker. In addition to the timing measurement, the SciFi detector can perform a time of flight measurement to help resolving the direction of rotation of the recurling tracks. The SciFi detector has a radius of 61 mm and a length of about 300 mm [50] [51] [42].

The **scintillating tile detector** is located in the recurl section inside the pixel layers as shown in figure 4.3. The aim of the scintillating tile detector is a time resolution below 100 ps and close to 100 % efficiency. This is necessary to identify a coincident signal from three electrons and suppress combinatorial background. With a time resolution below 100 ps the tile detector provides the most precise timing information of the particle tracks possible. Because the scintillating tile detector, unlike the fibre detector, is not located in the centred region of Mu3e, but in the recurl stations, there are no strong constraints in material budget. Nevertheless, the detector is placed inside the recurl pixel detectors leading to tight spatial constraints [52] [42].

Both the scintillating fibre and tile detector are read out by a custom mixed-signal Silicon Photo-Multiplier (SiPM) readout ASIC called MuTRiG (Muon Timing Resolver including Gigabit-link). The MuTRiG has 32 channels and is fabricated in UMC 180 nm CMOS technology. The output signals of the tile SiPMs are connected via a flexible printed circuit board to a MuTRiG chip. In [53] the MuTRiG is explained in detail.

Everything described until here, the different detectors, their electronics, the power distribution and the data acquisition systems are located inside the magnet. Everything in the magnet is packed densely, all parts produce heat, therefore a **cooling** concept for the whole experiment is needed. Except for the pixel tracker a water cooling system is used. The pixel detector has a special cooling system with gaseous helium to keep it at a temperature below 70 °C. The helium cooling system is a trade-off between cooling potential and radiation length [49] [42].

4.1.3 MuPix – sensor development for Mu3e

As explained in the previous section, one of the main detector systems for the Mu3e experiment is the pixel tracker. All parts of the tracking detector (central part and recurl stations) will be built from highly specialised custom smart sensor ASICs: the MuPix. The development of such a specialised smart sensor in different generations for Mu3e is one core part of this thesis.

There are several requirements for a sensor used in a tracking detector. It must be thin to reduce multiple scattering, for Mu3e the sensors have to be thinned down to 50 µm. In addition, time resolution in the nanosecond range is needed, less than 20 ns in the case of Mu3e. Spatial resolution is also important and leads to the desired pixel sizes, e.g. 80 µm × 80 µm in the case of Mu3e. For high efficiency, a 100 % fill factor of the pixel matrix is required.

These requirements can be fully met by HV-MAPS. These monolithic devices can be thinned to 50 µm. The pixel sizes for Mu3e can be realised. The HV-MAPS offer a time resolution of a few nanoseconds due to the fast charge collection by drift. Complex readout architectures and special data formats can be realised with the CMOS logic available in HV-CMOS processes. The sensitive sensor area can be maximised by a fully customised layout design.

Another advantage is that HV-MAPS are cost-effective, the cost per square meter is in the order of 85 000 € [6]. This includes wafers, production costs and post-processing. With multiple beam tests and detailed characterisations of the MuPix chips, it was confirmed that they meet the Mu3e requirements [54] [55] [38] [56]. Integration tests of the tracking detector with MuPix10 chips are currently under way at PSI.

The MuPix will be the first HV-CMOS chip produced in a standard industrial technology that will form – without any other ASICs – a tracking detector in a particle physics experiment. The successful use of the MuPix by Mu3e will be an important step for the HV-CMOS community.

4.2 Application for particle therapy

4.2.1 Particle therapy at HIT

he Robert Koch Institute predicts more than 500,000 new cancer diagnoses [57] for the year 2020. There are three main methods of cancer and tumour treatment, each with its own challenges: resection, chemotherapy and radiotherapy. For all of them, the biggest challenge is to treat the tumour and preserve the healthy tissue as much as possible. Often the tumour is close to or even inside organs, which makes treatment challenging.

The most advanced form of radiotherapy is currently particle therapy using protons or heavier ions [58].

About 40 % of all patients can be successfully treated by surgery and/or radiotherapy. However, in 18 % of all patients, local or regional treatment methods fail even though the primary tumour is still localised. In Europe, this corresponds to about 280 000 deaths per

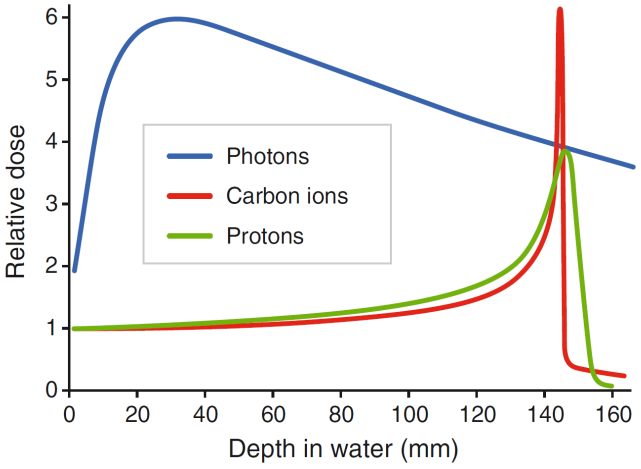

Figure 4.5: The depth-dose curves of ions differ significantly from that for photons. The ion curves have a plateau phase at low dose, followed by a sharp Bragg peak. (From [58])

year. From clinical studies in the USA and Japan, it can be estimated that 25 000 to 30 000 of these previously incurable patients can benefit from particle therapy. These are mainly tumours of the brain and skull base, sarcomas and prostate carcinomas [59].

In Europe more than 20 clinical facilities offer particle therapy. Particle therapy with ions creates new opportunities for advanced cancer treatment [58]. It enables better protection of healthy tissue due to the favourable depth-dose distribution [60]. The dose of photons decreases exponentially with the penetration depth. High energy ions deposit initially little energy but provide an increasing energy deposition with depth until reaching a sharp maximum (Bragg peak), see figure 4.5. This property enables tumour treatments with less damage to the tissue in front and behind the tumour, which is important for optic nerve or brain tumours [61] [62] [58].

The Heidelberg Ion Therapy center (HIT) is a university hospital-based therapy center that offers particle therapy since November 2009. Every year about 1 300 patients can be treated. The center has three treatment rooms, two with a horizontal beam line and one with a carbon ion gantry. The patients are placed on robotic treatment tables for maximal variability and flexibility for patient positioning [63]. The gantry allows a 360 degrees rotation of the beam, a photo of the gantry is shown in figure 4.6.

4.2.2 Beam monitoring at HIT

Successful particle therapy treatment requires precise planning and monitoring of the particle beam. For this, the beam characteristics such as dose, energy and position must be controlled and verified based on the monitoring information.

Figure 4.6: The upper picture shows the gantry and the lower one the gantry treatment room. The gantry at HIT enables a 360° rotation of the beam line. It is made of 670 tonnes of steel, has a length of 25 m and a diameter of 13 m. (From [64] [65])

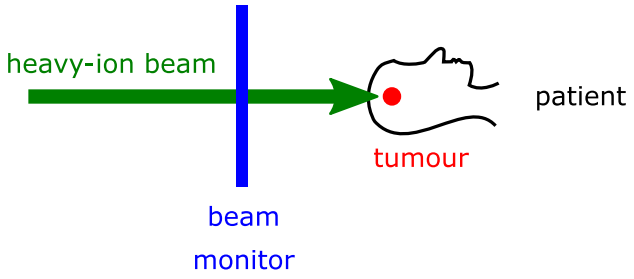

Figure 4.7: The beam monitor is placed inside the beam in front of the patient. The beam monitor at HIT has a size of 25 cm × 25 cm and measures the beam position in x- and y-direction. (Modified from [6])

In current medical ion beams, monitoring is realised with a stack of wire chambers [66] in front of the patient, see figure 4.7. At least two chambers are needed to determine the position in x- and y-direction. In addition, there is a limited spatial resolution due to the wire spacing and the irradiation becomes inhomogeneous due to the alternating pattern of wire and non-wire.

New solutions for beam monitoring are needed to improve the shortcomings of wire chambers. For HIT, new approaches based on HV-CMOS detectors are being investigated. The chip developed within the scope of this thesis makes a significant contribution towards this goal.

4.2.3 HitPix – sensor development for HIT

A radiation monitor for the beam used for particle therapy is placed directly in the beam, for example, at the HIT. The expected dose for one year at the HIT is about $1.3 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$. The expected particle rates go up 20 GHz on $0.5\,\mathrm{cm^2}$ [6]. The sensor material must be homogeneous. The final monitor will cover an area of 25 cm × 25 cm and consist of several 2 cm × 2 cm chips.

HV-MAPS was chosen as the concept for this beam monitoring system because HV-MAPS can meet the requirements. The material of the HV-MAPS chips is homogeneous because it is a monolithic ASIC. Hybrid sensors would not be an option because they are inhomogeneous due to the bonds between the two ASICs. In addition, silicon components are not affected by high magnetic fields. This is important for the HIT project because the sensor is to be operated in magnetic fields.

For the final large system, the sensitive areas should be uniformly distributed over the matrix. Since the relative rate is measured, the pixel matrix does not need a 100 % full

factor, but the insensitive periphery must be as small as possible. The dominant effect due to radiation damage in HV-CMOS sensors is damage in NMOS transistors leading to leakage current. This can be reduced with an enclosed NMOS transistor layout. For the high rates, hit counters with CMOS logic can be implemented and also fast projections of the beam can be realised with the CMOS circuits available in HV-CMOS processes.

The HitPix has a size of $4.9\,\mathrm{mm} \times 5.2\,\mathrm{mm}$. The pixel matrix contains 24 columns with 24 pixels each with a pixel size of $200\,\mu\mathrm{m} \times 200\,\mu\mathrm{m}$.

An adapter PCB to measure the HitPix with the existing GECCO setup [6] [67] has been designed, the firmware and software adapted and measurements in the lab and at testbeam were performed.

In June 2021 an enlarged version of the HitPix was designed as the last project of this work. The HitPix2 is similar to the original HitPix, but with a size of $0.98\,\mathrm{cm} \times 1.01\,\mathrm{cm}$. The differences between the two chips are discussed in section 10.1.

Part II

Development of integrated circuits for HV-MAP sensors

Chapter 5

Amplifier

In this chapter, the charge sensitive PMOS amplifier used in MuPix and in HitPix is presented. First the voltage sensitive amplifier is explained and then the charge sensitive amplifier is presented based on the results.

5.1 Voltage sensitive amplifier

First, the voltage-sensitive amplifier is explained. It was not used in this work, but by explaining it, the charge-sensitive amplifier necessary for HV-MAPS can be more clearly explained.

The voltage sensitive amplifier amplifies an input voltage signal. An amplifier has, in simplified terms, an input, an output and two supply voltages: one voltage connected to ground (GND) and one to a positive supply voltage (VDD), see figure 5.1.

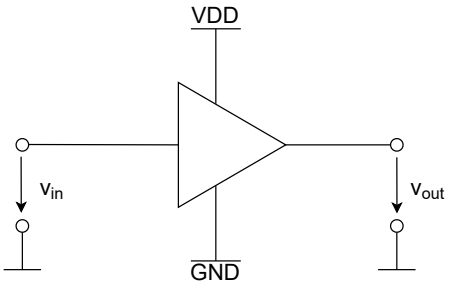

Figure 5.1: Amplifier with input, output and supply voltages.

A typical characteristics of the output voltage as function of the input voltage has different regions as shown in figure 5.2. For input voltages close to the supply voltages the amplification is small, the amplifier is in saturation. The region in-between with a high amplification is called active region.

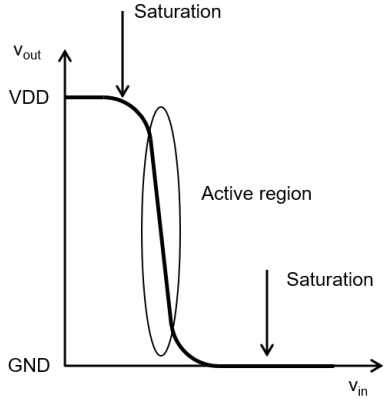

Figure 5.2: Output voltage as a function of input voltage for a typical amplifier. At input voltages near the supply voltages *VDD* and *GND* the amplifier is in saturation. In between is the active range with a high amplification.

The simplest amplifier with just one NMOS transistor is shown in figure 5.3. The resistor R_{load} has the purposes to guarantee an optimal DC operating point and to convert the output current into a voltage. For a high amplification the transistor has to be in saturation.

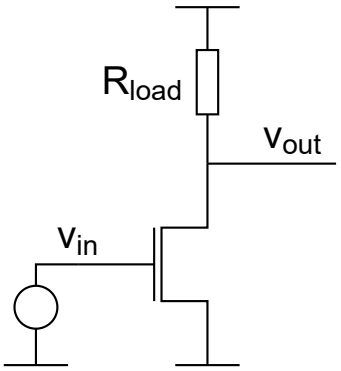

Figure 5.3: Simple amplifier with one NMOS transistor and one resistor R_{load}. The input voltage V_{in} is provided by a voltage source.

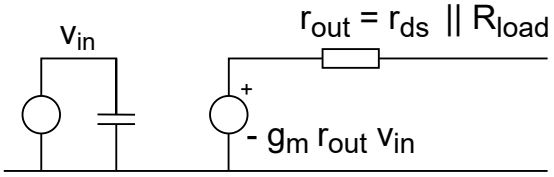

Figure 5.4: Small signal model of the amplifier with the drain-source resistance r_{DS} and the gain g_m.

From the small signal circuit shown in figure 5.4 the amplification can be described as:

$$A = \frac{v_{out}}{v_{in}} = -g_m(r_{ds} \parallel R_{load}) \tag{5.1}$$

To achieve a linear behaviour of the amplifier, a feedback circuit is added. The feedback circuit consists of a resistive feedback (R_{fb}) for DC signals to stabilise the operating point and of a capacitive feedback (C_{fb}) for a higher amplification of AC signals. The amplifier with resistive and capacitive feedback is shown in figure 5.5.

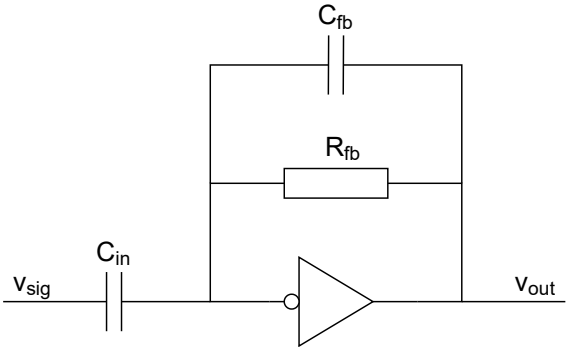

Figure 5.5: Amplifier with resistive (R_{fb}) and capacitive feedback (C_{fb}). C_{in} is the input capacitance and v_{sig} the input signal.

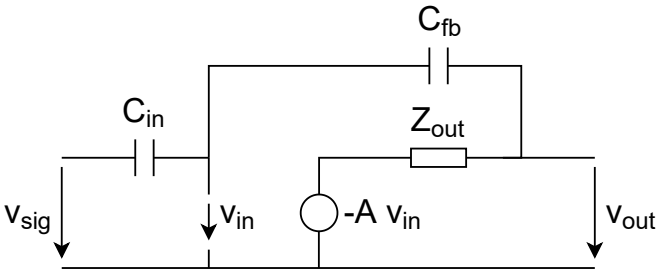

Figure 5.6: Small signal circuit of the amplifier with feedback, the resistor R_{fb} is negligible and not drawn.

In order to calculate the gain, the AC analysis (small signal analysis) is done with the assumption that R_{fb} is large so the impedance of the capacitor C_{fb} is for the considered frequencies, much smaller than R_{fb}. Therefore R_{fb} is negligible because the circuit is parallel. The simplified small signal circuit is shown in figure 5.6. The feedback amplification is described using the Mason's gain formula:

$$A_{fb} = \frac{A_{in} A_{ol}}{1 - \beta A_{ol}} \tag{5.2}$$

where A_{fb} is the gain with feedback, A_{in} is the amplification from signal source of the amplifier input, A_{ol} is the open loop gain from amplifier input of the main output and β the feedback from the main output to the amplifier input.

In the case $Z_{out} = 0$ the amplification with feedback is:

$$A_{fb} = \frac{-A_{ol} \frac{C_{in}}{C_{fb}+C_{in}}}{1 + A_{ol} \frac{C_{fb}}{C_{fb}+C_{in}}} \tag{5.3}$$

With the common assumption of $|\beta A_{ol}| \gg 1$ one gets

$$A_{fb} = -\frac{A_{in} A_{ol}}{\beta A_{ol}} = -\frac{C_{in}}{C_{fb}} \tag{5.4}$$

A large βA signifies that the voltage at the input of the amplifier is constant: The node in front of the amplifier is called virtual ground.

5.2 Charge sensitive amplifier

The expected signals in a tracking detector, like the one for Mu3e, are small. Therefore, a high SNR is important to distinguish between signals and noise. The most important

noise contributions in the amplifier are thermal and 1/f noise (see section 2.3). The 1/f noise is lower in the chosen HV-CMOS process for PMOS amplifiers compared to an NMOS amplifier, as simulations and measurements have shown [68]. The lower noise of the PMOS amplifier results in better SNR, hence a PMOS amplifier was chosen for MuPix10 and HitPix.

However, the PMOS amplifier has the disadvantage that it requires two supply voltages additional to ground, VDDA (1.8V) and VSSA (1.0V). The system in which the sensors are later used must provide these two voltages for each chip. This leads to a more complex routing on, for example, High Density Interconnect (HDI) circuits, with which the chips are connected to the outside.

The input signal of the charge sensitive amplifier is a current pulse with a charge Q. The output signal is proportional to the charge and independent of the pulse shape. The circuit structure is the same as for the voltage sensitive amplifier in figure 5.5. The current source representing the input current can be replaced by a corresponding voltage source: if the voltage source generates a voltage with amplitude $\frac{Q}{C_i}$, the corresponding current source generates an impulse with the charge Q. A current pulse with charge Q causes an output signal with amplitude $\frac{Q}{C_f}$.

A large C_{in} leads to an increasing feedback amplification but the amplifier gets slower. If one increases C_f, the amplification with feedback decreases and the amplifier gets faster until the minimum time constant $\frac{C_{out}}{g_m}$.

The pixel amplifier electronics contains a charge sensitive PMOS amplifier, its feedback circuit, the output driver and a test signal generator. The charge sensitive amplifier for the two chips is identical.

The circuit of the amplifier is shown in figure 5.7. In blue the bias part with the connection to the floating n-well (*nwell sensor*). The *nwell sensor* is capacitively coupled to the *AmpIn* of the "core" part of the amplifier shown in green and the amplifier feedback circuit in orange. The green amplifier part consists of a folded cascode and a source follower. The feedback circuit is connected to the *AmpIn* and the *AmpOut*. The *AmpOut* is AC-coupled to the output of the charge sensitive amplifier *AmpOutAC*.

For testing purposes, each pixel has a test injection circuit (figure 5.9), externally a signal charge can be injected into the pixel that then will be detected by the sensor.

The input transistor of the charge sensitive amplifier is chosen to a be PMOS transistor.The gate of the input transistor of the amplifier is AC-coupled to the n-well. This AC-coupling is necessary because the input node of the amplifier has a different DC-voltage than the n-well bias potential. The needed coupling capacitor is realised with a PMOS transistor. Every p-diffusion is capacitively coupled to the deep n-well by its parasitic junction capacitance. Because the n-well is floating and connected to the amplifier these parasitic

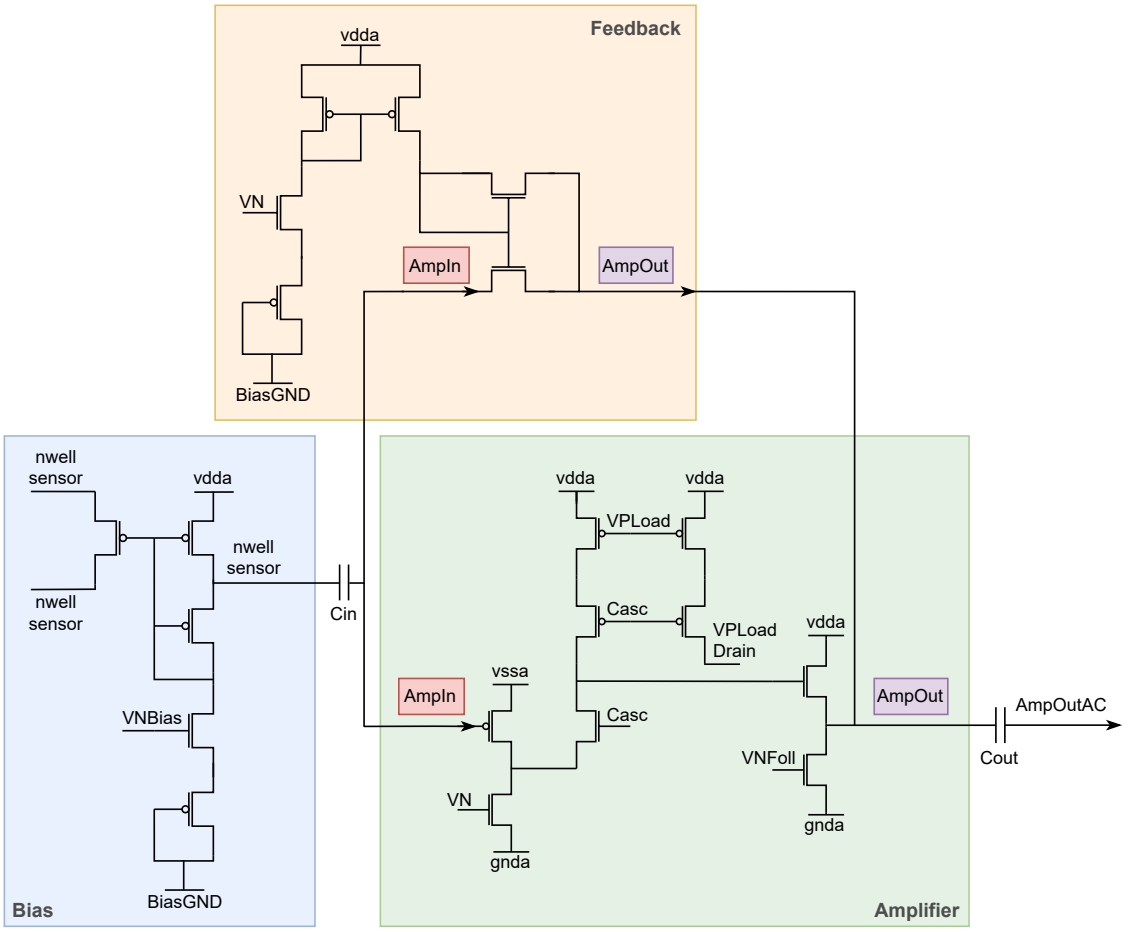

Figure 5.7: Charge sensitive amplifier as used for the MuPix10, the HitPix and the HitPixISO. The figure is separated in Bias (blue), Feedback (orange) and main Amplifier block (green).

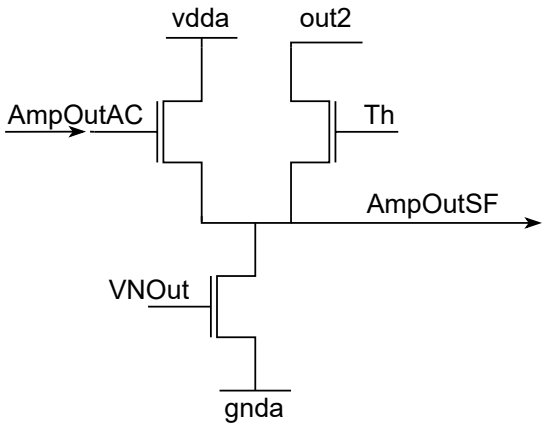

Figure 5.8: Signal driver realised as source follower for the MuPix. *AmpOutAC* is connected to the PMOS amplifier, *AmpOutSF* is connected to the signal transmission line.

capacitances are not just introducing capacitive loads, but can cause feedback. The parasitic capacitance between the n-well and the transistor connected to *VPLoad* is used as the capacitive feedback of the charge sensitive amplifier [36]. The parasitic feedback connects the output of the amplifier to the coupling capacitor C_{in} in front of the PMOS input transistor.

The feedback circuit (capacitive and resistive feedback) has several tasks: it ensures the stability of the amplifier and it shapes the amplifier output signal (steep rising and falling edge with a fast rise and fall time). The feedback circuit is biased by a current source connected to ground. A detailed description and derivation of the construction of the charge sensitive amplifier can be found in [36] [69] [70].

The amplifier output is AC-coupled to the line driver in case of the MuPix and to the comparator in case of the HitPix. The use of AC-coupling assures a well defined base line BL_{Pix}.

The amplifier output signal of the MuPix is connected to the driver, realised by a source follower. The output has nearly the same amplitude as the amplifier output signal. This voltage is transmitted to the readout buffer via a long line. In case of the HitPix the comparator is located in the pixel, like the amplifier circuit. Therefore no driver is needed.

The most significant contribution to the detector capacitance is the capacitance between the p-well and the deep n-well. In case of the MuPix, the shielding in the pixels is important to avoid capacitive coupling between the signal line and the pixel diode underneath. Two metal layers are used for shielding. The current consumption of the amplifier is programmable by on-chip digital-analogue converters (DACs).

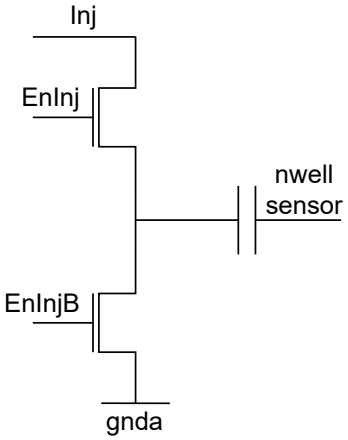

Figure 5.9: The used test signal circuit to allow lab measurements with test signals (injections). *Inj* sets the strength of the test signal.

5.3 Test signal generation

With the test signal generator, electrical tests without particle sources are possible, which allows for an easier start-up of new chips and an easier way for debugging in the laboratory. The test signal generator discharges a capacitor to inject a defined charge into the n-well. This injected charge is then collected by the n-well and amplified by the charge sensitive amplifier like the charge of an ionizing particle hitting this pixel. The test signal itself is produced in the chip periphery and from there distributed to all pixels. The amplitude of the test signal can be set by an 8 bit DAC. The injection can be individually activated for each pixel [36]. Figure 5.9 shows the test signal generation circuit of the MuPix and HitPix.

Chapter 6

Comparator

The comparator has two purposes. On the one hand to digitize the amplified analogue signal coming from the charge sensitive comparator and on the other to enable a time sensitive measurement. First, the design of the used comparator is shown. In 6.2 the different possibilities of comparator placement are discussed. Then, in 6.3 the timewalk problem is explained, followed by different methods for correcting the timewalk using two comparators.

6.1 Optimised comparator design

The comparator design is a standard PMOS comparator that has optimised transistor sizes. The comparators across the matrix should have a uniform behaviour. Thus, all pixels detect a hit under the same conditions. For this, the mismatch of the comparators must be small. This is achieved by optimising the transistor sizes. The mismatch is smaller if W and L of the transistors are larger, because then small deviations in the production do not matter so much. However, large transistors require more space. The optimisation should find the right compromise between space requirements and mismatch. This is done with Monte Carlo simulations, as explained in [71]. The measurements of the threshold distributions in section 9.2 and section 10.3 show that the mismatch of the comparators is acceptable.

The advantage of the PMOS comparator is that it uses only three NMOS transistors. NMOS transistors introduce leakage current after radiation damage, PMOS transistors are not affected (see section 2.4).

The amplifier output and the input of the comparator are AC-coupled. The AC coupling has several purposes: it assures threshold uniformity across the matrix, eliminates the influence of voltage drops, temperature and low frequency noise.

The comparator is shown in figure 6.1 can be fine tuned by adding a programmable offset via the *tune* input to the global threshold voltage *Th*. The tuning is necessary to provide an uniform low threshold over the entire chip. The amount of bit to allow this fine tuning of the threshold voltage is dependent on the implementation of the readout buffer. For MuPix10 3 bit for tuning the comparator are available. Furthermore, the MuPix comparator uses cascode circuits. The two *VP* voltages and the *casc* voltage are provided by the chip periphery and can be set by DAC values by the user. If the analogue signal at input *in* (signal from the amplifier) is above the threshold level, the output of the comparator is high.

The comparator of the HitPix has a slightly different implementation without the possibility of threshold tuning.

The purpose of the comparator and the meaning of the rising edge at the comparator output are the same for both chips: the rising edge at the output is recorded as a particle hit, in the following "hit". A rising edge occurs if the threshold voltage is crossed. Then the time information of the hit is stored in the readout buffer. The comparator input and output are shown in figure 6.2. The output signal length of the comparator is proportional to the amplitude of the analogue signal.

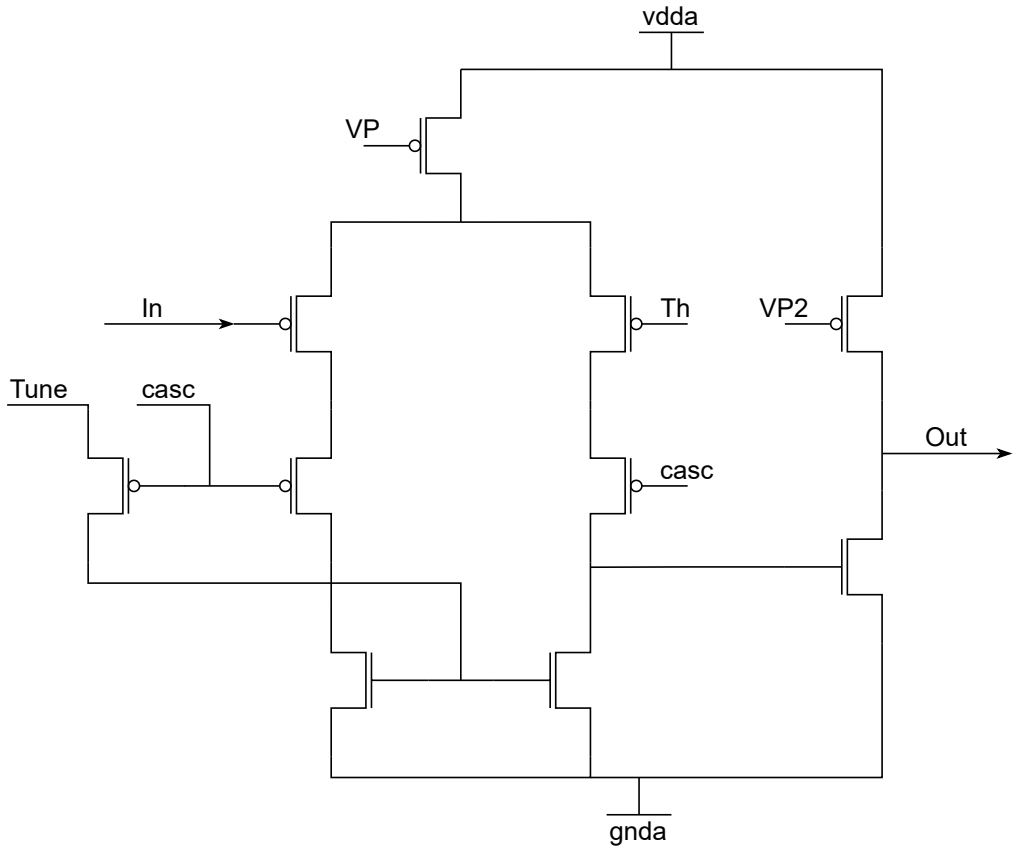

Figure 6.1: The comparator used for the MuPix is a PMOS comparator. With Th the threshold voltage is set and with $Tune$ the comparator can be tuned.

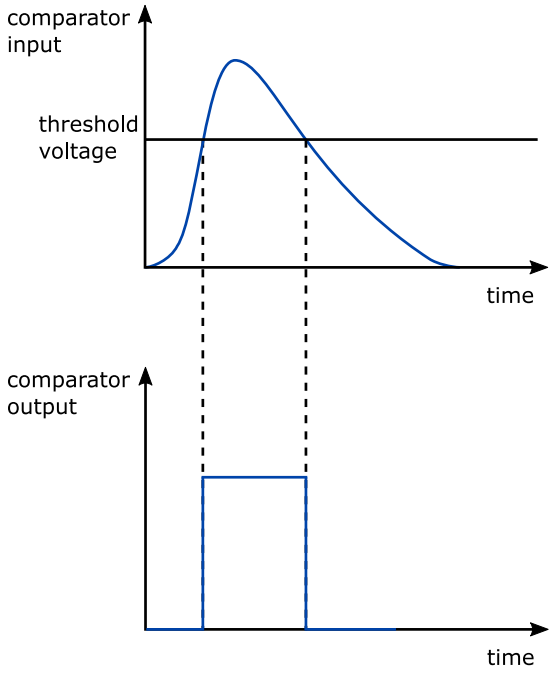

Figure 6.2: The upper diagram shows the comparator input (the output of the amplifier) in blue together with the threshold voltage. The lower one shows the comparator output in blue.

6.2 Comparator placement

There are different possibilities where the comparator is placed. The comparator position defines the signal transmission: either an analogue or a quasi-digital signal is transmitted from the pixel to the periphery. The well in which the comparator is placed must be connected to a fixed voltage. The n-well in the sensor is floating, so it can collect charge, but is therefore sensitive to crosstalk from p+ regions to the n-well. If the comparator is placed in the pixel, it must be in the same p-well as the amplifier, as this is connected to ground, or spatially separated from the sensitive part.

This leads to four different solutions for comparator placement:

First, the comparator can be placed in the periphery and the analogue signal is transmitted from the pixel to the comparator in the readout buffer via a long line. This is the safest solution for the sensor in the pixel, as the comparator is physically separated from the sensitive pixel. Here one achieves the full fill factor of the pixel matrix, as there are no insensitive areas in the pixel. However, there is also a disadvantage: the transmitted signal is sensitive to crosstalk. A signal generates crosstalk on the neighbouring lines and their comparators can detect a hit without a signal coming from the amplifier. For the MuPix, this solution was chosen at an early design phase. The crosstalk and possible corrections with special routing are investigated in [72].

The second option is to place the comparator in the pixel in wells that are not floating and are physically separated from the sensitive part of the pixel. This has the disadvantage that the pixel does not have a 100 % fill factor because the area where the comparator is placed is not sensitive. This implementation is chosen for the HitPix.

The third possibility is to place the comparator inside the pixel and at the same time achieve full fill factor. For this, the comparator is placed in the p-well like the amplifier, this well is connected to ground. The advantage is that a quasi-digital signal is transmitted from the pixel to the periphery and crosstalk between the lines no longer causes problems. The disadvantage is that only NMOS transistors can be used for the comparator, as it has to be completely housed in the p-well. A comparator built with NMOS transistors only has a lower voltage gain, which has to be compensated by using two or three stages. This has the disadvantage of greater power consumption and a larger layout. This option with a two-stage comparator was chosen for the AtlasPix3 in [36]. With the results from this chip, this solution would be chosen for the MuPix today.

The fourth option is to use an additional well. This allows a CMOS comparator to be placed in the pixel in the p-well and in an isolated n-well. The n-well is isolated by the additional deep p-well. This method is called ISO in the thesis and is used for the HitPixISO. The advantages are that it allows a 100 % fill factor and a CMOS comparator can be used. The CMOS comparator has a small layout and low current consumption. The disadvantage, however, is that the manufacturing process must implement the additional deep p-well.

In the MuPix design concept the first solution is chosen: the comparator is placed outside of the pixel in the periphery in the readout buffer. This implies that the analogue signal coming from the amplifier in the pixel has to be transmitted via a long connection line to the readout buffer. The matrix structure of the MuPix is divided into two matrices, one large pixel matrix and beneath a readout buffer matrix. Within the scope of this work the readout buffer has been developed and the readout buffer matrix organized. In the case of the MuPix10, due to layout design reasons, the readout buffer matrix has been designed as a double matrix. So one readout buffer cell is as wide as two pixels. In case of the MuPix10 the threshold voltage of the comparator can be fine tuned with three tune bit. The output of the comparator is connected inside the readout buffer.

Considering the HitPix: the comparator is placed in the pixel, see figure 10.2 in chapter 10.1.1. No long transmission line is needed because the amplifier and the comparator are placed side by side. The comparator of the HitPix is not tuneable. The layout of the comparator is designed to be radiation hard. The output of the comparator in the HitPix is connected to a counter. The HitPix is explained in detail in chapter 10.

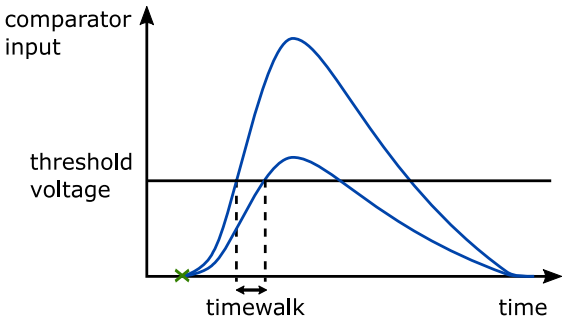

Figure 6.3: For two different signal amplitudes starting at the same time (marked by a green cross), the timestamps marking the threshold crossing point are not identical, their difference is called timewalk.

6.3 Timewalk problem

In case of time critical applications like the Mu3e experiment, different input signal amplitudes lead to a timing problem, the timewalk. For different input signal heights the output signals of the comparator are generated at different times. Figure 6.3 shows how this happens: For a higher input signal, the high amplitude also leads to a steeper signal rise causing an earlier threshold crossing point in comparison to an input signal with a lower amplitude [4]. In case of particle pixel detectors, the different amplitudes are caused by the fluctuation of the energy deposition when a particle passes through the pixel. Note that the rise time constant is independent of the deposited energy, but the time until the threshold crossing is dependent on the amplitude. The distribution of the energy deposition and the signal heights are Landau distributed for thin layers [22] [6].

But with this amplitude changes the timing of the signal is shifting and leading to a broader timing distribution [17]. For a theoretically infinite high signal, the threshold crossing point is identical to the signal start point because the rise is infinitely steep. In case the maximal amplitude is equal to the threshold voltage and an ideal comparator, the time of the start of the comparator output signal is equal to the peaking time. Figure 6.4 shows these two special cases. In this case the comparator is slow. The comparator threshold should be at least two times smaller than the minimum amplitude.

The timewalk was simulated for the MuPix. The results of the simulation for the MuPix10 are shown in figure 6.5. The input signal of 250 nA corresponds to 1500 electrons, 500 nA to 3000 electrons, 750 nA to 4500 electrons and the input signal of 1500 nA to 9000 electrons. For comparison, a ^{55}Fe source produces 1639 electron-hole pairs. The simulation shows that the timewalk becomes much larger for small signals and smaller for larger signals, also the differences of the timewalk between high signals become smaller.

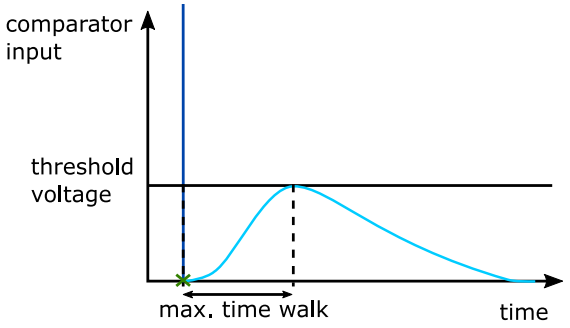

Figure 6.4: Extremal cases for an infinitely high signal (dark blue) and for a signal with an amplitude equal to the threshold voltage (light blue).

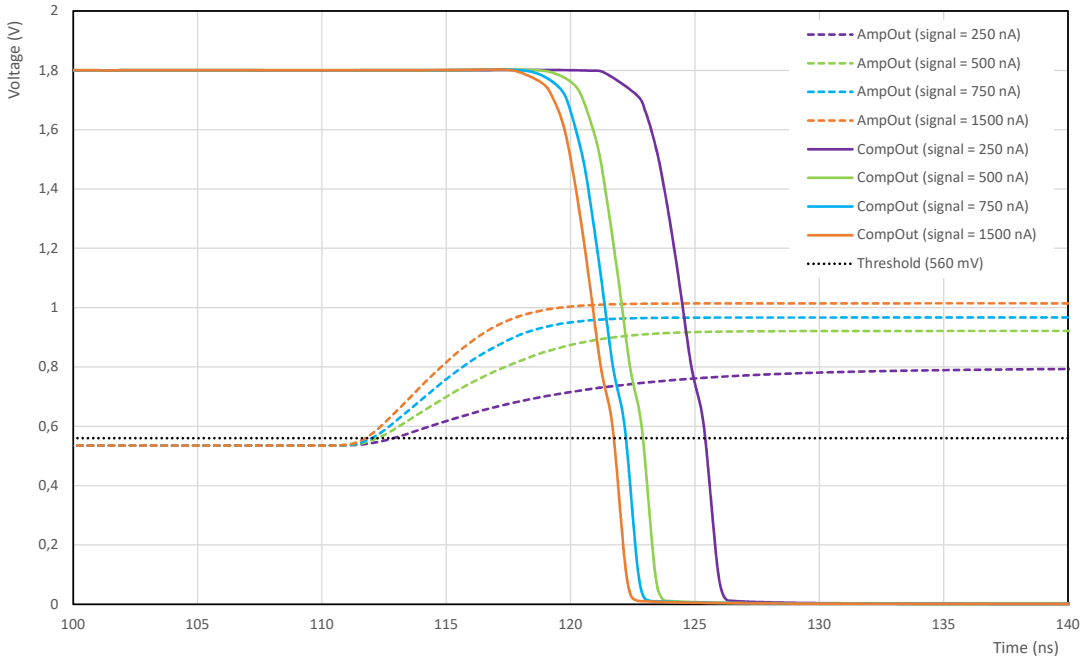

Figure 6.5: Simulation of the timewalk for MuPix10. The input signal of 250 nA corresponds to 1500 electrons, 500 nA to 3000 electrons, 750 nA to 4500 electrons and the input signal of 1500 nA to 9000 electrons.

6.4 Timewalk correction methods

There are different approaches to correct the timewalk explained in the section before. They can be divided into two groups: the ones that correct the timewalk after the measurement off-chip, like the time over threshold method (ToT), and the ones that try to reduce the timewalk on-chip. The MuPix8, 9 and 10 use both, the ToT method and a special on chip correction method to reduce the timewalk measurement error - the two threshold method.

First the standard ToT method will be explained and afterwards the two threshold approach.

6.4.1 Time over threshold method

For the ToT method two timestamps are needed. One timestamp marks the time when the amplified signal crosses the threshold of the comparator and the comparator output is set to high. The second timestamp marks the point in time when the signal drops again, below the threshold value of the comparator. This way, a time-over-threshold (ToT) is measured by calculating, off-chip, the difference of the two timestamps and getting the time span of the signal above the threshold, the ToT value. The larger the ToT the larger was the signal and its amplitude, see figure 6.6. So a large ToT marks a large amplitude and because of this, the timewalk of this signal is larger. With ToT the timewalk can be calculated and corrected off-chip.

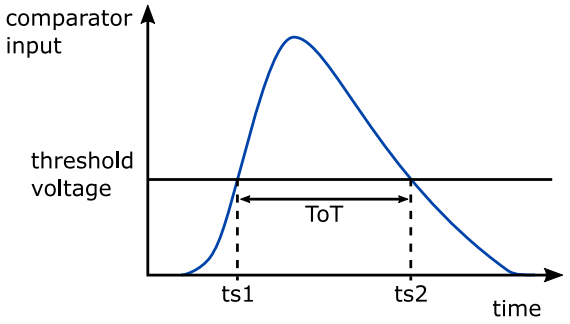

Figure 6.6: The time over threshold (ToT) is the difference between the first timestamp (ts1) and the second timestamp (ts2) marking the threshold crossing points of the signal.

6.4.2 Two threshold method

In [71] [73] the two threshold method was first implemented for the MuPix chips. The two threshold method on MuPix9 was identical to the one on the predecessor. The method was

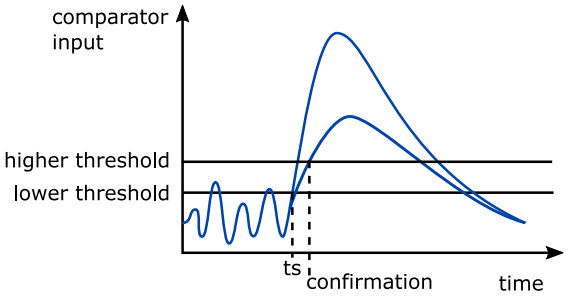

Figure 6.7: Two comparators with two different thresholds are used for on-chip timewalk reduction. The one with the lower threshold sets the timestamp value and the one with the higher threshold confirms the signals as a hit and the saved timestamp is read out. The timestamp is the same for both shown signals, the confirmation is marked for the signal with lower amplitude.

further developed for the MuPix10. In section 9.1.2 the integration of the two threshold method in the readout buffer is described. In this section the idea and realisation of the two threshold method, used for the MuPix10, will be explained.

The timewalk is caused by the variation of the amplitude height. The idea of the two threshold method is that instead of one comparator two comparators are used for each pixel. The simulated power consumption of both comparators is 2.52 µW ($2 \times 700\,\text{nA} \times 1.8\,\text{V}$) [74]. The total power consumption of the two comparators is small and the Mu3e requirements regarding power consumption are still fulfilled.

The two comparators are needed to realize two different threshold voltages for the input signal, a lower and a higher one. The lower threshold is set in the upper noise range. This threshold does not need to separate signals from noise in all cases, in comparison to the ToT with one comparator this threshold is set to a lower voltage. When the input signal crosses the threshold voltage the timestamp is saved. Because this timestamp is closer to the signal start, due to the lower threshold, the timewalk is smaller. But now one cannot be sure if this is really a signal and not just noise due to the smaller threshold. Therefore the second comparator is needed with a higher threshold. If the signal also crosses this threshold, it is a signal and not just noise, so this comparator confirms the signal and the timestamp of the lower threshold crossing point is read out. With both comparators one can be sure to separate noise from signals (higher threshold) and omit the timewalk effect (lower threshold, earlier timestamp). Figure 6.7 shows the explained two threshold approach.

With the two comparators it is also possible to do an on-chip timewalk reduction and to make an improved ToT measurement for an off-chip correction. With this combined reduction and correction approach the timewalk problem can be reduced improving the time resolution. ToT is formed, therefore, out of the first timestamp from the comparator with the lower threshold. The second needed timestamp for the ToT is the point in time

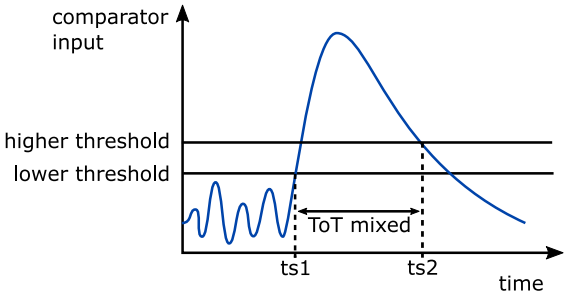

Figure 6.8: To build the mixed ToT the first timestamp is provided by the comparator with the lower threshold and the second timestamp is set by the comparator with the higher threshold.

when the signal falls again under the threshold voltage. Out of simulations one can see that the signal's falling edge is, compared to the rising edge, flat and noisy. The second timestamp for the ToT is defined by the comparator with the higher threshold. Because the ToT is now built out of the timestamps from two different comparators with different thresholds, this ToT is called mixed ToT. Figure 6.8 shows the signal, the two threshold and the mixed ToT time span.

Chapter 7

Radiation hard library

For the HitPix, a new intern radiation hard library optimised for minimum leakage current after radiation has been developed within this thesis. This library contains the most frequently used standard cells in a design with enclosed NMOS transistors (also known as gated-enclosed, edgeless or annular transistor) and additional guard rings.

7.1 Radiation hard elements with enclosed NMOS transistors

In beam monitoring, the sensors are placed inside the beam, so they are often exposed to a much higher dose than in a particle tracking detector such as Mu3e. Despite the high dose, the chips must remain functional. The expected dose for one year at HIT is approximately $1.3 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$.

This leads to the decision to develop a radiation hard library in this work for the HIT project and other projects that require a special radiation hard design. The radiation hard library is designed to minimise leakage current. For the 180 nm HV CMOS process used, the most relevant radiation damage is NMOS transistors causing leakage current (see section 10.3.2). These can be reduced by replacing all NMOS transistors with enclosed NMOS transistors with guard rings. The threshold shift is negligible for transistors in 180 nm processes, additionally this is a library for digital circuits. Therefore, the focus on leakage current minimisation is sufficient.

Higher leakage currents are critical as they lead to higher noise and power consumption. The measurements in section 10.3.3 show that the leakage current is higher after irradiation. This is to be expected, the chip is optimised for minimum leakage current, but not all circuits use the radiation hard library. Even if only elements of the library would be used, the effect of leakage current increase cannot be completely eliminated. The chips are functional without cooling in the beam at the HIT, see section 10.3.3. The observed leakage current is therefore acceptable and the use of the new library is reasonable.

The library was designed from scratch in the work described in this thesis.

For making the new cells easy to reuse and to guarantee an easy and fast full-custom layout design, all cells have a fixed height and a length that is always a multiple of a fixed value. The basic metric that was found to be suitable during the development process is 0.6 µm. An optimal height for an easy connection of the cells was found to be $12 \cdot 0.6\,\mu\mathrm{m} = 7.2\,\mu\mathrm{m}$. The basic cell dimensions then are $0.6\,\mu\mathrm{m} \times 7.2\,\mu\mathrm{m}$. Figure 7.1 shows the basic cell size and, as an example, an element of three basic cells to clarify the multiplication of the dimensions.

7.2 Library elements

The following cells were developed and most of them were used for the HitPix in the pixel, the row control or in the bias block.

- Inverter
- Gated Inverter (inverter with additional select and not-select input)

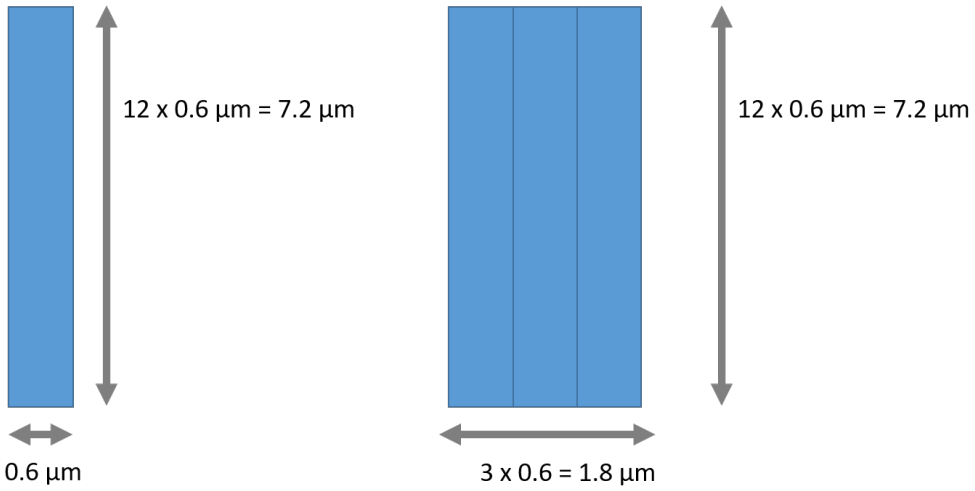

Figure 7.1: The base size of the new standard radiation hard library cells is 0.6 µm × 7.2 µm and can be seen on the left. On the right, the scheme and dimensions of an element consisting of 3 bases.

- 2×1 multiplexer
- Nor gate
- Nand gate with two, four and five inputs
- D-flip-flop
- D-flip-flop with reset
- D-flip-flop simple (D-flip-flop with only one output: QB)
- Scan-flip-flop
- Counter basic cell (explained in section 8)
- 8 bit Counter (explained in section8)
- Row control
- Shift register
- Bias current element

The following figures show the circuits and the corresponding layouts of the radiation hard library without the ones presented in section 8.

The difference between the gated inverter and the inverter is that the gated inverter has an additional select input. The gaetd inverter is necessary to built several digital circuits like flip-flops and multiplexers. The simple version of this cell has a select and a not-select

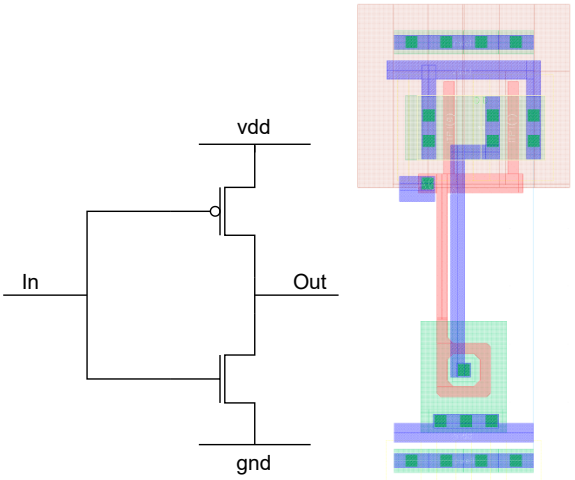

Figure 7.2: Circuit and layout of the radiation hard inverter.

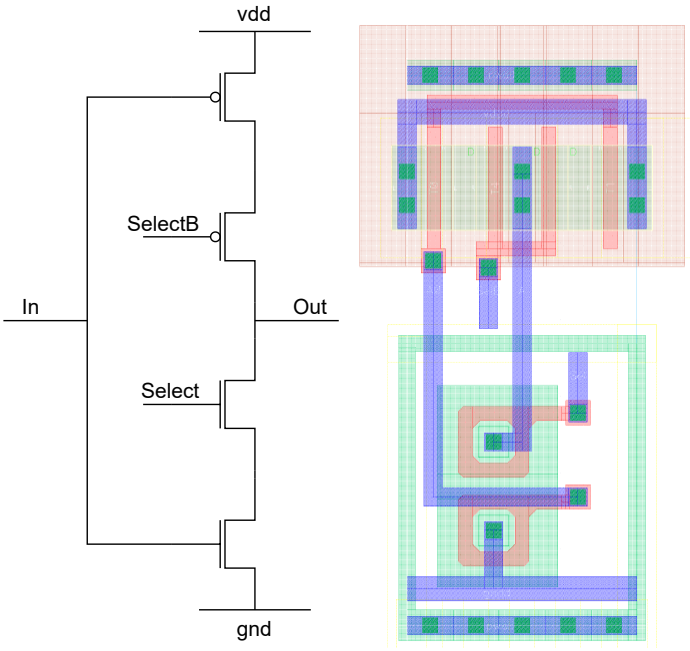

Figure 7.3: Circuit and layout of the radiation hard gated inverter in the simple version.

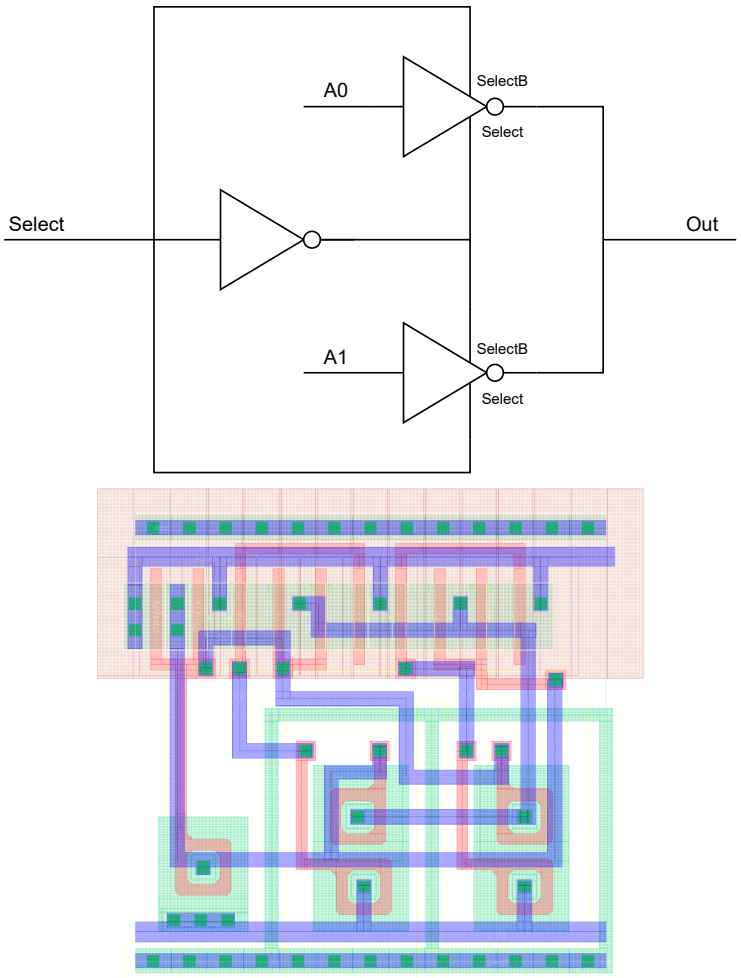

Figure 7.4: Circuit and layout of the 2×1 radiation hard multiplexer.

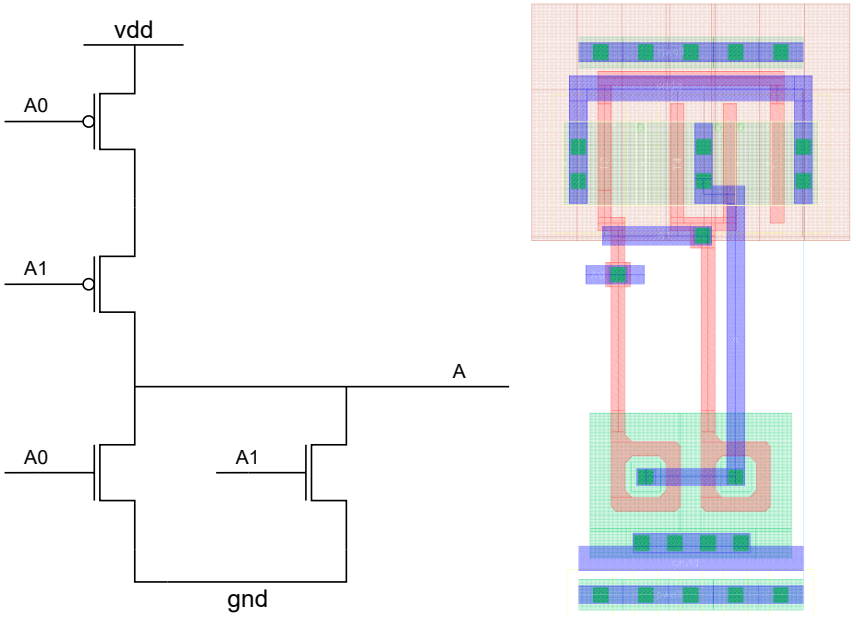

Figure 7.5: Circuit and layout of the radiation hard *nor*.

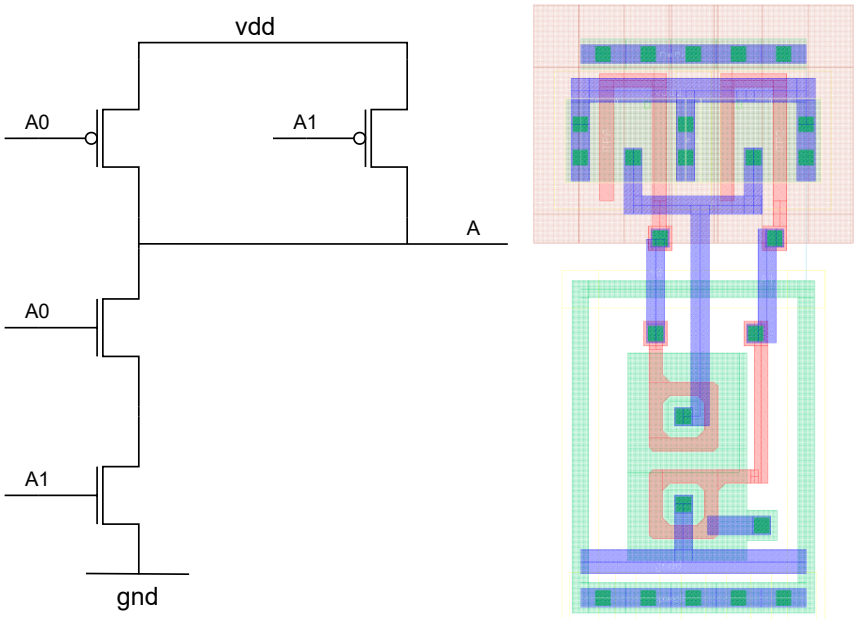

Figure 7.6: Circuit and layout of the radiation hard *nand*.

input (figure 7.3). The D-flip-flop simple is like the D-flip-flop but with just one output, the QB output.

Figure 7.17 shows the radiation hard bias block. This block is used in a non radiation hard variant for several chips from the ADL group building a basic element of the chip peripheries. The bias block generates and provides all needed internal voltages and currents. The radiation hard bias block has the exact same size as the ADL standard block to make it easily replaceable. However, due to the larger NMOS transistors, it does not offer all functions such as triple redundancy compared to the standard version.

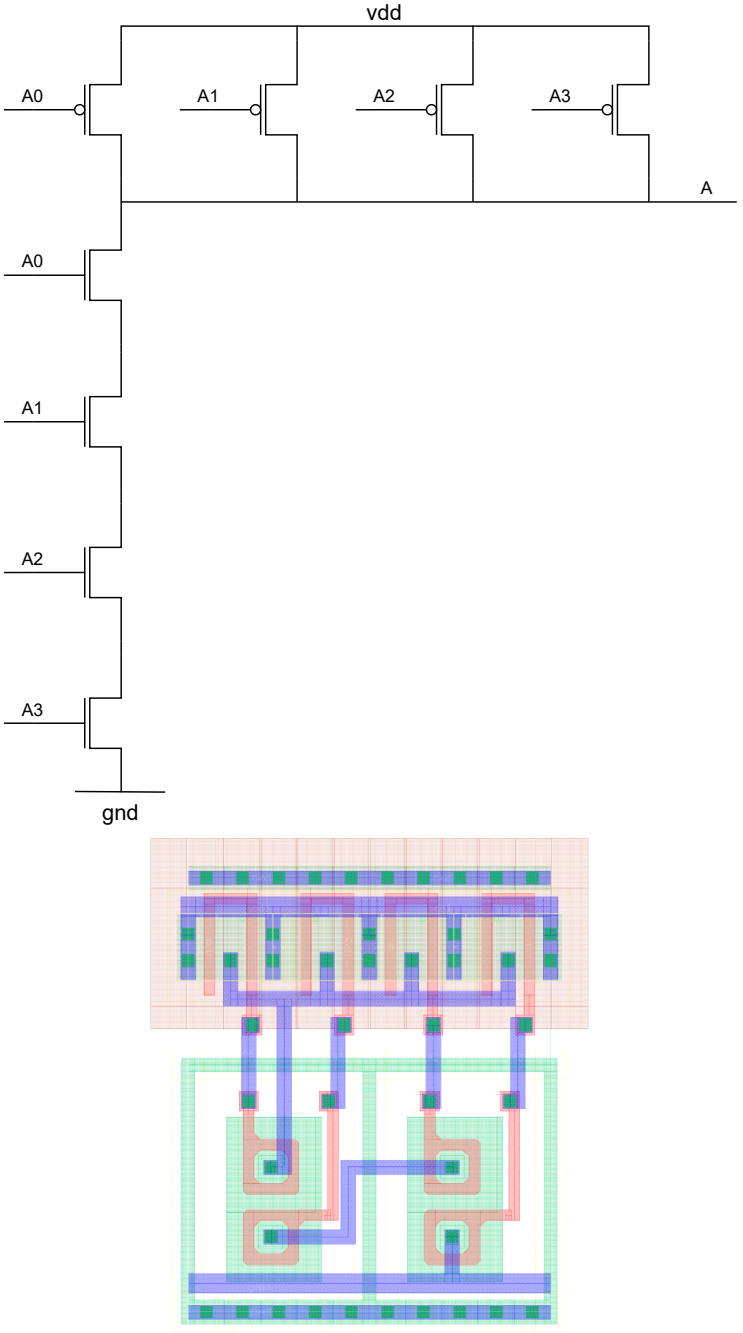

Figure 7.7: Circuit and layout of the radiation hard *nand* with four inputs.

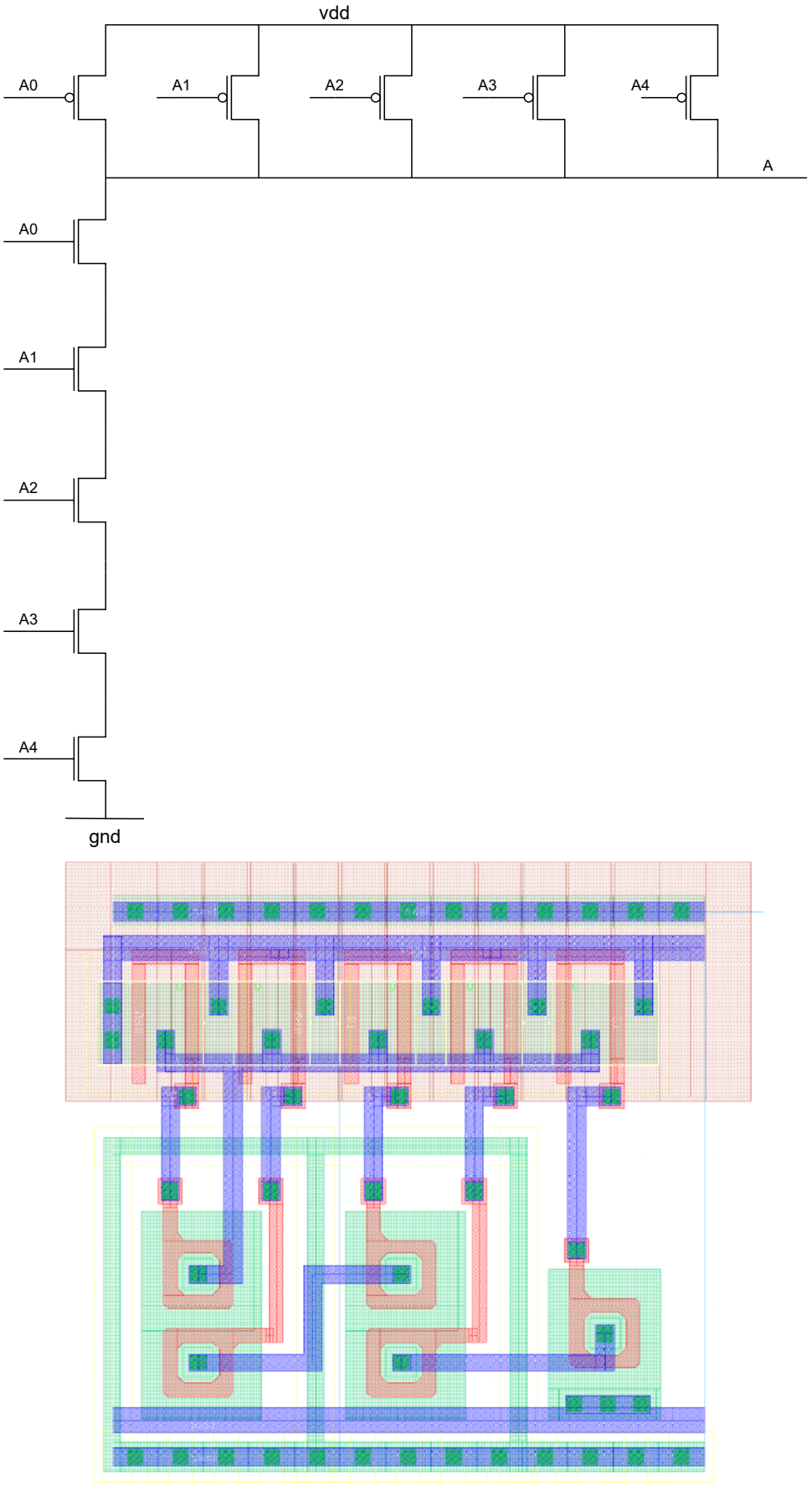

Figure 7.8: Circuit and layout of the radiation hard *nand* with five inputs.

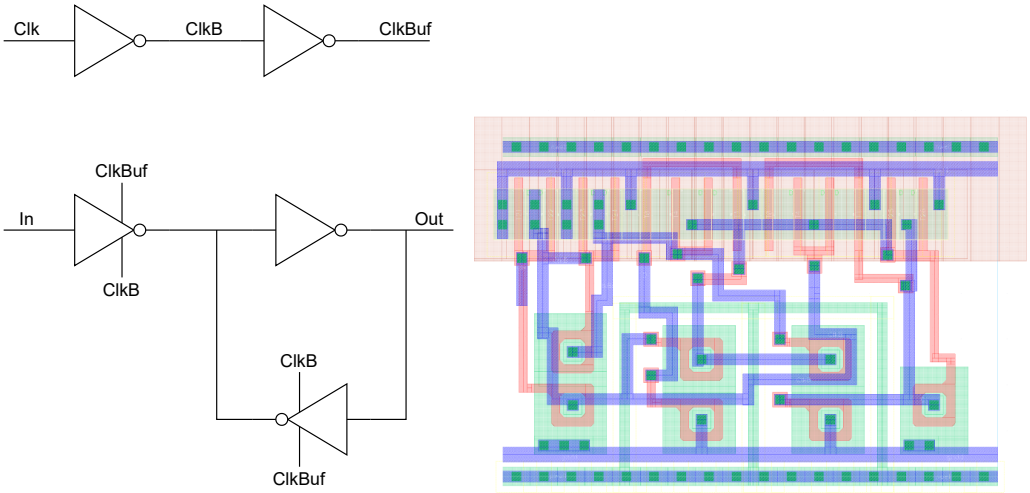

Figure 7.9: Circuit and layout of the radiation hard latch.

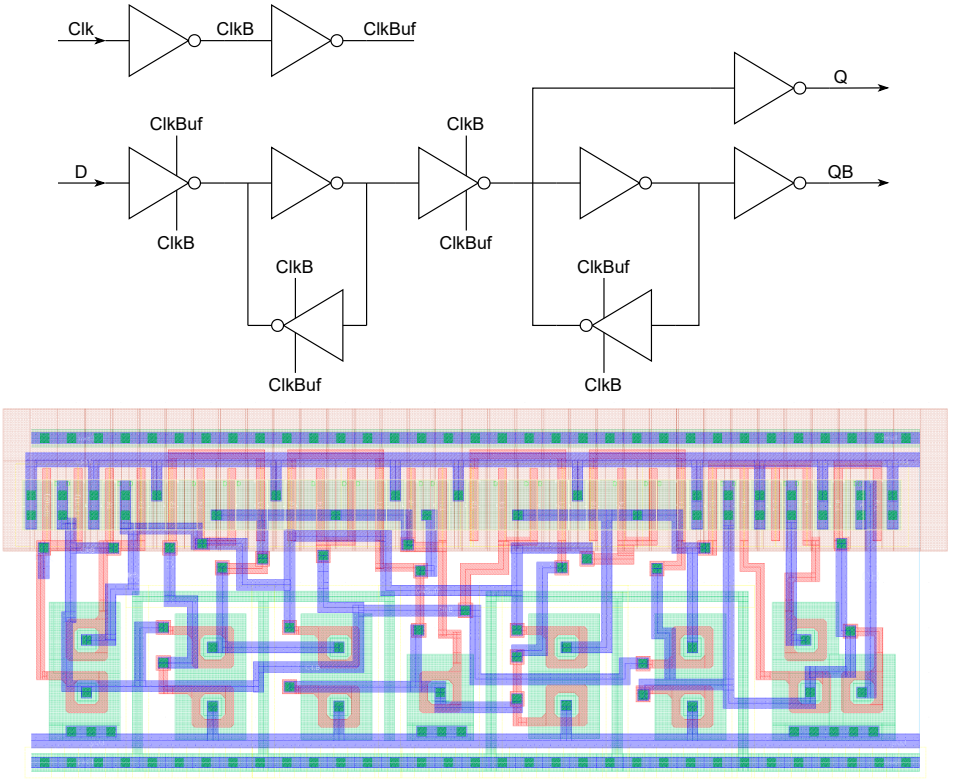

Figure 7.10: Circuit and layout of the radiation hard D-flip-flop.

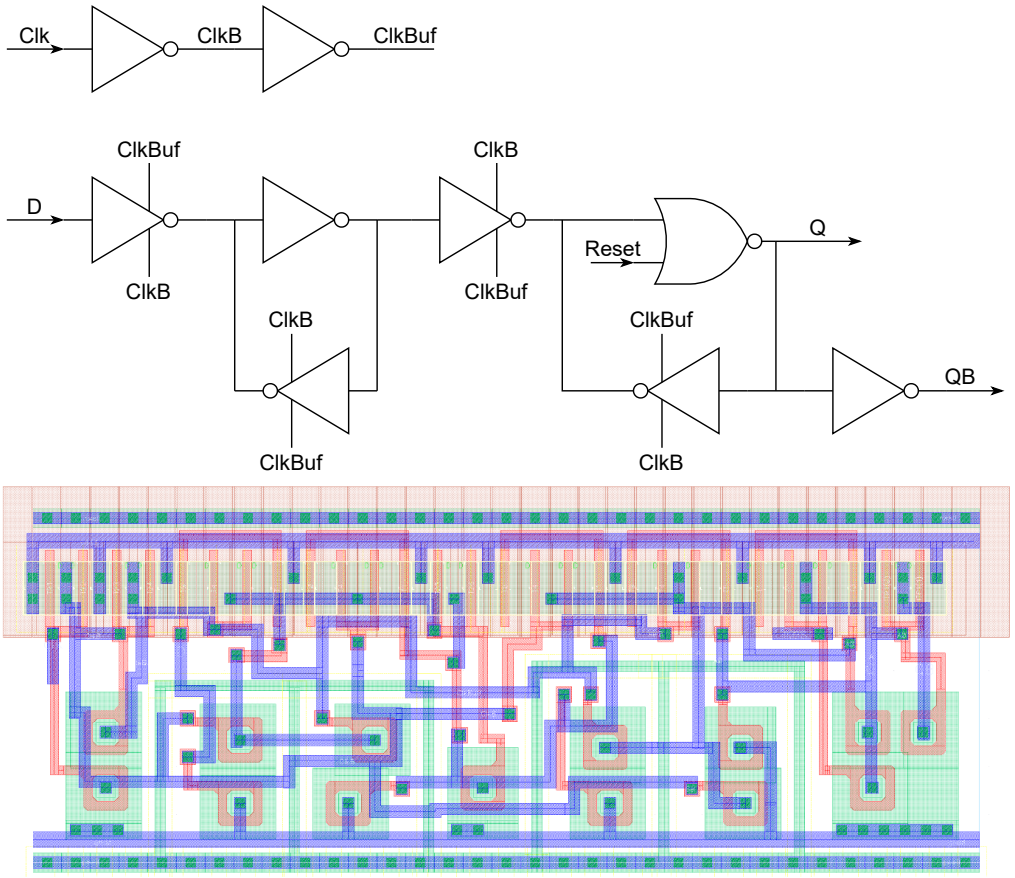

Figure 7.11: Circuit and layout of the radiation hard D-flip-flop with additional reset.

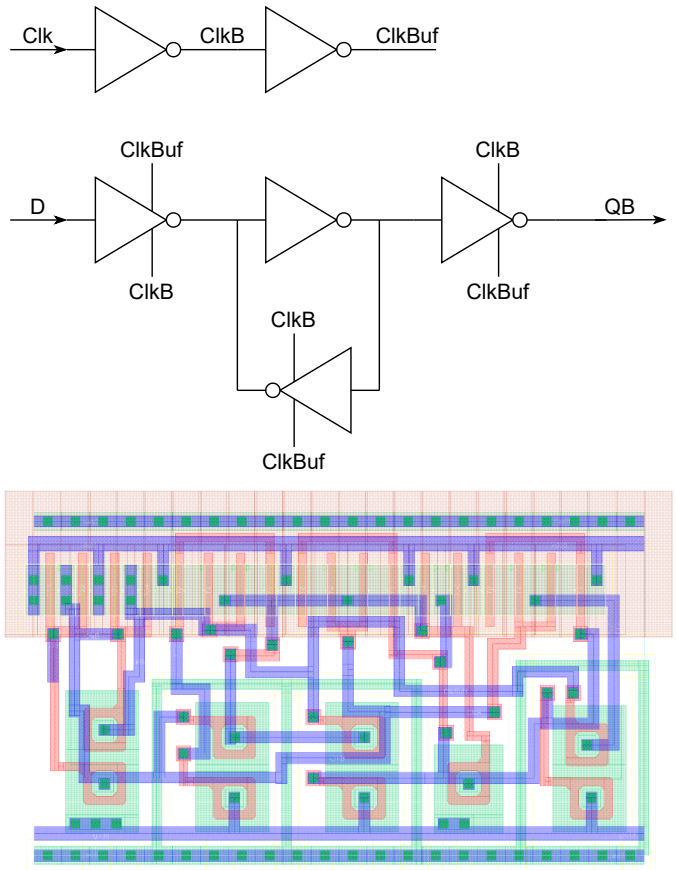

Figure 7.12: Circuit and layout of the radiation hard D-flip-flop in the simple version.

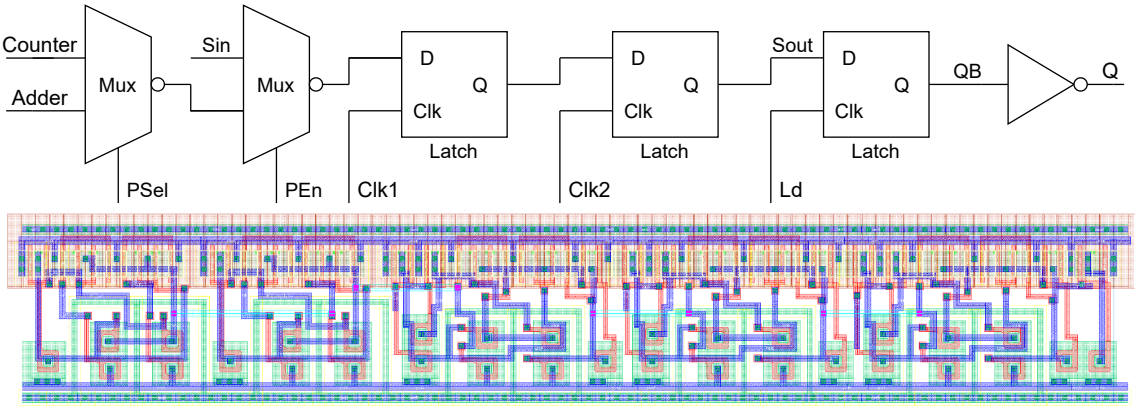

Figure 7.13: Circuit and layout of the radiation hard scan-flip-flop.

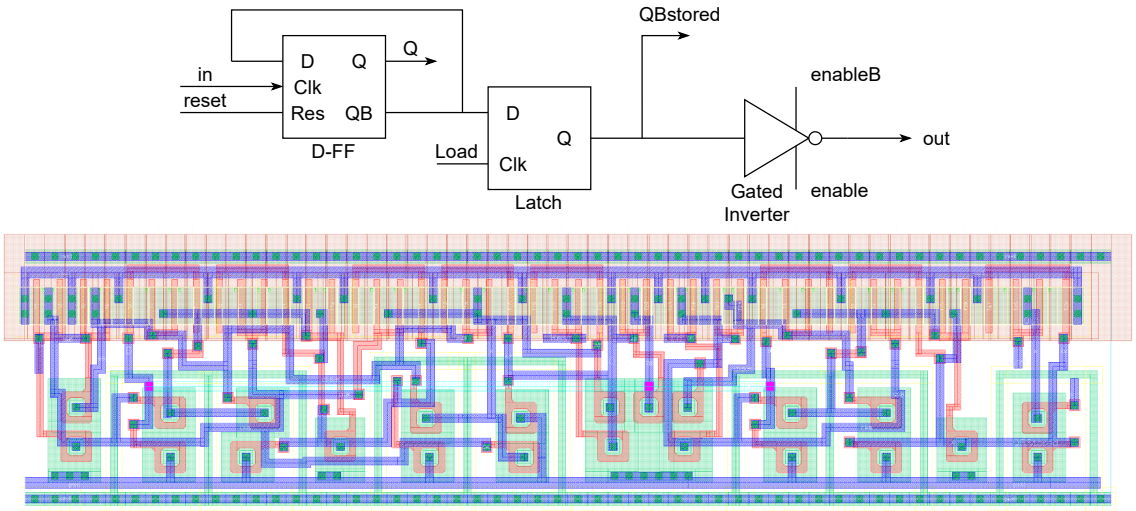

Figure 7.14: Circuit and layout of the basis counter cell.

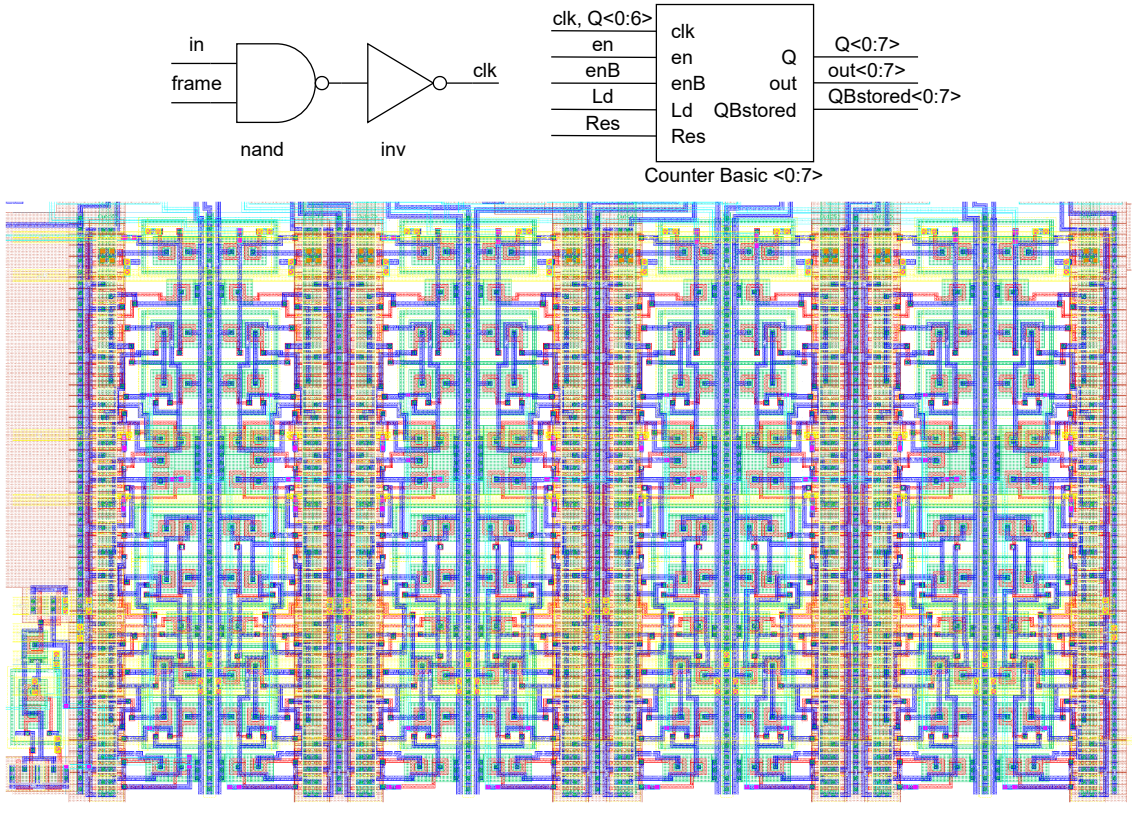

Figure 7.15: Circuit and layout of the radiation hard 8 bit counter.

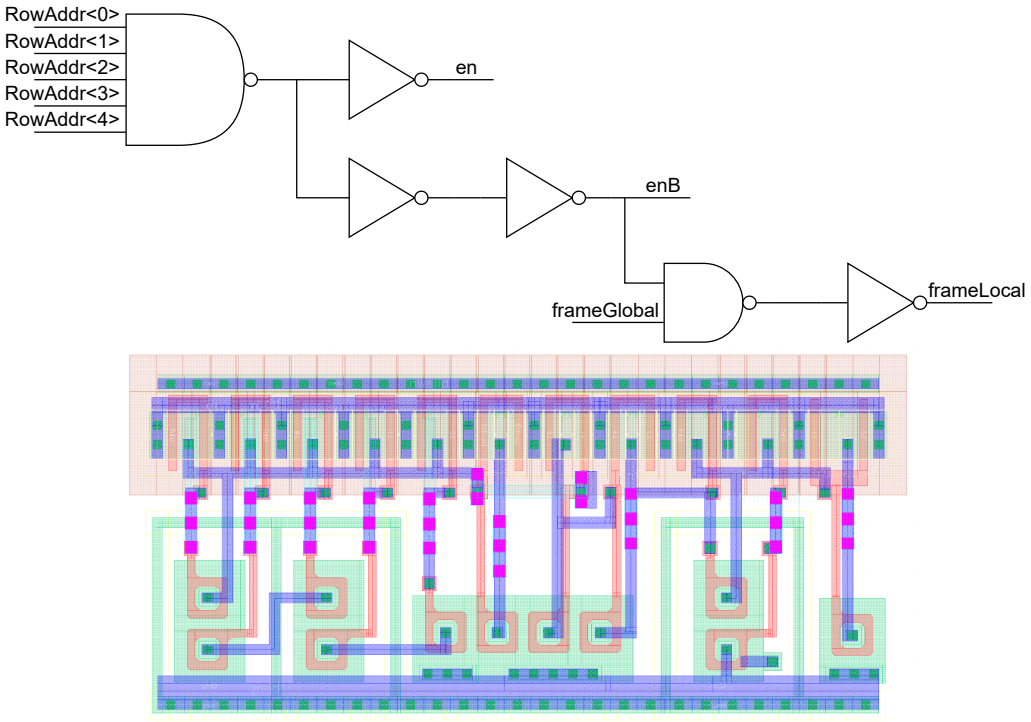

Figure 7.16: Circuit and layout of the radiation hard row control.

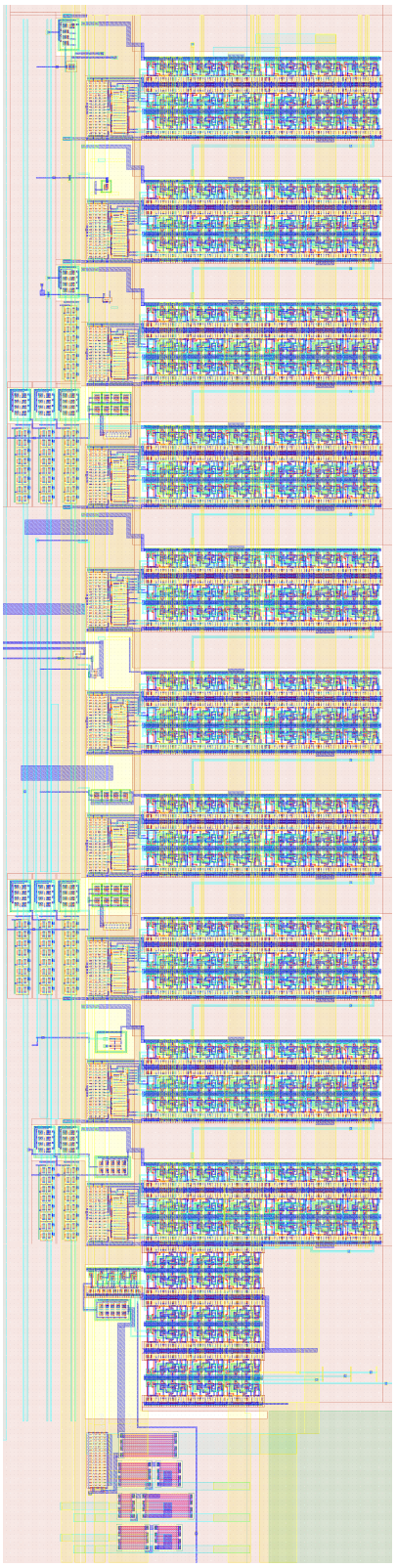

Figure 7.17: Layout of the radiation hard bias current element.

Chapter 8

Counter and adder

For the hit counting chip (HitPix) a radiation hard counter was designed during this thesis. Together with an adder, the counter provides special functionalities for the HitPix. The radiation hard design uses the new radiation hard library developed for this work (see chapter 7).

8.1 Radiation hard 8 bit in-pixel counter

Rates are high in beam monitoring applications and no timestamp of individual hits is needed. Measuring the relative rate in a readout cycle is important. Therefore, the idea was to implement an in-pixel counter that counts how many times this pixel was hit. This counter is then read out. The size of the counter depends on the application and the available space in the pixel.

For the HIT application, an 8-bit counter (256 counting states) was chosen. The expected particle rates go up to 20 GHz on 0.5 cm^2 [6]. With a pixel size of 200 µm × 200 µm and assuming 100 % fill factor, this equals 16 particles per µsec per pixel. With an 8 bit counter, this means that counters overflow on average every 16 µsec. To account for rate fluctuations, this time has to be reduced to be used as the integration time according to the variance of the rate distribution. The required integration times and readout speed can be achieved with the GECCO system [6] [67]. Of course, more bits would be even better, but more bits need more space, which would lead to larger insensitive areas. Furthermore, the counter can be combined with an adder like in HitPix and the size of the adder depends on the counter size and the number of pixels per column. An 8 bit counter is a good compromise with acceptable space consumption. The measurements at HIT shown in section 10.3.3 have confirmed that a counter size of 8 is sufficient.

The counter is designed as a rad-hard design with the special library designed for leakage current minimisation. The radiation hard layout is larger than a standard design, but there is enough space for it.

In each pixel of the HitPix an 8 bit ripple counter is placed. Each time the amplified signal crosses the threshold voltage, *hit signal* is detected and the counter adds one to the current value. Thereby, it is possible to have high hit rates, because each signal is not read out individually, but the hits are counted in a given time and the sum of the hits in one pixel is read out.

Figure 8.1 shows a schematic of the basic counter element. This element is for 1 bit counting. Therefore, for an 8 bit counter, this element has to be used 8 times. The basic counter element consists of a radiation hard D-flip-flop with an additional reset input, a radiation hard latch and a gated inverter. The input at the top of the gated inverter is the *SelectB* input and the one at the bottom the *Select*. This convention will be used in the whole chapter.

The radiation hard D-flip-flop is built out of several inverters, gated inverters and a *nor* element. The inner structure of the used D-flip-flop with external reset is shown in figure 8.2. The latch used in the basic counter element is constructed with three inverters and two gated inverters, see figure 8.3. In figure 8.4 the circuit and the symbol with its in- and outputs is shown.

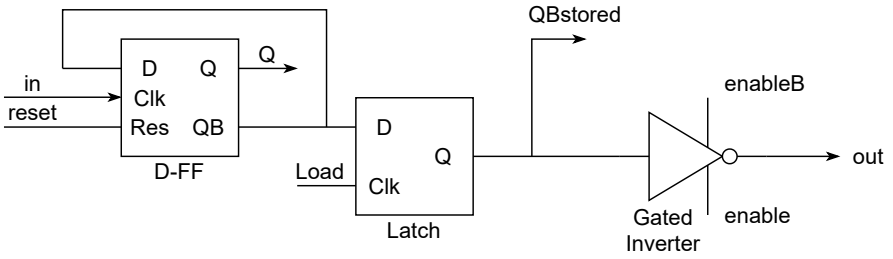

Figure 8.1: Basic element of the counter containing a D-flip-flop, a latch and a gated inverter.

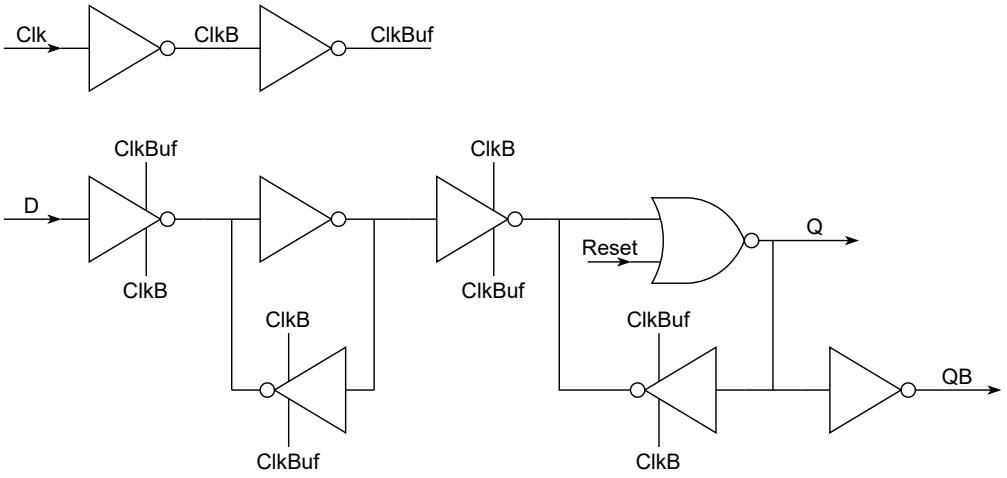

Figure 8.2: D-flip-flop with reset.

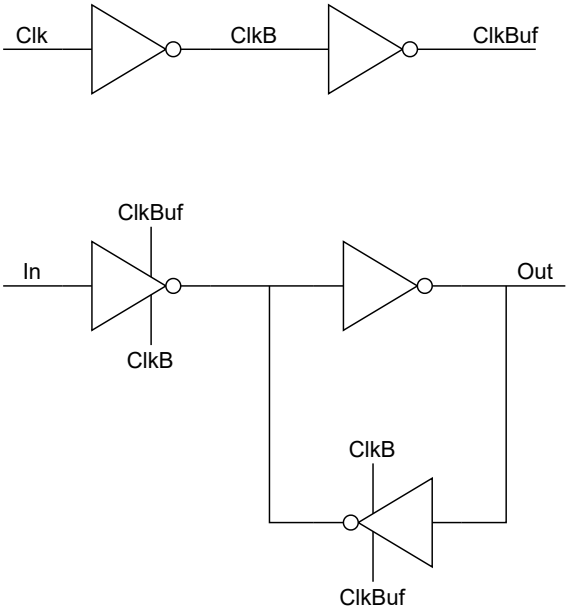

Figure 8.3: Latch.

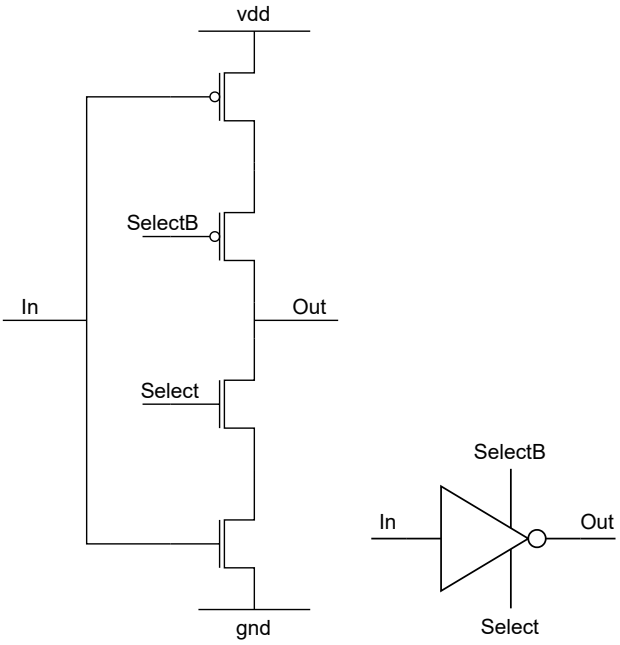

Figure 8.4: Gated inverter circuit and symbol.

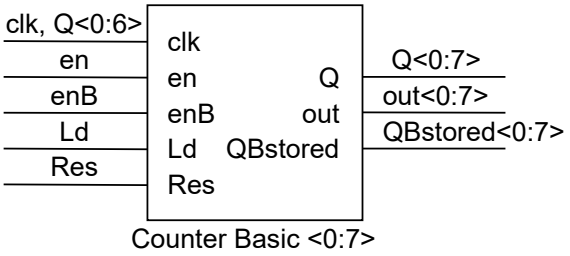

Figure 8.5: 8 bit counter realized out of 8 counter basic elements.

The 8 bit counter consists of 8 basic counter elements, see figure 8.5. Note the spelling *signal⟨0:7⟩*, due to the fact that the basic counter element is used 8 times, there are 8 in and outputs. The outputs *Q⟨0:7⟩* are connected to the *clk* input of the next basic element. With this connection, counting is realized. The *QBstored⟨0:7⟩* outputs are used for the adder, see section 8.2. The layout of the radiation hard counter can be seen in figure 8.6 and has a size of $62\,\mu m \times 33\,\mu m$. For the counter all NMOS transistors have an enclosed layout geometry and guard rings wherever necessary.

8.2 In-pixel 13 bit adder

As already mentioned in the part about the counter, the counter can be combined with an adder. For beam monitoring, the measurement of the beam profile by a projection is important. It must be possible to read this information fast. The projection of the beam can be done by adding the counter values of a column. The adders are distributed to the

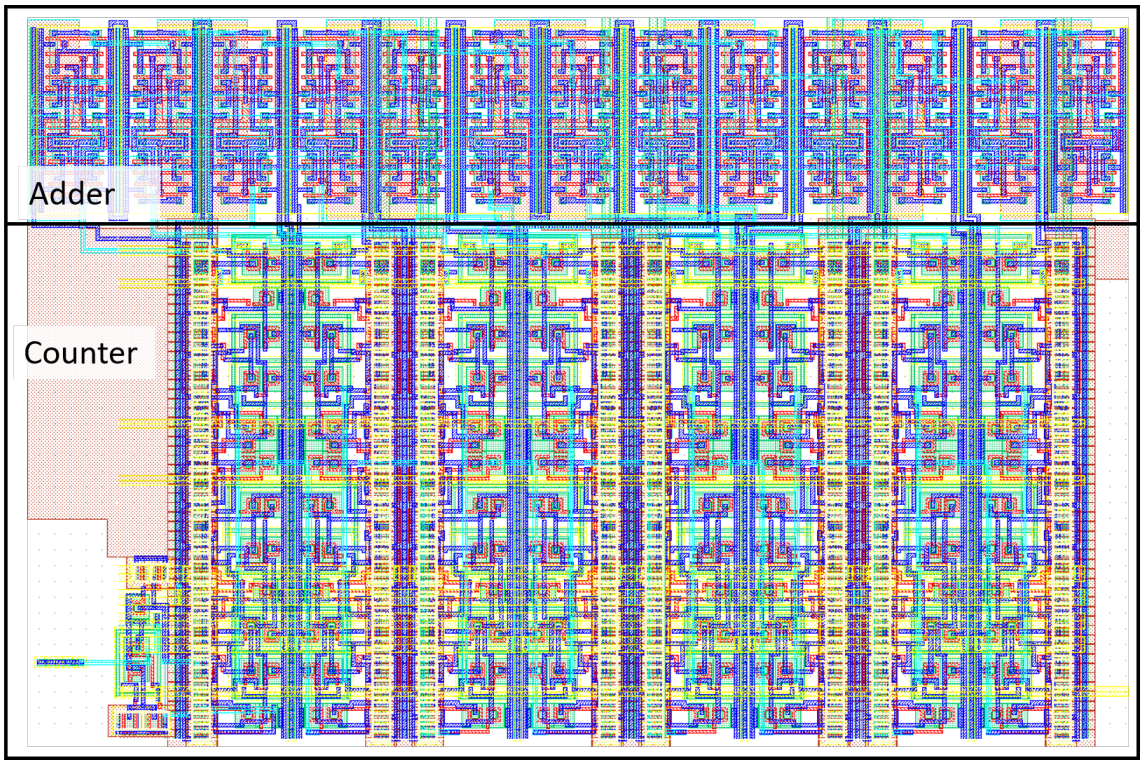

Figure 8.6: Layout of the 8 bit counter and the 13 bit adder. The size of the counter layout is 62 µm × 33 µm and of the adder 70 µm × 13 µm.

pixels so that each pixel adds its values to the sum from the pixel above and passes it on to the next. The values of the adders can be read out directly. Reading out the adders is fast because only one data set, namely the last result of the adders of each column, has to be read out. For the counter values of the matrix, one has to read out as many data sets as rows. In the example of HitPix, the adder needs one readout cycle and the counters need 24 cycles due to 24 rows.

The adder was not made in a radiation hard design. Since the radiation hard design is larger, there is always the trade-off between required area and leakage current due to the smaller non-radiation hard design. With the radiation hard design, the leakage current would be reduced, but the space required for the adder would be too large. Therefore, it was decided to reduce the leakage current by using the radiation hard library everywhere else except for the adder.

In figure 8.6 one can compare the size of the 8 bit counter with 184 PMOS and 184 NMOS transistors (62 µm × 33 µm = 2046 µm^2) with that of the 13 bit adder with 182 PMOS and 182 NMOS transistors (70 µm × 13 µm = 910 µm^2). The measurements of the irradiated HitPix on the HIT in the beam still show the beam spot and the chips are working. The leakage current generated due to the standard layout of the adder was tolerable.

For column addition the counter value of each pixel is added to the successor counter value. So the first counter in the first pixel will be added to the counter value of the second and

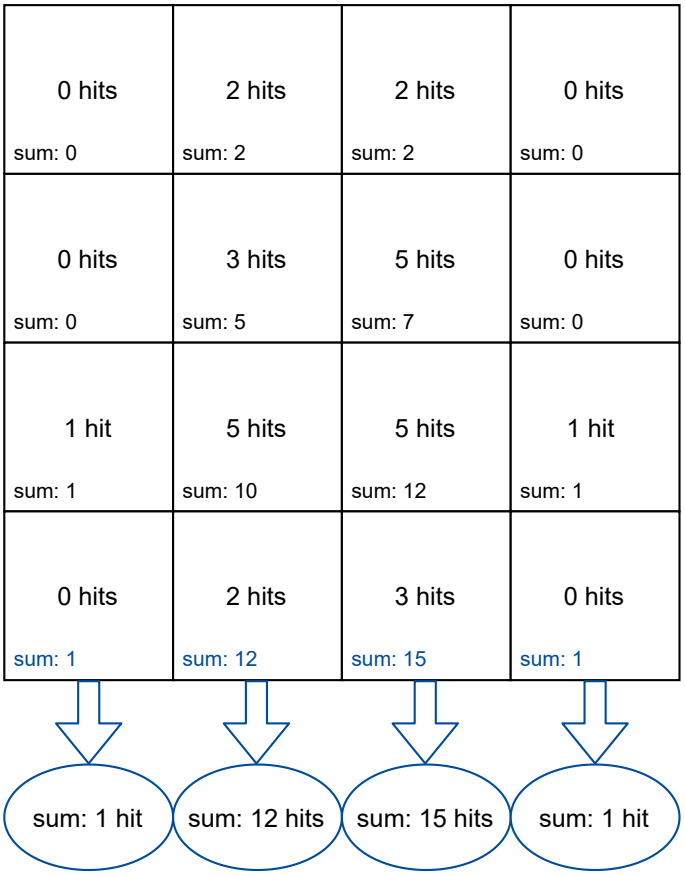

Figure 8.7: With the adder the hits in one column are added to a column sum. With the sum information a column projection is realised.

this sum will be added to the third pixel counter value and so on. Therefore, at the bottom of a column the sum of all counters in this column is obtained. The idea of the adder scheme is shown in figure 8.7. Each pixel needs, in the case of the HitPix, additional to the 8 bit counter a 13 bit adder to represent the maximum possible value of $24 * 256 = 6144$. For the in- and outputs of the adder see figure 8.8.

The adder allows for a different operation mode of the HitPix: reading out the column sums to create a projection instead of reading out all the counter value of the matrix. The measurement results of the HitPix using these two circuits are shown in chapter 10.3.

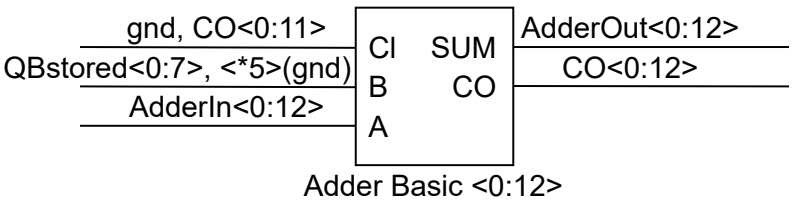

Figure 8.8: In- and outputs of the 13 bit adder.

Part III

Development of smart sensor chips and characterisation

Chapter 9

MuPix chip for particle detection in physics experiments

A series of HV-CMOS sensor chips called MuPix has been designed for the Mu3e experiment in the last years, leading to 9 generations of prototypes. Three generations were designed within this work: MuPix8, 9 and 10. They are all fabricated in a 180 nm HV-CMOS technology. The amplified signal from the amplifier inside the pixel is transmitted to the discriminators (comparators for hit digitizing) located in the readout buffer periphery. The MuPix uses a column drain readout architecture.

In the following, the architecture of the MuPix10 will be explained in detail, representing the latest version of MuPix. Afterwards, measurement results of the MuPix sensors will be presented.

The MuPix8 was designed and submitted in 2017 [73]. The MuPix8 is the first large size prototype with the dimensions of 8 mm × 19.5 mm. The pixel matrix consists of 128 columns and 200 rows of pixels with a size of 80 µm × 81 µm. One year later, in 2018, the MuPix9 (4.7 mm × 3.6 mm) was submitted. The first final size prototype – the MuPix10 – was submitted at the end of 2019. The MuPix10 is the last prototype before the final chip. The MuPix10 can already be used for Mu3e module building and integration tests[74]. Its size is 20.66 mm × 23.18 mm with a pixel matrix containing 256 columns and 250 rows, resulting in a sum of 64 000 pixels.

9.1 Architecture

In this section, the architecture and the column drain readout of the MuPix10 will be presented.

The MuPix10 has a size of 20.66 mm × 23.18 mm corresponding to the size intended for the production of the Mu3e pixel detector. The core element, the pixel matrix, consists of 64 000 pixels. The non-sensitive area (all parts of the chip except the pixel matrix) is comparatively small with only a height of 3.08 mm spanning the full width of the pixel matrix. The non-sensitive part is located at the bottom edge. Figure 9.1 shows the layout, in orange the pixel matrix and in blue the non-sensitive part including the readout buffers, end-of-column block (EoC) and the periphery. The fabrication was in a 180 nm HV-CMOS process.

In figure 9.2, the dimensions of the chip are shown. It should be noted that the sections are not to scale, the real dimensions are written on the arrows. First, the red arrows show the overall chip size and the sizes of the sensitive and non-sensitive parts. Around the chip, there is an unused area to ensure that the chip is not damaged during dicing. The pixel matrix consists of 256 × 250 pixels with a size of 80 µm × 80 µm. Below the pixel matrix the readout buffer matrix is placed. It comprises 375 × 128 readout buffer elements, the occupied area is 2 100 µm × 20 480 µm. Each readout buffer has a size of 5 µm × 160 µm. Next to the bottom edge of the readout buffer matrix, the end-of-column with a height of 160 µm is positioned. All other circuits in the periphery, as the digital readout state machine, the slow control, the power regulators and the pads, are placed in the region at the bottom edge and require an area of 591 µm × 20 480 µm.

In the following, the signal flow is explained. The signal generation takes place in the pixel, then it is amplified inside the pixel. Afterwards, the signal is transmitted to the readout buffer where the signal is discriminated with two comparators. From now on, it makes more sense to talk about hit information data that is transmitted instead of a signal, because in the readout buffer and EoC further information is added to the signal. From

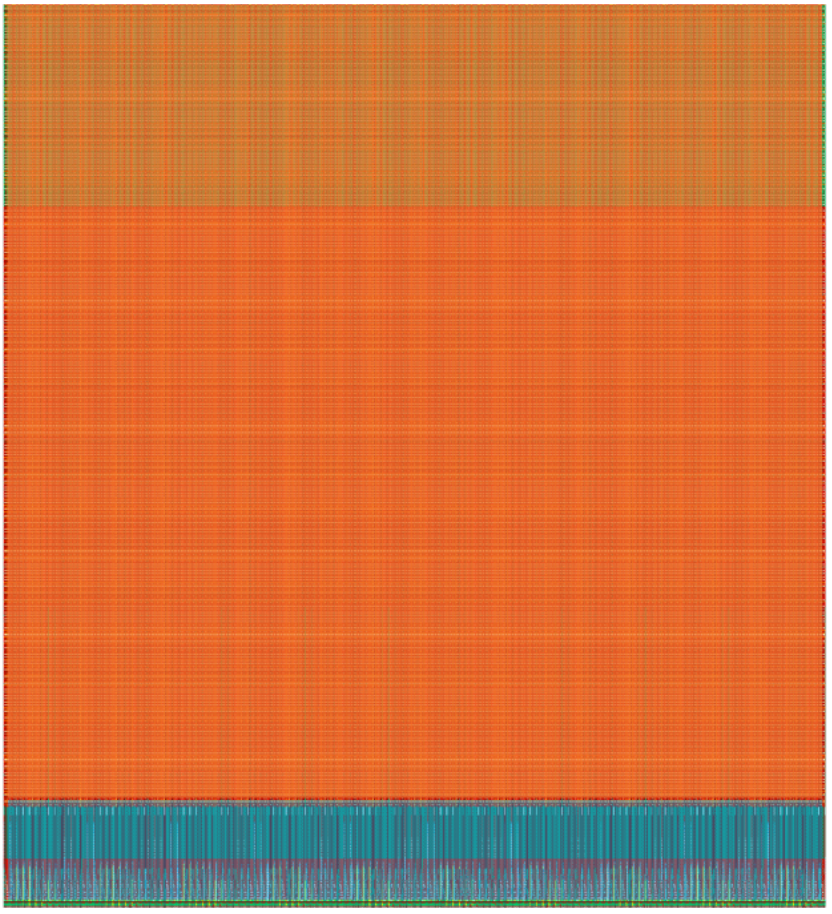

Figure 9.1: Layout of the MuPix10: the active pixel matrix in orange and the non-sensitive part (readout buffers and periphery) at the bottom in blue. The chips has a size of of 20.66 mm × 23.18 mm.

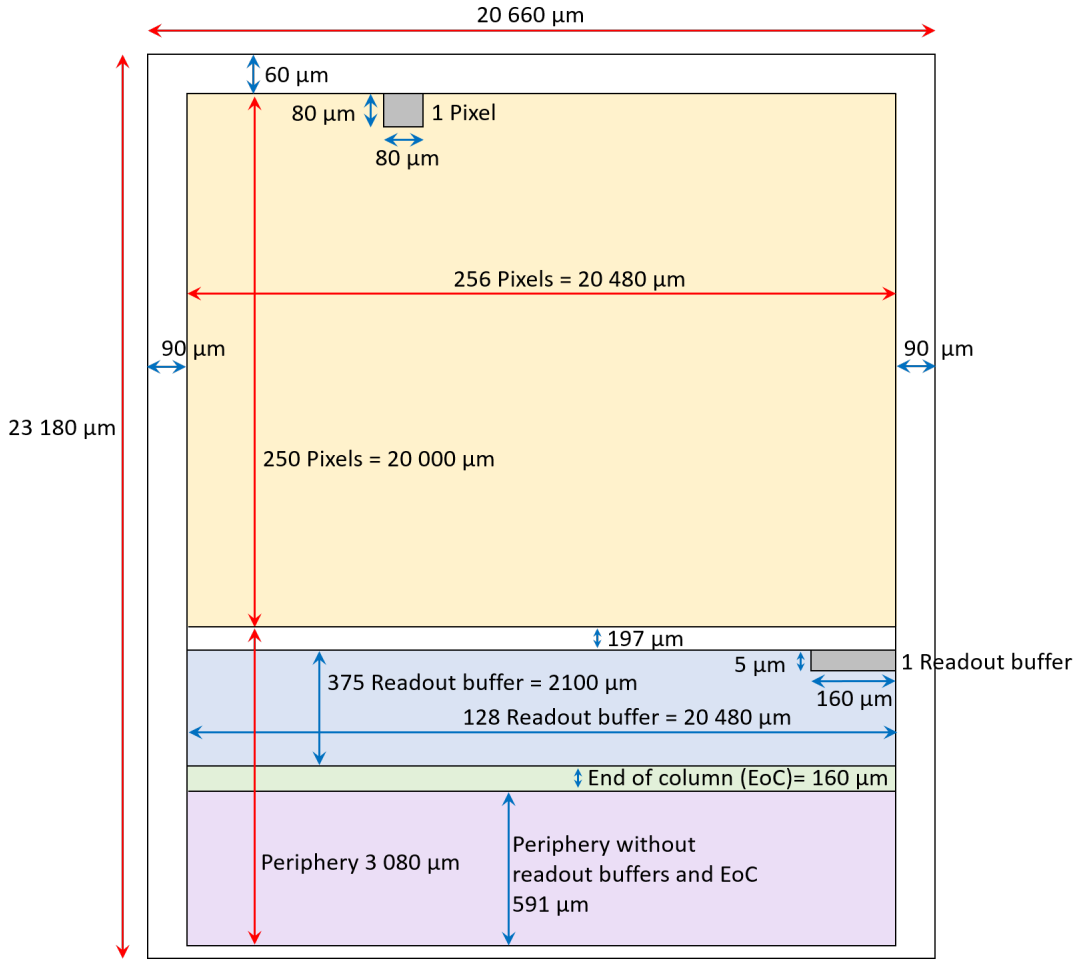

Figure 9.2: Sketch of all sizes of the MuPix10, the individual parts are not shown to scale. The red arrows show the chip size and the sizes of the sensitive and non-sensitive areas while the blue arrows show the sizes of specific parts and areas.

the readout buffer the hit information is forwarded to the EoC and from here to the digital readout control block. Then the data are passed to the output pads of the chip. This data flow is shown in figure 9.3.

For the Mu3e experiment it is important to read out the chip continuously because there will be no trigger information for the tracking detector. This leads to the requirement of a fast readout of the chip data in a well defined data format realised with the readout control block. To shorten the readout time the pixel matrix is divided into three segments of 84, 86 and 86 columns with a individual readout link for each segment. Each readout link has its own pad. The nominal bandwidth per readout link is 1.25 Gbit/s. By transmitting the date with the three individual links, a total rate of 90 MHit/s can theoretically be achieved [54]. Additionally, a fourth readout channel is implemented with the digital readout control to multiplex the three channels to one.

The readout control block is generated from hardware description language (HDL) code with digital synthesis tools. It includes the state machine for controlling the readout and transforming the hit data to the output data format with an 8b10b encoding. The drivers for the differential readout links as well as timestamp counter, clock generator and clock dividers are implemented in the readout control unit. Furthermore, the configuration shift registers are included in this part. They are implemented in triple redundancy preventing single event upset to allow a stable and safe operation of the chip.

A power regulator for the amplifier voltage *vssa* was also designed for the MuPix10 as part of this work. This reduces the number of supply voltages needed. The regulator works as a self adjusting voltage divider with the working point at 1.2 V.

9.1.1 MuPix pixel

The pixel of the MuPix has a size of 80 µm × 80 µm. The size was chosen to fulfil the Mu3e requirements regarding spatial resolution. Inside the pixel, the charge sensitive amplifier (see section 5) is located. A charged particle deposits charge by ionisation loss inside the pixel while passing through it. This charge is collected by a diode and amplified. The amplified signal is then transmitted to the comparator outside the pixel matrix. The pixel itself has a large guard ring (see wide blue rings in figure 9.4). The guard ring is optimized to increase the possible depletion voltage before breakdown. In the middle of the pixel, the amplifier electronics are placed. The pixel is shielded from the signal lines by different metal planes. The pixel electronics contains the charge sensitive PMOS amplifier, the output driver and the connection to a test signal generator.

The power grid is located on top of the pixels to supply the amplifiers. It has to be noted that there are no clock signals in the pixel and the pixel matrix. The pixel matrix works

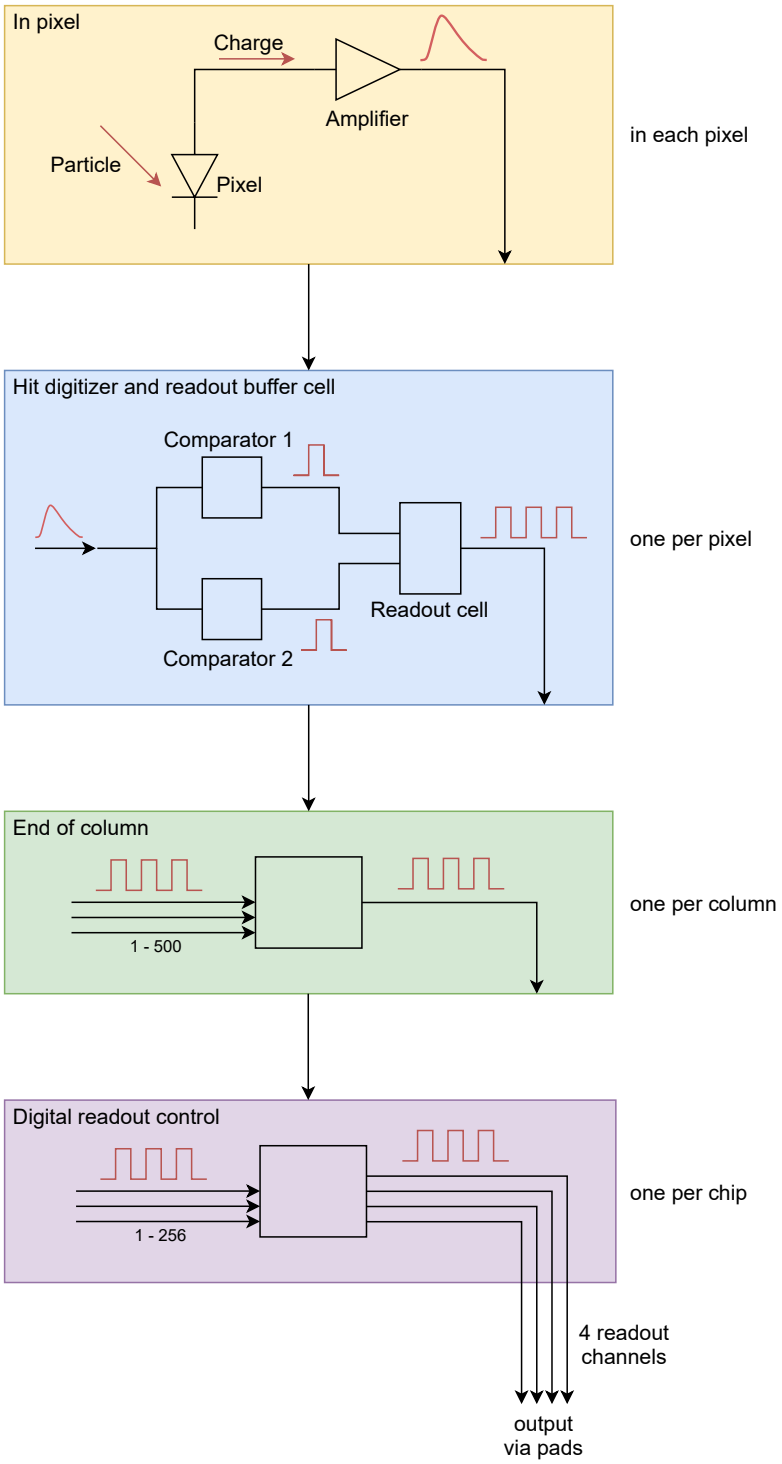

Figure 9.3: Signal flow diagram from the pixel to the pads in the MuPix10. The yellow part shows the electronics in each pixel. Here the signal is detected and amplified. The signal is transmitted to the readout buffer cell (blue), each pixel has one readout buffer. The information from the readout buffer is forwarded to end-of-column (EoC) (green). Each readout buffer column is connected to one EoC. The 256 EoCs are connected to a digital readout control block (purple).

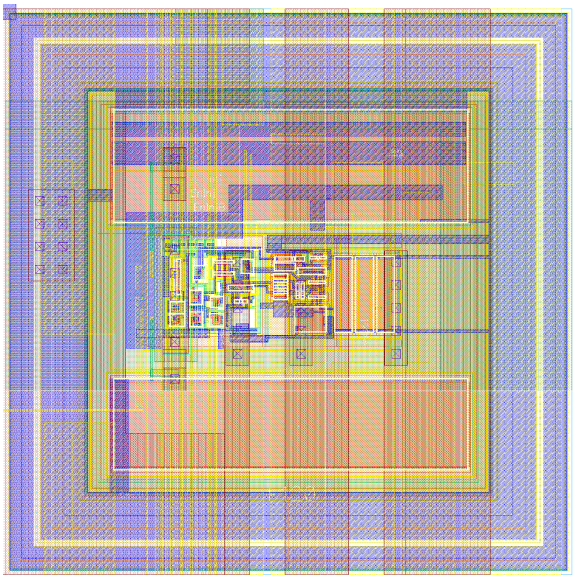

Figure 9.4: Layout of the MuPix10 pixel with a size of 80 µm × 80 µm. In the middle the amplifier is located.

asynchronously. Clock signals are avoided because the fast changing potentials of the clock lines lead to noise inside the sensitive pixel matrix.

The pixels are forming a matrix as large as possible to maximise the sensitive area of the MuPix which is important to get high tracking efficiency with the M3e detector. The pixel matrix covers 20.48 mm × 20.00 mm of the total chip area of 20.66 mm × 23.18 mm. This means around 85.5 % of the chip area is sensitive. The pixel matrix comprises 256 columns and 250 rows leading to a total amount of 64000 pixels.

9.1.2 Column drain readout

The choice of readout architecture is mainly determined by the application. The readout architecture must be reliable, provide the required information and ensure the required readout time. The column drain architecture is a column-level readout concept in which the pixel data is transferred directly to the column periphery formed by readout buffers [75]. Because the readout is dependent on the readout buffer columns, this architecture is called column drain readout.

With a column drain architecture, it is possible to realise a readout concept based on hits and timestamps, without a trigger signal in the pixel. It is suitable for readout concepts without an external trigger. The column drain architecture is already successfully used in many chips for particle physics [75] [16] [76] [77] [78].

In the column drain architecture, the mapping of pixel to readout buffer is 1:1, so one pixel has one readout buffer. It would be possible to change this to, for example, one pixel

to two buffers, so that the readout buffer could store two hits of the same pixel before it is forwarded to the end of the column. However, this would make the readout periphery much larger and since this area is not sensitive, it should be small. The 1:1 mapping is a good compromise between buffers and area.

Another alternative would be Parallel Pixel to Buffer (PPtB) as explained in [79] [80]. Here, 8 pixels are connected to 4 readout buffers, where each buffer can store the hit information of the 8 pixels. The disadvantage of this architecture is that no time over threshold (ToT) information can be provided. A ToT measurement is possible with Column Drain. The ToT allows a timewalk correction for a higher time resolution. In addition, PPtB is more complex and therefore requires significantly more space than Column Drain.

Column drain readout architecture for MuPix

Within the scope of this thesis, development of the readout buffer of MuPix8, 9 and 10 was carried out. Since the MuPix10 is the latest version, only the readout buffer version of the MuPix10 will be discussed in the following.

For Mu3e the data is read out continuously without an external trigger signal. This is possible with a column drain architecture. For the mapping of pixel to readout buffer 1:1 is chosen. That this mapping satisfies the requirements was shown in the beam test measurements of the MuPix, here no problems were seen with the expected rate of Mu3e. The rates in tracking detectors are low compared to in-beam monitoring applications.

The MuPix chip is organized in two matrices, the pixel and the readout buffer matrix as shown in figure 9.5, the EoC and the rest of the periphery, like the digital state machine. The pixel matrix is large in comparison to the inactive area of the chip, the pixel matrix size is $20.48\,\mathrm{mm} \times 20.00\,\mathrm{mm}$, the whole periphery has a height of 3.00 mm and spans the full width of the matrix. The readout scheme is defined by the organization of the readout buffer and the EoC. The readout buffer and the EoC are fully custom-made from schematic to layout.

The readout buffers in one column are connected to their predecessors and successors forming a chain. Each readout buffer column is one chain, the elements of this column chain are connected with a *priority logic*. The readout buffers make a digital signal out of the analogue amplifier signal and are adding additional information like the two timestamps and the address to the *hit information* and store it temporarily. The *priority logic* between the readout buffers in one chain select which *hit information* is given first to *end-of-column* (EoC).

Each readout buffer column chain is connected to the EoC row chain: the EoC is, like the column chain, organised with the same elements connected to their predecessors and successors forming a chain, but in contrast to the column chain this is a row chain because

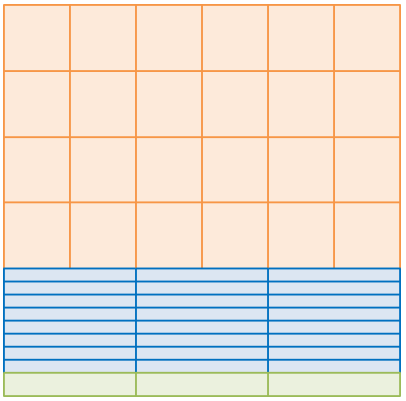

Figure 9.5: Scheme of the matrix structure with the pixels in red, the readout buffers in blue and the end-of-column in green. The pixels and the readout buffers form a double column structure, the figure is not to scale.

every column chain is connected once to it. The *hit information* from the – by the *priority logic* selected – readout buffer is given to the corresponding EoC cell and stored temporarily. Now the readout buffer does not need to store it longer and can store the *hit information* of the next signal from the amplifier in the connected pixel. Note, that this is all realised asynchronously without a clock limiting speed. The data in the EoC are then given to the digital state machine managing the four data output lines of the MuPix.

To summarize, there are two temporary storage locations (for each pixel one readout buffer, for each readout buffer chain one cell in the EoC) and two chains (the readout buffer column chain and the EoC).

Readout buffer for MuPix

Each pixel has its own readout buffer connected by a long line. The readout buffer contains several circuits for different purposes: time measurement, amplitude measurement, address signal generation, temporary storage of the hit information, priority ordered readout and hitbus signal generation.

The readout buffer consists of:

- Two comparators
- One eleven bit timestamp
- One five bit timestamp for ToT measurement
- One nine bit address
- One SRAM block
- One control logic
- Half a priority logic (one priority logic is shared by the two pixels)

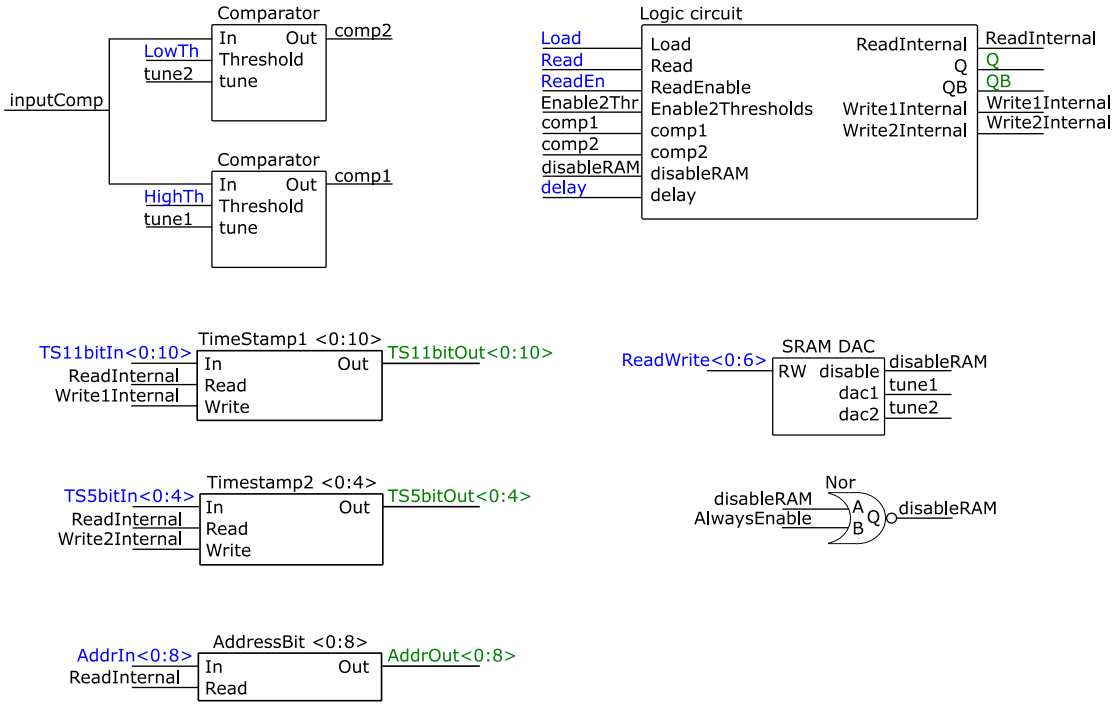

Figure 9.6: Overview of the readout buffer parts for one pixel without the priority logic. The inputs of each part are on the left, the global inputs of the readout buffer are in blue, the outputs of each part are on the right, the global outputs of the readout buffer are in green.

A schematic overview of the parts of the readout buffer without the priority logic is shown in figure 9.6.

Two pixel columns form, together with one readout buffer column, a double column containing 500 pixels. Two readout buffers share one priority logic. Therefore, the layout is repeated after two readout buffer The size of two readout buffer cells with the priority logic is $5\,\mu m \times 160\,\mu m$. The layout is shown in figure 9.7.

The used comparator in the readout buffer are presented in detail in section 6. The *comparators* are tuneable with 3 bit. The simulated power consumption of both comparators is $2.52\,\mu W$ $(2 \times 700\,nA \times 1.8\,V)$. The readout buffer can be operated in two different modes: in the first one, a time-over-threshold (ToT) is measured to allow for an off-chip timewalk correction by using only one comparator per pixel. In the second mode both comparators are used, as explained in section 6.4, for the on-chip timewalk correction or for the two threshold method. The different length of the two *timestamps* is based on the different purposes of the two timestamps and on the experiences with previous MuPix versions, mainly the MuPix8.

The core part of the readout buffer is the control logic which will be explained in the following. By the control logic, the hit information is correctly built and stored in the readout buffer. Figure 9.8 shows the elements of the readout buffer logic. With the *nor*,

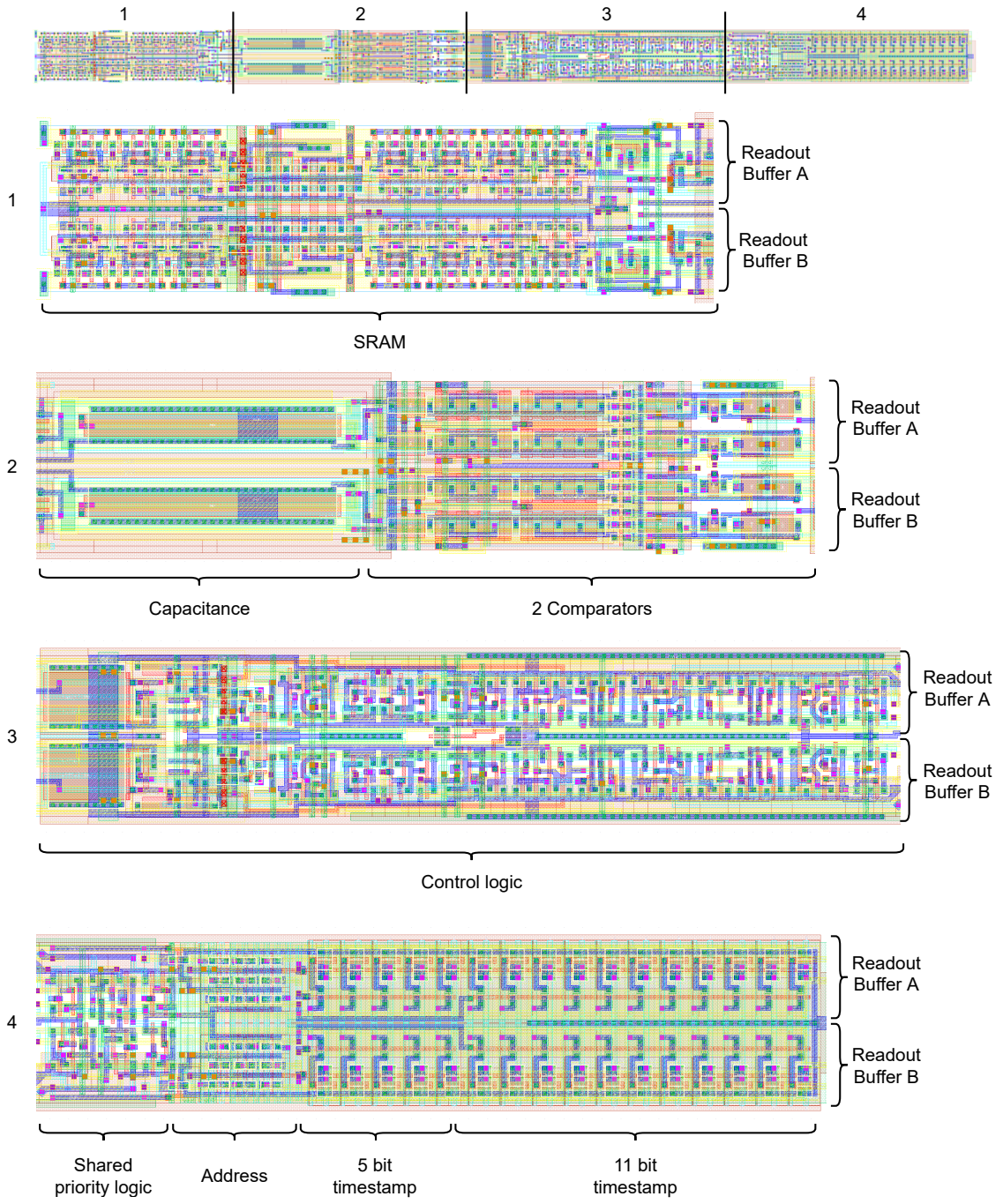

Figure 9.7: Layout of two readout buffers connected to two pixels, the layout has a size of $5 \times 160\,\mu m^2$. For a better illustration, the layout has been divided into four parts.

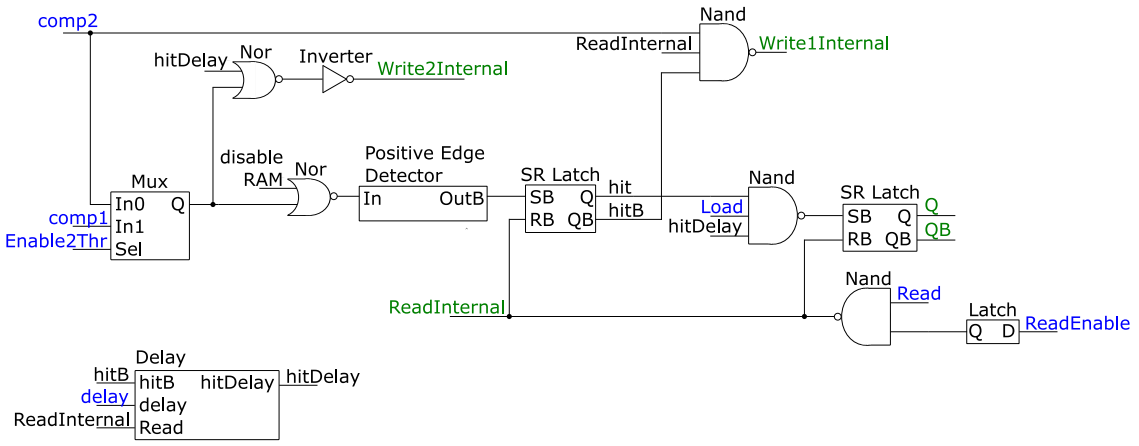

Figure 9.8: Control logic of the readout buffer, without the priority logic. The inputs of the control logic are in blue, the outputs in green. With the multiplexer (Mux), it is possible to choose between the two threshold mode or the single threshold mode. The delay circuit prevents the hits from being read out before the timestamp is stored.

the readout buffer can be disabled. Between the two operation modes can be switched using *enable2Thr* and the connected multiplexer. After the *nor*, the signal still looks like the output of the comparator. This changes with the next element, the *Positive Edge Detector* detecting the rising edge. The output is now a shorter negative pulse. After the first *SR latch* the inverted signal is connected to the *delay* circuit and the *nand* with 3 inputs at the top. The non-inverted signal is connected to the other *nand* with 3 inputs.

The delay circuit prevents the hits from being read out before the timestamp is stored (before the hit signal ended) by adding a fixed delay to all hit signals. Furthermore, for the planned Mu3e online hit sorting all hits should arrive in as small a time window as possible. The delay circuit works with a current source charging up a capacitor. The delay time is determined by reaching a fixed voltage at the capacitor and adjustable using the configurable strength of the current source. Now the signals provided by the EoC to the readout buffer *LoadPix* and *ReadPix* are used to generate the two most important internal signals of the readout buffer: *WriteInternalB* and *ReadInternalB*. These two outputs of the logic part are connected to the two timestamp blocks to enable the reading and writing of the timestamps.

In figure 9.9 the input and internal signals of the readout buffer are shown for the operation mode with one threshold and the two timestamps providing a ToT measurement. In orange the input of the comparator is shown (for simplification as a square signal), input signals of the readout buffer logic part are in blue, the internal signals in black and the outputs in green.

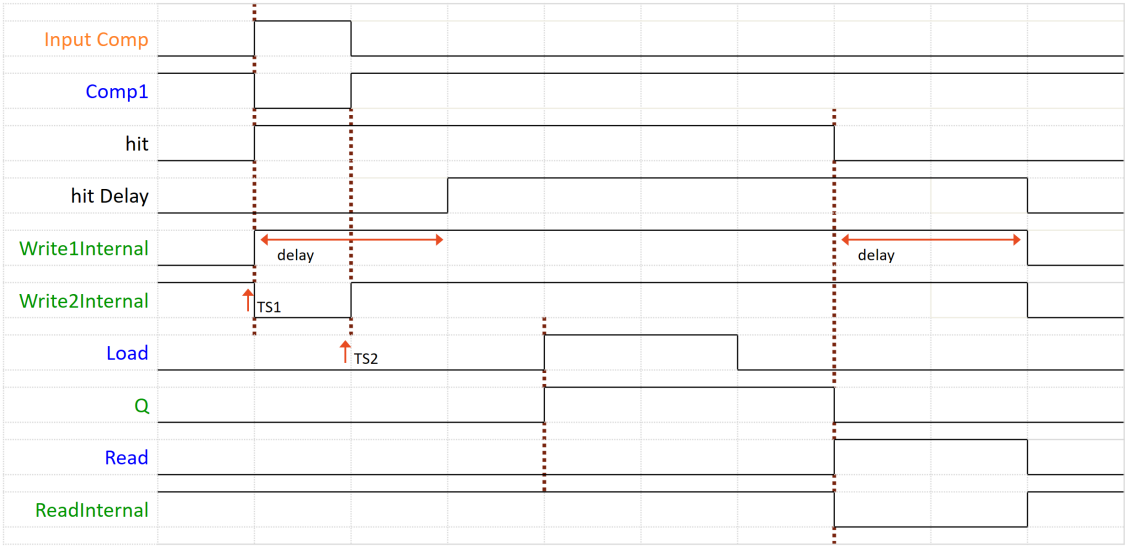

Figure 9.9: Here the most important inputs, outputs and internal signals of the readout buffer are shown. The input of the comparator is shown in orange (for simplification as a square signal not as the real analogue signal), input signals of the readout buffer logic part are in blue, the internal signals in black and the outputs in green. This shows the operation mode with one comparator and a ToT measurement: TS1 marks the beginning of crossing the threshold, TS2 the ending.

Readout buffer priority logic for MuPix

The next part to be explained is the priority logic defining which hit information from this readout buffer column is given to the EoC. The task of the priority logic is to assure that only one readout buffer (corresponding to one pixel and one hit information) is activated for readout at a time. This is important to prevent data mixing. If, for example, two hits are detected and are saved in the readout buffer, then the hit information in the geometrical first readout buffer will be selected first for read out.

The readout buffers in one column are connected to 500 pixels which are organized for the *or-cascading* in 25 groups, each containing 20 readout buffers. Every group shares a fast scan signal. The readout buffers in one group are connected with the *slow scan* signal, the last slow signal of one group is the fast scan signal for the next group, see figure 9.10. After the first hit in a readout buffer is found the slow scan signal changes and the next groups are bypassed by the fast scan signal. So the next readout buffers do not have to be checked one by one, they are skipped simultaneously. This leads to a time reduction speeding up the priority logic.

The priority logic is shown in figure 9.11. As input for the readout buffer logic negated and non-negated signal are needed. The negated signals do not need an inverter, they are provided by the previous parts in both ways.

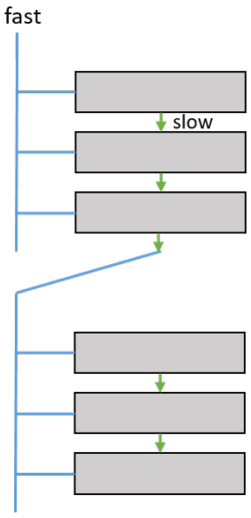

Figure 9.10: Visualisation of the speed up priority scan logic: the slow output signal of one group is used as the fast input signal of the next group.

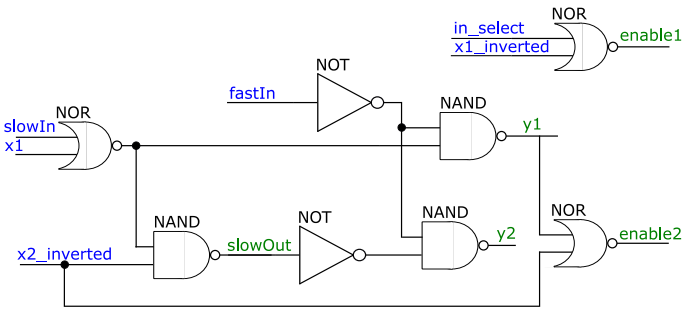

Figure 9.11: Or-cascading realized with alternating nor and nand gates, here the smallest repeating cell is drawn. The inputs are blue, the outputs green.

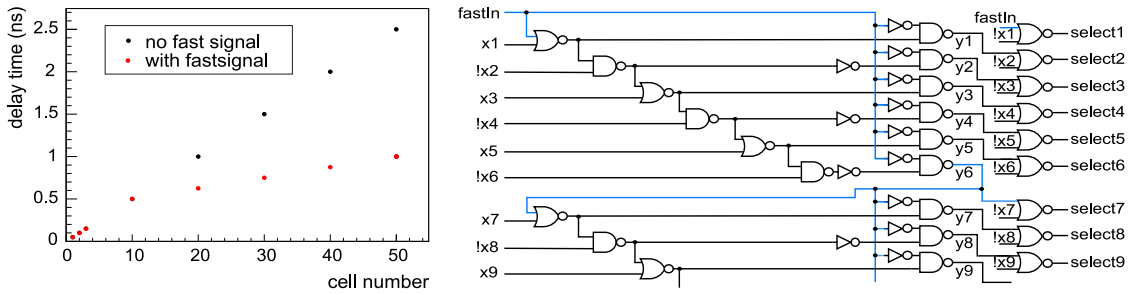

Figure 9.12: On the left side the simulated delay time without a fast scan signal and with the fast scan signals is shown for groups of ten cells. On the right side: or-cascading shown for two groups, the last slow signal is used as a fast signal for the next group, marked in blue. (From [81])

The priority logic is realized as an *or-cascading* optimized for speed. According to simulations, the worst case executing time for checking 500 elements in the priority logic, if they have detected a hit, is 6 ns. This is achieved using a *fast scan* signal. The delay time of the priority logic with and without the speed optimisation is shown for groups of ten cells in figure 9.12. Furthermore, the *or-cascading* is optimised concerning space, so as few transistors as possible are used. The needed functionality of the *or-cascading* priority logic is a long chain of *or* gates. With the use of boolean algebra this can be transformed to an alternating *nor* and *nand* scheme repeating for every second readout buffer. This alternating pattern has led to the scheme two pixels sharing one priority logic, because some nor and nand gates are not duplicated for every pixel.

End-of-column (EoC) for MuPix

The next part of the column drain readout scheme will be explained: the end-of-column (EoC). As shown in figure 9.5, there is one EoC cell (green) for each readout buffer column (blue) and double pixel column (red). The EoC temporarily stores the hit information from its readout buffer chain, both timestamps and row address. In the EoC, the column address is added to this hit information making it complete. Now the pixel belonging to the timestamps can be identified using the two addresses. The EoC generates the *ReadPixel* signal transmitted to the readout buffers. The readout control logic of the EoC is similar to the one in the readout buffers. The scan logic in the EoC selects the first EoC with a hit and its information is passed to the digital readout control block. Additionally, the EoC contains the driver for the timestamps and the other signals.

The inputs and outputs of the EoC are shown in figure 9.13. The global timestamps are buffered in the EoC. Based on the *LoadColumn* provided by the state machine in the digital readout control block and the column-level priority signal, *ReadPixel* is generated and connected to the readout buffers. *LoadPixel* is coming from the state machine, bufferd in the EoC and passed to the readout buffers. The *ReadColumn* signal has the same purpose for the EoC chain as the *ReadPixel* for the readout buffer chain.

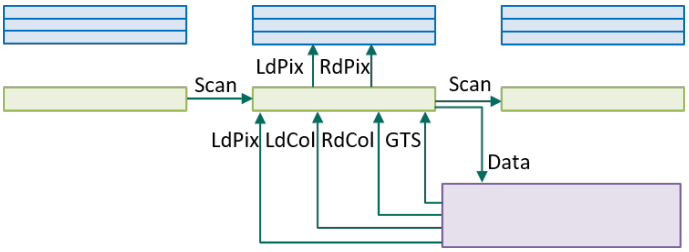

Figure 9.13: Inputs and outputs of the EoC shown for the EoC cell in the middle. In blue the readout buffers, in green the end-of-column and in purple the readout control block including the state machine. The EoC receives the scan signal from the previous EoC and provides the next scan signal for the next EoC. From the readout control block, the EoC receives the control signals *LoadPixel* (LdPix), *LoadColumn* (LdCol), *ReadColumn* (RdCol) and the global timestamp. Based on these control signals, the EoC sets the control signals for the readout buffers *LoadPixel* (LdPix) and *ReadPixel* (RdPix). The EoC passes the data to the digital readout control block.

The EoC has two outputs: one is the scan signal connecting the EoC cells to a chain and used for its priority logic and the other is data consisting of 16 bit timestamps and 16 bit addresses. The data are then passed to the state machine in the digital readout control block.

9.2 Characterisation

The full characterisation of the MuPix8, 9 and 10 was done by the Karlsruhe Institute of Technology (MuPix8) and the University Heidelberg (MuPix8, 9 and 10). Many results are published in several dissertations and papers: for example [56] [82] [83] [73] [38] [6] [54].

In the following, some results from groups of these two universities will be presented to prove that the MuPix as designed in the context of this work complies with its requirements. In addition, the tuning measurements made in the scope of this work are presented.

9.2.1 Measurements of efficiency and threshold tuning of MuPix8

According to the Mu3e requirements, the overall hit efficiency of the MuPix has to be better than 99%. The MuPix8 has a size of 10.8 mm × 19.5 mm with a pixel matrix consisting of 128 columns and 200 rows of pixels. The pixel size is the same as of the MuPix10. Multiple testbeams at DESY, PSI and CERN have shown a uniform high efficiency. At DESY an efficiency of 99.6 % for 4 GeV electrons was measured, see figure 9.14 [73]. To determine the efficiency of the sensor, it is used as a device under test in a telescope. The reference traces are extrapolated to the position of the test sample. These are matched to the hits on the sensor. The efficiency of the sensor is defined by the ratio between the number of matched

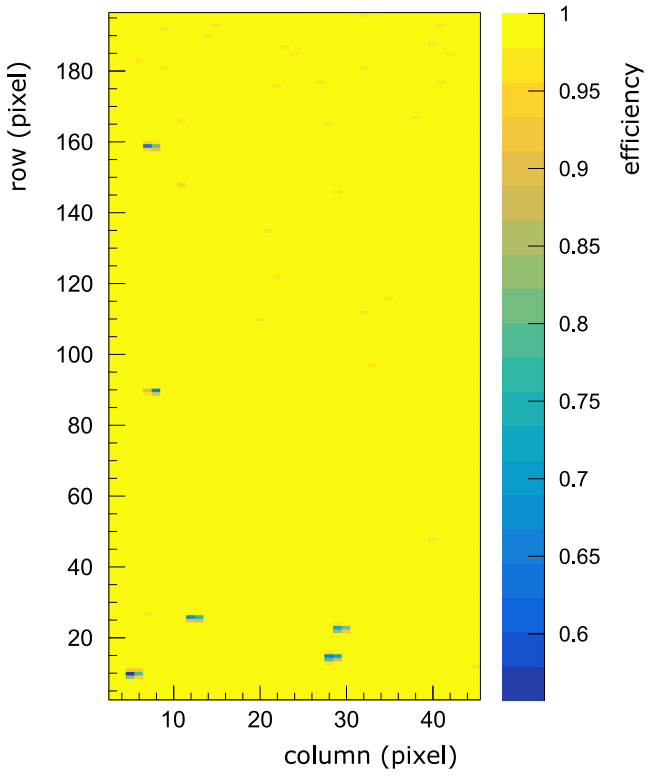

Figure 9.14: Efficiency map from beam test at DESY for 4 GeV electrons. The overall effinecy is 99.6 %. A few pixels have a significantly lower efficiency than the others. This is usually due to a mismatch of the transistors. (From [73])

tracks and the total number of tracks. Not all pixels have the same efficiency, a few have significantly lower efficiency than most. There are several explanations for this. First, the threshold is not the same for all pixels due to mismatch. The gain of individual pixels may also change due to transistor mismatch and can be lower for the ineffective pixels [83].

On MuPix8, it was only possible to tune one of the two comparators in the readout buffer with 3 bit. On the MuPix10, both comparators can be tuned individually, each with 3 bit. For the MuPix8 and the operation mode with one comparator for each pixel, the tuning procedure was tested with a test setup developed at KIT [6]. The comparator compares the analogue signal from the pixels to a given threshold. Due to production imperfections, the exact height of the threshold voltage at each comparator varies even though all threshold voltages of the comparators are connected and supplied with the same voltage. The behaviour of all readout buffers can be unified by adjusting the threshold of each comparator individually with three tuning bits. To find the optimal values for these tune DACs, the detection threshold of each pixel has to be determined. This is done by recording the test pulse detection efficiency S-curves for each tune value. Then the tune values are set to a value that shifts the S-curves onto each other, individually for each pixel. After setting the tune values, the global comparator threshold is lowered right

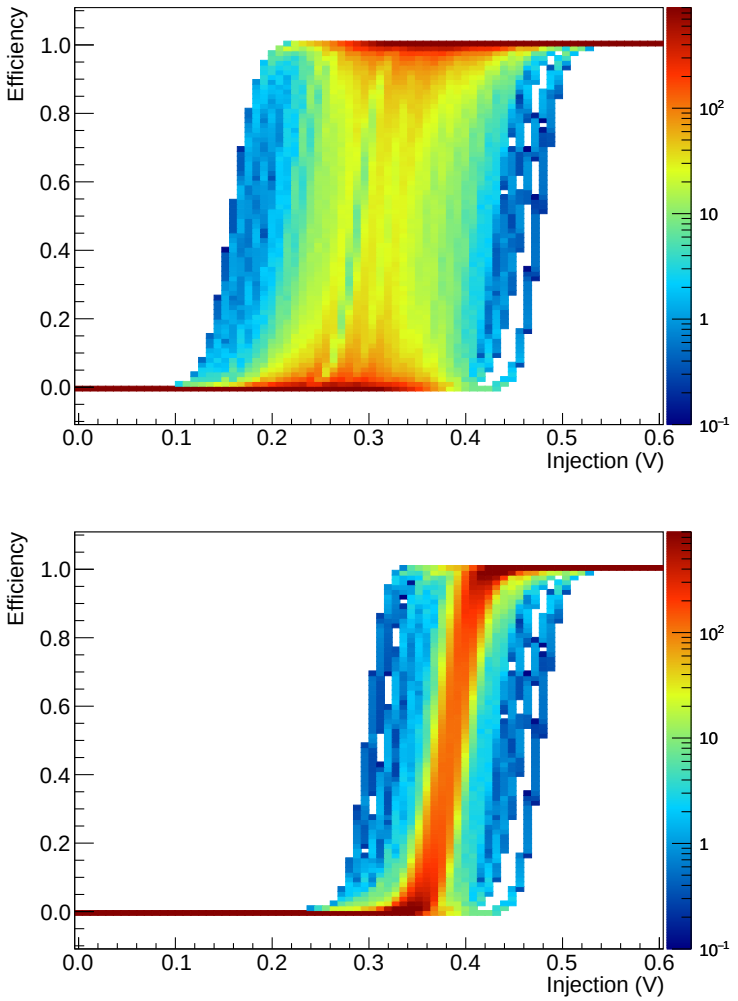

Figure 9.15: The test pulse detection efficiency of all measured pixels of matrix part A of the MuPix8. The S-curve density diagrams illustrate how large the spread of the S-curves is before tuning (top) and after tuning (bottom).

above the noise level. Figure 9.15 shows the test pulse detection efficiency of all measured pixels the MuPix8 before and after the tuning process. The tuning measurement of the MuPix8 showed that even for large scale sensors three tune bits are sufficient to obtain homogeneous threshold behaviour. Before tuning, the comparator threshold spread is $\sigma = 49\,\mathrm{mV}(= 231\,\mathrm{e}^-)$, after tuning, this value is reduced by a factor of 5 to $\sigma = 9\,\mathrm{mV}(= 42\,\mathrm{e}^-)$, see figure 9.16. For the conversion from mV to e^- see [6].

9.2.2 Measurements of threshold tuning and voltage regulator of MuPix10

For the commissioning of the MuPix10 at KIT with the GECCO setup [6], an adapter PCB was designed, see figure 9.17. Furthermore, the GECCO software and firmware were adapted for MuPix10, to provide the ADL group at KIT a functional setup.

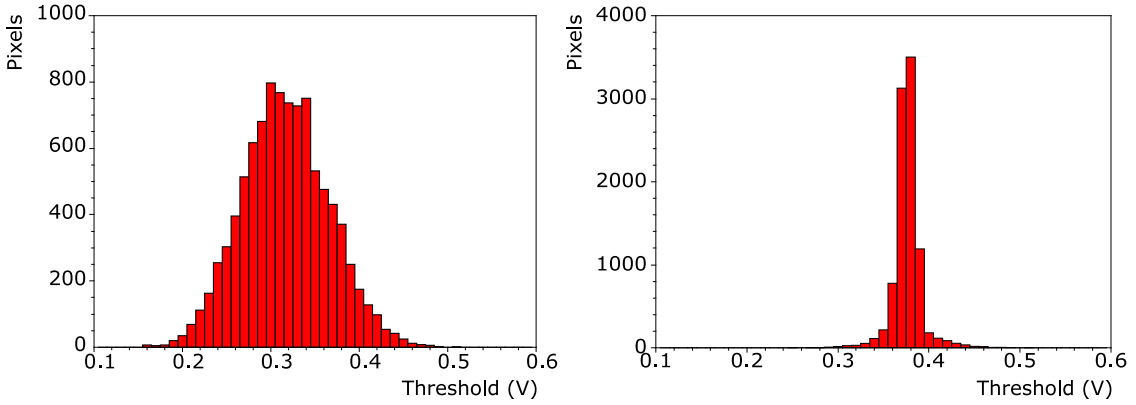

Figure 9.16: Before tuning (left), the comparator threshold spread is $s = 49\,\mathrm{mV}(= 231\,\mathrm{e}^-)$, after tuning (right) this value is reduced by a factor of 5 to $s = 9\,\mathrm{mV}(= 42\,\mathrm{e}^-)$.

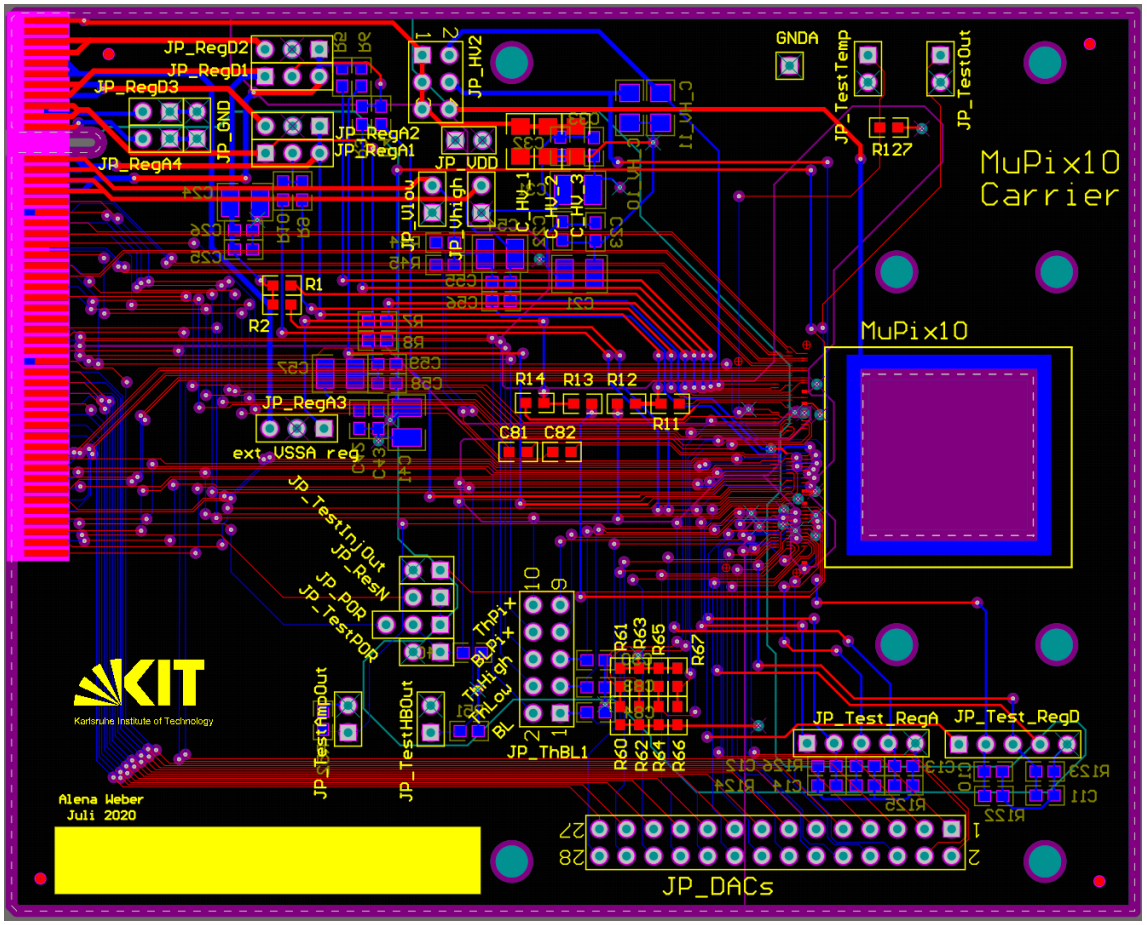

Figure 9.17: Layout of the adapter PCB for MuPix10, the dimensions are 10.5 cm × 8.4 cm.

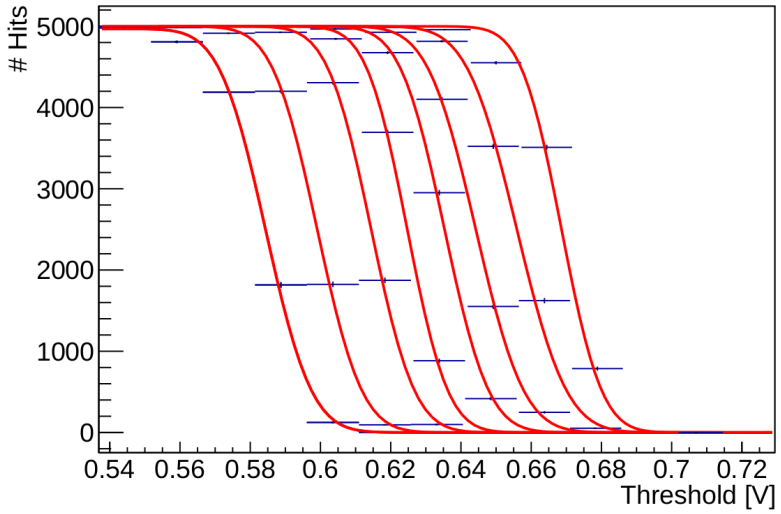

Figure 9.18: S-curves for the different tuning values from 0 (right curve) to 7 (left curve) for one pixel. Note that the threshold voltage is defined in this measurement as the sum of baseline voltage ($\approx 500\,\mathrm{mV}$) and threshold voltage. (From [84])

The characterisation of the MuPix10 was done at the Physical Institute, University Heidelberg. In [84], the MuPix10 was tuned to shift the threshold values of all pixels to get a uniform threshold for the whole matrix. In figure 9.18 it is shown that, as expected, different tuning values shift the S-curves of a single pixel. The linearity of the tuning steps is presented in figure 9.19.

By tuning all pixels individually, the threshold levels of the matrix can be equalised and lowered. This is shown in figure 9.20. The description of the full measurement is described in [84]. The tuning reduces the threshold distribution from 11 mV ($= 240\,\mathrm{e}^-$) to 4.8 mV ($= 74\,\mathrm{e}^-$) [54].

Efficiency and time resolution of the MuPix10 were measured in several testbeam measurement campaigns and analysed, both by the Mu3e group at the Physics Institute of the University of Heidelberg. First results are shown in [85] [86] [54]. The time resolution was measured to be 13 ns without off-chip corrections and 8 ns with corrections [85] [86]. The efficiny is above 99 % with a noise rate below 2 Hz/pixel [85].

The vssa regulator was measured by the Mu3e group at the Physics Institute of the University of Heidelberg. The vssa voltage has a linear behaviour and an operation range of 0 V to 1.4 V. The working point of 1.2 V is covered. In [54] the power consumption of the MuPix10 was measured to be between $200\,\mathrm{mW\,cm^{-2}}$ and $210\,\mathrm{mW\,cm^{-2}}$. The use of the vssa regulator reduces the necessary powering lines to only vdd and gnd, increasing the power consumption by approximately 10 %. Nevertheless, the power consumption requirement of Mu3e is met, it has to be lower than $350\,\mathrm{mW\,cm^{-2}}$. Figure 9.21 shows the vssa voltage and the supply current for a scan of the regulator reference voltage.

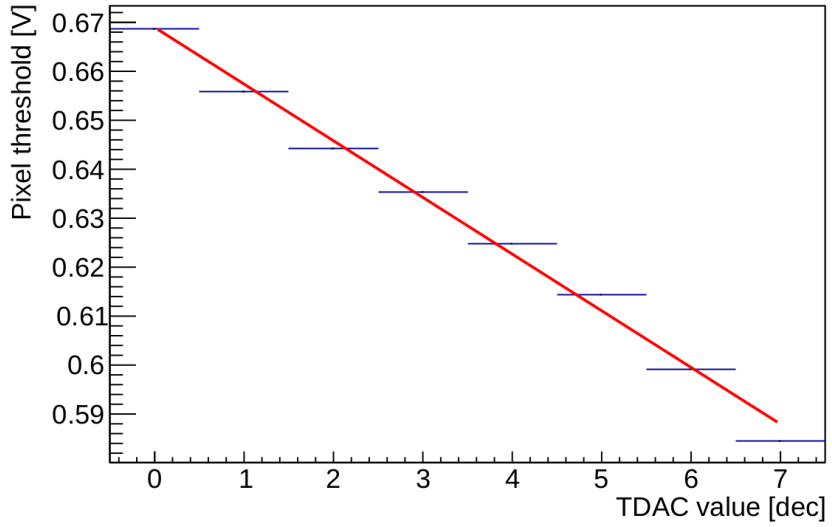

Figure 9.19: The tuning shifts the pixel threshold in linear steps. Note that the threshold voltage is defined in this measurement as the sum of baseline voltage ($\approx 500\,\mathrm{mV}$) and threshold voltage. (From [84] [54])

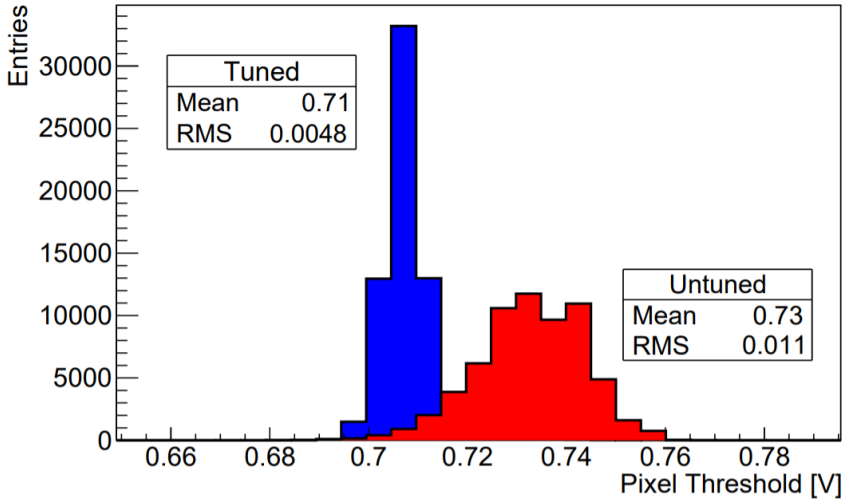

Figure 9.20: Pixel threshold distribution before tuning (red) and after tuning (blue). The tuning reduces the threshold dispersion from 11 mV ($= 240\,\mathrm{e}^-$) to 4.8 mV ($= 74\,\mathrm{e}^-$). Note that the threshold voltage is defined in this measurement as sum of baseline voltage ($\approx 500\,\mathrm{mV}$) and threshold voltage. (From [84])

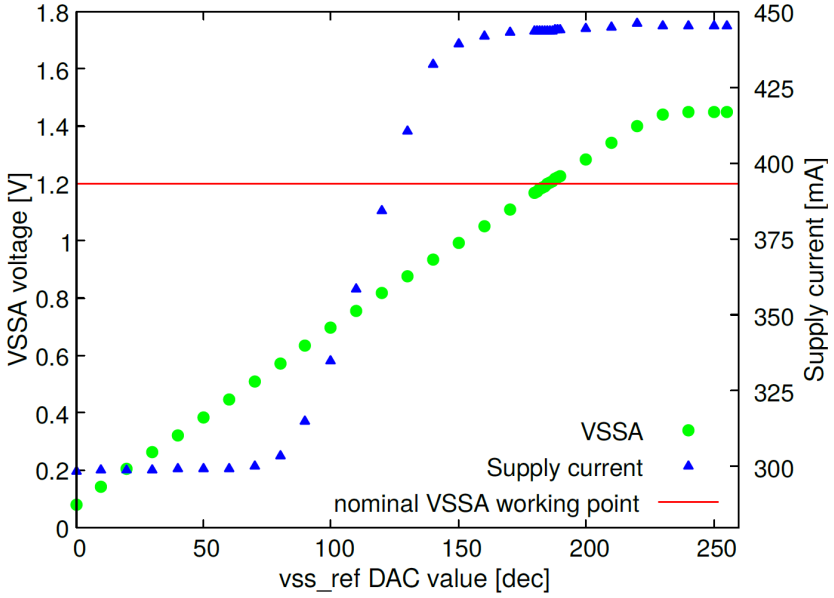

Figure 9.21: Vssa voltage and supply current for a scan of the adjustable reference voltage. The working point of VSSA is at 1.2 V and coverd by the regulator. (From [54])

Chapter 10

HitPix chip for particle detection in particle therapy

In this work, a radiation hard counting chip was developed from scratch. This is the first version of such a chip from the KIT ADL group, called HitPix. A variant of the HitPix with an additional manufacturing step was also designed, the HitPixISO. The development and submission was carried out in 2020. In the summer of 2021, the larger HitPix2 was developed in this work. This chapter first explains the architecture and functionality of the HitPix and then presents the measurement setup. Section 10.3 shows the results of the characterisation and test beam measurements.

10.1 Architecture

In a beam monitoring sensor, the spatial resolution does not need to be as high as in a tracking detector, so the pixels can be significantly larger. The pixel size in the HitPix is more than 6 times that of the MuPix. The final beam monitor system will consist of a matrix of several chips, in the case of the HIT project the monitor will be 25 cm × 25 cm. No full fill factor is needed as the relative rate measurement is sufficient. The sensitive areas should be distributed as equally as possible over the matrix. This results in the requirement that the insensitive periphery must be as small as possible. Part of the electronics can be realised within the pixels because they are large. For the HitPix the area of the electronics inside the pixel is not sensitive, leading to no full fill factor. In case of the HitPixISO this area is sensitive.

Larger pixels have a larger capacitance. Therefore, the same amplifier in a larger pixel results in a smaller amplification. This is not a problem for the HitPix because the signals are large and do not need such a large amplification. The amplifier used in the HitPix is the same as in the MuPix10, but because of the larger pixels, the signal amplification is much smaller. The comparison between the amplified signals of the HitPix and the ISO HitPix shown in section 10.3 also confirms the relationship between pixel size and amplification. The active pixel size of the ISO variant is the full pixel size, with the standard HitPix it is only a part of it. Consequently, with the ISO, the pixel capacitance is larger and thus the amplification is smaller. Both chips were tested at the HIT in the beam, it was shown that the ISO amplification is sufficient for the signals as well, see section 10.3.

The large pixels allow the placement of complex electronics inside the pixel: comparator, counter and adder. Since the circuits have to be isolated from the sensitive floating n-well, the active pixel area becomes smaller, so the HitPix does not have a full fill factor. This is fine, because only a relative rate measurement is made. This allows for a small periphery.

The HitPix has an area of 4.9 mm × 5.2 mm and has been submitted in 2020 in three different variants. The pixel matrix is built from 24 columns, each with 24 pixels. The pixel size is 200 µm × 200 µm. Three variants of the HitPix have been submitted, all have the same architecture. Their positions on the submission reticle is shown in figure 10.1. The fabrication was done in a 180 nm HV-CMOS process:

- HitPix with single ended in- and outputs
- HitPix with differential in- and outputs
- HitPixISO with differential in- and outputs and isolated PMOS transistors in an additional deep p-well)

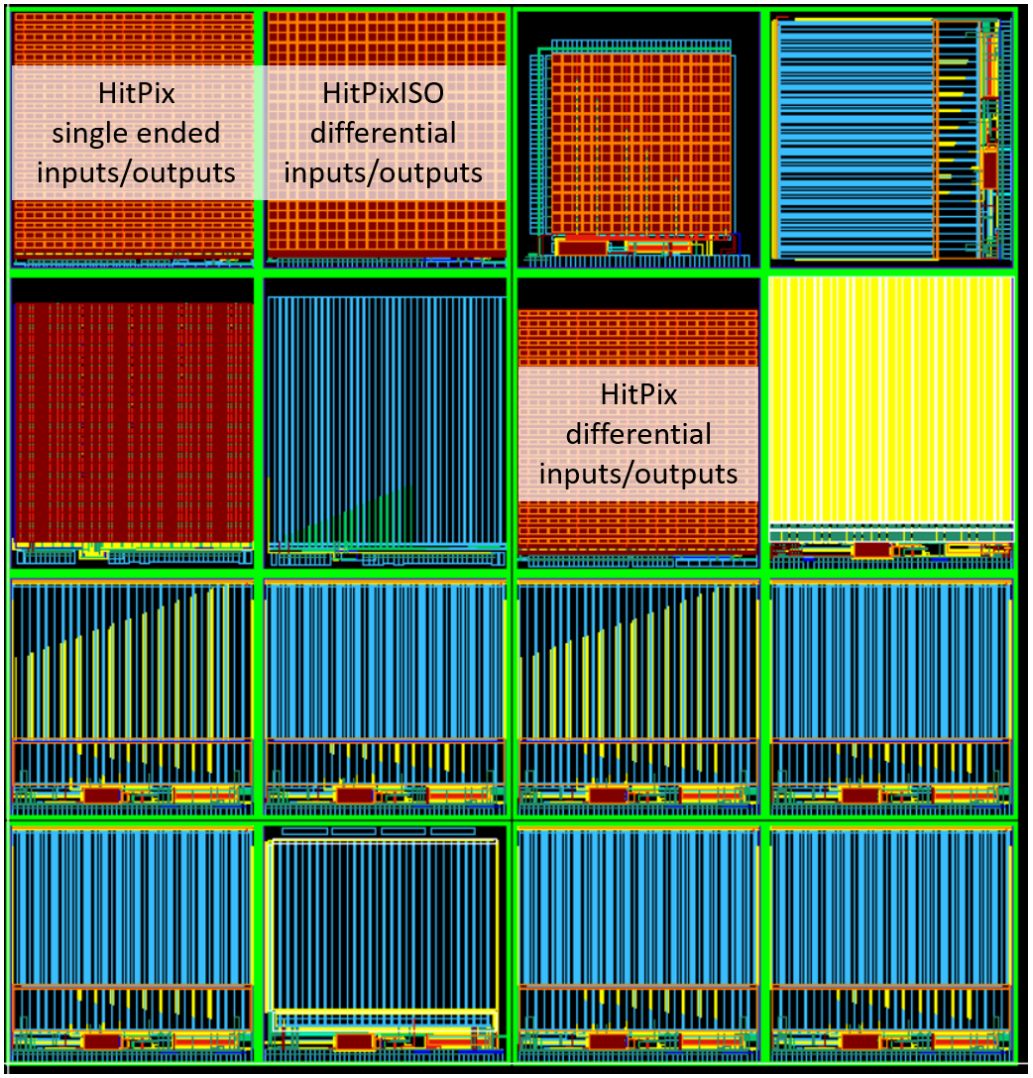

Figure 10.1: The position of the three variants of the HitPix in the reticle of the 180 nm HV-CMOS submission run in 2020.

10.1.1 HitPix pixel

The layout of the pixel of the HitPix is shown in figure 10.2.

The pixel is segregated into three parts: sensor diode, amplifier and comparator, counter and adder. The top part is the active part of the pixel acting as charge collection electrode. The sensor diode is formed by the deep n-well in the p-substrate. The sensor n-well in this part is electrically separated from the other pixel parts. The electronics are placed in shallow n-/p-wells, see figure 3.3. The sensor signal is then transmitted to the amplifier in the bottom right guard ring. The pixel has a size of $200\,\mu m \times 200\,\mu m$. The active sensor part of the pixel is smaller than the total area of the pixel, because only the upper part of the pixel is sensitive. Therefore, the sensor matrix of the HitPix has no full fill factor. This is not a disadvantage for the HitPix, because unlike in the Mu3e project, only the relative rate is important for beam monitoring.

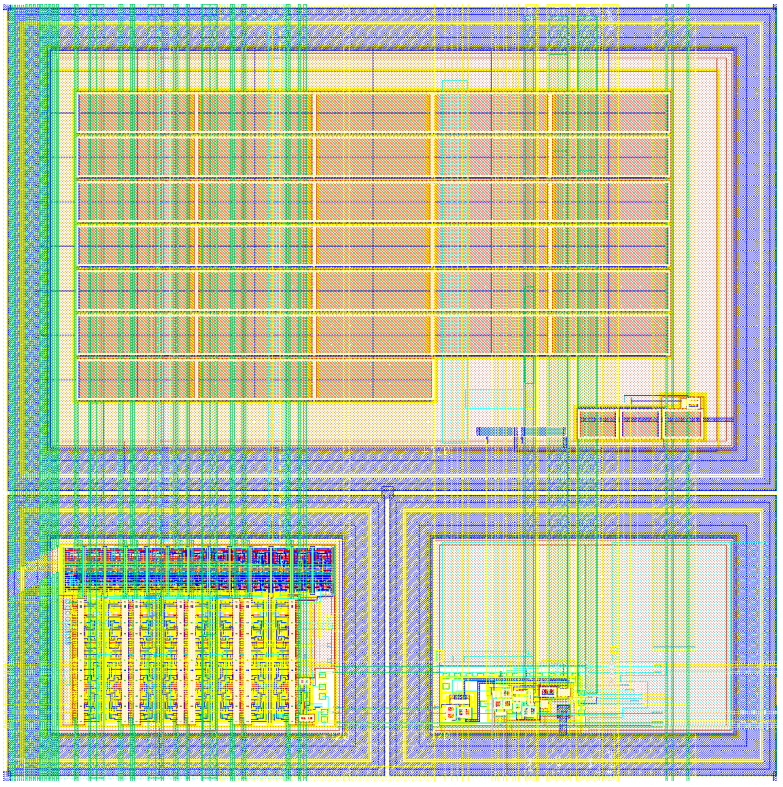

Figure 10.2: Layout of the HitPix pixel with a size of $200\,\mu m \times 200\,\mu m$. The area in the upper guard ring is the sensitive sensor part. At the bottom, in a non-sensitive part, the counter and adder (bottom left) and comparator and amplifier (bottom right) are implemented.

An alternative pixel design is used for the developed HitCounterISO chip which uses a slightly different fabrication process, the isolated PMOS (ISO) process. This process adds an additional deep p-well as it can be seen in figure 10.3. With this additional p-well it is possible to isolate the PMOS transistors, located in the n-well. Therefore complex CMOS

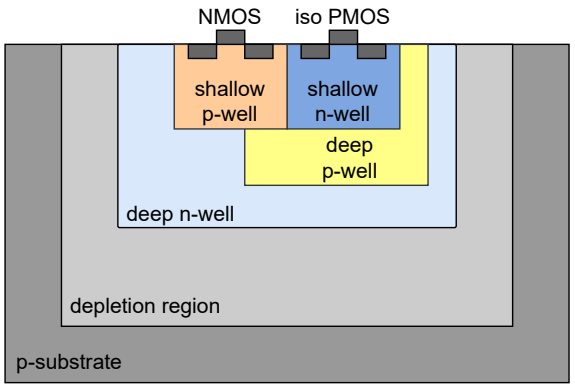

Figure 10.3: In the ISO process a deep p-well is added to the standard process. With this additional well the shallow n-well can be shielded.

circuits like the CMOS comparator, the counter and the adder can be placed inside the sensitive pixel area. Figure 10.4 shows the ISO pixel layout with a fill factor of 100 %.

With the radiation hard 8 bit counter presented in section 8.1, the in-pixel hit counting is realised. In section 8.2 in figure 8.7, the adder function is shown. The counter value of the pixel is added with its in-pixel adder to the adder result of the previous pixel. This leads to the required column projection of the counts.

The readout periphery is small, with a size of 4 800 µm × 64 µm, compared to the pixel matrix with a size of 4 800 µm × 4 800 µm. The division in active (pixel matrix) and inactive area (readout periphery and pads) leads to 92.31 % of active area and 7.69 % of inactive area. Figure 10.5 shows the top layout of the HitPix with differential in- and outputs.

10.1.2 Address based readout

The readout scheme of the HitPix is less complex then the one of the MuPix. The HitPix consists of many new features in the pixel matrix, therefore the readout was realized more simply in comparison to the MuPix. In the pixels of the HitPix, amplifier, comparator, counter and adder are placed, so no additional matrix with readout buffers is needed. Therefore, at the bottom of each pixel column an end-of-column (EoC) block is placed, leading to a structure as shown in figure 10.7.

The address based readout scheme of the HitPix is row-oriented, i.e. the user selects a pixel row for all columns by writing the desired row address of this row. Then this pixel row is read out. In most cases it makes sense to write and read out the individual row addresses one after the other. In this way, the data of the entire pixel matrix is read out row by row.

The pixels give only one information to the EoC depending on the operation mode. The HitPix has two operation modes specifying what information from the pixel matrix is read

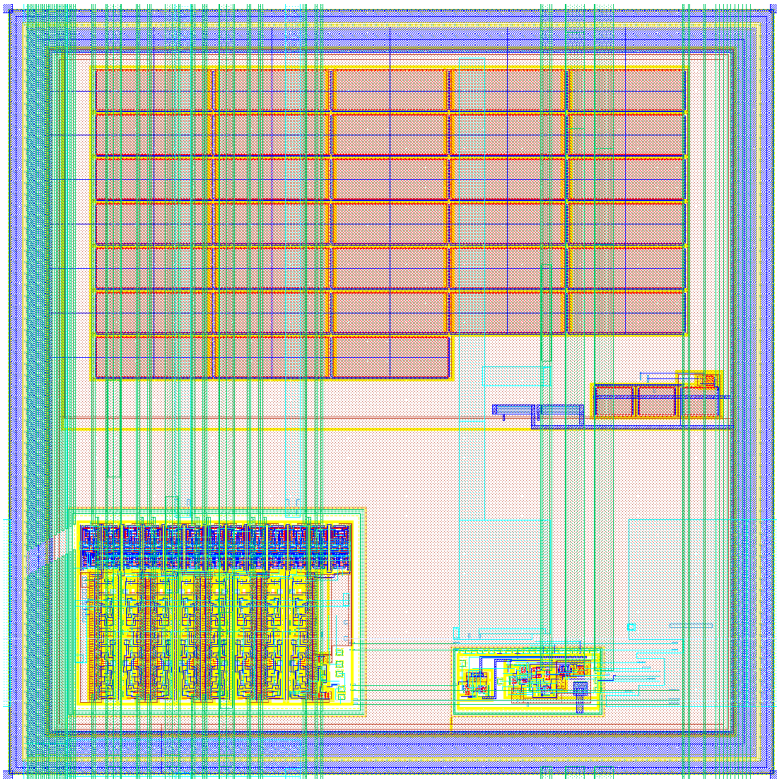

Figure 10.4: Layout of the HitPixISO pixel with a size of 200 µm × 200 µm. The entire pixel is sensitive leading to 100 % fill factor.

out: in one operation mode, the counter values of each pixel are given to the EoC and then read out. In the other mode, the sum of all counters of the pixels in one column is given to the EoC. In the following, the information coming from the column will be called *column information*. The counter and adder are explained in detail in chapter 8.

The EoC of the hit counting chip consists of two different blocks, see figure 10.8:

- Shift register, formed by 13 radiation hard scan flip-flops
- Row control block

The *column information* has, in case of the counter operation mode, 8 bit and in case of the adder operation mode, 13 bit. Therefore, the EoC consists of 13 bit by using 13 radiation hard scan flip-flops to form the shift register of one column. Figure 10.9 shows how the 13 scan flip-flops are connected for the shift register. For simplification the figure shows only three scan flip-flops.

All column shift registers are connected to one large shift register. The user utilizes this shift register to write the row addresses to the EoC of the columns. Then all the *column information* is written in the shift register. By shifting the data out of the large shift register, the data is read out.

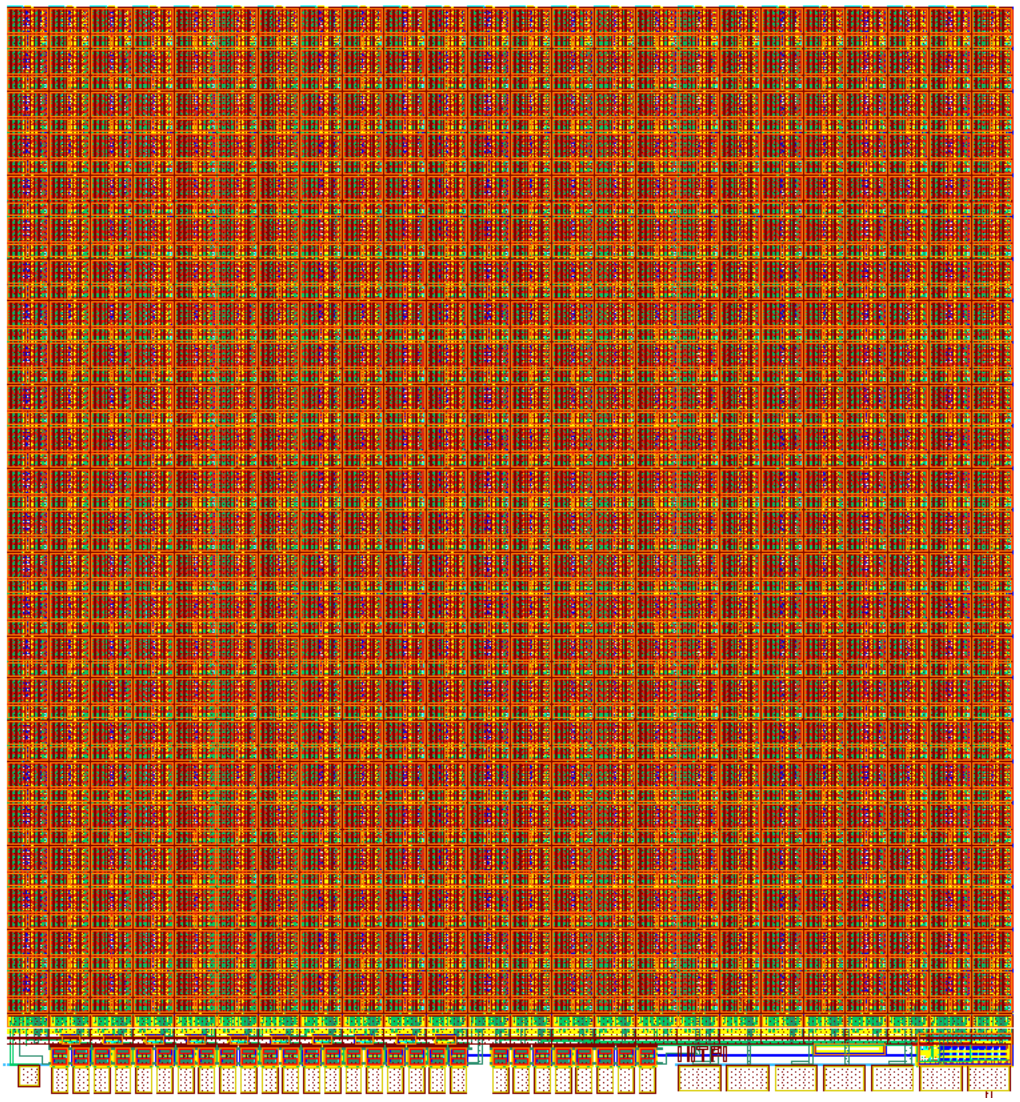

Figure 10.5: Layout of the HitPix in the variant with differential in- and outputs. The chip has a total area of 4.9 mm × 5.2 mm. The pixel matrix is shown in orange (4 800 µm × 4 800 µm), the readout periphery (4 800 µm × 64 µm) is the small yellow-green strip below the matrix and below are the pads.

Figure 10.6: Layout of the radiation hard EoC of the HitPix with a size of 200 µm × 64 µm.

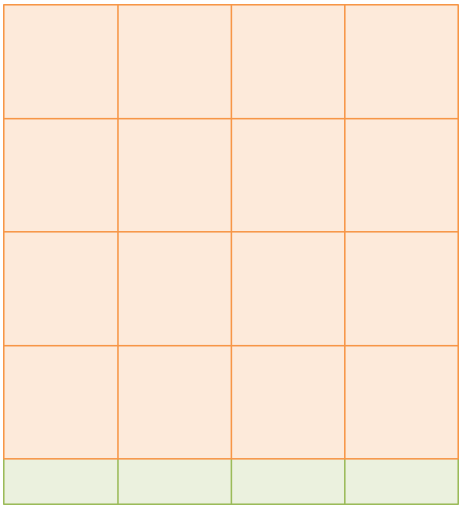

Figure 10.7: Scheme of the HitPix matrix structure with the pixels in red and the end-of-column in green. Compared to the MuPix10, no double-column structure is used.

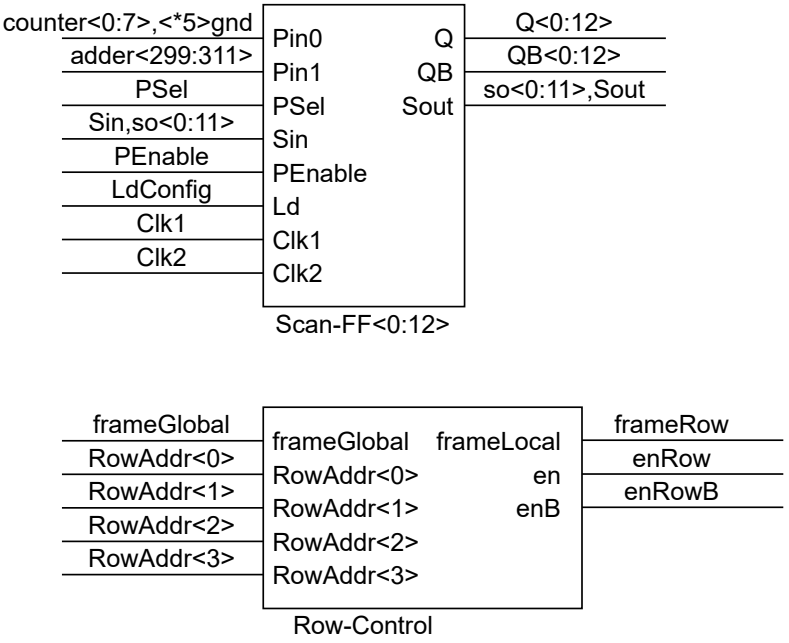

Figure 10.8: The 13 radiation hard scan flip-flops form a shift register that is used for configuration and readout. Together with the row control, it forms the end-of-column. The row control is used to set the correct row for reading out. The inputs are shown on the left side, the outputs are on the right.

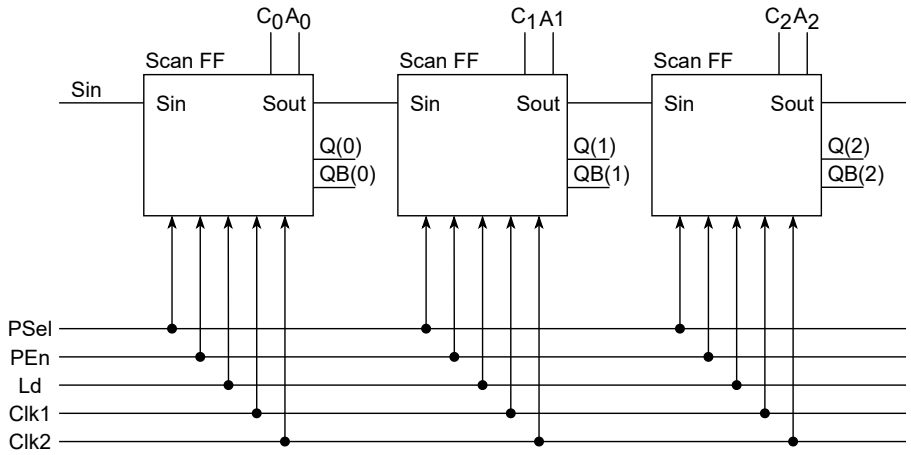

Figure 10.9: Inputs, outputs and connections of three scan flip-flops. The scan flip-flops share the control signals *PSel*, *PEn*, *Ld*, *Clk1* and *Clk2*. Each scan flip-flop is connected to a counter bit C_0 and an adder bit A_0 (when all adder bits are connected, the remaining scan flip-flops are connected to ground). Q_0 and QB_0 are the outputs of the scan flip-flops and are used for configuration. The S_{out} of one scan flip-flop is connected to the S_{in} of the next, creating a shift register. 13 scan flip-flops form the shift register of an EoC block.

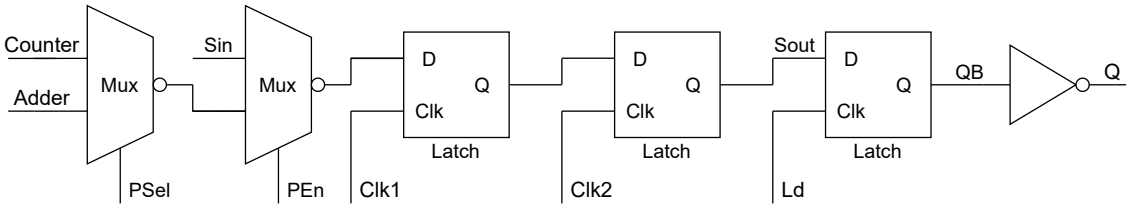

Figure 10.10: Inner structure of the scan flip-flop. The scan flip-flop consists of two multiplexers (*Mux*) to choose between configuration and readout (with *PEn*) and readout of the counter or adder (with *PEn* for readout and *PSel* for adder or counter). After the multiplexer, two latches are used for a safe shifting process with two clocks. With the signal *Ld*, the *Sout* is set as *Q* and *QB*.

To understand the EoC it is necessary to have a look inside the scan flip-flop. The inner structure is shown in figure 10.10. It can be chosen with *PSel*, if the value from the counter or the value from the adder is loaded into the shift register. *PEn* selects between *counter*/*adder* and *Sin*. The value of *Sin* is set by the user at the *Sin*-pad. From the figure it is seen the counter or adder value are shifted through the shift register, every second bit will be inverted, caused by saving inverters (which means transistors and space) in the EoC.

Figure 10.11 shows the inner structure of the row control. The *FrameGlobal* is set by the *frame* pad. The row control generates, from this signal, the *frameRow* signal connected to the rows. Here, the counters of one row share the same *frameRow* signal. Only when the *frame* signal to the counter is high, the counter is counting (see *nand* in figure 8.5).

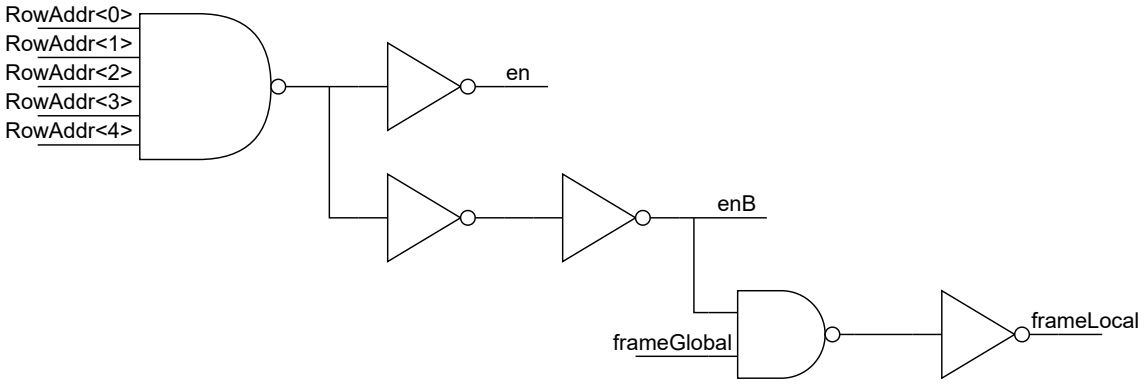

Figure 10.11: Circuit of the row control. The global frame signal *frameGlobal* is a signal set by the user. The row control stops the counters of the row selected for readout to ensure a safe reading. The counters are stopped when *frame* is low.

When *frame* is low the counter is not counting any more and can be read out without the counting value being changed during the readout process.

The shift register is used to configure the row control and for the data readout. The counter values are loaded in the shift register and shifted out. Increment errors are prevented during readout of the counters by stopping the counters. This is done with the frame signal generated in the row control. The counters in one column share the counter readout lines. Which row is read out is defined by the row control.

To copy the adder values to the EoC, the counters do not have to be stopped. Via the shift register the adder readout is selected in the row control and the values are copied in the EoC for shifting out. This allows an efficient data readout with minimal insensitive area. The adder readout is faster because only one data set has to be read out and is therefore more suitable for continuous beam monitoring while the counters give a more detailed measurement of the beam.

10.1.2.1 The HitPix2

In June 2021 an enlarged version of the HitPix was designed as the last project of this work. The HitPix2 is similar to the original HitPix: instead of 24 columns with 24 pixels each, it has 48 columns with 48 pixels leading to a total pixel number of 2 304. Therefore, the maximal number of hits in one column is $256 \cdot 48 = 12288$. The adder is enlarged by one bit to a 13 bit adder to cover this sum. There are still 8 connecting lines for the counter, the adder connecting lines are extended to 13. The shift register of the EoC has therefore also been extended by one bit. To address all pixels, the address also needs one more bit in comparison to the HitPix.

The final system will have an area of 25 cm × 25 cm consisting of several chips. The space in the system for connections to the chips is limited. Therefore, the sensor should require as few wires as possible. This led to the decision to use an NMOS amplifier for the HitPix2. The NMOS amplifier only needs one supply voltage, so it has one supply voltage less compared to the PMOS amplifier. The higher 1/f noise of the NMOS amplifier should not be a problem because of the large signals. In addition, the NMOS transistor is more radiation hard, since all NMOS transistors used can be replaced by enclosed NMOS transistors (see section 2.4). This is not possible with a PMOS amplifier because it requires a current source that can only be built with a linear NMOS. This cannot be replaced by an enclosed one due to the geometry leading to the W/L ratio.

Additionally, the shielding of the *enable* lines is improved. To save power all pads are single ended. The chip has a total size of 0.98 cm × 1.01 cm. In figure 10.12 the layout of the HitPix2 is shown.

10.2 Measurement setup

The HitPix was tested in the lab and at testbeams at HIT. A series of measurements with irradiated chips has been done, too.

For the measurements, the GECCO system from the KIT ADL group was used, developed by Felix Ehrler and Rudolf Schimassek. The GECCO system contains a PCB, firmware and software and is connected to an FPGA board with an FMC connector like the Digilent NexysVideo board. The GECCO system is presented in detail in [6] [67].

For connecting the existing system to the HitPix, an adapter PCB has been developed. The board was designed to fit for all three variants of the HitPix. The adapter PCB has a size of 5.1 cm × 5.1 cm. The main function of the adapter board is the chip fanout, its connection to the GECCO and the power delivery from the GECCO to the HitPix. Figure 10.13 shows the PCB layout. The chip has three power nets and high voltage: vdda as power for the analogue circuits (amplifiers and comparators), vddd for the digital elements (counters, adders, readout periphery) and vssa (second amplifier voltage). With the four jumpers on the left side, the power connection can be set up: vdda and vddd can be shorted on the PCB to vdd, then only the two voltages vssa and vdd are needed to power the chip. This option was used in all measurements.

The chip is glued onto the adapter PCB and the pads are wire bonded, see figure 10.14.

For the testbeam at HIT the same setup as in the lab was used. In figure 10.15, the setup at HIT is shown, the beam is coming from the photographers position.

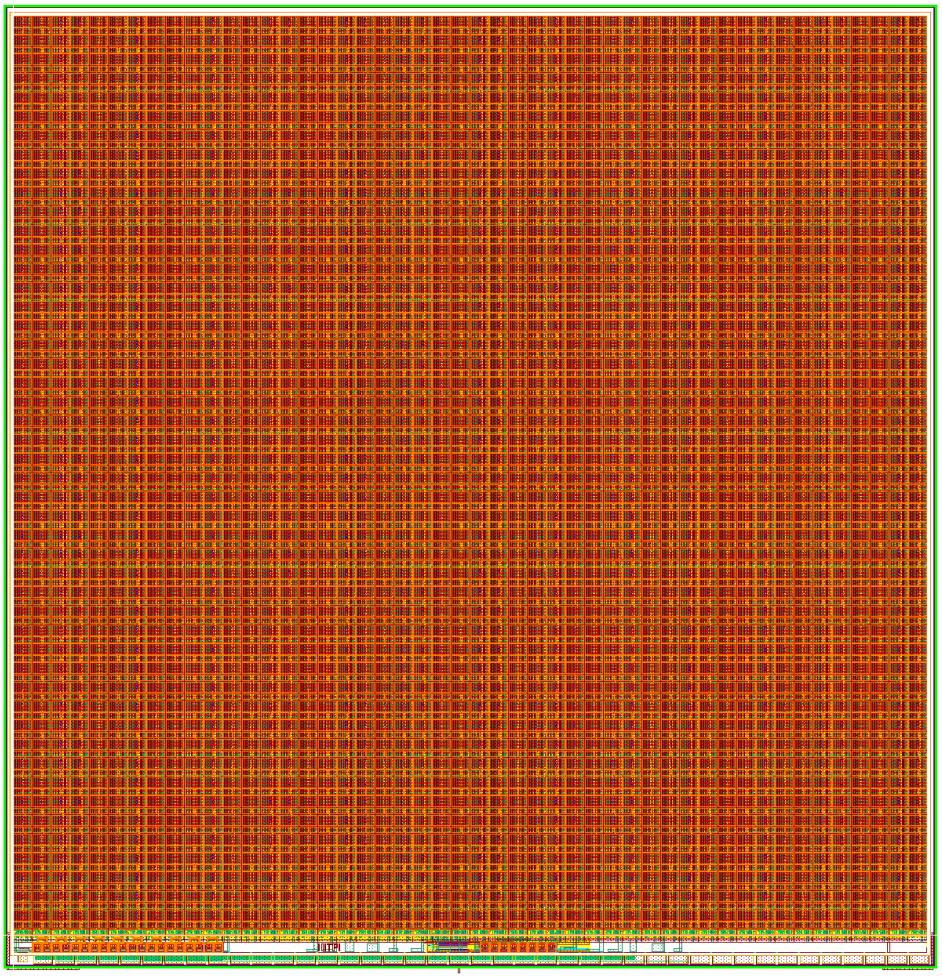

Figure 10.12: Layout of the HitPix2 with a size of 0.98 cm × 1.01 cm. The pixel matrix is shown in orange, the readout periphery is the narrow yellow-green strip at the bottom. Below this are the pads.

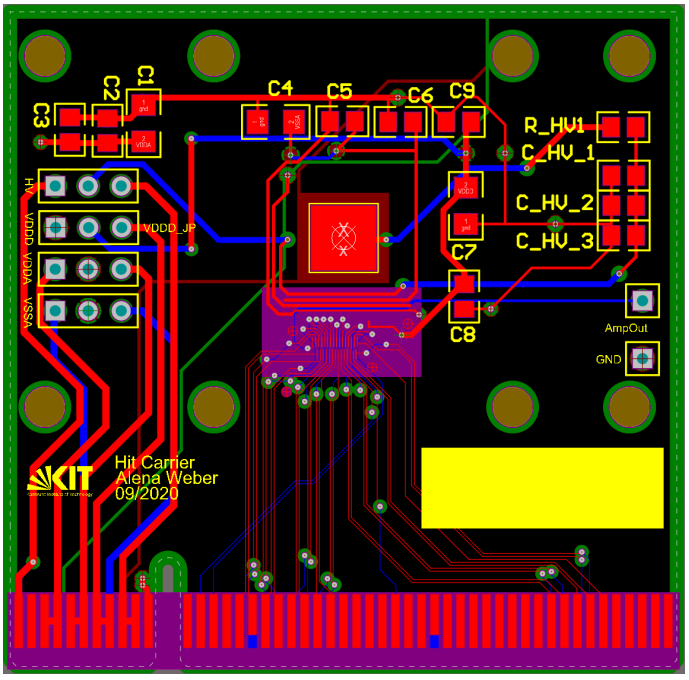

Figure 10.13: Layout of the adapter PCB, it can be used for the HitPix, the HitPix with single ended pads and for the HitPixISO. The PCB has a size of 5.1 cm × 5.1 cm.

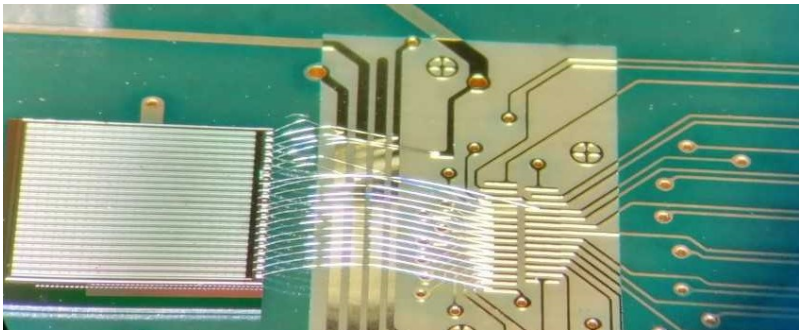

Figure 10.14: Wedge bonded HitPix.

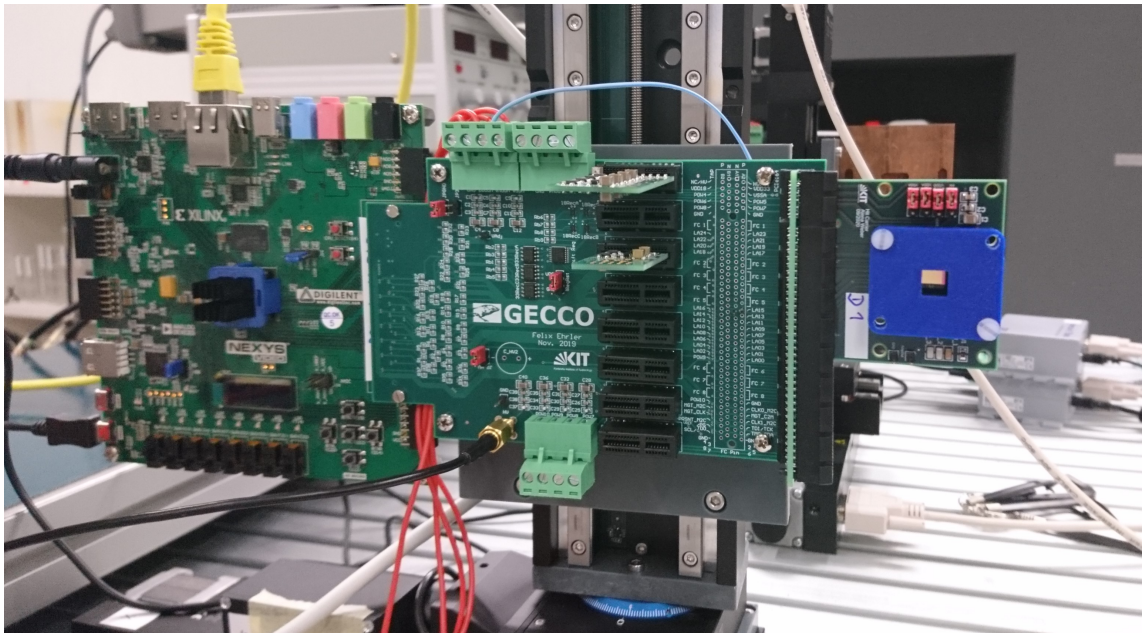

Figure 10.15: Test setup mounted on translational stages for ion beam measurements at HIT. The HitPix adapter PCB is connected to the GECCO system. The beam is coming from the photographers position. The HitPix is in the middle of the blue panel on the right side of the photo. The setup is aligned so that the HitPix is in the beam focus.

10.3 Characterisation

10.3.1 Measurements of leakage current, amplifier and mismatch of non-irradiated HitPix

Both process variants of the HitPix (standard process: HitPix, ISO process: HitPixISO) were tested in the laboratory and at testbeams.

Measurement of leakage current

By slowly increasing the high voltage (depletion voltage) and measuring the leakage current, the so called breakdown voltage of the sensor is determined. The resulting curve showing the leakage current dependence of the depletion voltage is called IV curve. At the breakdown voltage, the current starts to rise exponentially. To prevent the chip from damage, the leakage current is limited by the power supply. Figure 10.16 shows the IV curves with breakdown of one HitPix in the standard process and of one with ISO pixels. Both measurements were done at a constant temperature of 20°C.

Measurements of amplifier with ^{55}Fe

The functionality of the amplifier can be tested with a ^{55}Fe source. The emitted X-rays have the advantage of having a well defined energy of 5.9 keV. If such a photon is stopped in

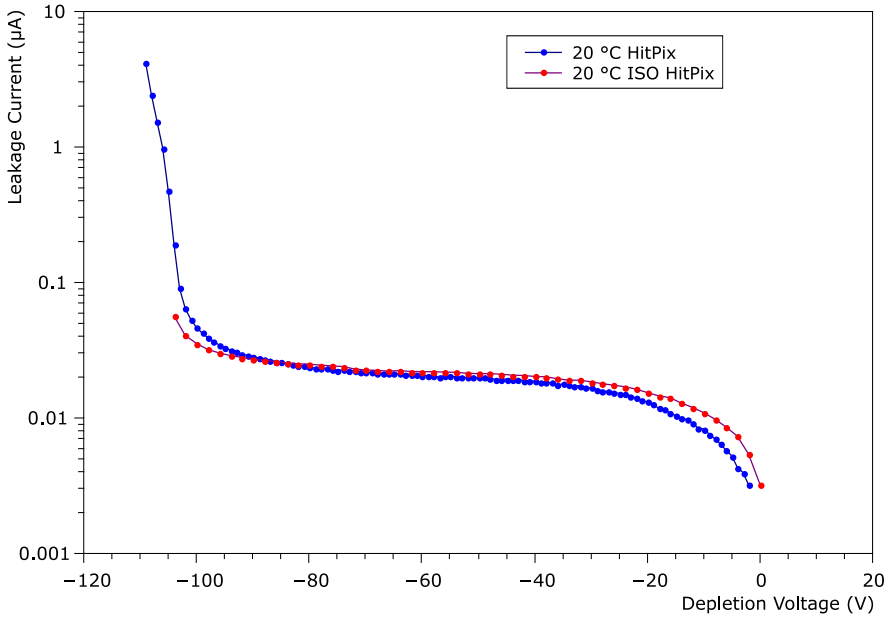

Figure 10.16: IV curves measured for the HitPix in blue (produced in the standard process) and for the HitPixISO in red. The behaviour is similar, the breakdown voltage is below -100 V for both.

silicon, it generates 1639 electron-hole pairs. The output voltage of one selectable amplifier is connected via an analogue buffer to a pad. With this pad, the amplifier output can be monitored directly before the signal is forwarded to the comparator and the counters. The amplifier output waveforms are measured with an oscilloscope and then analysed offline. The amplitudes of the signals of the amplifier output are then filled in a histogram. The expected shape of the histogram is Gaussian due to several uncertainties: the largest is the noise of the amplifier, smaller contributions are due to the uncertainties in charge generation and charge collection.

Figure 10.17 shows the signal height distribution of a signal generated by an ^{55}Fe source at 20°C. From the applied Gaussian fit the signal height is 17,81 mV $\pm 2.63 \cdot 10^{-7}$ mV.

Calibration of the charge injection

The charge injections can be calibrated in e^- by a combination of the ^{55}Fe measurement and a scan of the injection voltage.

Negative voltage pulses can be injected individually in each pixel by the GECCO setup. The properties of the injections like number of injections, injection voltage and injection speed can be controlled with the GECCO user interface (UI) of the GECCO software.

Changing the injection voltage in the UI and measuring the corresponding amplitudes at the amplifier output leads to figure 10.18. For the following approximation, the relation

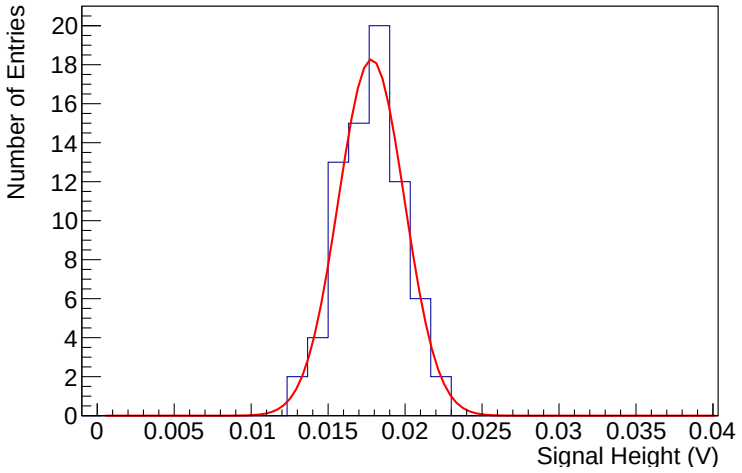

Figure 10.17: Signal height of signals from ^{55}Fe source at 20°C, measured with the HitPix at a depletion voltage of -30 V.

is assumed to be linear for the lower injection voltages. Each pulse height distribution is compared to the amplitude generated by the ^{55}Fe source. An injection voltage of 99 mV leads to the same signal height as ^{55}Fe. With this, the injection voltages can be related to an approximated number of electrons.

$$\begin{aligned} Q(^{55}\mathrm{Fe}) &= 1639\, e^- \\ U_{AmpOut}(^{55}\mathrm{Fe}) &= U_{AmpOut}(U_{Inj} = 0.099\, V) \\ Q(U_{Inj}) &= \frac{1639\, e^-}{0.099\, V} \cdot U_{Inj} \\ Q(U_{Inj}) &= 16555.56\, \frac{e^-}{V} \cdot U_{Inj} \end{aligned} \tag{10.1}$$

Measurements of amplifier with ^{90}Sr

A similar measurement to the ^{55}Fe measurement can be done with a ^{90}Sr source emitting β^- rays with an energy of 0.546 MeV. Here, the measured signals are higher allowing a comparison of the correlation of the signal height and length of the HitPix and the HitPixISO.

The signal height and length of the amplifier output signals are shown in figure 10.19. Out of this, the correlation of the height and length can be plotted, see figure 10.20.

This correlation can be compared with the one of the ISO variant of the chip in figure 10.21. It can be seen that with the ISO variant the signal height is clearly lower. The same amplifier is used for HitPix and HitPixISO. However, the two variants differ in their active pixel sizes. The active pixel size determines the pixel capacitance. Therefore, the

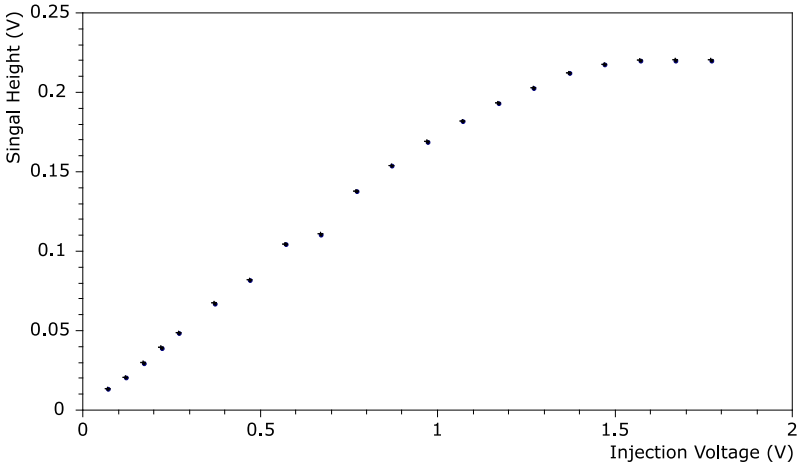

Figure 10.18: Measurement of the signal height for different injection voltages for the charge injection circuit of the GECCO setup. The depletion voltage was -30 V as for the ^{55}Fe measurement.

HitPixISO has a higher pixel capacitance compared to the HitPix because the ISO process allows for a 100 % fill factor. The pixel capacitance influences the amplification. With a higher capacitance, the amplification of the same amplifier is lower. This explains why the signals from the ^{55}Fe source are only seen by the HitPix and not by the HitPixISO: the amplification is not high enough to detect these signals.

All measurements were done with the same depletion voltage of -30 V. This is important to guarantee that the results are comparable because the signal height is also dependent on the thickness of the depletion layer, as the measurement in figure 10.22 shows.

Baseline noise

The baseline noise can be measured by an oscilloscope histogramming the amplifier output voltage. The shape of the histograms can be assumed to be Gaussian.

For the HitPix, the fitting algorithm delivers a noise sigma of 1.99 mV $\pm$ 0.03 mV. According to the calibration with ^{55}Fe, this corresponds to a charge equivalent noise of 183 electrons. For ^{55}Fe signals, the signal-to-noise ratio (SNR) would be 18, for ^{90}Sr signals, it would be 18. The small SNR for the ^{55}Fe signals explains again, why they are not detectable with the HitPixISO with its smaller amplification. It has to be mentioned that the HitPix is designed for the large signals at HIT, the small ^{55}Fe signals are not the expected use-case. Figure 10.23 shows the histogram plot. Figure 10.24 shows the same plot for the HitPixISO.

Efficiency S-curves for mismatch measurement

Although all pixels and circuits are designed exactly the same, there are differences between the transistors due to production imperfections. These differences in transistor characteristics are called mismatch [14][87] [88].

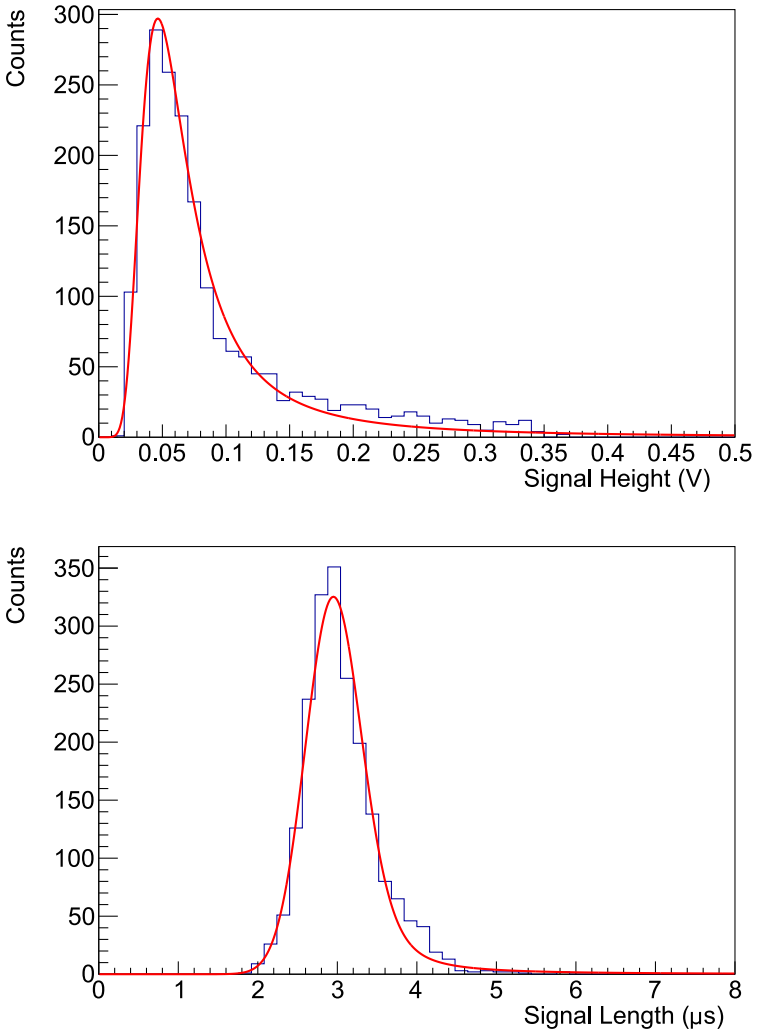

Figure 10.19: Measurement with the HitPix of the signal height and length for signals emitted by a ^{90}Sr source at a depletion voltage of -30 V.

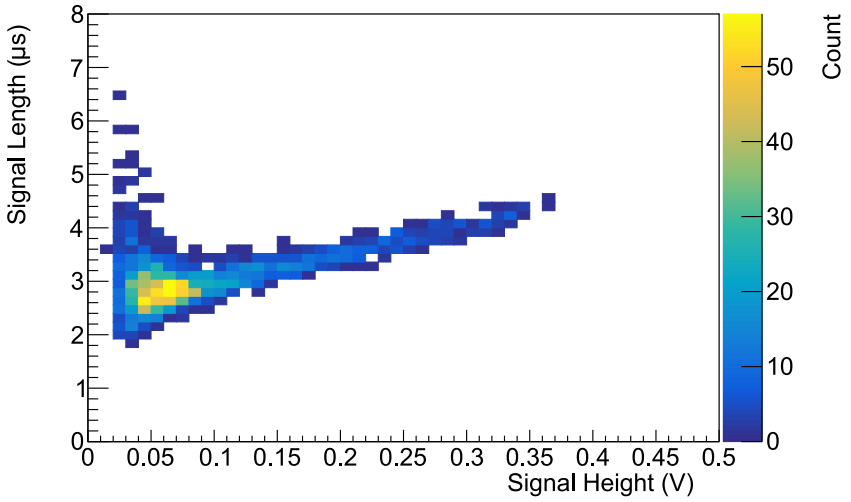

Figure 10.20: Correlation of signal height and length for signals emitted by a ^{90}Sr source, measured with the HitPix and a depletion voltage of -30 V.

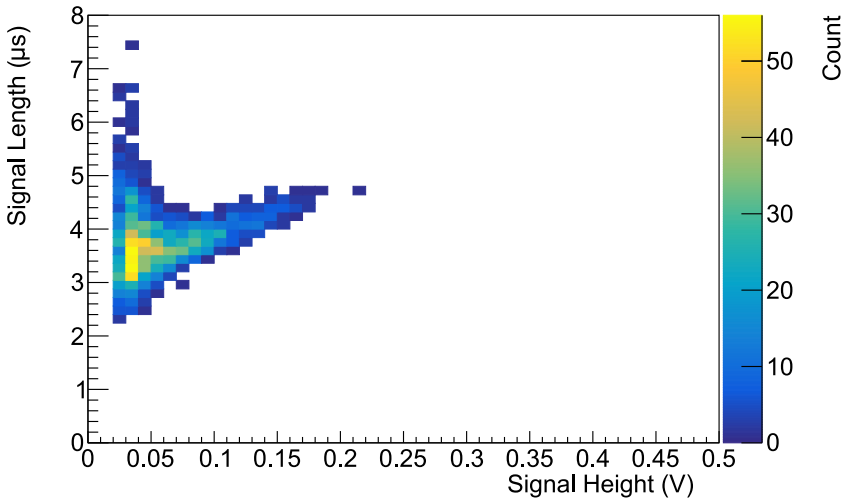

Figure 10.21: Correlation of the signal height and length of the HitPixISO for signals emitted by a ^{90}Sr source at a depletion voltage of -30 V.

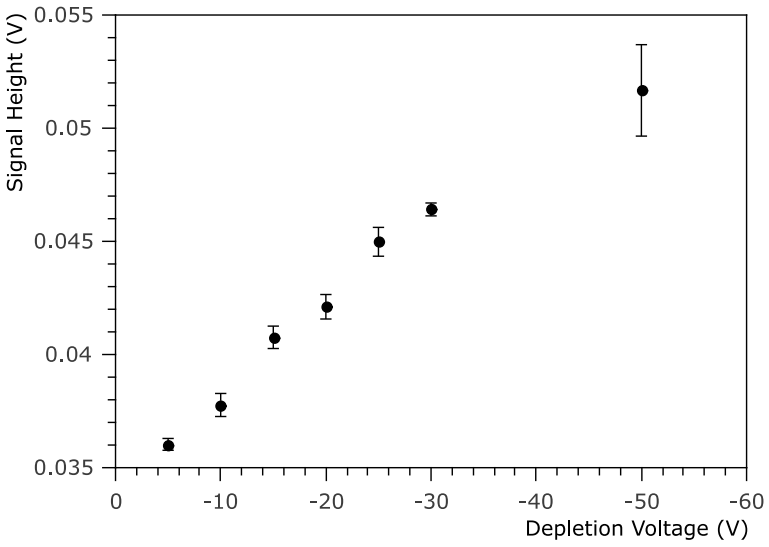

Figure 10.22: Influence of the depletion voltage on the signal height of the amplifier output of the HitPix measured with ^{90}Sr.

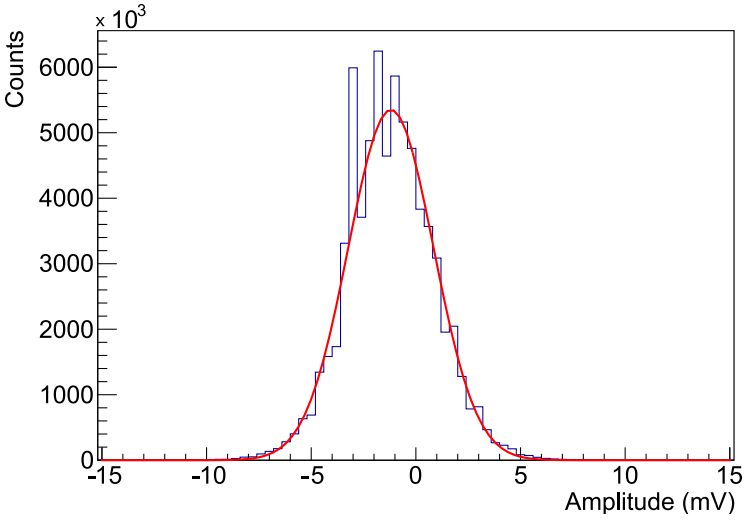

Figure 10.23: Histogram of the baseline noise of the HitPix, the noise sigma is 1.99 mV $\pm$ 0.03 mV.

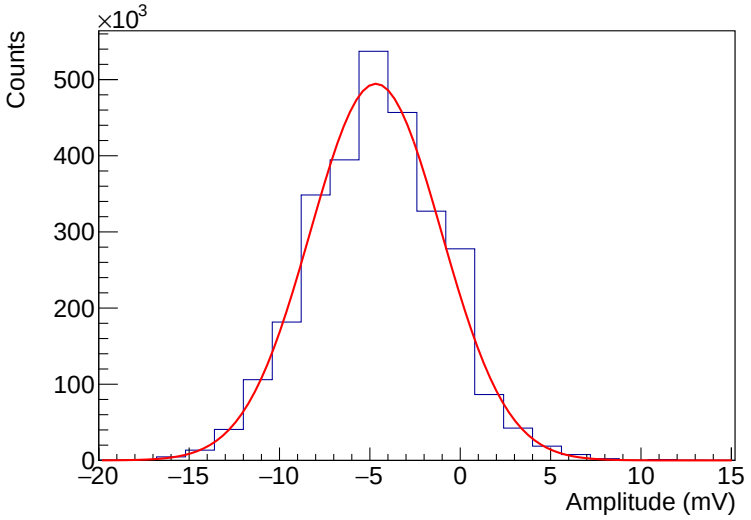

Figure 10.24: Histogram of the baseline noise of the HitPixISO, the noise sigma is 3.64 mV ± 0.03 mV.

Due to mismatch, the pixel matrix does not behave uniformly regarding detection threshold and noise. By measuring efficiency S-curves (also called test pulse detection probability S-curves) the mismatch of the chip can be determined. In a pixel, several test signals of a certain charge are injected here 100 injections were made in one pixel by the GECCO system. With the data read out from the HitPix, the detection efficiency for this injection is calculated. The measurement starts with a low injection voltage, where no signals can be detected, then the injection voltage is gradually increased until a voltage is reached at which all signals can be detected. With this an efficiency S-curve, as shown in figure 10.25, can be drawn, showing the efficiency over the injection voltage. If there was no noise in the system, the S-curve would be a step function. The noise leads to a smeared out step described by the Gaussian error function. The width of the S-curve is a measure for the noise. The point where 50 % of the total signal amount is detected is called detection threshold.

Without mismatch the S-curves of all pixels in the matrix would be identical, but due to mismatch they are shifted relatively to each other. The noise is not uniform and they do not have the same width.

The detection threshold for each pixel is shown in figure 10.26, while figure 10.27 shows the noise map determined by the width of the S-curves. In the figures 10.28 and 10.29 the histograms of the threshold and noise is shown. The observed differences in threshold voltages is, for the application at HIT, not critical. The signals there are all well above this voltage, the observed threshold variations at individual pixels will not affect the measurements at the HIT. Overall, the matrix has a reasonably uniform behaviour even with mismatch.

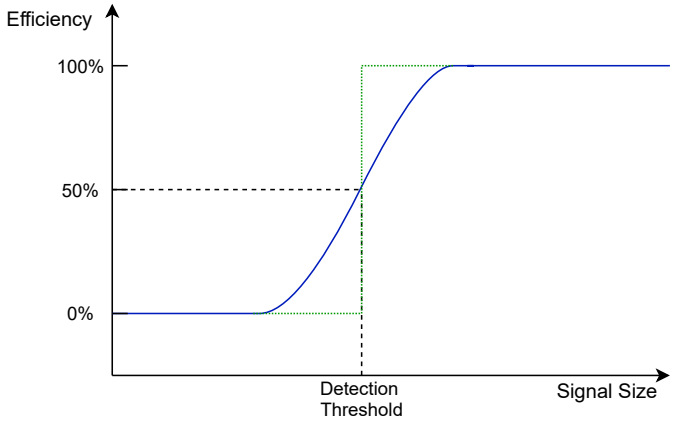

Figure 10.25: Efficiency S-curve showing the detection efficiency for different injection voltages. The detection voltage is defined as point where 50 % of the generated signals are detected.

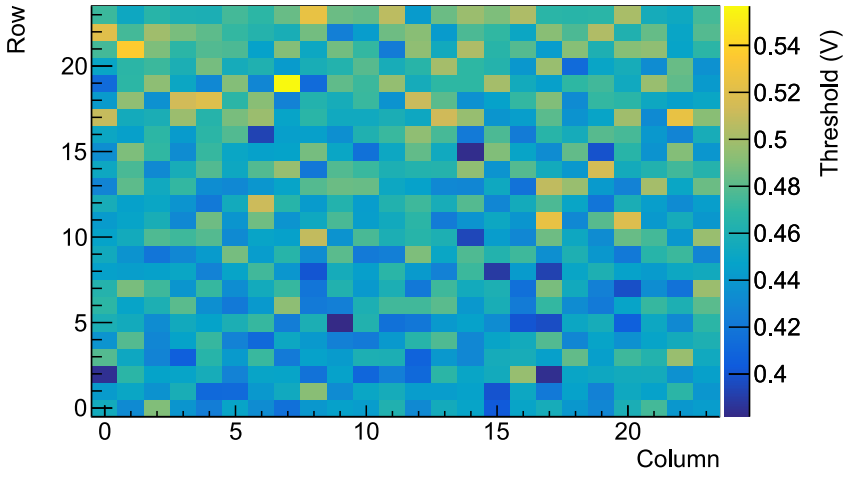

Figure 10.26: Detection threshold map at 20 °C for the HitPix, as a result of measuring the efficiency S-curves.

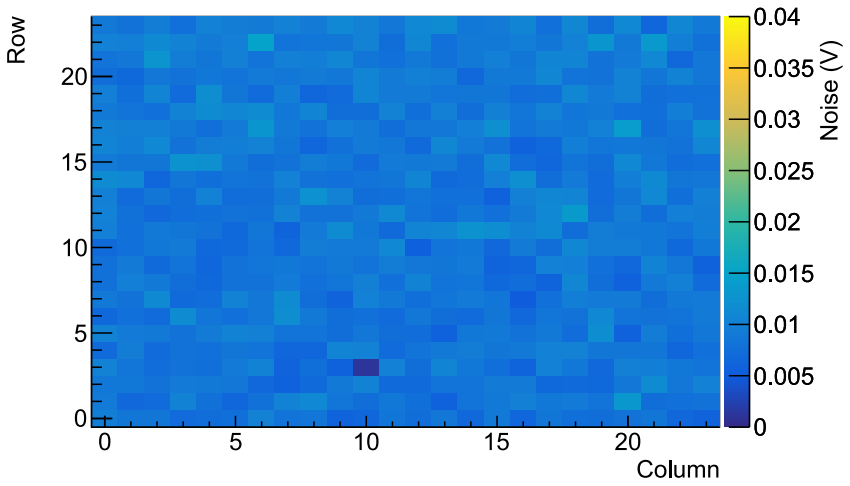

Figure 10.27: Noise map at 20 °C of the HitPix based on the transition width of the measured efficiency S-curves.

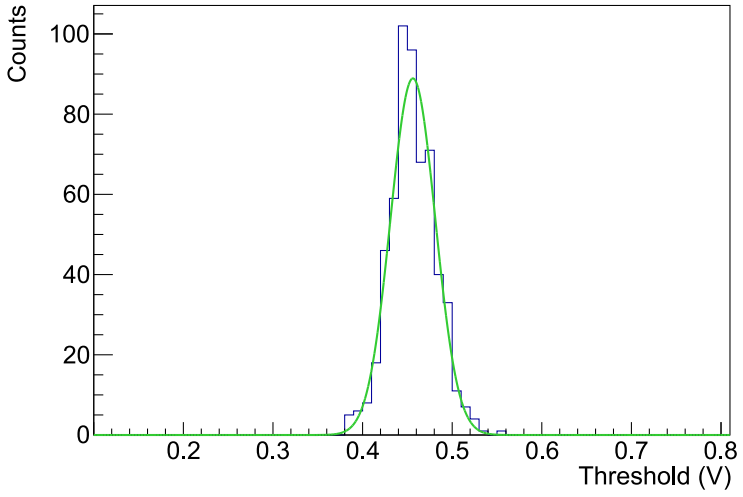

Figure 10.28: Histogram of the detection thresholds at 20 °C for the HitPix.

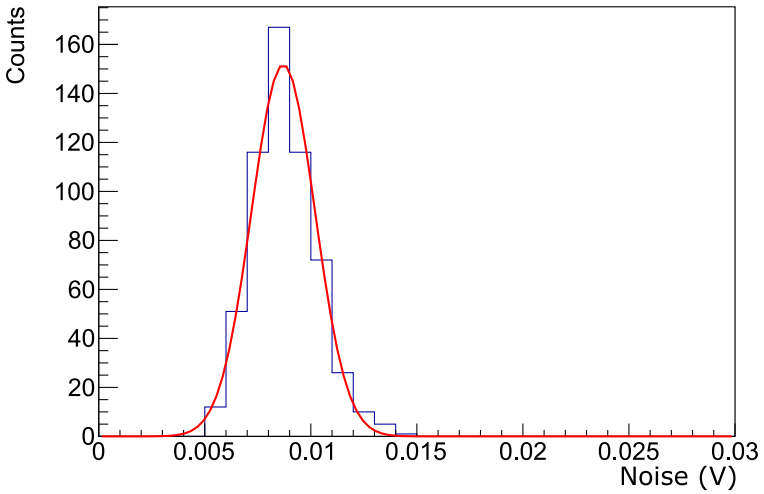

Figure 10.29: Histogram of the noise at 20 °C for the HitPix.

Table 10.1: Overview of the irradiated HitPix

Variant	Irradiation dose	Amount of sensors
Differential in- and outputs	$5.0 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$	2
	$1.1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$	2
Differential in- and outputs and ISO process	$5.0 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$	2
	$1.1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$	2
Single ended in- and outputs	$5.0 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$	2
	$1.1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$	2

10.3.2 Measurements of leakage current and amplifier of irradiated HitPix

12 chips were irradiated at KIT [89] with protons at an energy of 25 MeV. Afterwards, they were put in the freezer to prevent annealing processes. Table 10.1 shows an overview of the irradiated chips. For gluing to the PCB and bonding, the chips were defrosted for half a day and then again cooled down to - 40 °C. For the measurement, the setup was put into a climate chamber. After finishing the measurements with one chip, it was stored at - 40 °C again.

Measurement of the leakage current

The leakage current of the HitPix at the two doses was measured as a function of the depletion voltage. Due to the irradiation damage, the leakage current is expected to be higher than before irradiation. Furthermore, the leakage current should decrease with lower temperatures. The irradiation can also influence the breakdown voltage of the sensor. The

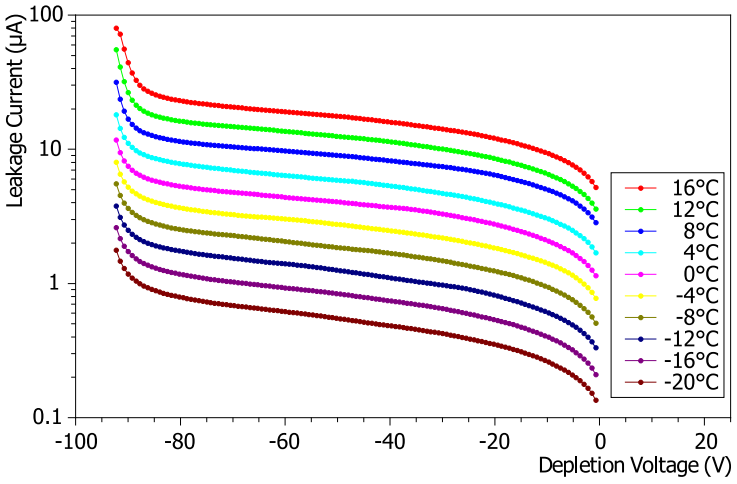

Figure 10.30: IV curves of the HitPix irradiated with 25 MeV protons to $5 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$ for different temperatures.

measurements were done in a climate chamber and the temperature was gradually reduced by 4 K at a time from room temperature down to - 20°C.

Comparing figure 10.30 and figure 10.31, one can see that the overall behaviour of the leakage current is quite similar for both doses. The leakage current increases with the dose and is, regarding figure 10.16, higher than the non irradiated ASIC. As expected, the leakage current decreases with lower temperatures, but even at -20°C, it is still significantly higher than for the non irradiated sensors.

Measurements amplifier with ^{55}Fe

With the HitPix irradiated to $5 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$, the signals of a ^{55}Fe source were recorded. To reduce the leakage current and the baseline noise, the sensor was cooled down to -20°C. From the measurement with the non irradiated sensor it is known that the ^{55}Fe signals are small. But even with the irradiated sensor, the ^{55}Fe signals could be identified, as figure 10.32 shows. For the non irradiated HitPix the signal height was 17.81 mV $\pm 2,63 \cdot 10^{-7}$ mV, for the irradiated one it is 19.27 mV $\pm 1,42 \cdot 10^{-4}$ mV. This shows that the amplifier is still working after the irradiation.

Baseline noise

The noise of the baseline was measured before irradiation at 20°C: 1.99 mV $\pm\, 3.1 \cdot 10^{-2}$ mV. Due to irradiation damage, the noise should increase and then decrease with temperature. Therefore, for the irradiated sensors, the baseline noise was measured at different temperatures, see figure 10.33 and figure 10.34. As expected the noise increased in comparison to the non irradiated one. Comparing the two irradiated chips, the higher irradiated one also shows a higher noise level. Due to the higher baseline noise small signals are more difficult to be detected. This leads to a decreased SNR for the irradiated sensors.

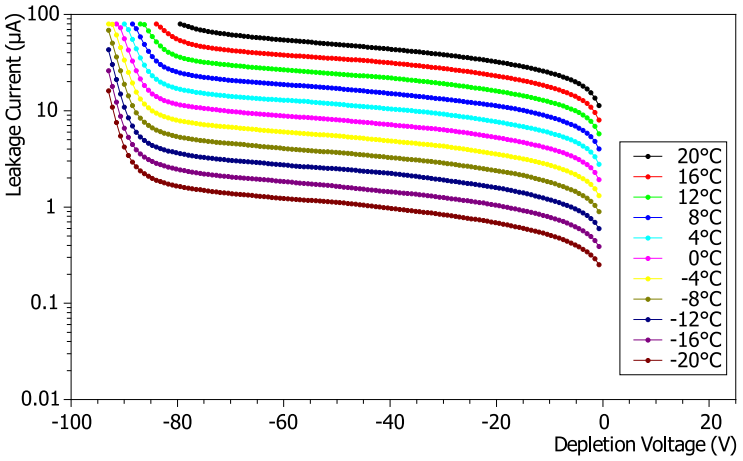

Figure 10.31: IV curves of the HitPix irradiated with 25 MeV protons and $1.1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ for different temperatures.

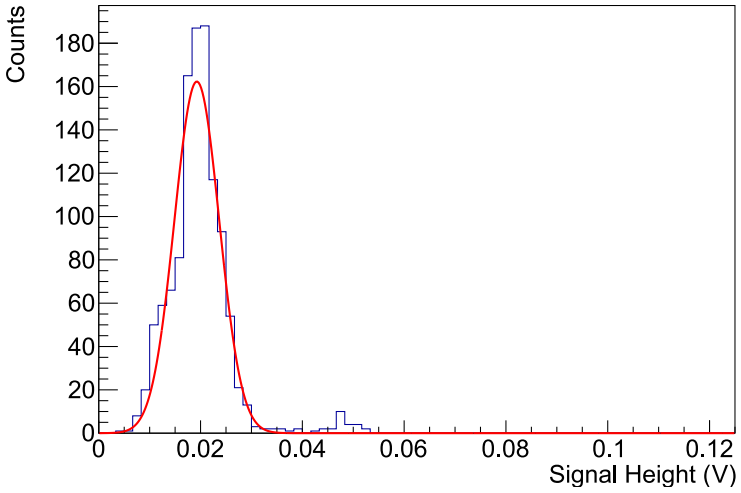

Figure 10.32: Measurement of the signals of a ^{55}Fe source at -20°C with a HitPix irradiated with $5 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$ with 25 MeV protons. The signal height is 19,27 mV $\pm\, 1,42 \cdot 10^{-4}$ mV.

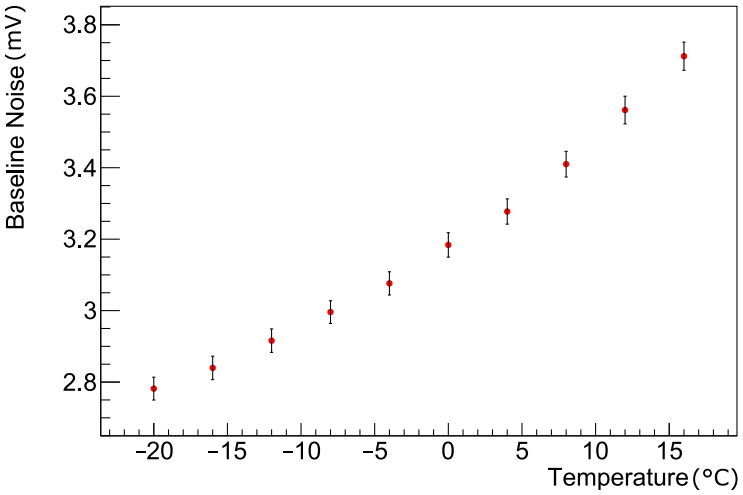

Figure 10.33: Baseline noise of the HitPix irradiated with 25 MeV protons to $5 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$ for different temperatures. For the non irradiated chip the baseline noise at 20 °C was $1.99\,\mathrm{mV} \pm 3.1 \cdot 10^{-2}\,\mathrm{mV}$.

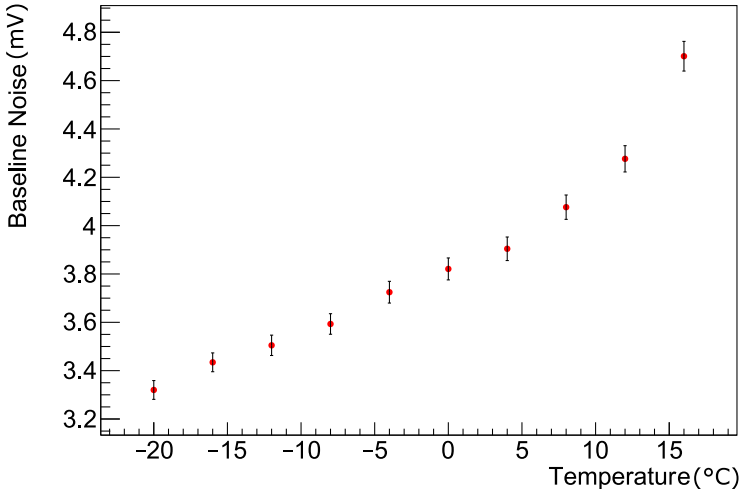

Figure 10.34: Baseline noise of the HitPix irradiated with 25 MeV protons to $1.1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ for different temperatures.

The measurements of the irradiated chips all show the expected results. It can be confirmed that the chips are still fully functional, despite the increased leakage current and baseline noise. The small iron signals could still be identified after irradiation with cooling. To verify that the chips still deliver the required results after irradiation, a beam test was carried out at the HIT. This confirmed that the chips were noisier but still functional. It should be noted that these were homogeneously irradiated chips. However, if the chips are used as beam monitors at the HIT, there will also be inhomogeneous radiation damage.

10.3.3 Testbeam measurements of counter and adder modes of non-irradiated HitPix

In two beam tests at HIT Heidelberg the functionality of the HitPix and the fulfilment of the chip's requirements were tested. The first testbeam took place in December 2020 and the second in April 2021. In the first, the focus was on the functionality of the HitPix directly in the beam, with different beam settings with proton and carbon ion beams. In the second testbeam, additionally irradiated samples were measured in the beam.

Measurements of counter mode

Exemplary hit maps and their projections for carbon ions and protons are presented. First for the non-irradiated samples the measurements of the counter and adder mode are shown. At the end, the first results of measurements with irradiated sensors are shown.

The following results are from a beam with $2{\cdot}10^6$ carbon ions/s at an energy of 396.29 MeV/u with three spills. At HIT the beam sends particles in spills of several seconds length followed by a several seconds break. The energy, intensity and focus of the particles can be configured.

Figure 10.35 shows the counts in pixel (12/12), in the middle of the matrix. The three spills can be identified and the counting rate in each spill is similar. Furthermore, the pixel does not count hits in between the spills. Hence, the pixel is counting as expected.

In figure 10.36, the hitmap of the HitPix after three spills is shown. The beam spot is clearly and sharply recorded. The beam spot is not exactly in the middle, slightly shifted to the left. The whole chip is inside the beam. For the beam monitor system, several large chips will be needed to record the beam including the tails. In the time between the spills, without beam, almost no hits are counted, see figure 10.37.

Out of the data from the hitmap in figure 10.36, the column (figure 10.38) and row projections (figure 10.39) can be computed. The beam center is around column 9. At the beam spot, most counts are measured. On the sides of the spot the counts are decreasing but not until zero, because the beam is larger than the chip, there are still many hits at

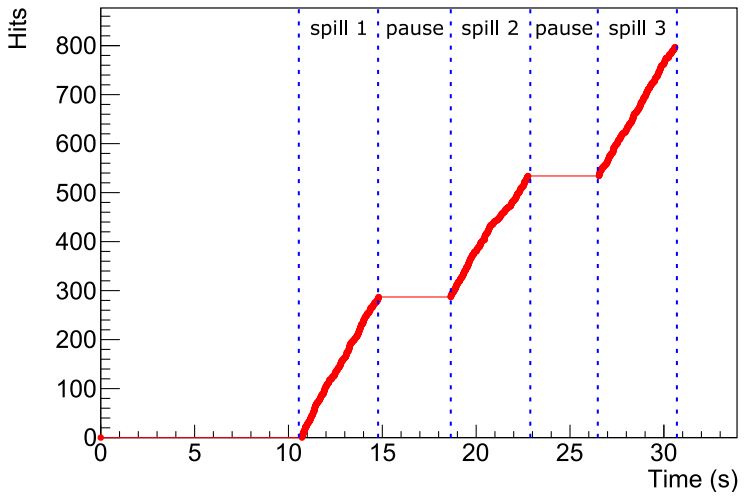

Figure 10.35: Hits in one pixel in the middle of the matrix (12/12). The beam was split in three spills as one can see form the counts. Between the spills, no hit is recorded. The beam was with carbon ions with an energy of 396.29 MeV/u and $2 \cdot 10^6$ ions/s.

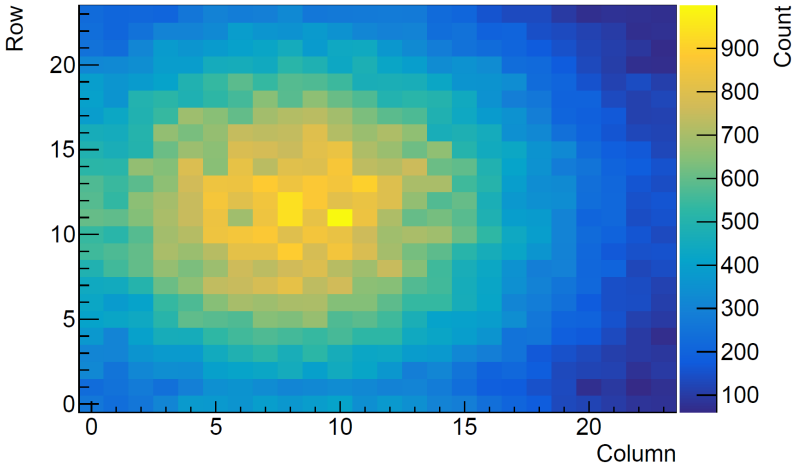

Figure 10.36: Hit map for $2 \cdot 10^6$ carbon ions/s at an energy of 396.29 MeV/u. The beam spot is clearly visible.

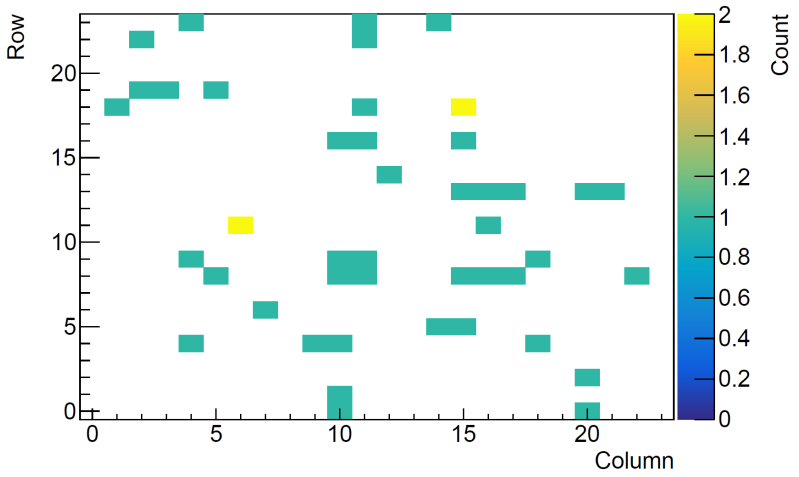

Figure 10.37: Hit map of the time without beam (time between the beam spills) of the measurement with $2 \cdot 10^6$ carbon ions/s at an energy of 396.29 MeV/u.

the chip edges. The column projection is the same as the on-chip column projection done by the adders, while a row projection is not implemented on the HitPix. From the row projection one can see that the maximum of the counts is quite in the middle of the HitPix. To get a 2D beam projection in the final version of the HitPix additional adders for row summation will be required, giving the same result on chip like the off-chip row projection. The projections in figure 10.38 and figure 10.39 show that one can get a beam profile from the counting value data.

The HitPixISO was tested at the HIT testbeam, too. It was shown that also the ISO variant is working in the beam and records a hit map of the beam, see figure 10.40.

Out of the measurements presented in figures 10.35 to 10.40, it was shown that the HitPix is working as expected and can handle the high rates in the beam at HIT. Also it was demonstrated that the counting mode records hit maps as needed to quickly depict beam profiles. This was confirmed with the projections in row and column direction (as the results are form the counter mode, the projections were done in the software), showing the both projections are enough to monitor the beam structure. This will be checked in the next part, showing the results of the adder mode, that gives the on-chip column projection without hit map.

Measurements of adder mode

During the beam test at HIT the adder mode of the HitPix was tested, too. Here, instead of the hits in every pixel, only the value of the last adder in each column is read out, returning the sum of the hits in this column. The adder readout mode is faster than the single pixel readout and shows the column projection directly . For the adder only one readout cycle is needed instead of 24 cycles as the counter values.

The figures 10.41 and 10.42 show the values of the column sums for a beam with $2 \cdot 10^6$ carbon ions/s at an energy of 368.21 MeV/u. The beam profile in figure 10.41 displays a slight

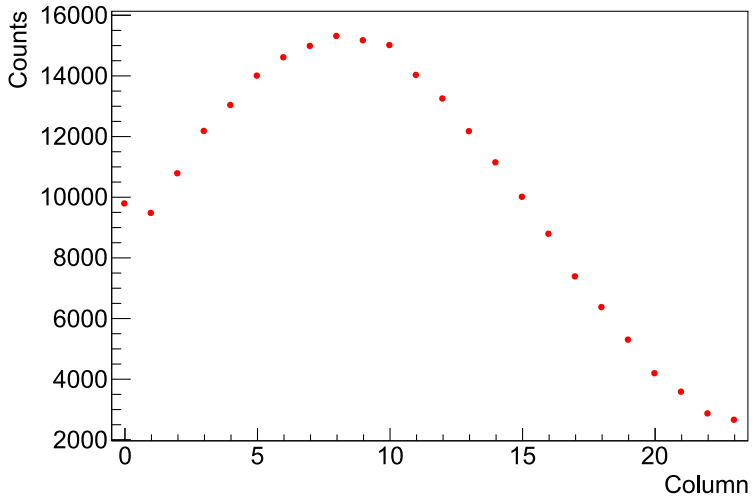

Figure 10.38: Column projection done off-chip with the counter data from 10.36. The result is a beam profile as generated by the adders on-chip. The value of the first and last column is higher, because the pixels in these rows collect additional charge from the region outside the pixel matrix.

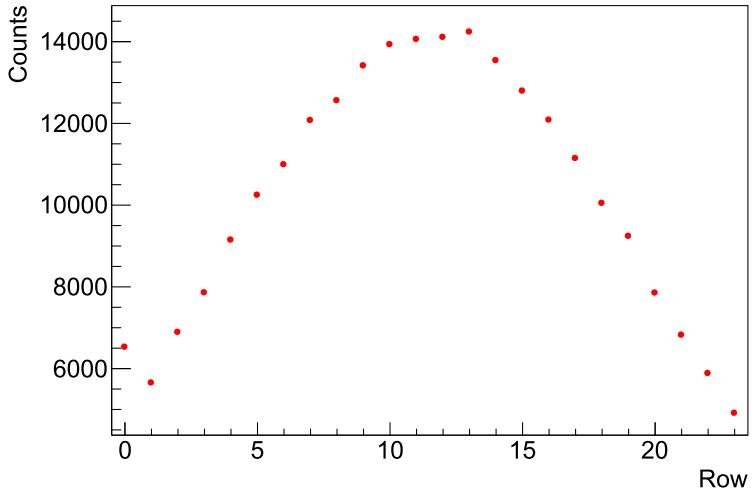

Figure 10.39: Row projection done off-chip with the counter data from figure 10.36. This is not implemented on-chip but planned for a later version of the HitPix.

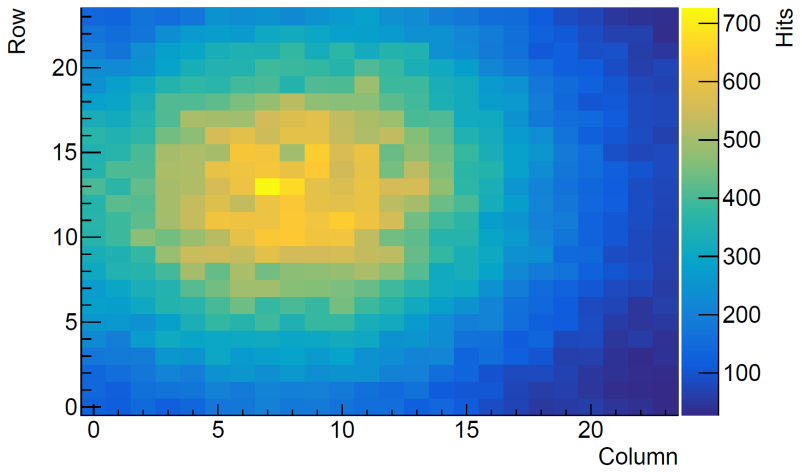

Figure 10.40: Hit map measured with the HitPixISO for $2 \cdot 10^6$ carbon ions/s at an energy of 430.10 MeV/u. The beam centre is visible.

shift of the beam centre to the left. To the right and left of the centre point, the number of hits in each column decreases uniformly. This can be compared to the column projection done offline with data from the counter mode of the chip in figure 10.38. The total number of hits cannot be directly compared because of the different beam energy and different measurement durations, but the shape of the beam profile can be compared. The profile of the beam projection is similar confirming, that the adder mode is giving the column projection as required with the same results as the projection generated from the counter data. This verifies the functionality of the adder mode. In figure 10.42 the column sums are displayed with colours, highlighting the smooth and uniform decrease of hits on both sides of the beam centre.

The adder mode of the HitPix was tested with the proton beam at HIT, too. The characteristics of the proton beam are different, the beam is wider and a little blurry in comparison to the carbon beam. This is also observable in the measurement results. Figure 10.43 and figure 10.44 show the column projection once in absolute adder values and once decoded with colours for a beam with $8 \cdot 10^7$ protons/s at an energy of 217.87 MeV/u. The beam profile is recognisable, but overall rather blurred. As in the measurement with the carbon ions, the maximum is due to the position of the setup shifted to the left. The maximum is wide and only on the right side the decrease of the counting rate is visible.

10.3.4 Testbeam measurements of counter mode of irradiated HitPix

The irradiated samples were measured in beam tests at the HIT. The sensors were operated at room temperature without cooling. Figures 10.45, 10.46 and 10.47 show the results for the measurement of a sensor irradiated with 25 MeV protons to $5 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$. The beam settings were $3 \cdot 10^6$ carbon ions/s at an energy of 430,10 MeV/u. The irradiated sensor

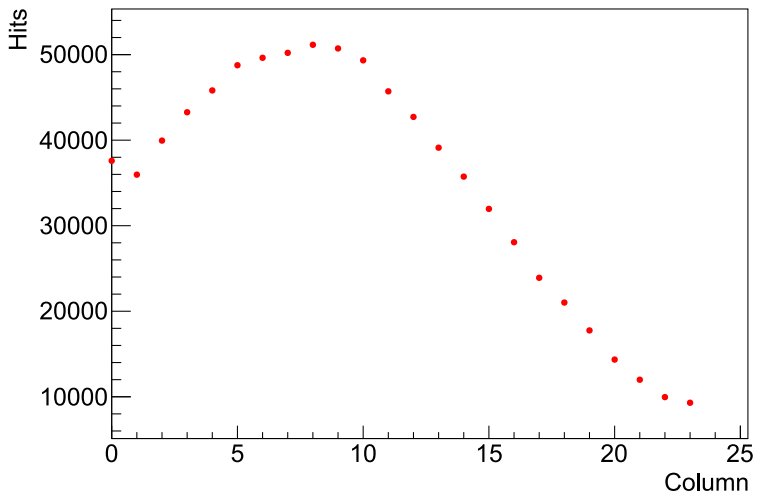

Figure 10.41: HitPix in the adder mode, the readout gives the sum of all hits for every column. The beam settings are $2 \cdot 10^6$ carbon ions/s at an energy of 368.21 MeV/u.

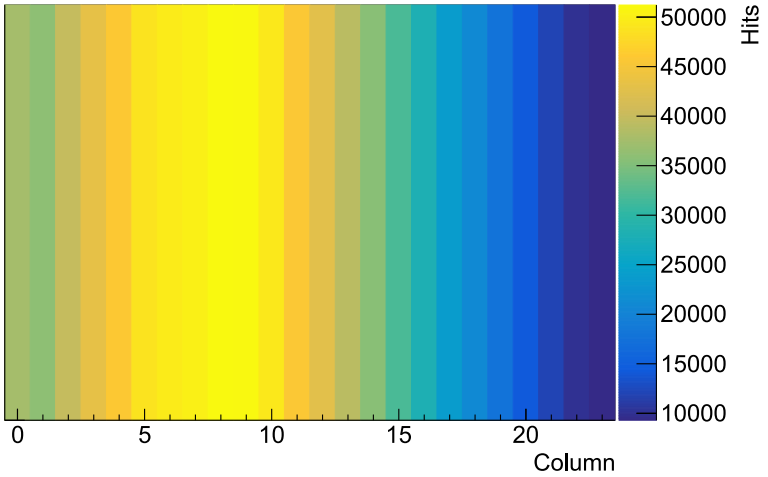

Figure 10.42: The adder values can also be plotted with colors, here again the data from figure 10.41 with $2 \cdot 10^6$ carbon ions/s at an energy of 368.21 MeV/u.

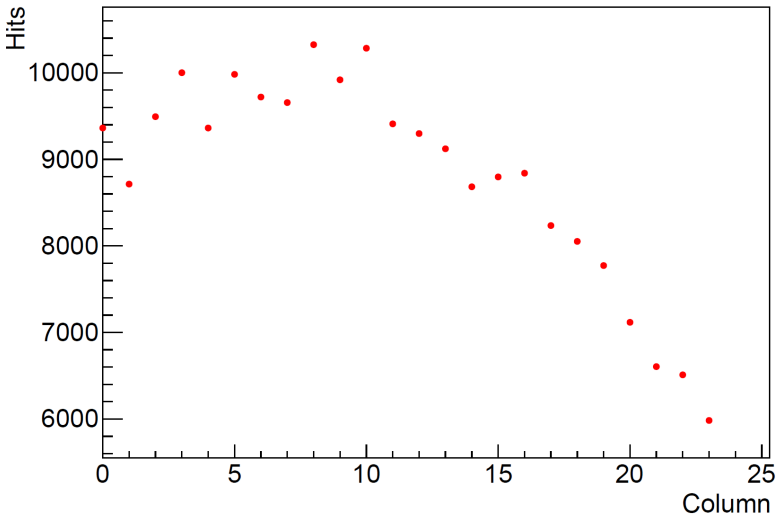

Figure 10.43: HitPix in the adder mode, the readout gives the sum of all hits for every column. The beam settings are $8{\cdot}10^7$ protons/s at an energy of 217.87 MeV/u. The proton beam spot is not as sharp and narrow as the carbon beam spot, which is no effect of the HitPix, it is a property of the beam.

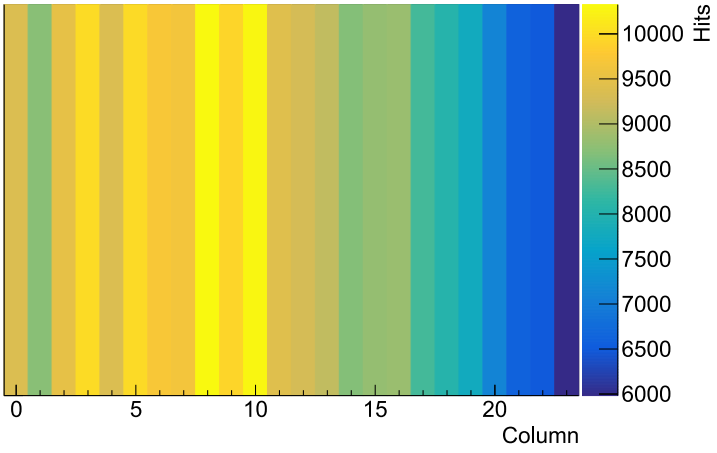

Figure 10.44: Here the column counts are plotted with colours, the proton beam has a different characteristic than the carbon ion beam. The measurement here was done with $8 \cdot 10^7$ protons/s at an energy of 217.87 MeV/u.

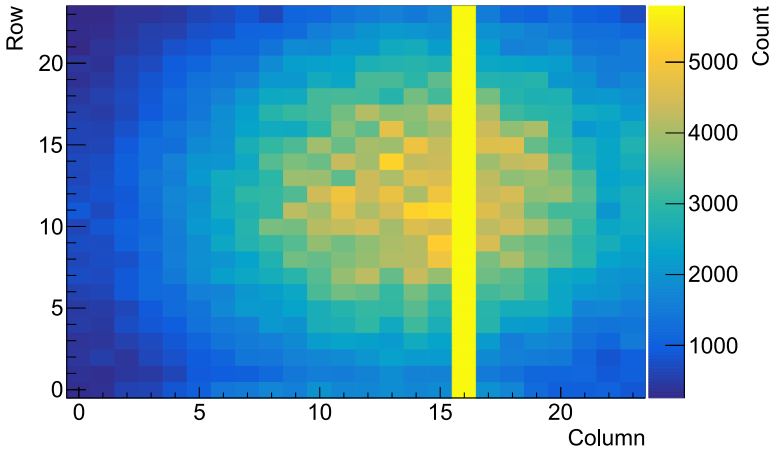

Figure 10.45: Hit map measured with the HitPix irradiated with 25 MeV protons to $5 \cdot 10^{14}\,n_{eq}/cm^2$ for $3 \cdot 10^6$ carbon ions/s at an energy of 430.10 MeV/u. The beam spot is clearly visible. The counting scale was adapted to the counting rates of the matrix without column 16. Column 16 is significantly more sensitive than the other columns, see figure 10.46. This behaviour is most likely a production-related property of this sensor and not due to irradiation.

operated at the HIT with the same settings as for the measurements in the laboratory in section 10.3.2.

The beam spot is visible, see figure 10.45. Here the counting scale was adapted to the counting rates of the matrix without column 16. In figure 10.46 the same plot but with the scale adapted to column 16 is shown. In the previous plot, one could think that column 16 is noisy, but this plot shows that it also maps the beam well. However, this column is much more sensitive than the others. Therefore, it has a much higher count rate. The sensor probably already had this property before irradiation.

The counts between spills are shown on a map, see figure 10.47. Only few hits were recorded in the pauses between the beam spills. These are due to noise. The sum of noise hits is comparable to that of an unirradiated sensor.

During the tests at the HIT Heidelberg, the functionality of the counter and the adding modes of the HitPix and the HitPixISO were tested in the beam and in the environment at HIT. The measurements were performed at different beam settings in terms of particle type, energy and intensity. Both hit maps and column projections were generated, allowing beam profiles to be recorded as expected. The irradiated sensors were tested without cooling at the HIT and show the beam spot on the hit maps as the non-irradiated sensors.

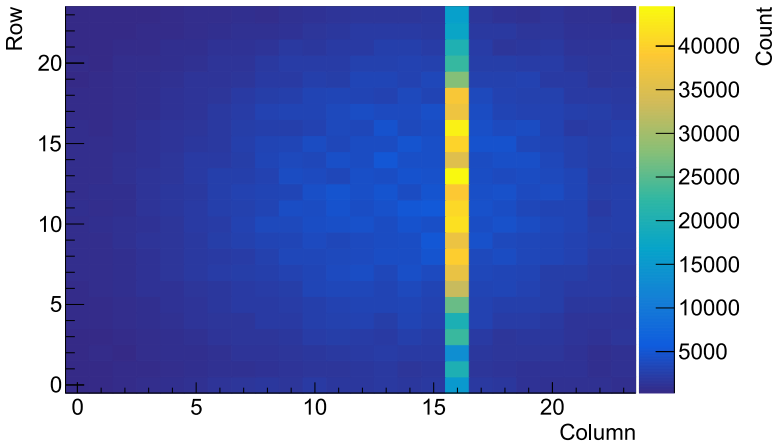

Figure 10.46: The same hit map measured with the HitPix irradiated with 25 MeV protons to $5 \cdot 10^{14}\,n_{eq}/cm^2$ for $3 \cdot 10^6$ carbon ions/s at an energy of 430.10 MeV/u as in figure 10.45. The counting scale was adapted to the counting rates of column 16. Column 16 is clearly more sensitive than the other columns.It can be seen that the column is not noisy, it images the beam like all other columns, only with much higher count rates.

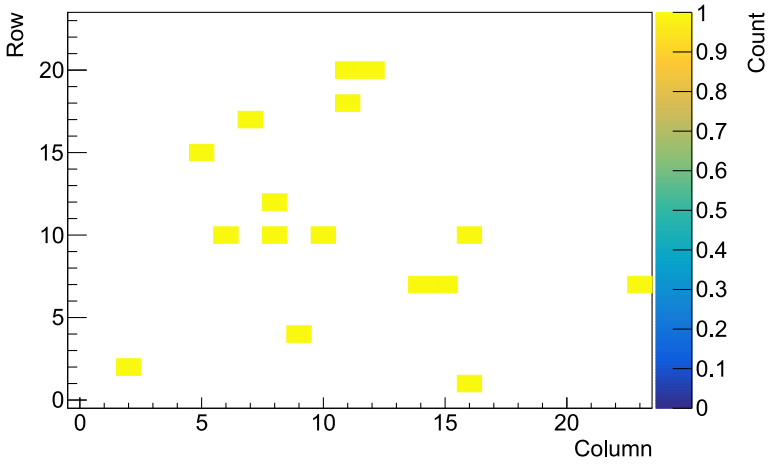

Figure 10.47: The map shows the counts of the measurement between the spills from the measurement shown in figure 10.45. The sensor has only a few noise hits despite irradiation and without cooling.

Part IV

Summary and conclusion

Particle detection is a core task in particle physics experiments and in particle therapy.

In order to discover new physics beyond the Standard Model of particle physics, new experiments are continuously planned and built to run with increasing resolution and at higher rates. Therefore, future particle detectors will have to meet increasingly high demands. Tracking detectors for the reconstruction of particle trajectories, for example, must provide high time and vertex resolution combined with high detection efficiency.

In medical physics in the field of particle therapy, reliable beam monitoring is the key to effective treatment. The radiation monitor is placed inside the beam to determine its properties and ensure safe treatment of patients with maximum effectiveness of tumour treatment and minimal damage to healthy tissue. An intelligent sensor for beam monitoring must be radiation hard, be able to handle high rates and at the same time be able to detect the beam accurately.

High Voltage Monolithic Active Pixel Sensors (HV-MAPS) are a new promising technology for the development of particle detectors. They are robust, thin, radiation hard and cost-effective. The HV-MAPS developed in this work were fabricated in a high voltage complementary metal-oxide-semiconductor (HV-CMOS) process using a triple-well structure. HV-CMOS sensors have fast charge collection, allow a high fill factor and enable the implementation of complex logic using CMOS circuits.

The focus of the thesis was to investigate the suitability of HV-MAPS sensors for tracking detectors and beam monitoring and to develop sensor chips for these applications. In this work, two HV-MAPS sensor families for two applications were developed and analysed. The MuPix family is specifically designed for tracking detectors, e.g. for the Mu3e experiment, and is based on existing prototypes. The HitPix is a special sensor for beam monitoring in the field of particle therapy and was designed from scratch. The sensor is radiation hard and optimised for high rates. Another variant designed by the author is the HitPixISO, where a deep p-well is added to the triple-well structure in an extra processing step.

An HV-MAP sensor consists of a pixel matrix and a periphery for the readout, which is located at one chip edge. In each pixel there is an amplifier to increase the detected signal. A charge-sensitive PMOS amplifier is used for the MuPix, HitPix and the HitPixISO. The three chips have different active pixel sizes, which leads to different pixel capacities. These capacitances affect the amplifier's gain. A larger pixel has a larger capacitance, which leads to a lower gain. The HitPix has more than three times the pixel size compared to the MuPix. However, the resulting lower amplification is still sufficient, as in beam monitoring the signals are larger than in the tracking application of the MuPix. The HitPixISO has the largest active pixel sizes of the three sensors. The measurements at the Heidelberg Ion Therapy Centre (HIT), which were conducted in the scope of this thesis, confirmed that the amplification of the HitPix and HitPixISO is suitable.

The next step in signal processing is the comparator. If the signal is above the comparator's threshold, it is considered a hit. The pixel matrix must have a homogeneous behaviour with regard to hit detection, i.e. a hit should be detected in each pixel starting at the same signal level. Therefore, the threshold voltages of the comparators should be the same for each pixel. Due to manufacturing errors (mismatch), each comparator behaves slightly differently, which is confirmed by the measured threshold distributions. The mismatch depends on the transistor sizes. Therefore, these were optimised for minimum mismatch. The threshold variations can be further compensated by individual tuning of each comparator. This is realised in the MuPix. After tuning, the threshold distributions are narrowed and the overall threshold can be lowered.

The position of the comparator determines the fill factor of the pixel matrix and the crosstalk. A sensor has a fill factor of 100 % when the pixel matrix is fully sensitive. Crosstalk is a problem when analogue signals have to be transmitted over long lines. A signal can introduce signals via crosstalk on neighbouring lines, resulting in "ghost" hits. Three different comparator positions are realised for the designed chips. In the MuPix, the comparator is located in the periphery, which has the advantage that the pixel matrix has a fill factor of 100 %, but brings with it the problem of crosstalk. In the HitPix, the comparator is located in the pixel, separated from the sensitive pixel part, which means that no full fill factor is achievable. With the HitPixISO, an additional deep p-well is used, which makes it possible to place the comparator inside the pixel and still reach a fill factor of 100 %. In the case of beam monitoring, a full fill factor is not needed as a measurement of the relative rate is sufficient.

The sensors used for beam monitoring receive a high dose of radiation (approximately $1.3 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ for one year at HIT). This radiation causes damage to the sensor. The main damage in 180 nm sensors is leakage current, which is caused by additional channels in NMOS transistors. This can be avoided by using enclosed NMOS transistors. For the beam monitoring project, a radiation hard library was developed by the author with focus on minimal leakage currents. The library cells use only enclosed NMOS transistors, which were then used for the design of the HitPix, HitPixISO and HitPix2. The measurements carried out at the HIT showed that the sensors work without cooling for in-beam measurements after irradiation with 25 MeV protons to $5 \cdot 10^{14}\,\mathrm{n_{eq}/cm^2}$ and with 25 MeV protons to $1.1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$.

An example of a particle physics experiment that uses HV-MAPS to build its tracking detector is the Mu3e experiment at the Paul Scherrer Institute in Switzerland. Mu3e searches for the lepton flavour-violating decay of $\mu^+ \to e^+e^-e^+$ with a new and highly sensitive detector system. As part of this work, an essential part of the final prototype, the MuPix10, was developed.

There are several requirements for a sensor used in a tracking detector. It must be thin to reduce multiple scattering. For Mu3e, for example, sensors must be thinned down to

50 µm. In addition, a time resolution of less than 20 ns is needed. Spatial resolution is also important and leads to the desired pixel sizes, e.g. 80 µm × 80 µm in the case of MuPix. For high efficiency, a 100 % fill factor of the pixel matrix is required.

In the scope of this work various generations of the MuPix sensors were developed including the final prototype.

Tracking detectors require high time resolution. The time resolution is limited by the timewalk: small signal amplitudes cross the threshold voltage later than signals with large amplitude, even if they start at exactly the same time. In the readout buffer developed for the MuPix, different modes of timewalk correction are implemented, e.g. time-over-threshold or the two-threshold method. The readout of the MuPix is triggerless, this is realised by a column-drain readout architecture.

Measurements were performed for the MuPix8 concerning the tuning of the comparator threshold. The tuning leads to significantly lower threshold fluctuations across the matrix and the overall threshold can be lowered. This was confirmed by measurements of the MuPix10, which were carried out by the Mu3e group at Physikalisches Institut (PI), Heidelberg. The characterisation of the MuPix10 is conducted by Mu3e at PI with measurements in the laboratory and several testbeam campaigns. The requirements are met with a time resolution better than 10 ns, an efficiency of over 99 % and successful integration tests.

The designs described in this thesis are the final designs that will be used for the upcoming final submission of MuPix, the sensor for detector construction. With the MuPix, an HV-MAPS suitable for tracking applications has been developed. In particular, it meets all the requirements of the Mu3e experiment.

An example of a beam monitor application is the Heidelberg Ion Therapy Centre (HIT). The HIT is a university hospital therapy centre that offers particle therapy for tumour treatment. The beam monitor is placed directly in the beam, meaning that the sensors must be radiation hard, able to cope with the high rates, enable fast readout and be made of an homogeneous material. The HitPix and HitPixISO are part of a new sensor family that is used to investigate whether HV-MAPS implemented in HV-CMOS can meet the necessary requirements. These new smart sensor chips were developed entirely within the scope of this thesis.

For the development of the HitPix and HitPixISO, a radiation hard library was developed to minimise leakage current caused by radiation damage. HitPix and HitPixISO have large pixels with a size of 200 µm × 200 µm. Since the relative rate is measured, the pixel matrix does not require a 100 % fill factor, but the insensitive chip edge with the periphery needs to be as small as possible. Therefore, the special circuits for beam monitoring are placed inside the pixels. A counter for in-pixel hit counting is implemented. Furthermore, a fast projection readout is realised with an adder, distributed in each pixel, that forms the hit

sum of a column. A shift register was designed for the readout to keep the periphery as small as possible.

The measurements confirmed the dependence between amplification and pixel size described in the amplifier section above. The beam tests at the HIT showed that the sensors can cope with the high rates and that both the counter and adder modes work as expected. The beam can be detected accurately. The irradiated sensors were also measured at the HIT without cooling and were fully functional.

Studies on the use of HV-CMOS for beam monitoring in the field of particle therapy were started with the HitPix and will be continued. The results of the measurements carried out are promising and led to the development of the HitPix2, also conducted by the author. The HitPix2 is a larger version of the HitPix with a size of $1\,\mathrm{cm} \times 1\,\mathrm{cm}$. It is currently in production. With this chip, it will be possible to build a beam monitoring prototype that covers a larger area with multiple sensors.

The smart sensor development carried out in this work showed that HV-MAPS offer solutions for many particle detection applications. With the developed MuPix, the suitability of HV-CMOS sensors in tracking detectors was confirmed. It fulfils all requirements of the Mu3e experiment and will be used for the construction of the Mu3e tracking detector. Furthermore, with the developed HitPix, it was shown that HV-CMOS sensors can be used in medical physics in the field of particle therapy as a beam monitor. Therefore, the work conducted in the frame of this thesis constitutes an important contribution to the further development of a promising new technology and demonstrates its successful application both in the field of medical and particle physics.

Part V

Appendix

Publications

Publications by or with contribution from the author of this thesis. Publications marked with * have been explicitly discussed in this thesis.

1. T. Rudzki *et al.*, "The mu3e experiment: Toward the construction of an hv-maps vertex detector," 2021.
2. R. Schimassek *et al.*, "Test results of atlaspix3 — a reticle size hvcmos pixel sensor designed for construction of multi chip modules," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 986, p. 164812, 2021.
3. K. Arndt *et al.*, "Technical design of the phase i mu3e experiment," 2021*.
4. I. Perić *et al.*, "High-voltage cmos active pixel sensor," *IEEE Journal of Solid-State Circuits*, 2021*.
5. H. Augustin *et al.*, "The mupix sensor for the mu3e experiment," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 979, p. 164441, 2020*.
6. M. Prathapan *et al.*, "Atlaspix3: A high voltage cmos sensor chip designed for atlas inner tracker," *PoS*, p. 010, 2020.
7. A. Schöning *et al.*, "Mupix and atlaspix – architectures and results," 2020*.
8. H. Augustin *et al.*, "Mupix10: First results from the final design," in *Proceedings of the 29th International Workshop on Vertex Detectors (VERTEX2020)*, p. 010012, 2021*.
9. I. Perić *et al.*, "A high-voltage pixel sensor for the atlas upgrade," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 924, pp. 99–103, 2019. 11th International Hiroshima Symposium on Development and Application of Semiconductor Tracking Detectors*.

10. M. Prathapan *et al.*, "Towards the large area hvcmos demonstrator for atlas itk," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 936, pp. 389–391, 2019. Frontier Detectors for Frontier Physics: 14th Pisa Meeting on Advanced Detectors.

11. F. Ehrler *et al.*, "Characterization results of a hvcmos sensor for atlas," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 936, pp. 654–656, 2019. Frontier Detectors for Frontier Physics: 14th Pisa Meeting on Advanced Detectors.

12. H. Augustin *et al.*, "Performance of the large scale hv-cmos pixel sensor mupix8," *Journal of Instrumentation*, vol. 14, pp. C10011–C10011, oct 2019*.

13. M. Kiehn *et al.*, "Performance of cmos pixel sensor prototypes in ams h35 and ah18 technology for the atlas itk upgrade," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 924, pp. 104–107, 2019. 11th International Hiroshima Symposium on Development and Application of Semiconductor Tracking Detectors.

14. M. Kiehn *et al.*, "Performance of the ATLASPix1 pixel sensor prototype in ams aH18 CMOS technology for the ATLAS ITk upgrade," *Journal of Instrumentation*, vol. 14, pp. C08013–C08013, aug 2019.

15. H. Augustin, , *et al.*, "Mupix8 — large area monolithic hvcmos pixel detector for the mu3e experiment," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 936, pp. 681–683, 2019. Frontier Detectors for Frontier Physics: 14th Pisa Meeting on Advanced Detectors*.

16. M. Prathapan *et al.*, "Design of a hvcmos pixel sensor asic with on-chip readout electronics for atlas itk upgrade," in *Topical Workshop on Electronics for Particle Physics (TWEPP2018)*, vol. 17, p. 21, 2018.

17. H. Augustin *et al.*, "Mupix8-a large-area hv-maps chip," in *26th International Workshop on Vertex Detectors*, p. 57, 2017*.

18. I. Perić *et al.*, "Status of HVCMOS developments for ATLAS," *Journal of Instrumentation*, vol. 12, pp. C02030–C02030, feb 2017.

19. R. Blanco *et al.*, "HVCMOS monolithic sensors for the high luminosity upgrade of ATLAS experiment," *Journal of Instrumentation*, vol. 12, pp. C04001–C04001, apr 2017.

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