Dissertation

submitted to the

Combined Faculty of Mathematics, Engineering and Natural Sciences

of Heidelberg University, Germany

for the degree of

Doctor of Natural Sciences

Put forward by

Keller, Michael

born in: Mannheim

Oral examination: 26.07.2022

Design and low temperature characterization of low noise single photon detector arrays for rare event search experiments with liquid noble gases

Referees: Prof. Dr. Peter Fischer
Prof. Dr. Hans-Christian Schultz-Coulon

Zusammenfassung

In vielen Experimenten zum Nachweis von Dunkler Materie werden flüssige Edelgase als szintillierendes Nachweismaterial verwendet. Für die VUV-Licht detektion wird ein rauscharmer und empfindlicher Detektor benötigt. Die vorliegende Arbeit prüft, ob digital SiPMs hierfür geeignet sind. Dafür wurde ein Testchip gebaut und bei tiefen Temperaturen ausführlich untersucht. Digital SiPMs bieten den Vorteil, dass bei diesen Single Photon Avalanche Diodes (SPAD) in einem CMOS Herstellungsprozess angefertigt werden. Somit kann die Ausleselogik auf demselben Chip untergebracht werden. Die Elektronik digitalisiert das SPAD Signal, sodass im Gegensatz zu herkömmlichen SiPMs kein weiterer Auslesechip benötigt wird. Der Testchip wurde für einen hohen Füllfaktor optimiert und besitzt eine datengesteuerte Auslese mit niedrigem Stromverbrauch. Auf dem Testchip befinden sich SPADs verschiedener Größen und Formen. So konnte das Rauschverhalten in Abhängigkeit zur SPAD-Geometrie untersucht werden. Außerdem wurde das Rauschen der SPADs bei tiefen Temperaturen optimiert. Bei tiefen Temperaturen von $T = 165\,\mathrm{K}$ ergibt sich ein von der geometire unabhängiger Wert von $0.02\,\mathrm{Hz}$ pro mm^2 aktiver Fläche. Des Weiteren wurde ein niedriger Leistungsaufnahme von $\sim 2\,\mathrm{m\,W}$ gemessen und es konnte eine optimale SPAD-Größe ermittelt werden. Für diese ist der Füllfaktor 74%, wenn alle SPADs mit erhöhtem Rauschen ausgeschaltet sind. Darauf aufbauend wurde ein Chip mit hohem Füllfaktor und datengesteuerter Auslesearchitektur entwickelt.

Abstract

Dark matter search experiments, with liquid noble gas targets, require a detector with a low noise and a high VUV-light sensitivity. Within this thesis it was evaluate whether Digital SiPMs are a suitable candidate. For this, a test-array was developed and characterized at low temperatures. The advantage of digital SiPMs is that Single Photon Avalanche Diodes (SPAD) are manufactured in a CMOS process so that the readout logic can be placed on the same chip. The output signals are digital, and no readout chip is required, as in the case with common SiPMs. The test array was optimized for a high-fill-factor and possesses a low-power data-driven readout. It houses SPADs of different geometries, to investigate the noise as a function of size and shape. Furthermore, optimizations for the SPAD noise at cold temperatures, were made. At low temperatures of $T = 165\,\mathrm{K}$ a dark count rate independent of the geometry of $0.02\,\mathrm{Hz}$ per mm^2 of active area, was observed. An optimal SPAD size was found, for which the fill-factor is 74% when the noisy SPADs are turned off and, finally, a power dissipation of some $\sim 2\,\mathrm{m\,W}$ was observed. Based on this, a high fill-factor array with a data-driven readout was developed.

Contents

1 Introduction **1**

2 The Search for Dark Matter **3**

2.1 Evidence and a Promising Candidate 3

2.2 Detection Methods 4

2.3 Existing experiments 6

2.4 The DARWIN Experiment 7

3 Single Photon Avalanche Diodes **15**

3.1 Introduction 15

3.2 Manufacture 20

3.3 Quenching and Recharge Circuits 22

3.4 Breakdown Voltage 24

3.5 Photon Detection Efficiency 26

3.6 Uncorrelated Noise 27

3.7 Correlated Noise 36

4 Digital SiPM Readout Architectures **39**

4.1 SiPMs and Digital SiPMs 39

4.2 IDP2: Single Photon Camera 40

4.3 DARWIN Test Array and Process Variations 44

4.4 Time-Resolved Single Photon Camera 55

5 Setup for Cryogenic Measurements **61**

5.1 Simple Approach 61

5.2 Cryogenic Setup 65
5.3 Readout Electronics 68
5.4 Firmware and Software 71

6 Digital SiPMs at Various Low Temperatures 77

6.1 Data Acquisition 77
6.2 Data Analysis 81
6.3 IDP2: Breakdown Voltage and Sensitivity 84
6.4 IDP2: Dark Count Rate 87
6.5 IDP2: Hot SPADs 90
6.6 Photon Emission of the Readout Electronics 93
6.7 DARWIN Test Arrays: Breakdown Voltage 95
6.8 DARWIN Test Arrays: Dark Count Rate 96
6.9 Effect of SPAD size and shape 99
6.10 Power Consumption 105
6.11 Correlated Noise 107
6.12 SPAD Start-Up Behavior 110

7 New Digital SiPM Array for DARWIN 113

7.1 Requirements and Architecture 113
7.2 Implementation 114
7.3 Summary and Discussion 119

8 Summary and Outlook 121

1. Introduction

The quest to uncover the true nature of dark matter is one of the most important questions of modern physics. The evidence for its existence is striking and a broad variety of well motivated theories exist, but even after decades of experimental efforts, it still remains a mystery. Yet experiments cover a wide spectrum of possible detection channels, ranging from its production in high energy particle collisions [1] and the observation of its decay products in astrophysical objects [2] to the direct observation of a recoil with standard matter here on earth [3]. The latter is where most experiments are carried out and, among these, are the direct dark matter search experiments using liquid noble gases as target material, like, for example, the DARWIN experiment [4].
The DARWIN experiment is currently in the planning phase and will use liquid Xenon as target material for a recoiling dark matter particle. Based on the experience of numerous of previous experiments, it aims to ultimately answer the question of the existence of dark matter. In a recoil, Xenon atoms are excited and ionized, so that scintillation light with a wavelength of $\lambda = 178\,\mathrm{nm}$ is created and electrons are freed, both of which are signals available for a readout. A time projection chamber is utilized to collect the electrons, by applying an electric field to the liquid Xenon, and finally, converting them to a secondary light signal. These, and the primary scintillation light, are detected by photo sensors. With the deduced number of photons, the recoil energy and the position of the event can be determined and, with the relative signal strength, even the recoil type, meaning interaction with the nucleus or the outer electronic shell, can be discriminated. Especially the latter two quantities, form a strong tool for background rejection. For a good energy resolution and to be sensitive to very low recoil energies, it is necessary to resolve the number of detected photons very precisely [5]. So, a low noise and very sensitive light detection system is required. Mostly photomultiplier tubes (PMT) fulfill these demands. They show a formidable low noise and have a high detection efficiency [6]. However, their manufacture is quite complicated and comprises many individual parts, which introduces a significant amount of radio activity. Furthermore, it is quite fragile, since the outer shell of a PMT is basically a glass tube with vacuum inside, and tents to become leaky and is very expensive. Other light detectors might overcome the latter weaknesses. To investigate alternative light detector approaches a dedicated Work Group was formed in the DARWIN experiment. Among the proposed technologies are digital SiPM arrays.
In a digital SiPM, single photon avalanche photodiodes (SPAD) are manufactured in a CMOS porcess so that the readout can be placed on the same silicon dye. A SPAD is a diode light structure capable of detecting single photons by exploiting the avalanche breakdown as an internal amplification mechanism. With the readout logic a SPAD signal is directly digitized and processed, making the output signals of a array purely digital. Furthermore, very noisy SPADs can be turned off permanently with a masking bit. Compared to standard SiPM arrays [7], which are also possible candidates for the DARWIN experiment, no additional amplification circuitry on an extra chip is required, resulting in a simpler mechanics, reducing the power consumption and lowering the overall cost.
This thesis is a first step towards answering the question as to whether digital SiPMs are a suitable candidate for the light readout of the DARWIN experiment or any other rare event search experiments involving liquid noble gases. For this, digital SiPMs were extensively tested and characterized at low temperatures, with focus on the noise performance, which is one of the most crucial parameters. Firstly, a single photon camera digital SiPM array, not at all optimized

for low temperature operation, was tested at cold temperatures. The noise was higher than permitted by the DARWIN experiment, but it turned out that it is possible to lower it with a extra effort on the part of our supplier. In the next step, a dedicated test array, approaching the requirements of the DARWIN experiment, was developed. For it a series of optimizations to control the noise at low temperatures, were implemented. The array was then tested in terms of noise and other parameters, at various low temperatures. The results are very encouraging so that a new array is currently in development. This tends to be a realistic approach to the rare event search experiments, like DARWIN, in terms of the readout architecture.
In Chapter 2 an introduction to the evidence of dark matter, a quite promising candidate and, the current efforts to detect it, is given. Finally, the DARWIN experiment and the Work Group for alternative light detectors is introduced.
In Chapter 3 single photon avalanche diodes are extensivly discussed. First the working principle is explained, then parameters such as the breakdown voltage and the photon detection efficiency, are described. The main part of the chapter, however, covers the noise sources of a SPAD with respect to their temperature profile.
In Chapter 4 the characterized and developed digital SiPMs arrays are presented. The single photon camera for the first cold measurements was already present at the start of this thesis, while the DARWIN Test array was still to be developed. Furthermore, efforts were made to address other experiments with digital SiPMs, and thus a Time-Resolved Single Photon Camera was also developed.
In Chapter 5 the cryogenic measurement setup is presented. The starting point for the first cold measurements was a simple bath cryostat. Several cooling mixtures and, especially liquid nitrogen, provided numerous constant low temperatures. With the quest ahead being to measure the noise of test series of optimization for the DARWIN Test array, a more sophisticated cryogenic setup was implemented, equipped with new readout electronics for the array.
In Chapter 6 the results gained from the numerous tests of Digital SiPMs at low temperatures are presented. First of all, the characterization of the single photon camera is presented, with the temperature profile of the noise curve as a central part. After this, other observations, like the photon emission by the readout electronics, are explained. Then the extensive characterization of the DARWIN test array is discussed. The focus is on the noise curve, especially the of the optimized SPADs. However, hot SPADs are also extensively investigated as their number decreases at low temperatures, making them actually usable for photo detection.
In Chapter 7, the new digital SiPM array, with a realistic readout architecture for the DARWIN experiment, is explained.

2. The Search for Dark Matter

In this first chapter a introduction to dark matter search is given. The starting point will be the description of its evidence and possible candidates, then detection methods are presented. Since the quest in physics to uncover the true nature of dark matter is rather old, the search for it can look back on a long history. Therefore an introduction into various existing experiments is given before the field of liquid noble gas search experiments by means of the DARWIN experiment, is described in detail.
The DARWIN experiment is currently in the planning phase and will use liquid Xenon as the dark matter target. It has the novel goal to ultimately answer the question of the existence of dark matter. In the beginning of its description, the signal formation in liquid xenon and the Time Projection Chamber used to readout these signal is described.
The authors contribution to this experiment is not directly the search of Dark Matter, but rather of a technical nature. The focus of this work is to test the suitability of the so-called digital SiPMs as light detectors for DARWIN, which may replace Photomultiplier tubes (PMTs). These are part of the baseline design of DARWIN and are formidable light detectors. However, they have shown some weaknesses in recent years, which make other technology potentially more favorable. The search after alternative approaches is taking place in Work Group 5 of the DARWIN experiment, in which the author is participates. So, in the end of this chapter the constraints for a new light detector are discussed and some examples from the research of the Work Group 5 are presented.

2.1 Evidence and a Promising Candidate

Various astrophysical and cosmological observations cannot be sufficiently described with our current understanding and model of matter in the universe. Among those are, the galactic rotational curves [8]. The velocity of stars and gas in the disks of rotating galaxies, with respect to their distance to the center of the galaxy, was measured. Astonishingly, the velocity at the outer edge of the galaxy does not decrease with increasing distance, as predicted by Newtonian mechanics but stays constant. An additional gravitational interaction at the outer edge of the galaxies is required to explain this effect.
Furthermore, massive objects in the universe like galaxy clusters change the trajectory of light via gravitation, allowing, for example, the observation of objects behind them, which is the so-called gravitational lensing effect [9]. However, the required gravitational potential of the objects baryonic or luminous matter is, in many cases, not sufficient to describe the curving of the light [10], [11].
These are just two examples out of various observations (see for example [12]), which all require the presences of a non observable but gravitational interacting matter to be fully described. The so-called dark matter is postulated, which is supposed to neither interact strongly nor electromagnetically, but only via gravitation and weak interaction with our known baryonic matter.
The precise measurement of the anisotropy of the microwave background of the universe, also a perfect example for the evidence of dark matter, has made it possible to estimated the abundance of this dark matter. The Planck satellite currently provides the most precise measurement of the microwave background radiation, which is well described by the so-called Standard Model of Cosmology [13]. In this model, dark matter is an inherent part and its abundance in the universe is determined to be up to 27% of the total energy content. The fraction of our known baryonic matter however, is only about 4% and the remaining fraction is attributed to dark energy, which

is beyond the scope of this work.
The search for dark matter is presently one of the most important issues in modern physics and this had lead to a broad variety of theoretical approaches to describe it. Attempts have been made, like modifying Newtonian dynamics [14] or attributing it to very dense and massive objects like neutron stars or black holes. Both have failed because the first is not able to describe large scale objects sufficiently [15] and massive objects make up only about 20% of the total amount of dark matter [16]. A promising approach is to describe it as a neutral particle, which only interacts weakly. From the known particles of the standard model of particle physics only the neutrino has the assumed properties of dark matter. It turns out that the neutrinos relativist traveling speed, is actually too fast, so that large structures in the universe could not have evolved [17]. Evidence for a particle beyond the standard model is given.
A broad variety of candidates can be assumed [18]. These are, for example, Axion like particles, intentionally believed to solve the strong CP problem in Quantum-Chromo-Dynamic [19] or sterile neutrinos, only interacting via neutrino mixing [20]. However, a candidate of particular interest is the weakly interacting massive particle (WIMP), which is, in theory, well motivated [21]: In the early hot and dense phase of the universe, WIMPs were produced from, and annihilated into, standard model particles with equal rates. On expansion and cooling of the universe, WIMPs decoupled from the primeval plasma as the temperature dropped below their production energy. Decoupling of the WIMPs, possessing a WIMP mass between a few $5\,\mathrm{GeV}/c^2$ up to $1\,\mathrm{TeV}/c^2$, happened at a non-relativist velocity. After decoupling, production ceased and only annihilation occurred, of which the rate and corresponding cross section is low. On the further expansion of the universe the annihilation rate dropped and approaches zero. A relic WIMP density was formed, which in case the WIMP is stable is present until today. The estimated abundance of the WIMP is in the same order as determined by the cosmic background measurement mentioned above.
Independent of this theoretical approach the so-called Supersymmetry model [22] also postulates the existence of a WIMP like particle. This model is an extension of the standard model of particles in which all particles of the standard model have symmetrical partners with difference in spin of 1/2. Subsequently, bosons have a fermion as partner and vice versa. The lightest supersymetric particle is the so-called neutralino, which possesses the same mass as a WIMP, only interacts weakly and is the symmetrical partner of a bosons.

2.2 Detection Methods

As broad as the theoretical approaches to explain dark matter are the variety of experiments performed to detect it. To actually prove the existence of dark matter one has to observe its interaction with our known baryonic matter, i.e. standard model matter (SM). There are three possible ways that a dark matter particle interacts with SM particles to produce a traceable signal for a detector. These ways are shown in figure 2.1. A dark matter WIMP can be created from SM particles, it can annihilate or decay into SM particles and weakly interact (recoil) with SM particles.
WIMPs could possibly produced within a high energy particle collider such as the Large Hadron collider (LHC). With the center of mass collision energy up to 13 TeV, which is in the order of the assumed WIMP mass, it should be possible to produce them. A WIMP production is then observed via missing momentum of the detected particle tracks. Atlas and CMS are both large experiments, situated at the LHC, searching for a WIMP signature in particle tracks. So far, however, neither has found such a particle [1], [23].
Indirect detection experiments search for WIMP decay or annihilation products by observing astrophysical objects [24]. WIMPs could either decay or self-annihilate, which would make them

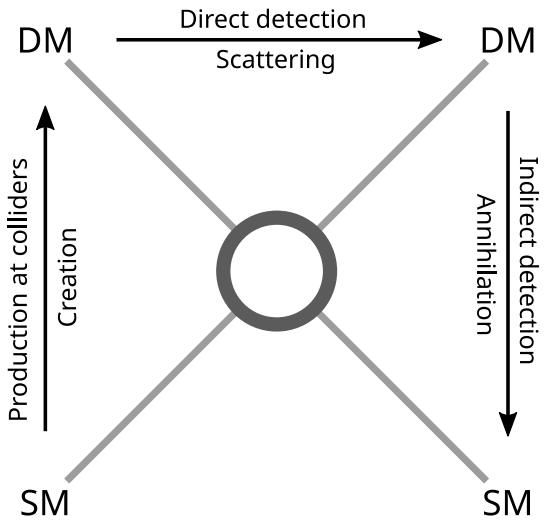

Figure 2.1: Possible interaction channels of dark matter with standard matter, that can be utilized to detect it. First it can be produced in a high energy particle collision, then its annihilation or decay products can be observed, and finally it can recoil at standard matter particle.

mayorana particles. Products of both processes are particles from the SM, like positrons, neutrinos or γ-rays, which are luminescent or traceable. Of particular interest for the search for decay or annihilation products, are massive objects in the universe, like galaxy centers or close galaxy clusters. Dark matter can accumulate in this massive objects, by gravity, in such a way that its abundance is high and a possible signature is naturally enhanced. Telescopes performing an directional search for annihilation or decay products are either earth-bound, like the VERITAS experiment [25], or satellite-borne, like the Fermi Large Area Telescope (LAT) [2]. However, none of these have shown a significant signature of DARK Matter.

Last, and of special interest for this work is the direct detection of a WIMP scattering at an SM particle. Assuming that the Milky Way is surrounded by dark matter (see section before), so that it is also present in our solar system, it should be possible to detect dark matter with an earth-based detector [26]. Inside the target volume of the detector a WIMP scatter event leads to heat dissipation, ionization and light emission. By measuring those signals the recoil energy, which is in the order of 1 to 100 keV for a WIMP with mass between $5\,\mathrm{GeV}/c^2$ and $1\,\mathrm{TeV}/c^2$ [27], can be reconstructed.

For the direct dark matter detection, a crucial part is the target material for the WIMP interaction. Over the years a broad variety of experiments utilizing different target materials to read out recoil signatures have evolved [3], [28]. Especially, materials with a high atomic number are utilized and target volumes are steadily increased to further enhance the sensitivity. Some of these are discussed in the next section. However, due to the low scattering cross section of the weak interaction the actual WIMP recoil rate inside such a detector is extremely low and often sensitivity is compromised by background events [3]. Again, so far, no evidence of dark matter has been found.

In the next generation of direct dark matter experiments, to which DARWIN belongs, ann attempt is made to increase the sensitivity by increasing target volume, extending exposure times and decreasing background [3]. Mostly aiming for a sensitivity level where neutrino scattering becomes the dominant background source, which cannot be overcome [29].

2.3 Existing experiments

Direct detection experiments are currently the main driving force in the search for dark matter. A broad variety of earth-bound experiments try to find signs of a WIMP recoil in a suitable target material, by means of scintillation light, ionized electrons or heat. The detector types of the experiments can roughly be divided in two groups: Solid state detectors, and liquid target detectors [30]. In recent years solid state detectors have been shown to be a powerful tool for WIMPs with low mass below $10\,\mathrm{GeV}/c^2$, while for higher mass liquid targets perform better [30]. However, having a broad variety of experiments utilize different target materials but also being complementary, is of vital importance for the dark matter search. Misidentification, like in the case of the DAMA experiments [31], can be excluded in this way. In figure 2.2 an overview of the limits for the spin independent cross-section set by leading dark matter search experiments, is shown. Only a few examples are discussed. A more comprehensive list of experiments can be found in [30].

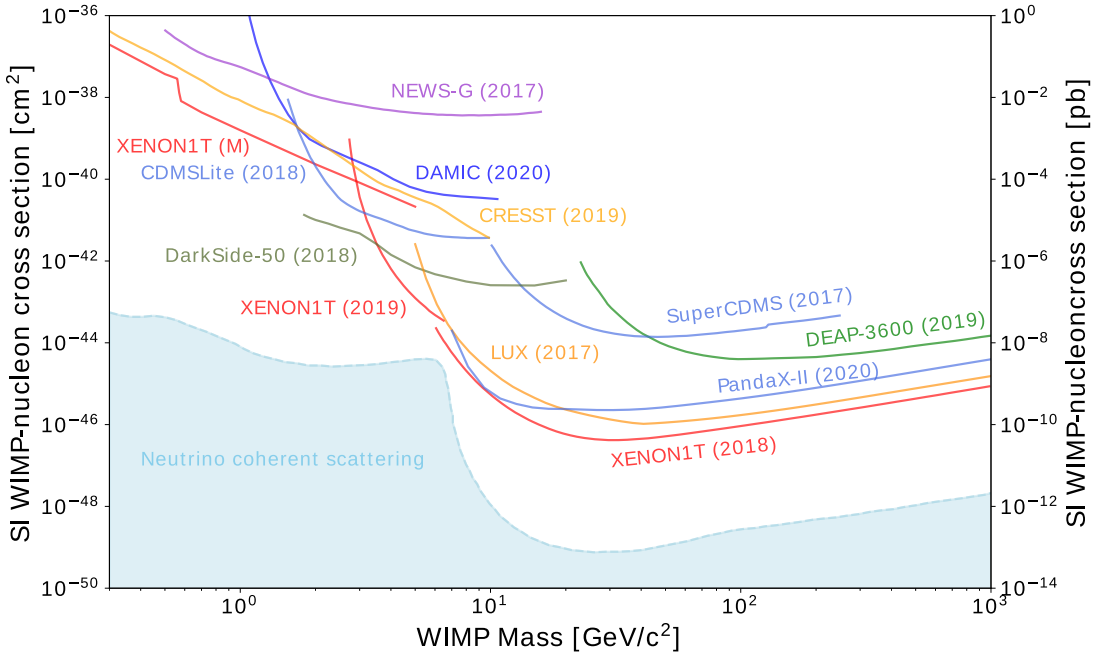

Figure 2.2: Overview of the current cross-section limit for various WIMP masses set by different experiments, of which only some examples are described in this section. The area marked light blue is the assumed region where neutrino scattering becomes the dominant noise source. With respect to lower WIMP mass, mostly solid-state detectors set the lower limits, while for higher WIMP mass, the liquid noble gas detectors do so. The picture is taken from [32], which is an updated version of [30].

Two prominent examples for experiments utilizing solid-state detectors are CRESST and SuperCDMS. Both use target materials cooled to cryogenic temperatures of some 1 mK and measure the heat dissipated in a recoil.
SuperCDMS [33] utilizes high purity germanium and silicon crystals, cooled to cryogenic temperatures. The so-called iZIP detector reads out charge and heat signals from a recoiling particle. With this combined readout it is possible to identify the recoiling particle and hence, effectively reject background signal. The so-called iZIP detector, comprising an interleaved electrode structure, is microfabricated on the front and back of the crystals. One electrode is for applying an electric field for the charge collection. The other electrode consists of superconducting aluminum

and, in combination with a Transition Edge Sensor (TES), measures the phonons. A TES is a superconducting material operated at the superconducting phase transition so that a heat input results in a significant change of its resistance [34].
The experiment is most sensitive for Wimp mass of about $20\,\mathrm{GeV}/c^2$, where it has reached quite a formidable lower sensitivity, which has been limited by background events. With CDMSLite, a spin off experiment, the phonon (heat) signal was internally amplified and a lower energy threshold reached. By combining the technology of SuperCDMS and CDMSLite the next generation of this experiment, called SuperCDMS SNOLAB, was born [35], [36]. Commissioned at SNOLAB in Canada [37] and currently data taking, the aim is to observe the low mass WIMPs parameter space.
CRESST [38] utilizes calcium tungsten crystals, which are light scintillators, as target material. Currently, the third phase of the experiment is data taking with an array of ten crystals. Again, by reading out the phonon signal and the light recoil, particles can be identified and background significantly reduced. The combined readout of both signals is done by two TES: One is mounted directly on the target crystal, the another, which detects the light, is mounted on a silicon-sapphire substrate at some distance to the crystal. The TES offer a high energy resolution so that a lower energy input of 50 eV can be detected, enabling recoils of WIMPs with only $0.5\,\mathrm{GeV}/c^2$ mass to be measured. The CRESST experiment has a formidable sensitivity with respect very low WIMP mass. Conceding higher WIMP mass background signals again lower the sensitivity.
A last example of a solid-state detector experiment, also sensitive in the low WIMP mass region, although its approach is simpler than both examples mentioned above, is DAMIC [39]. In this experiment a straight-forward approach is chosen which utilizes silicon CCD cameras to detect low mass WIMP recoils. The CCDs are also operated at a moderate cryogenic temperature of $T = 140\,\mathrm{K}$.
One of the most frequently used materials, and of special interest for this work, are liquid noble gases, like Argon and Xenon. The major advantage of liquid noble gases is their excellent scale ability [40]. Present experiments reach the ton scale target volume, which greatly increases sensitivity. A recoil creates scintillation light and ionized electrons, which can both be read out. This will be discussed in detail in the next section. Typically, a time projection chamber, which is a good tool for background reduction, is utilized to collect the charge and detect the light signal which is also part of the discussion in the next section. However, there are also experiments, which read out only the scintillation light, like for example the DEAP experiment [41]. Here, also an excellent background reduction is achieved by utilizing the so-called pulse-shape discrimination [42].
Argon, in comparison to Xenon, is much cheaper but it offers less sensitivity for low mass WIMP [3]. Current experiments using Argon are, for example, DarkSide [43] and DEAP. Xenon, on the other hand, is utilized in detectors like LUX [44] and Xenon1T [45]. The latter has achieved the current lowest cross-section limit of $4.1 \times 10^{-47}\,\mathrm{cm}^2$ at a WIMP mass of $30\,\mathrm{GeV}/c^2$. Currently, the next generation of liquid noble gas detectors is in planning phase. The target volume will be enlarged from the $\sim$1 t to several 10 t to increase the sensitivity down to the neutrino floor [46]. DARWIN [4], in which the author participates, is among those next generation experiments using liquid Xenon.

2.4 The DARWIN Experiment

The DARk matter WImp search with liquid xenoN (DARWIN) Experiment is a next generation dark matter search experiment with the scientific goal of being the ultimate detector for WIMPs with a mass between $5\,\mathrm{GeV}/c^2$ and $50\,\mathrm{GeV}/c^2$ [4]. Liquid Xenon is the dedicated target volume,

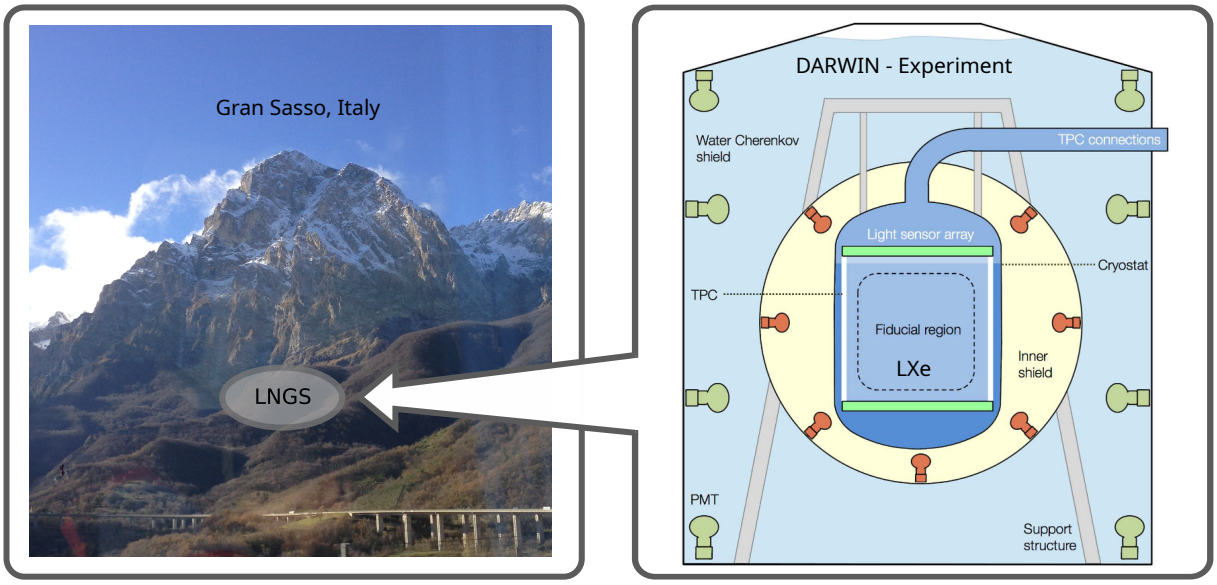

Figure 2.3: The dark matter search experiment, DARWIN, will most likely be commissioned in the under ground lab LNGS situated below the Gran Sasso Massif. The position of the lab is shown artistically in the photo of the Gran Sasso mountains on the left side. The central part of the experiment is the cryostat housing the liquid Xenon target volume and the time projection chamber to readout the scintillation light and charge signal from a WIMP recoil. The cryostat is placed into a water tank, acting as active muon and muon induced neutron veto.

with which a sensitivity of $1 \times 10^{-49}\,\mathrm{cm}^2$ shall be reached for a WIMP mass of $50\,\mathrm{GeV}/c^2$. Below this value neutrino scattering is supposed to become the dominant source of background, which cannot be overcome [29]. To achieve this novel goal, the successive reduction of background of the previous experiments (like Xenon1T [47]) will be continued and, at the same time, the target volume will be massively increased to 50 t of liquid Xenon. Apart from WIMPs, a further scientific goal of the DARWIN Experiment is it to investigate also other rare events [4], [48]. With a natural abundance 9% of ^{136}Xe in the liquid Xenon target volume, which is a double beta emitter, neutrino less double beta decay could be observed. Furthermore, axion-like particles, solar neutrinos and coherent neutrino-nucleus scattering shall be observed.
DARWIN will most likely be commissioned in the underground laboratory, Laboratori Nazionali del Gran Sasso (LNGS) in Italy, of which the position is artistically shown on the left side of figure 2.3. Located in a side arm of a traffic tunnel below 1400 m of rock from the Gran Sasso massif, the cosmic muon flux is about $1\,\mathrm{m}^{-2}\,\mathrm{h}^{-1}$ [49]. A cryostat, shown on the right side, will house the vast amount of liquid Xenon. It is roughly 3 m in height and diameter and is commissioned out of radio pure materials, like ultra clean titanium or stainless steel [4]. The base temperature of the cryostat is $T = 165\,\mathrm{K}$ at room conditions [50]. The cryostat itself is placed in a water tank of 14 m diameter, which is instrumented with Photomultiplier tubes. The water tank acts as an active cosmic muon veto and shields the cryostat further from environmental radioactivity and muon-induced neutrons. The inner shield also shown in the figure 2.3, is filled with an additional liquid scintillator neutron veto, which might be optional [4]. Outside the water tank, there is a purification and cooling system for the liquid xenon, which is circulated through the cryostat [4]. Distilling especially radioactive contaminations like Krypton, which is a β emitter, out of the liquid xenon to reduce radioactive background [51].
A rather conservative and straight forward detector approach is chosen for the detection of a WIMP recoil. A Time Projection Chamber (TPC), which is technology established in many

predecessor experiments [40], will be utilized. However, a TPC is an excellent tool for background discrimination. It is housed inside the cryostat's inner volume and has a cylindrical structure with a diameter and height of roughly 2.6 m. By measuring the scintillation light as well as collecting the free electrons, it is possible to reconstruct the 3D position of the event and also to discriminate between the recoil type. With the latter, WIMPs, which are supposed to interact with the nucleus (nuclear recoil), can be discriminated from γ and β radiation, which interact with the outer electronic shell (electronic recoil). With the position information events from the cryostat's walls, where most of the background originates [52], can be rejected and an inner fiducial target-volume can be defined.
The final and very crucial part of TPC is the light detector technology for the actual readout of the scintillation light signal and charge collection signal, which is also converted to a light signal in the TPC. Two planes, one on the bottom the other on the top of the TPC, have to be equipped with photosensors. In the baseline design, Photomultiplyer tubes (PMTs) [4], with their excellent noise and quantum efficiency for the scintillation light, are foreseen. However, in recent years also other novel light detectors have made great progress in the field of cryogenic operation. Within the DARWIN Work Group 5, in which the author participates, these alternative light detector approaches have been studied and compared. The author's contribution to this group was to investigate the novel Digital SiPMs.
In the following the cryostat´s inner detector parts will be discussed. This means the light and charge emission in liquid Xenon, which is crucial for the signal formation, is described and the structure of the Time Projection Chamber discussed. In the last subsection, the constraints DARWIN has for the light detector operated inside the DARWIN experiment, are listed and some novel detector approaches of the Work group 5 are introduced.

2.4.1 Signal Formation

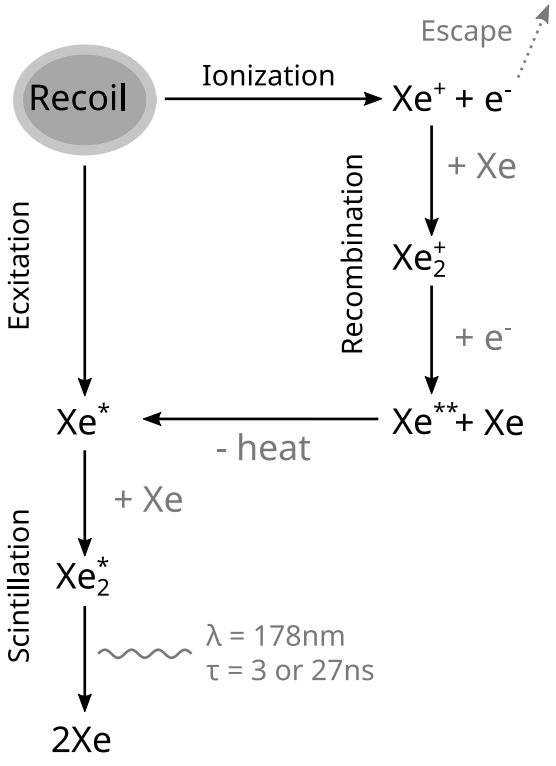

Figure 2.4: A recoiling particle in liquid Xenon causes ionization (Xe^+) and excitation (Xe^*) of Xenon atoms. An excited Xenon atom forms an excimer (Xe_2^*) with a neighboring atom, which, in turn, emits scintillation light with $\lambda = 178$ nm during its de-excitation. The ionized electron on the other hand can either escape from the interaction site or recombine with a xenon ion. The latter case eventually leads to an excimer state and thus to scintillation of light. Figure adapted from [53].

Liquid Xenon is a particularly good target material because it offers an excellent charge and light yield, of roughly 10 photons per 1 keV and a charge yield of 5 electrons per 1 keV for WIMP recoils [32]. Furthermore, it is radio pure due to the absence of any natural long-life radioisotopes, apart from ^{136}Xe. The latter has a half-life of 2.165×10^{21} years, which is utilized to probe neutrino-less double beta decay [54]. Finally, with the ratio of charge and light yielded, an event background can be identified and rejected with high accuracy [55].
Inside the liquid Xenon target volume, a recoiling particle causes the emission of scintillation light and ionizes the Xenon [56]. A small portion of the energy is, however, lost to heat, which cannot be read out. Accelerated, Xenon atoms and free electrons, in return, can themselves further ionize and excite neighboring Xenon atoms (Xe^*). A diagram of the light and charge emission mechanism of Xenon is shown in figure 2.4.
An excited Xenon atom collides with a neighboring atom and forms a diatomic excited molecule state (Xe_2^*), which is called excimer. The excimer enters the ground state and releases a photon with a wavelength in the vacuum ultraviolet range (VUV) range of $\lambda = 178$ nm [57]. A singlet and triplet state can be occupied, resulting in a life time of 2.2 ns and 27 ns, respectively [58]. The energy of the photon $E = 7$ eV is below the band gap energy $E_G = 9.28$ eV of liquid Xenon such that the photons are not absorbed in the detection volume [59]. However, especially in large volumes heavy scattering happens, delaying the arrival time of the photons on the photosensors up to 200 ns [60].
A Xenon atom is ionized (Xe^+) by an average recoil energy of 15.6 eV [61]. The recombination with an electron creates additional light. Ionized Xenon atoms form charged molecule states with neighboring atoms, which can recombine with a free electron. A double excited Xenon is created, which relaxes by low energy collision with a neighboring atom, resulting in undetectable heat emission. The excited Xenon then again forms an excimer and a follows the described scintillation process.
With an additional electric field applied on the Xenon volume, escaped electrons are collected and drawn away from the interaction site before they can recombine. The collection efficiency is determined by the electron lifetime, which depends on the purity of the Xenon. Especially, Oxygen contaminations are very effective traps for free electrons [40].
The ratio of the detected light and collected charge depends on the recoil type and is utilized to effectively discriminate background [55]. WIMPs are supposed to interact with the nucleus and perform so-called nuclear recoil (NR) [62]. γ or β radiation resulting from a background decay event interact with the outer electronic shell and perform so-called Electronic Recoil (ER). Nuclear recoil creates a dense track of excited and ionized Xenon atoms. The closer ions are to electrons, the more recombination happens, and the less electrons can escape. The light yield is higher than the charge yield.
In an ER event, a less dense track is formed, and electrons can escape more easily from the interaction site. Consequently, more charge is collected than scintillation light detected. Moreover, for an ER, the portion of light and charge can even be modulated by the applied electric field strength. The higher it is the more charge is collected and the less light is emitted, which is the so-called anticorrelation of both signals [55]. The ratio between light and charge is utilized to discriminate nuclear and electronic recoil and reduces background effectively.

2.4.2 Time Projection Chamber

With a time projection chamber (TPC) both, the prompt scintillation light (S1) signal and the number of escaped electrons, the so-called ionizaton (S2) signal can be measured. This has the advantage that, on the one hand the position of the event can be reconstructed and on the other hand, as described in the previous section, the type of interaction, i.e. electronic and nuclear

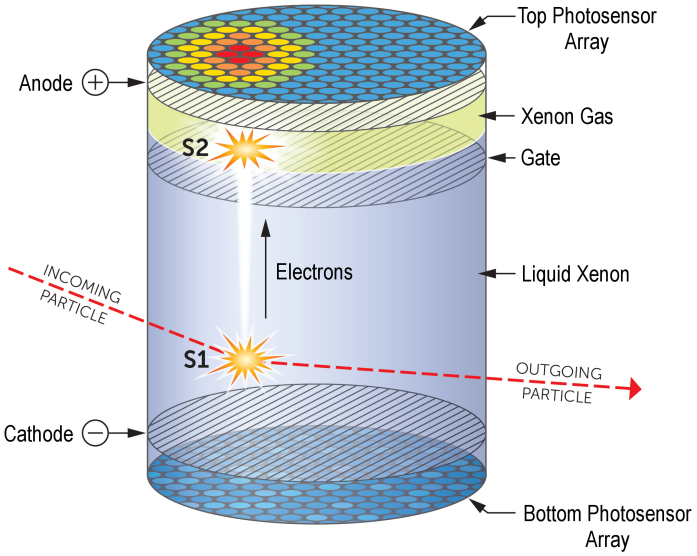

Figure 2.5: Illustration of a time projection chamber filled with liquid Xenon for reading out the direct scintillation signal S1 and the charge signal S2 from a recoiling particle. Top and bottom plane are equipped with photosensors, for light detection. An electric field inside the TPC causes the freed electrons to drift upwards, where they scintillate as they enter the gas phase. Picture taken from [32]

recoil, can be discriminated by determining the ratio between the S1 and S2 signal. Both properties are a strong tool to actively reject background events.
The structure of a TPC, including a example of a WIMP recoil inside, is depicted in figure 2.5. The TPC has a cylindrical shape with a diameter and height of roughly 2.6 m [4]. It is housed inside the cryostat described at the beginning of this section and is completely immersed in Xenon, except for a small layer of gas on the top. The top and bottom area are covered with VUV light sensor, with the bottom array in liquid Xenon and the top array in Xenon gas. In the baseline design of the DARWIN TPC [4] the top and bottom plane, are covered with VUV light sensitive Photomultiplier Tubes (PMTs), which are described and characterized in [6]. The walls of the TPC are covered with polytetrafluoroethylene (PTFE) a VUV reflective material, minimizing absorption of the scintillation light [4], [63].
In a WIMP interaction, the prompt scintillation light signal S1 is emitted isotropically and detected by both photosensor arrays. The free electrons on the other side drift towards the top array and produce a secondary scintillation signal as they enter the Xenon gas phase. In total, three electrodes, which are the cathode, the gate and the anode, are utilized to create a drift field inside the liquid and an extraction field at the gas-liquid surface. The cathode is installed close to the bottom photosensor array and is typically an array of thin parallel wires, which possess a low absorption probability for the S1 photons [64]. The cathode is biased with a negative high voltage of about $-100\,\mathrm{kV}$ and forms, with the gate electrode, which is at ground potential and mounted on top of the TPC, a drift field of about $\mathcal{O}(0.5\,\mathrm{kV\,cm^{-1}})$ [4]. Field shaping electrodes are attached at the outer wall of the TPC below the PTFE reflector to confine and homogenize the field inside the cryostat (not shown in the figure). Consequently, the trajectory of the electron is not deflected, so that the position resolution described later is not compromised [4].
When the electrons reach the gate electrode, they come into the influence of the extraction field. The anode is at a high positive voltage, creating typically an extraction field of $>9\,\mathrm{kV\,cm^{-1}}$ [65]. The gate and, furthermore, the Anode, are both hexagonal meshes, which is a more suitable shape for charge collection [64]. This field accelerates the electrons towards the xenon gas layer and on entering the gas phase, scintillation light is created. Recoiling electrons excite the Xenon atoms and de-excitation happens in the same manner as described in the previous section. Ionization on the other side is less probable, no avalanche process is initiated, and hence, the amount of secondary light is proportional to the number of electrons [66]. The scintillation light is again spreader isotropic and will be detected by both top and bottom array again. However, the top

array is only about ∼1 cm away from the interaction point [47], so most of the light is emitted to a small spot on the top photosensor array. By evaluation of the center of gravity of the lightspot the x/y-coordinates of the event can be reconstructed with mm precision [47]. The z-coordinate, on the other hand, can be determined with even better resolution of sub mm by evaluation of the time delay between the S1 and S2 signal [47]. Finally, with the amount of detected scintillation light from the S1 and S2 signal the energy of the recoil event can be determined [5], [67].
Background rejection using position reconstruction and recoil discrimination then works as follows: The walls of the TPC and cryostat are the origin of most background events [52]. Consequently, the inner volume of the Xenon target is defined as fiducial region and events, of which the reconstructed position is near the walls are rejected [52]. In fact, in liquid Xenon the outer non-fiducial volume is quite small, since the attenuation length for neutrons, as well as γ and β radiation, is in the range of some 1 cm [68]. For example, a 100 keV γ can roughly travel 3 cm before it is fully absorbed. Inside the fiducial volume, the ratio of the S1 and S2 is utilized to reject further background caused by electronic recoil (see section 2.4.1). A prominent example for a xenon contamination, creating β radiation is Krypton [4].
Light detection inside the TPCs, though only discussed briefly in this subsection, is a crucial part to reach the lowest WIMP sensitivity with the TPC structure. All signal identification and discrimination is based on the number of photons detected [5]. As already stated above, in the baseline design of the DARWIN detector, both the upper and the lower detector plane are equipped with photomultiplier tubes (PMT) [4]. All components are housed in evacuated glass. A photon hits a metalized cathode and ionizes an electron. An strong electric field accelerates it towards a cascade of dynodes, where new electrons are ionized and the initial signal is amplified many times over. PMTs are formidable and well-established light detector, which has been used for decades in a broad variety of experiments. There is a unique low dark count rate of well below $0.01\,\mathrm{Hz\,mm^{-2}}$ and it simultaneously offer a high quantum efficiency (the probability to detect a single photon) of $\sim 35\%$ at the wavelength of 178 nm [6], [69], making it well suited for the DARWIN. However, in recent years, when PMTs have been used extensively in liquid Xenon based rare event search experiments, several weaknesses have become apparent. They tend to become inoperable in long term operation, they introduce a significant background contribution due to their high material budget and, moreover, they are also expensive to manufacture [4]. Therefore, in the DARWIN experiment the Work Group 5 has been formed, in which the author participates, to search for an alternative detector approach. Many promising technologies have been tested, which might be cheaper, more stable or in some other way more advantageous then PMTs. However, to be competitive a lot of strict constraints have to be complied with. These will be mentioned in the next subsection.

2.4.3 Requirements for the Light Detectors

As alternative light detector technology to replace PMTs in the DARWIN experiment, various constraints have to be met. Some of these may arise due to the excellent performance of the PMTs. However, other light detectors, discussed in more detail in the next subsection, may be inferior with the constraints, like the noise rate, but offer other advantages like a lower number of cables, simple mechanics or a better quantum efficiency, which then compensate for the deficiencies. Unless otherwise noted, the specified values can be found in [4].

- Low dark count rate of $< 0.01\,\mathrm{Hz\,mm^{-2}}$ to minimize the accidental coincidence to reach a low energy threshold. The sensitivity for low recoil energies is very dependent on the number of detected photons which could be artificially enhanced by noise. With a three fold photon coincidence a energy threshold below 5 keV can be reached [70].

- Highest possible photon detection efficiency (PDE) for Xenon scintillation light with $\lambda = 178\,\text{nm}$. The PDE is the product of the fill factor multiplied by the quantum efficiency. The fill factor is the fraction of the total sensitive and dead area of the detector. The higher the PDE, the more photons are detected, such that the noise might be less constrained. Currently, a single PMT has a PDE of 25%.

- The low flux S1 and the very focused S2 signal (see section before) have to be measured not only for WIMPs with a recoil energy of some 10 keV but also for the 2.5 MeV recoil of a neutrino-less double beta decay. Consequently, the dynamic range of the photon detector must start in the single photon regime and end in an overwhelming large burst of photons. For example, for a WIMP with in S1, roughly 100 photons are emitted, and in S2 roughly 1000 [32]. In the case of neutrino-less double beta decay, in the S1 about 10000 photons are emitted, while for S2 the number rises to 1×10^6 [71]. Nevertheless, the overall event rate is in the order of 10 Hz so that the event procession in the detector can be slow.

- The single photon time resolution is in the order of $\sim$10 ns. Time information is important to deduce the z-coordinate resolution of the position reconstruction (see section before), but the electrons drift speed is rather low with some $1\,\text{mm}\,\mu\text{s}^{-1}$ [47]. Mostly this corresponds to the digitization rate of the PMTs and is not required to be more granular.

- A very gradual spatial resolution is not required. With the current PMTs ($\varnothing \approx 49\,\text{mm}$), in previous experiments an x/y resolution of the event of some 1 mm was achieved [47], which was sufficient to define the fiducial volume.

- Low power dissipation of some $\text{mW}\,\text{cm}^{-2}$ to prevent excessive heating of the liquid and keep the overall cooling power low. In the baseline scenario about 150 W of cooling power are provided by two cryopulse coolers.

- Simple mechanics and low number of cables. Two detector planes with a diameter of 2.6 m have to be equipped with light sensors as dense as possible. It is preferable to have simple mechanics and a low number of cables.

- Highest radio-purity to keep the background induced by the photon detector low.

- Stable in long-term operation at cryogenic temperatures of $T = 165\,\text{K}$. The experiments will run for years and, after commissioning, the cryostat is sealed so that no access to the detector plane is possible.

2.4.4 DARWIN Work Group 5: Alternative Light Detectors

Within Work Group 5 of the DARWIN experiment, alternative photo sensor technologies are being investigated, which may replace PMTs. The chosen detector technology must, above all, be suitable for mass production and operable at liquid xenon temperatures.
One prominent candidate that has improved tremendously in terms of noise and quantum efficiency in recent years is a Silicon photo multiplier (SiPM). A SiPM is an array of single photon avalanche diodes (SPAD) microfabricated on silicon substrate. A SPAD is a diode-like structure capable of detecting a single photon by using the avalanche breakdown as an internal amplification mechanism (see next chapter). Made out of silicon they should be cheaper and due to the high purity less radio active than PMTs. In recent years, the dark count rate has reached values of $0.01\,\text{Hz}\,\text{mm}^{-2}$ at low temperatures and a photo detection efficiency of 50% for visible light [72]. This has made them, for example, the detector of choice for the DARKSIDE experiment [73], a liquid argon based dark matter search experiment. However, liquid argon is less

constraining than liquid xenon. On the one side it is colder ($T = 98\,\mathrm{K}$), which, in fact, reduces the SiPM dark count rate compared to warmer liquid xenon temperatures ($T = 165\,\mathrm{K}$) [72]. On the other hand, liquid argon scintillation light has an even shorter wavelength of 128 nm [57], which is too short for most of the present single photon detectors. The SiPMs are placed behind a wavelength shifting material, which is tetraphenyl butadiene (TPB) coated on a window [74]. The genuine scintillation light wavelength of argon is shifted to $\lambda = 420\,\mathrm{nm}$, where SiPMs, as mentioned before, have an excellent photon detection efficiency. However, TPB tends to dissolve in liquid xenon and is not planned to be used in DARWIN, although there is the possibility of installing TPB-coated windows in the gas phase. Great efforts are currently being taken to optimize the SiPM dark count rate for the higher temperatures in liquid xenon and make them directly sensitive to its scintillation light ($\lambda = 178\,\mathrm{nm}$) [75], [76].
Another investigated type of light detectors are so-called hybrid detectors, which combine the advantage of two or more established light detectors. The ABALONE detector is one of them [77]. It has the shape of a half dome, there is vacuum inside it and the working principle is quite similar to a PMT: An incident photon ionizes an electron on the photo cathode. However, instead of attracting it, with a high electric field, towards a cascade of dynodes, it is accelerated towards a scintillating crystal. Once hit, a well-defined amount of secondary light is emitted, which is, in return detected by an SiPM array. With the short, intense burst of scintillation light, a signal is generated that is clearly different from any SiPM dark count signal. The greatest advantage, compared to PMTs, is that the material budget is much lower, which on one side lowers the radioactivity and may also lower the cost [78]. However, a disadvantage is that a large bias voltage per device of around 25 kV is required and a electron back-scattering effect compromised the signal height. Around 35% of the electrons are back-scattered from the scintillator without depositing their energy completely. Some of them return to the scintillator, but others do not, so the signal strength is lower and the number of incident electrons underestimated. This effect is currently being closely studied and the first test in liquid xenon is planned soon.
The author's own contribution to Work Group 5 is the extensive study of so-called Digital SiPMs. This is a light detector technology, in which SPADs and complementary metal-oxide semiconductor (CMOS) logic can be fabricated side by side. A compact light detector on a single silicon dye is created, which, for example, puts out only digital information of the number of detected photons. Compared to standard SiPMs no subsequent ASIC for signal digitization is required, as signal digitization and processing happens on the very same chip. With this attractive solution, the number of cables, the power consumption and the complexity of the mechanics can be drastically reduced.
Throughout this work Digital SiPMs were excessively characterized at low temperatures to test some of the basic constraints for the DARWIN experiment, listed in the previous section. Starting with an array that already existed in the authors work group in Heidelberg, a first insight into the low temperature characteristics of Digital SiPMs was gained. The results showed, the reduction of the dark count rate is necessary. As the next step a dedicated test array for the DARWIN experiment was developed, for which several process variations to tackle the noise are implemented during the manufacture. The test array itself was equipped with a prototype of a for a low-power readout and is intended as a test platform for SPADs, mainly to measure the dark count rate and find the optimal SPAD size to maximize the fill factor. Improvements for the PDE at VUV light are also included in the manufacture, as it is currently close to zero. However, the characterization of the PDE was beyond the scope of this work. Finally, based on the good results gained within the DARWIN test array a realistic approach for a possible readout architecture for DARWIN was developed.

3. Single Photon Avalanche Diodes

A Single Photon Avalanche Diode (SPAD) is a diode like structure, made on a silicon substrate. It is a single photon detector, that internally amplifies a photon signal by exploiting the avalanche breakdown mechanism that occurs at large reverse bias voltages. Am incident photon initiates a avalanche current, which is macroscopic and therefore easily measured.
In this work the focus in on whether SPADs made in a CMOS process, so called Digital SiPMs (see section 4.1), are suitable as light detectors for the dark matter search experiment, DARWIN (see section 2.4). Most important for this experiment is the SPAD intrinsic noise and the photon detection efficiency at liquid xenon temperatures of $T = 165\,\mathrm{K}$. Therefore, the understanding of these parameters is essential and their description part of this chapter.
However, before going into the details, a general introduction to SPADs is given at the beginning of this chapter. For this, the properties of intrinsic and doped silicon, as well as the basic principles of a diode, are briefly discussed since they are fundamental to SPADs. The operation principle of SPADs is then described, followed by the manufacture and the quench and recharge circuits which are essential for their operation.
Next, all key parameters of the SPAD are discussed in terms of the temperature dependence. Starting with the description of breakdown voltage, an essential element for the SPAD operation, and continuing with the photon detection efficiency. However, since the determination of the latter is beyond the scope of this work the description is rather qualitative. Finally, the SPAD internal noise sources will be described in detail.

3.1 Introduction

This section is a first introduction to SPADs. The starting point is a brief review of the properties of intrinsic such as doped Silicon, as the SPADs are essentially p/n-junction made on plain silicon. Furthermore, the p/n-junction or diode, as a photon sensor will be introduced and the necessary steps to use it as a SPAD will be depicted. Finally, the operating principle of the SPAD as a single photon detector will be discussed.

3.1.1 Fundamental Properties of Silicon

All SPADs and the additional CMOS logic, used within this work, are made on silicon, which offers the following advantages: On the one hand the material is suitable for detecting visible light [7] and on the other hand, silicon is excessively used in industry as the primary choice for integrating electric circuits. Manufacture of the SPAD can count on well-developed processing methods from industry, making it possible to have SPADs with consistent quality and low price. Both are necessary to equip large areas with detector devices for a rare event search experiment.
Silicon is a semiconductor material, where the conduction and valance band are energetically separated by the so-called band gap. The band gap has an energy of $E_\mathrm{G} = E_\mathrm{C} - E_\mathrm{V} = 1.12\,\mathrm{eV}$, where E_V and E_C are the corresponding energies of the valence and conduction band [79]. A schematic of the energy bands is shown in part a) of figure 3.1. As a result of this separation, at a temperature of absolute zero all states up to the edge of the valence band are fully occupied and no electron can gain any thermal energy to overcome the band gap. Electrons within a full band can not move and, therefore, silicon acts as insulator.
At higher temperatures a small fraction of the electrons acquire enough thermal energy to over-

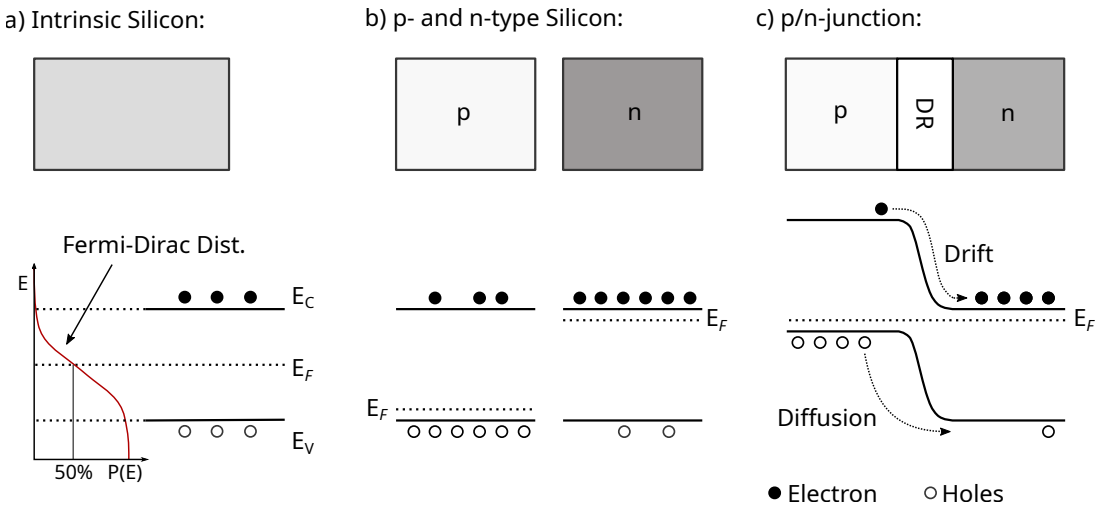

Figure 3.1: Schematic band structure of intrinsic and doped silicon, where the black dots and white dots indicate the electron hole density, as shown in part a) and b). In addition, in part a) an exemplary Fermi-Dirac distribution at $T > 0\,\mathrm{K}$ with the corresponding Fermi level, is depicted. The Fermi level shifts from the middle towards the edge of the band when doping is introduced. In part c) p- and n- silicon is joined forming a diode.

come the band gap. In the conduction band, electrons are free to move through the silicon crystal, so there is a little conductivity. When an electron enters the conduction band it leaves behind an unoccupied state in the valence band. Those states can, in return, be occupied by other valence band electrons. This can be described as movement of positive charge carriers, the so-called holes. In untreated silicon, which is called intrinsic silicon, the number of holes and electrons must be exactly equal. Their density is determined by the number of free states in the conduction band and the probability of being occupied at a certain thermal energy, which is given by the Fermi-Dirac distribution. For the latter one defines the energy level, where a state has a 50% probability of being occupied as Fermi level E_F. It has to be noted that the Fermi level should not be confused with the Fermi Energy $E_{\mathrm{F_i}}$, which is only defined for $T = 0\,\mathrm{K}$. Here the Fermi Dirac distribution is box-like and the Fermi Energy is the energy of the highest occupied state up to which all states below are fully occupied. At temperatures above $T > 0\mathrm{K}$ the Fermi level is located approximately in the middle of the band gap and the Fermi Dirac Distribution is symmetrical around this point, as depicted in figure 3.1. For an increase in temperature the Fermi level shifts towards the conduction band. Moreover, if the effective mass of the electrons or holes, which varies with the position inside the silicon band structure, differ, the Fermi level is also shifted away from the band gap middle. The effective mass is a concept where the modulating force, applied by the energy band structure when electrons and holes move through it, is described by a change in mass [80]. In both cases shifting of the Fermi level happens in order to equalize the local electron and hole concentrations, which have to be the same in intrinsic silicon.
The predominant electron and hole density in thermal equilibrium, where only temperature is supplying energy to the system, can be expressed by the so-called intrinsic carrier density, which is written as

$$n_\mathrm{i} = p_0 = n_0 = 2\left(\frac{m^\star k_\mathrm{B} T}{2\pi\hbar^2}\right)^{3/2} \exp\left(-\frac{E_\mathrm{G}}{2k_\mathrm{B}T}\right). \tag{3.1}$$

Here, n_0 and p_0 denote the densities of electrons and holes in thermal equilibrium, $m^\star$ is the product of the effective mass of holes and electrons, k_B is the Boltzmann constant, $\hbar$ the Plank

constant and E_G the energy band gap of silicon. As depicted in part a) of figure 3.1, the overlap between Fermi-Dirac distribution with the bands is quite small and at room temperature the charge carrier density is only around $n_i \approx 10^{10}\,\mathrm{cm}^{-3}$, which is orders of magnitude lower than in metals.
However, the real power of silicon is revealed by introducing doping. Doping is a process whereby impurity atoms are added to the bulk material thus, altering the electric properties of silicon. One can distinguish between two types of doping: n- and p-doping. By smart arrangement of areas with p- and n-doping all kinds of unique electrical devices can be implemented on silicon. Among them, the simplest, and at the same time the basis of the SPAD, is the p/n-junction, where an n- and p-doped area are brought into close contact.
N and p-doping is created by adding impurity atoms to the bulk material, which possess either one more or one less valence electron than silicon. Suitable elements are, for example, boron and phosphorous, respectively. These doping atoms create additional energy states in the direct vicinity of the conduction or valance band. The Fermi level is shifted in the direction of the levels provided by the corresponding doping atoms, as depicted in part b) of figure 3.1. In n-type silicon, states in the vicinity of the conduction band are occupied by electrons. Little energy is needed to ionize these states, creating an excess of free charge-carriers in the conduction band. On the other hand, in p-type silicon, energy states near the valence band are empty and can easily be occupied by electrons of the valence band, leaving behind holes. Compared to intrinsic Silicon, the density of electrons and holes is no longer equal. In n-type silicon, electrons are referred to as the majority carriers and holes as the minority carriers and vice versa for p-type silicon. An important equation for silicon is the so-called mass action law, which is written as $np = n_i^2$, with n as electron density and p as hole density in n- or p-type silicon. This means, the product of the electron and the hole density is constant for a given temperature and doping and can be expressed in terms of the intrinsic carrier density.
Bringing both types together, a p/n-junction is formed, which is shown in part c) of figure 3.1. Electrons from the n-type silicon diffuse to the p-region and holes form the p-region diffuse into the n-region. Positive- and negative-charged doping ions are left behind inducing an electric field over the junction. Electrons and holes within the junction drift back into their respective region. A thermal equilibrium is established, where the Fermi-levels of both sides equalize, which corresponds to a bending in the band structure, and a fixed potential across the junction develops, which is called build-in potential V_{bi}. The junction volume depleted of charge carriers, is called the depletion region.

3.1.2 Light Detection with Diodes

In general, applying a bias voltage to the diode structure means to bringing the junction out of thermal equilibrium. The Fermi levels of the p- and n-side will no longer be equal and current starts to flow to re-establish thermal equilibrium again. One can distinguish between two polarities of the applied voltage. These are: forward bias and reverse bias. Both bias polarities are shown in figure 3.2 by means of a voltage current characteristic of the diode. In addition, a schematic band structure in the respective bias condition is also shown. In forward bias, where the polarity opposes the build-in potential, the potential barrier created by the bent band structure is lowered. Hence it becomes more probable that charge carriers gain sufficient thermal energy to diffuse across the barrier. The current increases exponentially with increasing bias voltage and, simultaneously, the depletion region shrinks in size.
In reverse bias, where the applied voltage is of the same polarity as the build-in potential, the potential barrier increases and prevents a significant current from flowing. The depletion region grows in size and diffusion over the barrier becomes unlikely. However, there is still a small current

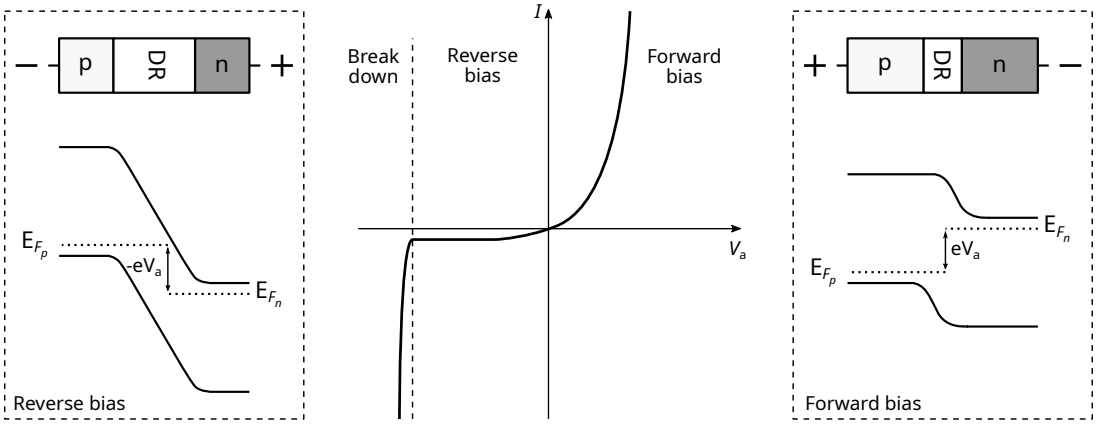

Figure 3.2: In the middle the voltage current characteristics of a p/n-junction is shown. To the left a schematic picture of the band structure in reverse bias is shown, while on the right the band structure in forward bias is shown.

flowing in reverse bias, the so-called leakage current, which is caused by two distinct physical processes: On the one hand, pairs are thermally generated inside the depletion region and on the other hand minority charge-carriers from the p and n-side can diffuse into the depletion region. In the depletion region they are influenced by the electric field, drift towards the respective junction side and a current evolves. The leakage current is the dominant source for noise in an SPAD and will be discussed in detail in section 3.6. For increasing reverse bias voltage, at the so-called breakdown voltage, the junction will break down. This means the electric field inside the junction is high enough, so that charge-carriers moving inside the depletion region gain sufficient energy to eject secondary pairs by impact ionization. Those secondary pairs repeat this process and a large current evolves, destroying the diode if it is not stopped.
A diode in reverse bias can then be used as a photon detector in the visible range of light in the following way: When silicon is exposed to a photon flux, electrons can be lifted to the conduction band if the incident photons transfer a minimum energy equal to the band gap energy of silicon $E_{\mathrm{G}} = 1.12\,\mathrm{eV}$. Photons in the visible range of light possess some 1 eV, and are mostly stopped directly. They create an electron and lose the rest of their energy to the silicon lattice. Therefore, the number of excess charge-carriers is somewhat proportional to the number of incident photons. Pairs created inside the depletion region, are directly influenced by the electric field and drift towards the neutral regions where they are collected. Moreover, the collection happens in the absence of a strong current as only a leakage current is flowing. The collected charge is therefore a measure of the number of incident photons. The depletion region, where the created pairs are directly collected, is referred to as active detection volume.
However, in the special case of a rare event search experiment, where it is necessary to detect single photons, a photo diode is no longer sufficient. A single electron hole pair created by an incident photon cannot be distinguished from the leakage current flowing constantly through the diode [7]. However, an internal amplification can be achieved by exploiting the break down mechanism inside a diode and internal amplification is enabled. A single pair, liberated by an incident photon, gain sufficient energy to eject secondary pairs by impact ionization. They repeat the process and a large breakdown current is triggered, which is easy to measure. However, the breakdown current will not vanish of its own accord. An external circuit has to lower the reverse bias voltage below the breakdown voltage so that the electrons and holes cannot perform impact ionization anymore.

3.1.3 Operating Principle of a SPAD

A SPAD exploits the breakdown mechanism of a p/n-junction to generate a macroscopic, well-defined and equivalent signal for each photon detected. The signal formation is given by three different phases, which are passed in one detection cycle [81]. The first is the triggering of breakdown current, also called avalanche current, followed by the stop of the avalanche current and, finally, restoring the quiescence state again. It has to be mentioned, that the primary process for the breakdown inside the SPAD is impact ionization, which should not be confused with the Zenner breakdown, where tunneling of charge-carriers through the band gap is the primary breakdown mechanism [79].

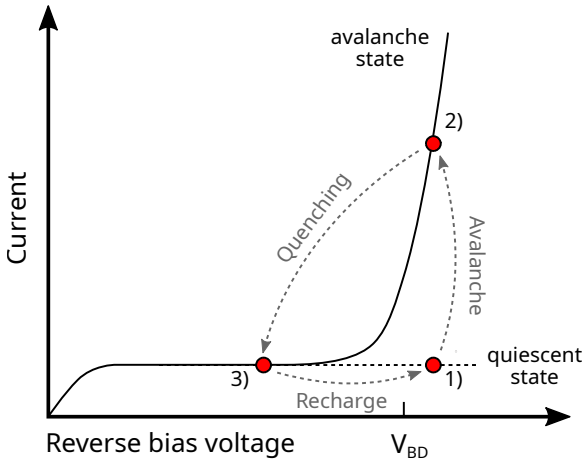

Figure 3.3: Schematic of reverse bias characteristics of a p/n-junction with its breakdown voltage V_{BD}. The points in red are the working points corresponding to the different modes a SPAD passes then detecting a photon: 1) Idle mode, 2) avalanche Mode, 3) quenched mode.

In figure 3.3 the three processes with their corresponding operation points are shown by means of a qualitative reverse bias characteristic of a diode. At point 1) the SPAD is in quiescent state so that the bias voltage V_{A} is above the breakdown voltage V_{BD}, but the avalanche has not yet been triggered. Qualitatively the breakdown voltage $\mathrm{V_{BD}}$ is defined as bias voltage where the electron and hole pair gain sufficient energy to eject secondary carriers by impact ionization. Quantitatively it can be defined by the so called breakdown integral [82], which is written as

$$1 = \int_0^{W_{\mathrm{D}}} \alpha(V,T)\,\mathrm{d}z \tag{3.2}$$

where, W_{D} is the width of the depletion region and α is the ionization rate for electrons and holes, which is defined as the number of pairs created by a charge-carrier traveling a unit length [79]. The ionization rate α is very dependent on the temperature and the electric field inside the SPAD, which, in turn, is determined by the SPAD doping profile and the applied reverse bias voltage (see section 3.4). With a reverse bias voltage equal to the breakdown voltage, the integral reaches unit, which means the primary pair create at least one secondary pair by impact ionization.
The voltage added to the breakdown voltage is called the excess bias, which is given by $V_{\mathrm{Ex}} = V_{\mathrm{A}} - V_{\mathrm{BD}}$. Quantities like the dark count rate (see section 3.6) and photon detection efficiency (see section 3.5) greatly depend on the applied excess bias voltage. The dark count rate or photo detection efficiency of a SPAD array operated at various temperatures are often compared at a constant excess bias voltage $\mathrm{V_{Ex}}$ (see for example [83]).
Finally, in quiescent state, nearly no current is flowing through the diode, apart from a small leakage current. This small current is the primary reason for so-called dark counts, signals which are indistinguishable from photon signals (see section 3.6). In order to detect a low flux of

photons the leakage current has to be well controlled and small.

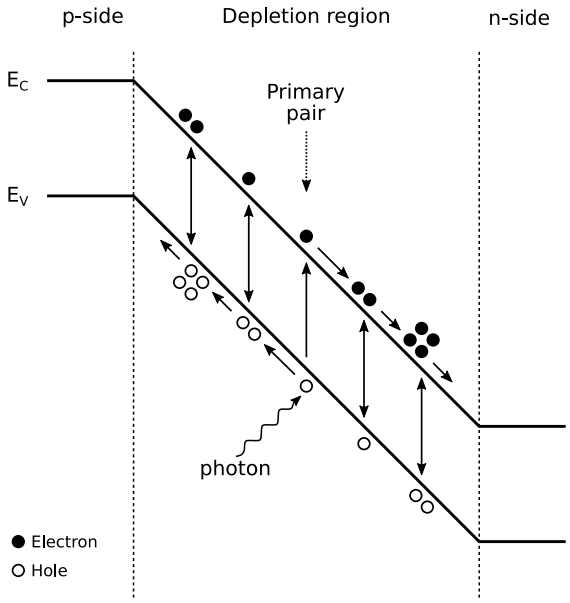

Figure 3.4: Schematic of the avalanche process inside the depletion region of a SPAD. An incident photon creates a primary pair, which itself ejects secondary pairs by impact ionization. The secondary pairs themselves repeat this process and a self-sustained current evolves. For the sake of clarity only the pair creation of the primary pair is shown.

When a photon with an minimum energy of the band gap of silicon $E_g = 1.12\,\text{eV}$, is absorbed in the SPAD it creates an electron hole pair and an avalanche is triggered. Consequently, the operation point shifts to point 2) in figure 3.3. A macroscopic current develops, which is a result of impact ionization performed by electrons and holes. In figure 3.4 a schematic picture of the breakdown process is shown. The initial electron and hole pair drift in exactly opposite directions and both charge carriers-create secondary pairs by impact ionization. On both junction sides new charge-carriers are ejected and they themselves again create secondary pairs. A macroscopic current, which is self-sustained, evolves. The amplitude of the breakdown current settles to a constant value defined by the excess bias voltage and the diode's own series resistance, above which the current flows [84].
In order to prevent the diode from melting and to detect subsequent photons, the avalanche has to be interrupted by setting the bias voltage of the SPAD below V_{BD}. This is done by an external circuit which is connected either to the SPAD anode or cathode. Once quenched, the operation point of the SPAD shifts to point 3) in Figure 3.3. The bias voltage of the SPAD is below V_{BD} and the quiescence state is re-established by increasing the voltage of the SPAD, again, above V_{BD}. For each detected photon this cycle is repeated, whereby, photons absorbed within these cycle wont be detected. The duration of one cycle is therefore also referred to as dead time of the SPAD, which is typically in the order of 100 ns up to 1 µs.

3.2 Manufacture

The basic structure of a SPAD is a p/n-junction embedded in silicon. Two different layouts are typically applied: The planar devices and the so-called reach through devices. In the former the active volume is only several micro meters below the silicon surface while in the later the whole cross-section of the silicon die is used as active volume. A thick active volume is especially useful for the detection of deep-penetrating radiation like infrared photons with energies near or below the band gap. However, to yield an active volume covering the cross section of a silicon wafer with several 100 µm of thickness, the reverse bias voltage has to be in the order of 100 V and the front and back have to be electrically contacted. Furthermore, the large active volume increases

the noise and lowers the timing response [84].
In a planar geometry the p/n-junction is implanted near the surface of the silicon wafer, with the corresponding electrical contacts on the surface of the same wafer side. The depth is, in this case, limited to some micrometers leading to a thin active volume, which is more favorable for photons with short penetration depths, such as optical ones. With a p-type substrate the straightforward implementation of a SPAD is shown in figure 3.5 a).

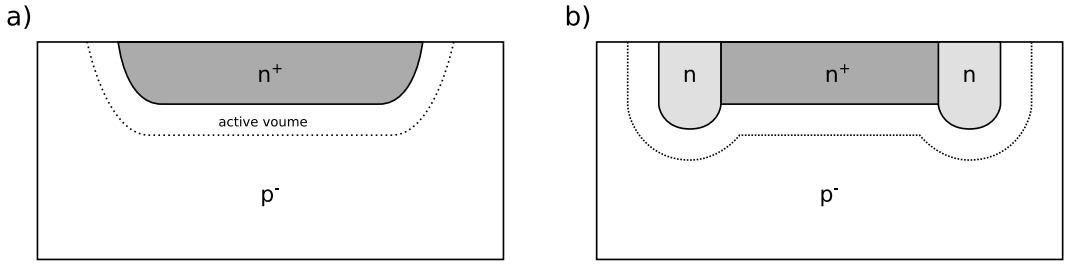

Figure 3.5: Cross-section of a basic SPAD in a p-type substrate and an additional implant to avoid premature breakdowns at the edges: **a)** A strong n doping layer forms the p/n-junction. **b)** A guard-ring structure as n doping implant at the edges of the junction.

Only a strongly n-doped layer near the surface has to be implanted to create a p/n-junction. The n doping also acts as an entrance window for the photons. They have to penetrate this window in order to be detected. A strong and shallow n-implant is therefore favorable. At the same time the electric field created in the junction has to be homogeneous to guarantee a uniform detection efficiency. Sharp curvatures at the edges of the doping profile [85], but also defects in the junction [86], [87], can locally increase the field, leading to an effect called premature breakdown. Here, a small fraction of the volume has a significantly lower breakdown voltage than the rest of the junction, hence the active volume has a highly non-uniform detection efficiency. The edges of the simple diode structure shown in part a) of figure 3.5, which are the result of a implantation process, would without doubt, lead to premature breakdown. To lower the field at the edges, several structures have been established. An overview can be found in [88], [89]. One common solution is a lightly-doped n implantation surrounding the junction. This is called a guard-ring [86]. The cross-section of this structure is shown in part b) of figure 3.5. The guard-ring masks the edges of the junction, and due to its lighter doping, it possesses a higher breakdown voltage than the highly n doped implantation, thus eliminating premature edge breakdown.
The structures shown in figure 3.5 are electrically connected to the bulk material. Free electrons of the bulk can diffuse into the depletion region triggering an avalanche not correlated to a photon. By integrating the p/n-junction into an n-well, it is isolated from the bulk [91]. A doping well is a small volume inside the bulk material which has opposite doping to the bulk, forming a diode-like structure that insulates the inside from the bulk. Figure 3.6 shows the p/n-junction embedded in an insulating n-well with the corresponding electrical contacts, as well as its electric field along the vertical axis. Moreover, the doping profile is extended by a deep n-enrichment implantation below the strong p doping layer at the surface. This sandwich-like structure modulates the electric field such that, within the sandwich, there is a very narrow high-field and a low field region extending into the n-well, as depicted in the field diagram of figure 3.6. Subsequently, the field is divided into a drift region and a thin high-field multiplication region, where most of the impact ionization occurs. The advantage of such an assembly is that

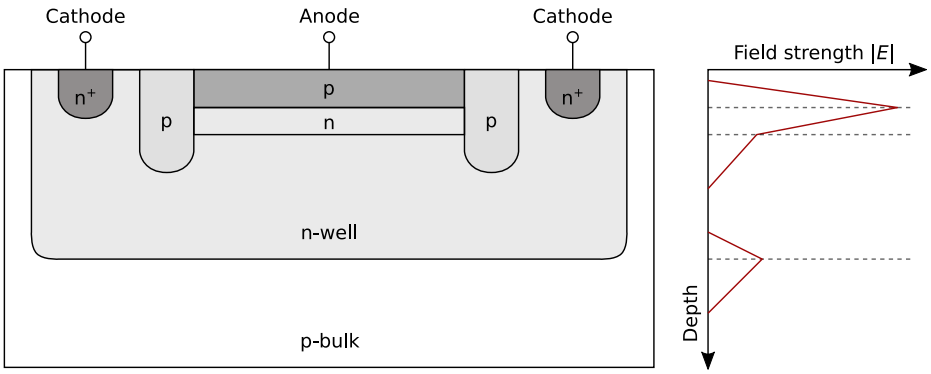

Figure 3.6: Cross section of a p/n-junction with extended doping profile and guard-ring integrated into an n-well. The corresponding electric field strength along the center of the device is shown to the right [90].

carriers created in the drift region have to pass the whole multiplication region, yielding the highest probability to trigger an avalanche [92].
The structure described in the last part of this section was chosen for this work. It is made within a standard 0.35 µm CMOS process and is fully compatible with the given CMOS logic. Readout electronics, quench and recharge circuits are placed next to it on the same wafer substrate.

3.3 Quenching and Recharge Circuits

Only with a small extra circuit, the SPAD can be used as a single photon detector generating macroscopic and well-defined signals for each individual photon. Biased above the breakdown voltage, an absorbed photon triggers a self-sustained avalanche. A current only limited by the series resistor of the SPAD evolves and continues flowing. To prevent the device from breaking and having the possibility to detect another photon, it is necessary to interrupt the avalanche and restore the quiescent state. These two processes are called quenching and recharging and are undertaken by external circuits. A broad variety of different quench and recharge schemes exist, which can roughly be divided into two classes: Purely passive circuits and those which apply feedback to the SPAD. Each solution has its benefits and drawbacks in terms of occupied space, effects on induced noise and maximum rate. In the following the focus of the discussion is on properties most favorable for a low rate experiment. Here, faint photon fluxes will be detected mostly at lower temperatures and therefore maximum speed is not the greatest concern. In figure 3.7 two quenching schemes and their corresponding voltage signals at node S are shown. In addition, a simple equivalent circuit of the reverse bias SPAD is shown in 3.7 a), which consists of a parasitic capacitance C_p, the series resistance R_S and a switchable voltage source [84]. R_S is given by the junction resistance and that of the neutral region, the voltage source is set to the breakdown voltage V_BD and the onset of the avalanche is simulated by closing the switch.
As depicted in figure 3.7, the simplest quench and recharge circuit is a high value ballast resistor R_Q in series with the SPAD. A buffer connected to node S digitizes the SPAD voltage signal, by setting its output to high if the threshold voltage V_th is reached. When an avalanche is triggered at time t_hit, the current rises rapidly due to the discharge of the combined parasitic capacitance C_p of the SPAD and that of node S through the series resistance of the SPAD. Subsequently the voltage $\mathrm{V_S}$ rises exponentially towards the excess bias V_Ex voltage whereas the current falls, in the same manner, to a steady state value provided by R_Q and V_Ex. The steady state current,

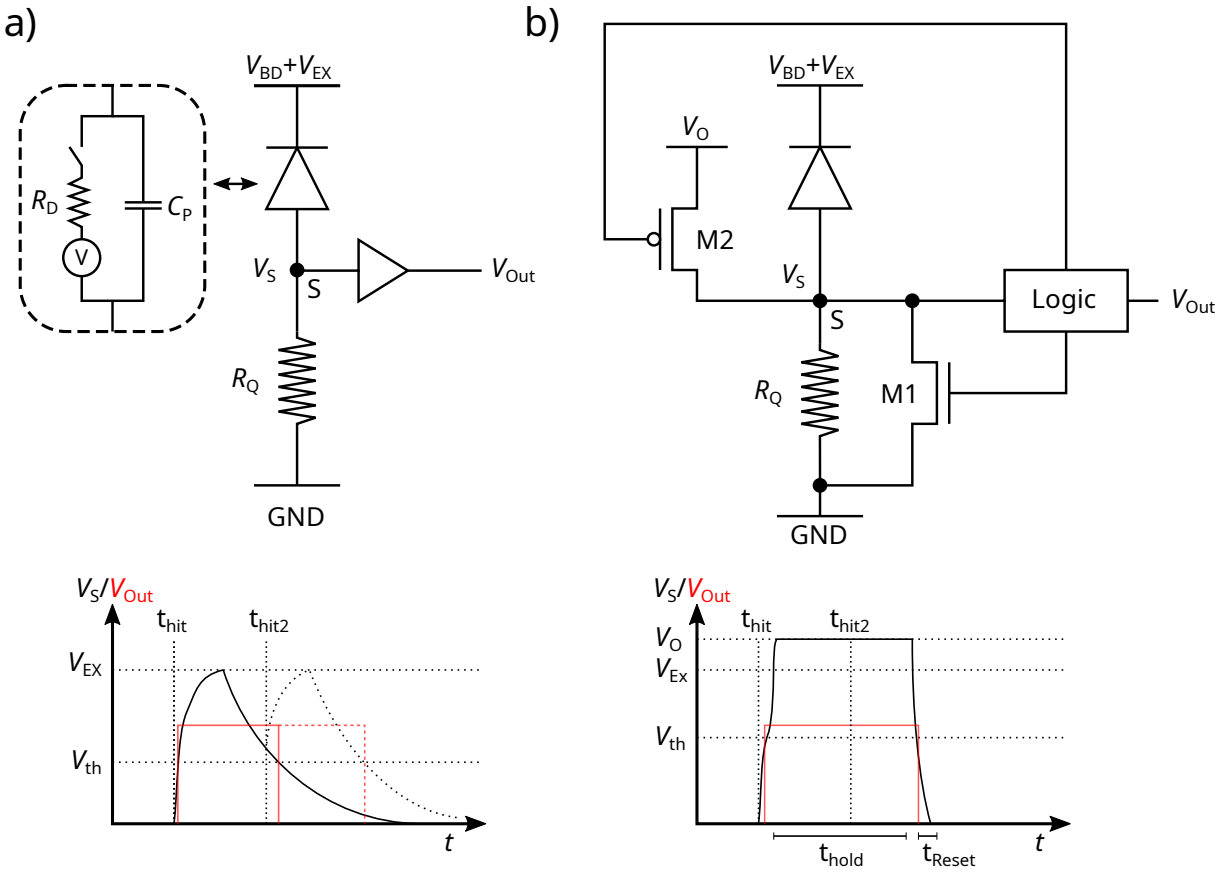

Figure 3.7: SPAD quenching and recharge schemes. a) A passive scheme only using a resistor for the quench and recharge. b) A feedback logic is included, which has the ability to turn the SPAD of with transistor M2 and perform a fast recharge with transistor M1. Below, the circuits voltage signal at node S and the buffers output are shown for one detection cycle.

i.e. the rate of charge carriers traversing the diode, has to be chosen small enough so that the effective probability of said charge-carriers to perform impact ionization is too low to maintain. This condition is fulfilled when the steady state current is below 100 µA and consequently R_Q is in the order of 100 kΩ [84]. After the avalanche is quenched node S will be recharged through the ballast resistor setting up the quiescence state in a slow manner. As $R_S \approx 1\,k\Omega$ is much lower than R_Q the recharge time clearly dominates the overall signal length. Furthermore, it has to be noted that the voltage drop of the SPAD approaches the breakdown voltage but will not drop below it. The SPAD is never really turned off and in fact an avalanche can be triggered before the recharge has finished. On the one hand, this limits the overall detectable rate because the recharge is prolonged as depicted on the lower left side in figure 3.7. On the other hand, which is of more concern for a low-rate experiment, this circuit is prone to afterpulsing. Here, charge-carriers of the primary avalanche, crossing the depletion region, are trapped in energy levels near the conduction band. Those levels are created by impurity atoms and lattice defects and release the charge-carriers after a certain lifetime. Additional avalanches are triggered, which are not correlated to the primary one [93]. A more detailed description will follow in section 3.7.1.
As long as the SPAD is still in recharge, with V_S above the threshold voltage of the buffer, the output signal is only prolonged. If V_S is below the threshold voltage a second signal is created not correlated to a photon. Especially for low temperatures the release time constant of the traps is gets longer and the effect is more pronounced. With the assistance of additional electronics

applying feedback in order to turn off the SPAD for a well-defined time, masking of afterpulsing is possible. Nevertheless the simplicity of the implementation, the reliability and the incomparably small amount of space occupied, are unique features of the resistor circuitry, making it perfect for high density arrays of SPADs.
In b) of Figure 3.7 a simplified schematic of a common feedback quench and recharge circuitry is shown, which can be found, for example, in [94] or [95]. In addition to the resistor, two transistors and a feedback logic are added. The transistors M1 and M2 are off, in quiescent state. If an avalanche is triggered, V_S rises and the feedback logic starts to counteract. M2 is switched on so that node S is charged up to V_O, which exceeds V_{Ex}. In return the SPAD is fully turned off and stays in this mode for a certain hold-off time t_{hold} before the SPAD recharge starts, where M2 is turned off and M1 is enabled. M1 is designed to deliver a high current so that the charge is carried out in a fast manner, as shown in the timing diagram on the lower left side of figure 3.7. In this way, the quiescence state is restored and M1 is switched off again. Throughout this cycle the SPAD is insensitive to additional photon hits or afterpulsing [95]. Furthermore, this logic can be used to turn the SPAD off completely. This yields a reduction of the overall noise if SPADs are disabled that show an enhanced noise level but also comes with the cost of losing active sensing area [94].
However, the additional features explained here, come with the cost of more occupied space thus reducing the fill factor of the overall array. Nevertheless, with a careful designed logic the fill factor can reach high values of more than 70 % without sacrificing those features (see section 4.3).

3.4 Breakdown Voltage

The breakdown voltage is defined as the bias voltage, for which a hole or electron at least creates one additional pair by impact ionization. With the so-called breakdown voltage integral (eq. 3.2) this condition is quantified. However, in silicon the ionization coefficients for electrons and holes, differ and equation 3.2 has to be refined [96]. The breakdown integral for electrons becomes

$$1 = \int_0^{W_{DR}} \alpha_n(E(z),T)\, \exp\left(- \int_0^{W_{DR}} (\alpha_n(E(z'),T) - \alpha_p(E(z'),T))\, dz' \right) dz \tag{3.3}$$

where W_{DR} is the width of the depletion region and α_n and α_p are the ionization coefficients for electrons and holes. To rewrite the breakdown integral for holes, one has only to exchange the ionization coefficient α_n with α_p and vice versa. The ionization coefficients reflect the ability of the charge carriers to perform impact ionization and strongly depend on the temperature and the electric field strength. The field strength defined by the SPAD doping profile and the applied bias voltage, so that breakdown voltage can be yielded by solving equation 3.3. However, typically the complex electric field distribution of the SPAD and the still existing discrepancies among the current theories of the ionization coefficients [97]–[99], prevent an analytic solution. Nevertheless, the discussion of the SPADs breakdown voltage can be held in a qualitative way. Here, two parameters play a key role: Firstly, the field distribution $E(z)$, given by the SPAD doping profile and applied bias voltage, and secondly, the temperature T.
In general, the breakdown voltage increases with increasing width of the depletion region of a SPAD [100], [101]. The increase of width is accomplished by lowering the doping concentration of at least one side of the junction. In figure 3.8 two examples of abrupt p/n-junctions are shown with their respective field and potential distribution along the x-axis [79]. The doping concentration of the n- and p-side of junction b) are four times lower than that of junction a). The horizontal line, marked with E_C corresponds to the critical field which is needed to gain enough energy for impact ionization. As visible in the potential distribution of junction b) the

same peak field strength as in junction a) is only reached by applying a four times higher bias voltage. On the other hand, the depletion region for junction b) becomes four times larger than that of junction a).
Furthermore, since in a wider junction a higher field is maintained over a wider ranger, the probability that a charge-carrier moving is this field triggers an avalanche is enhanced [101]. Consequently, the peak electric field can be lower and therefore the breakdown voltage is actually also lower. So for the example shown above the breakdown voltage for the wide junction is less than four times higher than that of the small one. Widening of the junction is a measure used to reduce tunneling noise, since it depends strongly on the peak field (see section 3.6.3).

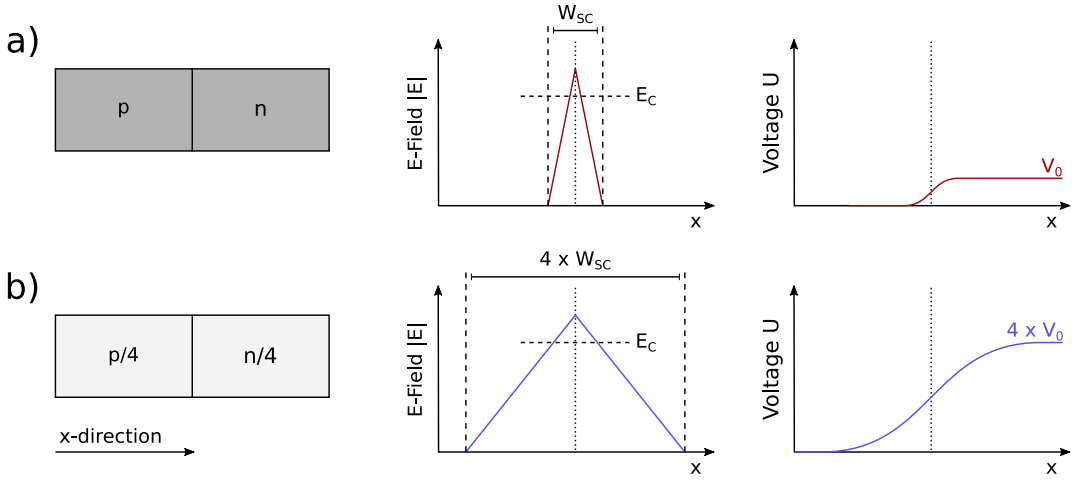

Figure 3.8: Two examples of p/n-junctions are shown with their respective electric field and potential distribution. The critical field E_C, at which electrons and holes gain sufficient energy for impact ionization, is marked with a dashed line. Junction b) has a four times lower doping concentration on both sides compared to a). Consequently, the voltage has to be increased four times to reach the same field strength at the junction boundary, and the breakdown voltage for junction b) is about a factor of 4 higher.

The temperature dependence of the breakdown voltage is determined by the mean free path of the holes and electrons in silicon [102]. To create a secondary pair by impact ionization the charge-carriers have to gain sufficient energy between the scattering process. As the rate of non-ionizing events, like scattering with the lattice structure or phonons, increases with temperature, the mean free path decreases [80]. The field has to be increased, so that charge-carriers can reach the required energy for impact ionization. Consequently, the breakdown voltage increases with temperature.
Besides the absolute value of the breakdown voltage, the temperature coefficient is also a crucial parameter. It determines the stability of various SPAD parameters, like noise and the PDE, against temperature fluctuations of the detector system in which the SPAD is operated [103]. As already mentioned the decrease of the mean free path of the carriers with rising temperatures has to be compensated for with a higher electric field. For a wider junction the applied voltage has to be increased more than for a thinner junction in order to reach the critical field strength. Subsequently, temperature coefficient increase with the junction sizes.

3.5 Photon Detection Efficiency

The photon detection efficiency (PDE) is the ability of a photon detector to detect an individual photon. It is the ratio between detected and all incident photons. For an array of SPAD it is written as

$$\mathrm{PDE}(\lambda, V_{\mathrm{Ex}}) = FF \cdot AE(\lambda) \cdot P_{\mathrm{t}}(\lambda, V_{\mathrm{Ex}}) \tag{3.4}$$

with the fill factor FF, the absorption efficiency $AE(\lambda)$ and the avalanche trigger probability $P_{\mathrm{t}}(\lambda, V_{\mathrm{Ex}})$ [104]. The fill factor is the ratio between active sensing area and the total area of the detector. The absorption efficiency describes the probability of a photon to penetrate the SPAD and actually create an electron hole pair inside the depletion region of the SPAD. The avalanche trigger probability is the probability of the charge carrier-actually triggering the avalanche. It has to be noted that, in [104] the absorption efficiency is denoted as quantum efficiency. However, for most light detectors, the quantum efficiency refers to the probability of detecting a single photon, regardless of the fill factor, and is used as such in this work. In equation 3.4 the quantum efficiency corresponds to multiplication of the absorption probability and the trigger probability. The absorption efficiency and the trigger probability very much depend on the composition of the SPAD [105], which is illustrated in the cross-section of the SPAD shown in figure 3.2.

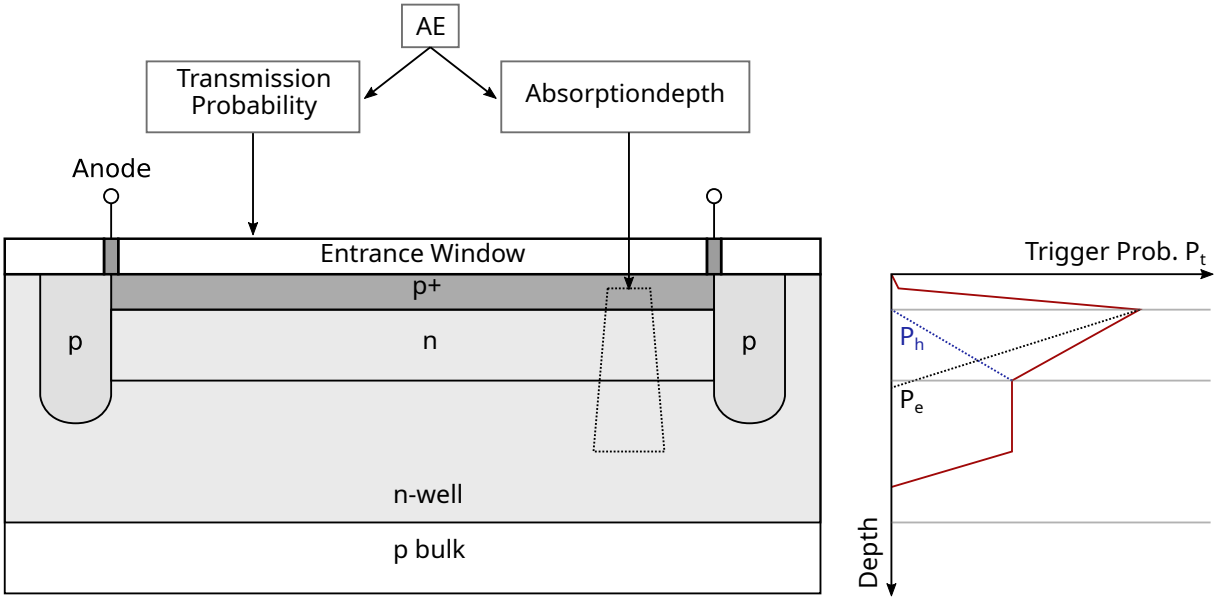

Figure 3.9: **Left:** Cross-section of a SPAD used within this work. The entrance window protects the silicon surface from oxidation but may prevent the photon, by reflection or absorption, reaching it. When it reaches the surface it can be absorbed in the silicon. The longer the wavelength the deeper the photon penetrates in the silicon. **Right:** The avalanche trigger probability P_{t} as function of the depth where the electron hole pair was created by the absorbed photon (taken from [104]).

Part of the absorption efficiency is that the incident must pass though an entrance window above the actual SPAD, which is described by the transmission probability. This topmost layer, typically, is made out of silicon nitrite or silicon dioxide, which protects the doped silicon underneath from further oxidation [90], [106]. Visible light with wavelengths between $400 - 700$ nm mostly passes through it and only a small part is reflected or absorbed [107]. Strong UV light, on the other hand, will probably not be transmitted, so that additional optimizations are needed. These are described in section 4.3.1.

After passing through the entrance window the photon penetrates the silicon, where it is absorbed. The wavelength of the photons determines their mean absorption depth, which is described within the absorption efficiency: Short wavelength light is mostly absorbed within a few 10 nm; that means, in the topmost p-implanted region. More reddish light, on the other hand penetrates several 1 µm into silicon and is absorbed in the n-well [79]. The electron-hole pair created, has the chance to trigger the avalanche when it actually comes in the influence of the electric field. When they are absorbed in the vicinity of the silicon surface or deep inside the n-bulk, the electric field is low (see section 3.2) and has little influence on them so that the charge-carriers can recombine or somehow diffuse in the depletion region. Consequently, the absorption efficiency is very low at those points.
The avalanche trigger probability P_t depends on the depth of absorption and the electric field, which in turn depends on the applied bias voltage. On the right side of figure 3.9 a distribution of P_t as function of the depth, is schematically shown.
Absorbed in the p-side, the electron drifts to the n-side, while absorbed on the n-side, holes drift to the p-side, so that either only holes or electrons trigger the avalanche. Since the ionization coefficient for electrons is larger than for holes, the trigger probability of the electron is higher than that of the holes [108]. Within the multiplication area both carriers take part in the triggering process and P_t is a superposition of the trigger probabilities of both carriers. P_e and P_h decrease towards the n- and p-side respectively, since the trigger probability is highest when the charge-carrier crosses the whole multiplication area [92]. As noted before, close to the surface and deep in the n-well, the field is low and so the chargers mostly recombine before entering the depletion region. Therefore, P_t is very low in those regions. Lastly, with the low absorption depth of short wavelength light, it is obvious that the SPAD shown in figure 3.9 has the highest PDE for those wavelengths and this, then drops towards longer wavelengths [90], [104].
The trigger probability P_t further depends on the SPAD bias voltage V_Ex, since the electric field in the SPAD increases with it. The ionization coefficient of electrons and holes increase rapidly with increasing electric field and so does P_t [109].
Finally, with lower temperatures the PDE seems to increase by a small fraction [83], [110]. The reason for this is attributed to an increase in the trigger probability, as mobility of the electrons and holes increases at low temperatures. However, further investigation is needed for a better understanding of this effect.

3.6 Uncorrelated Noise

Every single electron or hole reaching the multiplication area of the SPAD has the ability to trigger an avalanche. However, the creation of an electron hole pair is not inevitably correlated to a photon absorption. Several physical processes happening inside the SPAD could create charge carrier pairs in the absence of light. These carriers have, indeed, the chance to trigger a well-defined SPAD signal, which is not distinguishable from any photon signal and are called dark counts. Consequently, dark counts disturb the outcome of any counting experiment, especially when their amount is in the same order of magnitude as the flux of photons to be detected. The processes of the generation of these unwanted pairs have to be known and controlled in order to build a detector sensitive enough for DARWIN experiment.
In figure 3.10 an overview over the most prominent generation processes happening inside the SPAD is given by means of a schematic p/n-junction in reverse bias. The source of generation of pairs can roughly be classified into two processes: Thermal generation and tunneling.
In the following section both processes will be discussed in detail with a special focus on their temperature dependency. The latter has a quite unique shape for each process of generation and makes it possible to distinguish between both types of noise. In the third section the relative

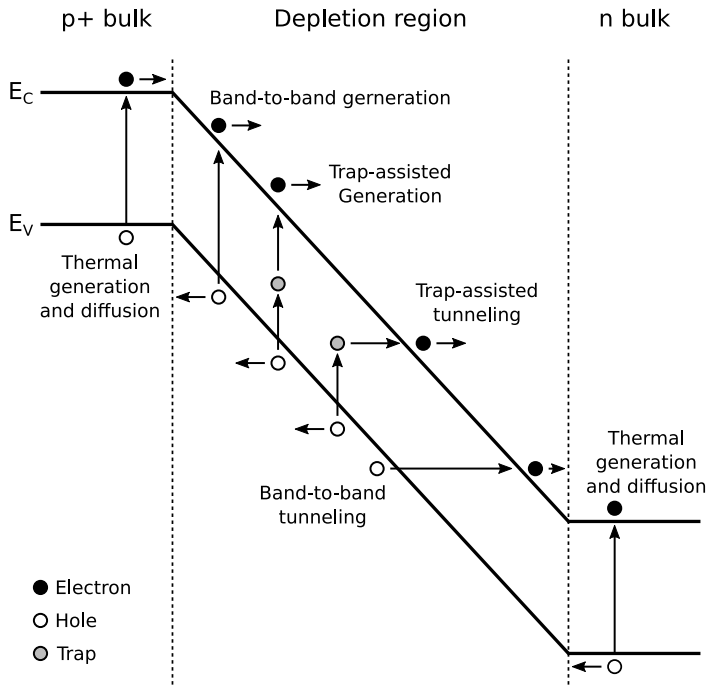

Figure 3.10: A schematic view of a reverse biased p/n-junction with the most prominent processes for generation of electron hole pairs in the absence of light. From the neutral region, carriers can enter the depletion region by diffusion. However, only minority charge carriers have the right polarity to travel through it. Inside the depletion region there is a variety of generation processes taking place, like thermal generation, happening directly or through trap states and tunneling processes induced through the electric field.

weight of the noise sources over a temperature range from room temperature down to $T = 100\,\mathrm{K}$, which is the lowest achievable one for most of the measurements, will be described. Here, the discussion is mostly focused on the means of fulfilling the noise demand of the DARWIN experiment at liquid Xenon temperatures. The chapter closes with the discussion of so-called hot SPADs, which are single SPADs showing a significantly higher amount of dark counts than the average SPAD.

3.6.1 Thermal Generation in the Depletion Region

In general, thermal generation is a process where an electron in the valence band acquires enough thermal energy to overcome the band gap and is excited into the conduction band. A hole is left behind in the valence band and therefore a charge-carrier pair is created. It is a fundamental process occurring in any semiconductor and, due to the nature of the thermal process, it happens randomly but with a constant rate.
If the semiconductor is in thermal equilibrium, generation is always compensated by the reverse process of recombination. Meaning, if an electron comes into the vicinity of a hole it can recombine with it and one pair of charge-carriers is annihilated again. Both processes happen at the same rate, and therefore the electron and hole density stay constant.
Inside the depletion region of a SPAD, obviously only generation can happen, because all free charge-carriers are removed by the strong electric field. Furthermore, the electric field forces each generated pair to directly drift apart and a dark count can be triggered. The rate at which

the generation process happens is therefore directly proportional to the dark count rate and can be understood in the following way: Thermal generation occurs to restore the thermal equilibrium of the system, which means to restore $np = n_\mathrm{i}^2$. However, imbalanced electron or hole densities cannot be restored as only pairs are created and consequently the system tends towards $n = p = n_\mathrm{i}$. The process of generation, on the other hand, creating each single pair, happens randomly but with a certain probability, which can be associated with a lifetime τ. The lifetime is a measure of how effective the generation process is for one pair inside silicon. The generation rate inside the depletion region can then be written as

$$R_\mathrm{G} = \frac{n_\mathrm{i}}{\tau}. \tag{3.5}$$

It has to be noted that the given generation rate has the units of rate per volume. In the further discussion it will be multiplied by the width of the depletion region W_DR so that it can be handled as particle flux and is not confused with the absolute generation rate.
In conclusion, the equation given above shows that the absolute generation rate depends on three quantities: 1) The volume of the depletion region 2) the lifetime of the generation process 3) the intrinsic charge carrier density n_i. The latter itself is an exponential function on temperature (see equation 3.1).

As already shown in figure 3.10, generation inside the depletion region can happen either by

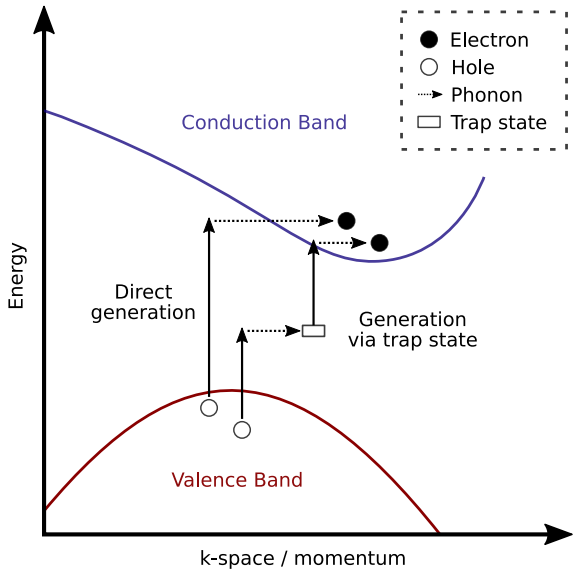

Figure 3.11: Example of the band structure of a indirect semiconductor, in which the minimum of the conduction band and the maximum of the conduction band have different momenta. The direct band to band thermal generation of a pair, and generation via a trap, are visualized.

direct band-to-band excitation or via an intermediate state inside the forbidden band gap. The latter is created by impurities or lattice defects [79]. Consequently, the total generation rate is a superposition of both processes and can be written as

$$\Phi_\mathrm{G} = \left(\frac{n_\mathrm{i}}{\tau_\mathrm{d}} + \frac{n_\mathrm{i}}{\tau_\mathrm{i}}\right) W_\mathrm{DR}. \tag{3.6}$$

with n_i as intrinsic carrier density, τ_d the generation lifetime for the direct transition and τ_i the lifetime for the transition via an intermediate state. The lifetimes of both processes are, however, not equal. As silicon is an indirect semiconductor the valence band maximum and the conduction band minimum, forming the band gap, are separated in the k-space, i.e. the associated states have different momenta [111]. A direct transition from the conduction band minimum to the valence band maximum has to be accompanied by a momentum change of the electron, which is

possible by interaction with a phonon.
In figure 3.11 there is an example of the bandstructure of an indirect semiconductor, in which the direct, as well as the trap-supported transitions are visualized. In both cases the transition has to be accompanied by a phonon interaction. A transition via a trap state is, however, split into two parts. First an electron from the valence band has to occupy the trap state after which it has to be released into the conduction band. Compared to a direct transition, each single process requires less thermal energy and fewer momentum transfers. Although this kind of generation includes two subsequent transitions it is much more likely to happen. A rigorous theoretical calculation in [112], shows that the trap-aided transition is about a factor of $1e+9$ more probable.
The Shockly-Read-Hall Theory [113], [114] states that the flux for the trap-aided generation process, which is called SRH generation noise and is written as

$$\Phi_\mathrm{i} = \frac{n_\mathrm{i}}{\tau_\mathrm{i}} W_\mathrm{DR} = -\frac{N_\mathrm{t}\nu_\mathrm{th,n}\sigma_\mathrm{n}\nu_\mathrm{th,p}\sigma_\mathrm{p}n_\mathrm{i}}{\nu_\mathrm{th,n}\sigma_\mathrm{n}\exp\left(\frac{E_\mathrm{t}-E_\mathrm{i}}{k_\mathrm{B}T}\right)+\nu_\mathrm{th,p}\sigma_\mathrm{p}\exp\left(\frac{-E_t+E_\mathrm{i}}{k_\mathrm{B}T}\right)} W_\mathrm{DR} \tag{3.7}$$

with the trap density N_t, the energy level of the trap E_t, the intrinsic Fermi level E_i, which is approximately the mid band gap level, is the product of thermal velocity and the capture cross-section $\nu_\mathrm{th}\sigma$ for electrons and holes respectively. The flux is proportional to the number of traps, so directly entangled with the purity of the silicon wafer. On the other hand, the probability that an electron enters and leaves the trap is strongly dependent on the ambient temperature and also on the energy of the trap level.

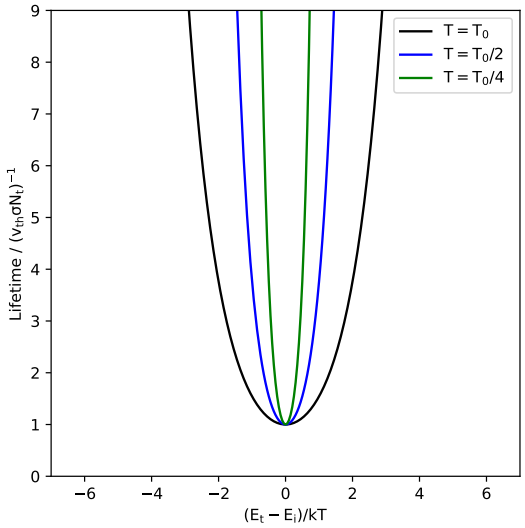

Figure 3.12: Normalized generation life time of electron hole pairs for trap levels around the intrinsic levels and the simple case that $\nu_{\mathrm{th},n}\sigma_n = \nu_{\mathrm{th},p}\sigma_p$. The effect of decreasing temperatures is illustrated by means of half and quarter of ambient temperature T_0.

In figure 3.12 the generation lifetimes for three temperatures are plotted in dependency of the trap energy for the simple case that $\nu_\mathrm{th,n}\sigma_\mathrm{n} = \nu_\mathrm{th,p}\sigma_\mathrm{p}$. Obviously, traps in the direct vicinity of the intrinsic Fermi level have the shortest lifetime and therefore are the most effective generation centers. For trap centers close to the edges of the band gap the lifetime increases exponentially and increases with a decrease in the system temperature.
Finally, thermal generation noise depends on the applied excess bias voltage in two possible ways: With traps exposed to a strong electic field other than thermal realses mechanisms such as tunneling can cause the traps to be emptied, which is described in section 3.6.4. Furthermore, With increasing bias voltage the width of the depletion region and also the PDE increases. The latter makes it more probable that a charge-charrier actually trigger a avalnche.

3.6.2 Diffusion from the Neutral Region

In the neutral region, in the absence of an electric field, charge-carriers move only by diffusion. Those generated in the vicinity of the depletion region can reach the influence of the electric field and drift deeper. However, only minority charge-carriers, meaning electrons on the p-side and holes on the n-side, possess the right polarity to drift through the depletion region and trigger an avalanche. Consequently, a concentration gradient develops within the neutral region [111], where the thermal equilibrium density of the minority charge-carriers, far away from the edge of the neutral region, decreases to zero at its edge. Newly generated charge-carriers tend to diffuse to the low concentration area and the constant rate of generation leads to a stationary gradient. According to Ficks first law of diffusion this gives rise to a constant flux of charge-carriers entering the depletion region. For a one dimensional or isotropic junction, the total rate of charge-carriers diffusing into the depletion region is a superposition of the rate from the p- and n-side and is then written as

$$\Phi_{\mathrm{D}} = n_{\mathrm{i}}^2 \left(\frac{D_{\mathrm{n}}}{L_{\mathrm{n}} N_{\mathrm{A}}} + \frac{D_{\mathrm{p}}}{L_{\mathrm{p}} N_{\mathrm{D}}} \right) [115]. \tag{3.8}$$

Here, n_{i} is the intrinsic carrier density, D_{n} is the diffusion constant and L_{n} the diffusion length for electrons in the p region. D_{p} and L_{p} are the respective constants for holes in the n-region. N_{A} and N_{D} are the doping concentrations of acceptors and donors in the p- and n-doped regions, respectively. With increasing density of the minority carriers at thermal equilibrium, given by $n_{\mathrm{i}}^2/N_{\mathrm{A/D}}$, and with a decreasing diffusion length, the gradient in concentration is enhanced and, therefore, the rate increases. The diffusion length is the mean length a minority carrier can travel before it recombines and can also be stated as recombination lifetime with $\tau = \sqrt{DL}$, where D is the diffusion constant in silicon. If the physical size of the neutral region becomes smaller than the diffusion length of the carriers the diffusion length has to be limited to the diode's physical size [115]. Moreover, it has to be noted that diffusion of minority carriers is not limited to the main p/n-junction but takes place at every location where n-silicon meets p-silicon [116]. So, for example, the guard-ring structure, as a boundary for the SPAD multiplication region, is also a source of diffusion (see section 3.2).
Being a function on the minority carrier density and the diffusion length, the diffusion rate depends strongly on temperature. The former decreases exponential with temperature (see equation 3.1), while the temperature dependency of the latter is determined by the diffusion constant, which is given by the Einstein relation and can be written as

$$D = \frac{\mu_{\mathrm{n/p}} k_{\mathrm{B}} T}{e}. \tag{3.9}$$

Here $\mu_{\mathrm{n/p}}$ is the mobility of electrons or holes and e the elementary charge. However, the dominate part is clearly the intrinsic carrier density. Compared to the flux of charge carriers generated inside the depletion region, which is, according to equation 3.7, proportional to the intrinsic carrier density n_{i}, the diffusive flux shows a stronger temperature dependence as it is proportional to n_{i}^2.
Finally, diffusive noise does not direct depends on the applied excess bias voltage and therefore the electric field inside the SPAD. However, the probability that, a charge-carrier traversing through the depletion region triggers an avalanche increases (see section 3.5), so that the number of dark counts increases.

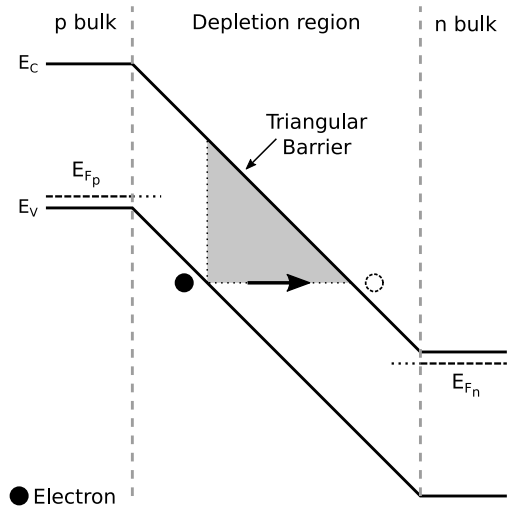

Figure 3.13: Illustration of an electron tunneling from the valence band through the band gap into a free state in the conduction band. The potential barrier through which the electron tunnels has a triangular shape. The width and therefore the tunneling probability is modulated by the field inside the depletion region.

3.6.3 Tunneling Noise

Tunneling is a quantum mechanical process, where a particle traverses a potential barrier with finite height, which is larger than its own energy. Within this process no energy is consumed or gained by the particle. In figure 3.13 the process of tunneling inside a reverse-biased p/n-junction is schematically shown. An electron from the valence band, tunnels through the bend band structure into an unoccupied state of same energy in the conduction band. A hole is left behind in the valence band and the newly created pair starts to drift apart. The rate at which tunneling happens depends on two quantities: 1) The shape of the potential barrier 2) The number of occupied states inside the valence band with the same energy as unoccupied states in the conduction band.
The potential barrier is approximately triangular shaped and the tunneling probability, can be written as

$$T_{\mathrm{T}} = \exp\left(-\frac{4\sqrt{2m^{\star}}E_{\mathrm{G}}^{3/2}}{3e\hbar F}\right) \tag{3.10}$$

where, E_{G} is the band gap energy, $m^{\star}$ is the effective mass of an electron, e the elementary charge, $\hbar$ the reduced Planck constant and F is the mean electric field strength inside the junction [117]. The probability increases with the field strength since the width of the barrier decreases with the field. On the other hand, tunneling is nearly independent on temperature: The band gap increases with decreasing temperature but the changes are very small. For example, the difference between room temperature $T = 296\,\mathrm{K}$ and $T = 100\,\mathrm{K}$ is $\Delta E = 0.04\,\mathrm{eV}$ [118], while E_{G} is in the range of 1 eV. Finally, the dependency on the effective mass of the electrons, which is lowest at the conduction band minimum and the valence band maximum [80], makes the tunneling most likely to happen between those points. For silicon this again means a tunneling transition is accompanied by a phonon. This will be discussed later in this section.
The number of occupied states in the valence band, facing unoccupied states of same energy in the conduction band, depends on the applied reverse bias voltage. Qualitatively, this is associated with the increasing distance between the valence edge of the p-side and the conduction band edge of the n-side. Within the depletion region nearly no free carriers are available, consequently the higher the difference of the edges, the more bound electrons of the valence band, face unoccupied states in the valence band.

The flux of electrons tunneling through the band gap is then written as

$$\Phi_{\mathrm{t}} = \int_{E_{\mathrm{V}}}^{E_{\mathrm{C}}} \left[F_{\mathrm{C}}(E) - F_{\mathrm{V}}(E)\right] T_{\mathrm{t}} N_{\mathrm{C}}(E) N_{\mathrm{V}}(E) dE \tag{3.11}$$

where E_{V} and E_{C} are the energies of the valence and conduction band edges, T_{t} is the tunneling probability shown in equation 3.10, N_{C} and N_{V} are the density of states and $F_{\mathrm{C}}(E)$ and $F_{\mathrm{V}}(E)$ are the Fermi-Dirac distribution functions for the conduction and valance band, respectively [119].
As already mentioned, for silicon the tunneling transition needs a phonon interaction for a momentum change. Including phonons indeed reduces the tunneling probability compared to the case of direct semiconductors [117], but also complicates an analytical theoretical description. Various attempts were taken to gain a solution, for example [117], [120] or [121]. However, a simplified model is presented in [122], which is commonly used in device simulation (for example [107]). In this model the tunneling rate is given in dependency on the energy of the electrons, which is determined by the electric field [122]. The tunneling rate is written as

$$R_{\mathrm{t}}(E) = -B \left|F\right|^{\frac{5}{2}} D(E, F, T) \exp(-F_0 / \left|F\right|) \tag{3.12}$$

with the maximum of the electric field strength or peak electric field strength $|F|$. The temperature independent material constant B includes the phonon contribution to tunneling [123]. The exponential term corresponds to the tunneling probability. The so-called critical field F_0 includes the temperature dependency of the band gap [122], [123]. The function $D(E, F, T)$ depends on the energy of the initial electrons, the field strength and temperature and modulates the flux with respect to the number of states available for the transition from the valence to the conduction band. $D(E, F, T)$ is unity until the energy of the incoming electron is close to one of the band edges, where it goes to zero [122].
In conclusion, the tunneling rate is mostly dependent on the electric field inside the depletion region, but only weakly dependent on temperature. It forms a natural limit for the SPAD noise, where in contrast to thermal generation further cooling leads to no improvement. Only changes of the SPAD peak electric field strength can lower the rate of tunneling (see section 4.3.1).

3.6.4 Traps in an Electric Field

Impurities and defects inside the silicon lattice form so-called trap states located in the band gap, which, as described in section 3.6.1, increase the thermal generation rate. When, in addition, these trap states are inside the depletion region, they are exposed to an electric field, leading to a significant enhancement of the generation rate [124]. The emission process of the charge carrier is affected by the Poole-Frenkel effect and the occurrence of tunneling. However, the charge carriers still enter the trap by thermal excitation. In figure 3.14 an example of a trap state exposed to the electric field of depletion region is illustrated. For holes, this picture is equivalent, though they enter the trap from the conduction band and leave it towards the valence band.
The potential of the trap can either be coulomb-like, which is the case when the trap is ionized by the emission of the charge-carrier, or Dirac-like if no charge effect is involved [122]. In the case of a coulomb-like potential, the emission rate is enhanced by the Poole-Frenkel effect: The tilting of the coulomb potential in the electric field, compared to the Dirac potential, leads to a reduction ΔE of the barrier height, which facilitates thermal escape of the trapped charge carrier [125].

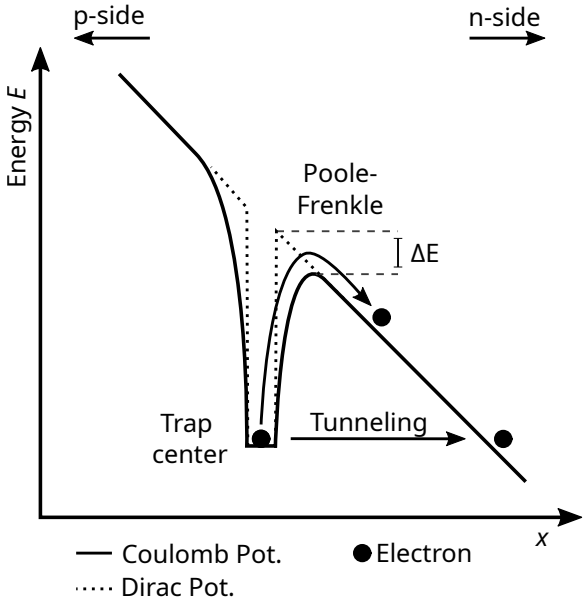

Figure 3.14: The potential of a trap state exposed to the electric field of the depletion region. The potential can either be coulomb like, if the trap is ionized then the electron leaves, or Dirac-like when charge effects are not involved. The Poole-Frenkel effect eases thermal escape in the case of a coulomb potential by lowering the barrier. Tunneling on the other side is possible for both potentials.

Tunneling out of the trap state on the other side is very similar to pure band-to-band tunneling [126]. However, the energy barrier is significantly lower and shorter in width, making it more likely than without a trap state.
Both effects result in an effective reduction of the generation lifetime, such that the generation rate given by equation 3.7 can be rewritten as

$$R_{\mathrm{i}} = \frac{n_{\mathrm{i}}}{\tau_{\mathrm{i}}}\Gamma(E) = \frac{n_{\mathrm{i}}}{\tau_{\mathrm{i,eff}}(E)} \tag{3.13}$$

with the enhancement factor Γ and effective lifetime $\tau_{\mathrm{i,eff}}$ [124]. The SRH generation rate becomes dependent on the present electric field, which was only indirectly included in equation 3.7. Here, with increasing field the depletion region enlarges and the photon detection efficiency increases (see section 3.5). The consequence is that defects located in the strong electric field, like inside the multiplication area of the SPAD, significantly increase the noise of this SPAD compared to one where a trap is located in the drift region. However, the temperature dependency of thermal generation via traps stays roughly the same. The Poole-Frenkel effect only lowers the barrier, so that the emission lifetime is reduced [127] and tunneling is only weakly dependent on temperature.

3.6.5 Temperature Dependence of the Dark Count Rate

The SPAD intrinsic noise composes thermal generation, which are minority charge-carriers diffusing in the depletion region or SRH generation (see section 3.6.2 and 3.6.1), and electrons tunneling through the band gap. While the contribution of thermal generation in general decreases rapidly as temperatures drop, tunneling remains largely unaffected. A typical SPAD at room temperature has a dark count rate dominated by thermal noise, which then rapidly decreases as temperature drops and eventually falls below tunneling noise. The latter will not decrease significantly for further cooling and builds a natural noise limit. In Figure 3.15 several dark count rate temperature profiles are shown, which are composed for values found in literature. The lines in black are examples of tunneling contributions and the lines in green and red are diffusive noise and generation SRH noise contributions, respectively. For simplicity, tunneling noise is assumed to be constant, as its variation with temperature is small (see for example [107]). Diffusive and SHR generation rates as a function of temperature are calculated by

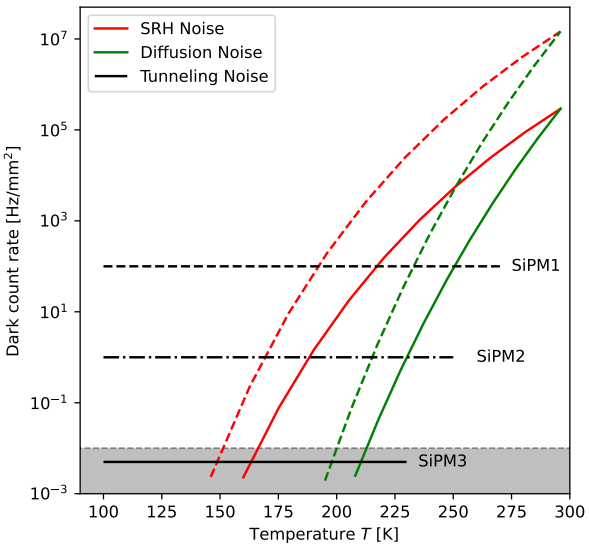

Figure 3.15: Several simulated dark count rate temperature profils of a SPADs. Shown in black are typical tunneling noise limits, of which the values are taken from [83], [128]. The area in grey corresponds to the noise constrain of the DAWRIN experiment of $0.01\,\mathrm{Hz\,mm^{-2}}$ at $T = 165\,\mathrm{K}$. The green line is temperature profil of diffusive noise and the red line that of SRH noise. The dashed line is the upper limit, while the solid lines are the lower limit for thermal generation rate typicaly found for SPADs [129]–[131].

means of equation 3.8 and 3.7, respectively. For simplicity only the temperature dependency of the intrinsic carrier density is considered, which mostly dominates the temperature dependency, in both equations, the rest is kept constant. Lastly the gray area shows the noise constraint of the DARWIN experiment.

With respect to the DARWIN experiment, the SPAD noise level at liquid xenon temperatures of $T = 165\,\mathrm{K}$ should be below $0.01\,\mathrm{Hz\,mm^{-2}}$ (see section 2), which, on the one hand constrains the tunneling noise and on the other hand also the thermal generation contribution.

At lower temperatures the tunneling contribution is dominant. The three black lines in the example correspond to three different SiPM arrays. The tunneling noise level of the SiPM1 [83] and SiPM2 [128], which are SiPMs designed for room temperature usage where thermal generation dominates, are orders of magnitude higher than required, whereas, SiPM3 [128] was optimized for low temperature usage. For this, tunneling was successfully reduced by lowering the peak field strength inside the depletion region, since tunneling strongly depends on it (see section 3.6.3). It is an essential step to reduce the peak field inside the SPAD to actually reach a low tunneling noise contribution at liquid Xenon temperatures.

At higher temperatures thermal generation is the dominant noise source. Typical values for thermal generation noise at room temperature are between $100\,\mathrm{kHz\,mm^{-2}}$ and $10\,\mathrm{MHz\,mm^{-2}}$ [129]–[131]. The solid and the dashed lines mark those upper and the lower noise limits. The green line is a simulated temperature profile of the noise when diffusion noise dominates, while the red line corresponds to a simulated temperature profile in which SRH noise is dominant. As can be seen in figure 3.15, diffusive noise drops more rapidly with temperature as it is proportional to n_i^2 (see eq. 3.8), while SRH generation rate is only proportional to n_i (see eq. 3.7). The upper limit for SRH noise (red dashed line) even crosses the design goal of DARWIN below liquid xenon temperatures of $T = 165\,\mathrm{K}$ such that it would still be dominant. Consequently, DARWIN's noise limit of $0.01\,\mathrm{Hz\,mm^{-2}}$ cannot be reached. This was actually observed for SPAD arrays with highly optimized tunneling level [132]. Obviously, it is necessary to decrease SRH noise as well as possible, which means introducing nearly no defects during manufacture.

However, the measurement of individual SPADs in a large array also showed that only a fraction of the SPADs, so called hot SPADs (see next section), actually suffering from SRH generation noise [123]. The average SPADs are mostly defect free and, for these, diffusive noise is dominant. Consequently, switching these hot SPADs off leads to a SPAD array where diffusive noise is dominant at high temperature and no extensive improvement of material cleanness is required.

3.6.6 Hot SPADs

In a SPAD array so-called hot SPADs are SPADs, which show a significantly higher noise level than the average SPAD. Their noise can be orders of magnitude higher and therefore they impair the overall noise performance of the array [133], [134]. Particularly, due to their high activity, they strongly increase the influence of crosstalk in the neighboring SPADs. For the DARWIN experiment where the noise is constrained to be below $0.01\,\mathrm{Hz\,mm^{-2}}$ (see section 2.4.3), it is essential to switch off hot SPADs and operate the array at its genuine noise performance. Naturally, this also means a loss in active area of the detector.
A SPAD is "hot" when it contains one or several impurities creating trap levels, which are situated close to the center of the band gap [123]. Those trap levels are most likely introduced while the arrays fabrication. Two prominent examples are so-called E-centers and contaminations with tungsten. The first are phosphorous doping atoms, which are next to an atomic vacancy, causing an open bond [135]. They create a trap level situated about 0.4 eV below the conduction band edge. Tungsten, on the other hand, is used for electrical contacting of the silicon surface [136] and creates a trap level situated 0.37 eV above the valence band [137].
As already described before, mid band gap traps are most efficient for thermal generation. Exposed to the SPAD electric field their generation rate is further enhanced (see section 3.6.4). Moreover, with increasing active area it is more probable that at least one defect is included. The fraction of hot SPADs increases with the size of the active area of the single SPAD [90].
With trap levels as a cause, the temperature dependency of their noise is the same as for SRH generation which is proportional to the intrinsic carrier density. Towards lower temperature the generation rate drops very rapidly and at a certain temperature it may drop below the tunneling noise level (see previous section). Consequently, the hot SPAD becomes indistinguishable from a normal one so that, at lower temperatures, the number of hot SPADs should decrease. Fewer SPADs have to be turned off and the loss in active area is not so drastic.

3.7 Correlated Noise

Besides the intrinsic noise sources of the SPADs, extensively discussed in the previous sections, there are signals induced by processes inside the SPAD itself, or somewhere in its close vicinity. This kind of noise is known as correlated noise and can be categorized into three main groups: Afterpulsing, crosstalk and, though quite unique for CMOS based SPAD arrays, emission of light and charge by the circuitry surrounding the SPAD. All those effects are described briefly, qualitatively and with respect to their temperature dependence within this section.

3.7.1 Afterpulsing

While the avalanche current is flowing through the depletion region charge-carriers can be captured by trap levels located in the band gap. After a certain life-time they are released and can trigger a subsequent avalanche not correlated with an incident photon [93]. However, not every electron triggers an avalanche (see section 3.5), so that the probability to create a so-called afterpulse depends on the amount of released charge-carriers. Furthermore, it is strongly influenced by the employed quench and recharge circuit of the SPAD. Afterpulsing is quantified as the probability that on a primary SPAD signal one or more secondary signals follow [138].
The amount of released charge-carriers is determined by the number of traps inside the depletion region and the number of charge carriers-crossing it during the primary avalanche [93]. The number of traps decreases with increasing purity of the wafer material. The charge flow depends on the applied excess bias V_{Ex} and the SPADs capacitance, which decrease with the width of

the depletion region and increase with the active area (see section 3.3). Finally, the release of the trapped charge-carriers is a statistical process, where the number of releases decreases exponentially in time. The lifetime of this process is given by the energy level of the trap state and increases towards lower temperatures [139].
For an active feedback circuit with programmable hold time, in between which the SPAD is turned off, afterpulsing can be completely masked. Though towards lower temperatures the increasing lifetime introduces a long hold time, decreasing the maximum detectable photon rate. For a passive quenching circuit on the other hand, it depends on the recharge status. Due to the exponential behavior of charge release most of the carriers exit their trap within a short period of time. The trigger probability in an early recharge state is very small due to the present low excess bias voltage, which also recovers exponential in time (see section 3.3). However, the trap lifetime is prolonged at low temperatures so that the release time is in the order or even longer than the recharge time. In this case the afterpulsing probability increases rapidly towards lower temperatures [83], [110], [140].

3.7.2 Optical Crosstalk

Crosstalk is an induced noise signal, where an avalanche in one SPAD causes a signal in another SPAD somewhere in the array. The origin are photons created by the avalanche current inside the depletion region. Crosstalk signals can be divided into direct prompt ones and delayed ones [141]. In the first case the photons are absorbed directly in the depletion region of another SPAD while in the latter case they create an electron hole pair in the undepleted region. The charge-carriers then are able to diffuse into the depletion region, causing a signal with a delay of around 1 ns compared to the primary signal.
Crosstalk is quantified as probability that a primary signal triggers a secondary event in the surrounding SPADs. The probability depends on the number of emitted photons and also on the SPADs spacial extension and arrangement in the array.
The underlying mechanism for the photon emission are accelerated charge-carriers of the avalanche, so-called hot carriers, which relax inside the valance and conduction band itself or perform recombination between conduction and valence band [142], [143]. Silicon is an indirect semiconductor, so that radiative recombination is, in orders of magnitude lower, compared to a direct semiconductor (see section 3.6.1). The spectrum of the emitted light is broad [144], [145] with its main part situated in the infrared, which is most important for crosstalk. While photons of shorter wavelength are most likely absorbed in the same SPAD, those infrared photons are able to travel several 10 µm in the silicon and be absorbed in a neighboring SPAD [146].
The number of emitted photons increases with the number of charge-carriers flowing through the depletion region while the avalanche is active [104]. The charge flow depends on the SPAD capacitance and the applied excess bias (see section 3.3). Whereas, at higher bias voltages the PDE of the SPADs also increases, so that neighboring SPADs are more sensitive to emitted photons.
Within the array, crosstalk is reduced by a larger pitch between the SPADs while a high lateral and transverse expansion of their active volume increases it [147]. With additional measures like optical isolation between the SPAD either by isolating trenches or doped layers the probability for direct crosstalk can be reduced [147], [148].
A temperature dependency of crosstalk has, so far, not been found [83], [132], [140]. Neither the PDE nor the photon emission mechanisms seem to be affected by temperature.

3.7.3 Photon emission of MOSFET transistors

A noise contribution that is important and quite unique for the CMOS SPAD, which are studied in this work, is introduced by the readout logic placed next to the SPAD: MOSFET transistors emit photons when drawing current [149], [150]. A well-known phenomenon which is even exploited in the so-called photo emission microscopy to debug integrated circuits [151], [152]. For a more detailed description of the MOSFET transistors the reader is referred to [79] or [111].
Very comparable to optical crosstalk in the SPAD, high fields at the drain diode of the MOSFET in saturation mode, cause the carriers to gain a large amount of kinetic energy. Becoming so-called hot carriers, which perform relaxation inside the valence and conduction band or make transitions between these bands [142], [153]. Band-to-band transitions need, as stated before, a momentum change so that the emission rate much lower than for light emitting devices built of direct semiconductors (see section 3.6.1). Again, the resulting spectrum is dominated by red light [154]. Those photons are able to penetrate deep into silicon and trigger the nearby SPAD (see previous section). The rate of emission increases with the electric field and the current inside the MOSFET [154].
An efficient way to reduce the photon emission is to implement the readout electronics in pure CMOS logic. Then a charge flow and subsequent photon emission only happens on a change of the polarity of the logics input and output signals, that is, when its active [151]. Consequently, logic with a low signal load and without active clocking should keep the emission rate very low (see section 4.3).
Finally, with regards to low temperatures, the emissions seem to increase, if the MOSFET is operated with constant bias voltages [155]. The mean free path length increases with decreasing temperatures. When the electric field distribution, i.e. the applied bias voltage, is kept constant the mean energy of the hot carriers increases, which makes a radiating transition more likely. As CMOS logic is operated at constant bias, at lower temperature the photon emission rate could increase. Moreover, with decreasing temperature the SPADs intrinsic noise drops very rapidly so that the photon emission can become the SPAD's dominant noise source.

4. Digital SiPM Readout Architectures

In this chapter the Digital SiPM arrays are described, which were characterized and developed within this work. All of these are manufactured by the IMS in Duisburg [156], [157]. Their CMOS technology has a minimum gate width of 350 nm and four metal layers are available for signal and power routing.
Most of the measurements and array developments were concerned with the question as to whether Digital SiPMs are a suitable light detector for the DARWIN experiment. If so, they would present an alternative to the currently used PMTs [4]. A first insight into the low temperature operation of Digital SiPMs was given by the single photon camera, called IDP2, which already existed at the start of this work.
Encouraged by the already low noise level of the IDP2, the decision was made to develop a first Test chip for the DARWIN experiment. However, to be competitive with PMTs two intrinsic SPAD parameters had to be optimized: Firstly, the noise at liquid xenon temperatures and secondly, the photon detection efficiency for xenon scintillation light ($\lambda = 178\,\mathrm{nm}$). Our manufacturer, IMS, aimed to improve both parameters by variations in their SPAD technology, which have been included in the array submission. The latter, however, was an engineering run, where our work group produced several novel designs for different applications. One of these designs concerned a time resolved single photon camera, which was also developed as part of this work.
This chapter starts with a brief revision of the difference between Digital SiPMs and standard SiPMs. Then the individual arrays are described. First the IDP2, then, in detail, the DARWIN Test array with its process variations and finally, the time resolved single photon detector.

4.1 SiPMs and Digital SiPMs

In a standard Silicon Photomultiplier (SiPM) all SPADs are connected in parallel, which is shown schematically on the left side of figure 4.1. Biasing and readout is done via the two common terminals A and B. The output signal of the SiPM is a superposition of all the SPAD signals so that the voltage, or current amplitude at the output, is a measure of the number of incident photons [101]. Three examples of signals are depicted on the lower left side of figure 4.1. For the readout of these signals an analog amplifier is needed. These are mostly charge or trans-impedance amplifiers [158]. With respect to the DARWIN experiment this topology, has the drawback that the detection of individual photons in a very low flux demands a power-consuming high gain amplifier [158]. Even with a highly optimized readout circuit operated at low temperature, the power consumption will be in the order of 80 mW [159].
Digital SiPMs on the other hand are special SPAD arrays, where CMOS logic can be fabricated alongside the SPADs. An example is depicted on the right side of figure 4.1. A simple CMOS discriminator, consisting of two subsequent CMOS inverters, connected to the SPAD anode, is sufficient to digitize its signals. During the avalanche the anodes have a peak voltage roughly equal to the applied excess bias voltage [89]. Consequently, when the bias voltage is equal or higher than the threshold voltage of the first CMOS inverter ($\sim$0.8 V) and a signal is triggered, the CMOS inverter changes its output voltage level from the supply voltage level $V_{\mathrm{DD}} = 3.3\,\mathrm{V}$ to ground potential (0 V). The discriminator outputs a digital signal, with a pulse width corresponding to the duration of the SPAD signal. No additional analog amplification is required for recovering the signal of an individual SPAD. The digital signals are then directly processed, by a tailor-made readout architecture, placed on the very same chip. A fully functional single

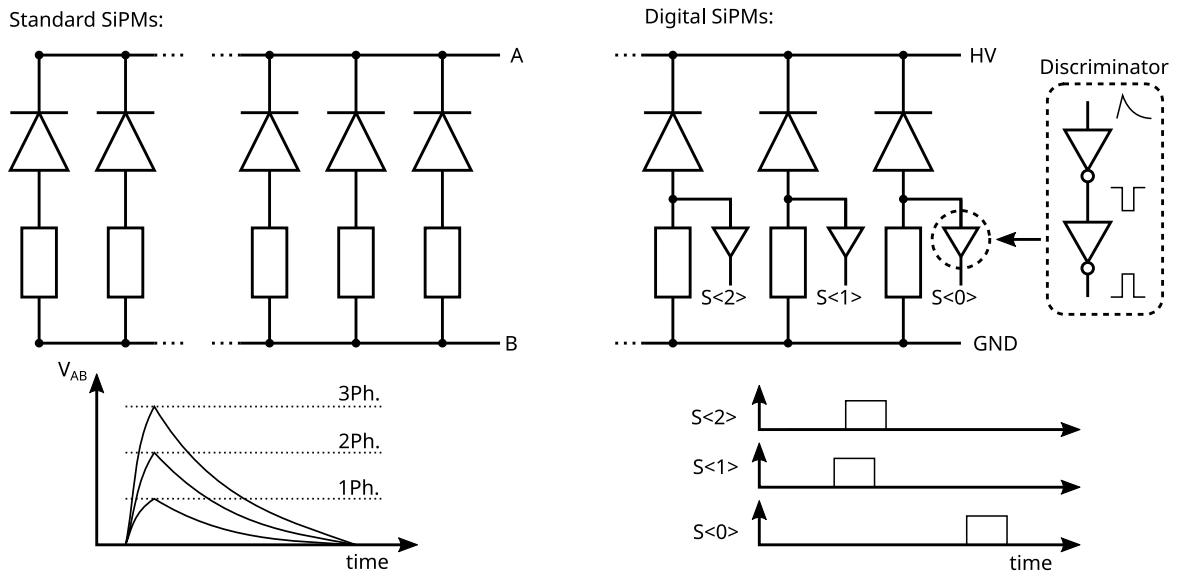

Figure 4.1: **Left:** Standard SiPM, where all SPADs are connected in parallel. The output signal, example shown below, is a superposition of all SPAD signals. **Right:** Digital SiPM, where CMOS logic can be placed alongside the SPAD. Each SPAD is read out individually by a simple discriminator connected to the anode, digitizing the signals. The individual single photon signals are illustrated below.

photon detection system is created on a single silicon dye.
With respect to the DARWIN experiment, digital SiPMs offer the following advantage: An array with the power consumption of only a few 1 mW (see section 4.3) can be implemented. By reading out the individual SPADs, a spacial resolution down to the SPAD level is naturally available. With a little extra circuit alongside the SPAD, afterpulsing can be controlled and noisy SPADs disabled, reducing the overall noise level of the detector (see section 3.3). Moreover, having only a single chip significantly simplifies the mechanics, which is most helpful for a large detector system (see for example [160]).
Nevertheless, the additional CMOS electronics brings certain drawbacks: First the electronics increase the amount of dead area and therefore the fill factor is reduced. Then, due to the CMOS fabrication, the number of hot SPADs is higher and mostly the noise and also the photon detection efficiency is worse than for standard SiPMs [161], [162]. Finally, the lower temperature performance, which was extensively studied for standard SiPMs, is, for digital SiPMs, still an open question.

4.2 IDP2: Single Photon Camera

The Digital SiPM array called IDP2 is a single photon camera (of which a micro photograph is shown in figure 4.2), was the starting point of the low temperature noise measurement campaign. It was already available, at the start of this work and its rather simple readout logic makes it suitable for first low temperature tests. The name IDP stands for Interpolating Digital Photosensor and is derived from its predecessor [163].
The IDP2 is a single photon camera, which delivers binary 2D images containing the one bit hit information of all SPADs. The highlights of this array are the remarkably high fill factor of about 55 % and the fast frame-wise readout which has a frame rate of up to several 100 kHz. Possible applications for this fast single photon camera are, for example, readout of a fast scintillating

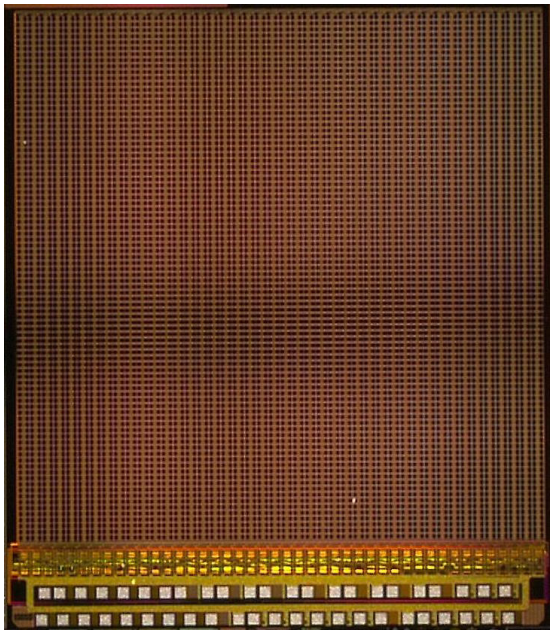

Figure 4.2: Photograph of the single photon camera IDP2.

crystal in particle or medical physics [162], [163] or florescence lifetime imaging in biology applications [164]. The array is comprised of 88×88 pixels with a size of $56 \times 56\mu m^2$ and a SPAD size of about $40 \times 45\mu m^2$. Photons are detected and recorded over the course of a programmable accumulation time window, in which all pixels are enabled. A one-bit hit buffer, present in each pixel, saves the hit information until the next readout. After closing the accumulation time window, the readout of the single pixel data is carried out by means of horizontal shift registers running along each column of the matrix and a vertical shift register on the bottom of the matrix. Furthermore, a hit multiplicity logic is implemented, scanning the columns for coincidence hits, which can be used for a self-triggered mode. A more detailed description of the multiplicity logic can be found in [163].

4.2.1 Pixel Electronics

A schematic of the electronics inside the pixel is depicted in figure 4.3. The SPAD is passively quenched with a polysilicon resistor of $500\,k\Omega$, connected to its anode. A negative bias is applied to the resistor while the cathode is connected to the supply voltage V_{DD}. The terminal to readout the SPAD signal is the anode, which is AC coupled to the CMOS discriminator (see previous section). With the AC coupling, the SPADs n-well (cathode) can be at supply voltage V_{DD} potential, so that it can be merged with the PMOS n-well. In this case the layout is denser and the fill factor higher, compared to an array where the cathode is biased with a high voltage and the discriminator is directly connected to the anode (see section 4.1).
The SPAD signal is digitized as soon as the voltage at the input node surpasses the threshold ($\sim$0.8 V) of the discriminator. A variable load transistor recharges the input node again, with a recharge current provided by current mirror and adjustable through the bias voltage V_{AC}. Furthermore, hit signals can be simulated, i.e. electrically injected, for test purposes, by triggering the inject signal.
A hit signal from the discriminator sets the Hit flip-flop, while the accumulation signal is active. The duration of the this signal is programmable and on its ending the matrix readout can start:

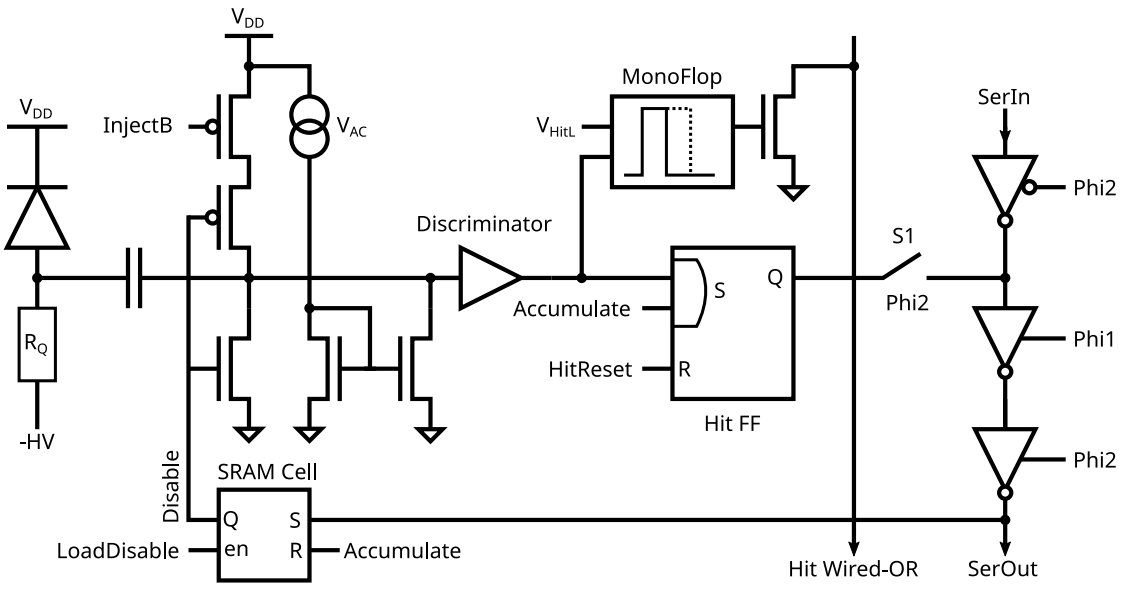

Figure 4.3: Schematic of the pixel electronics. The SPAD is passively quenched and AC coupled to the discriminator. While the accumulation single is high a SPAD signal sets the hit flip-flop. By closing S1, the hit bit is transferred to a dynamic shift register, which shifts the data to the bottom of the matrix. The fast hit wired-or, common to all pixels in a column, is as rate monitor.

By closing the switch S1 the hit bit is transferred to a compact dynamic shift register. While the bit is shifted through the pixel matrix, the flip-flop can be reset and a new accumulation can be started. The readout process can be pipelined, which minimizes the array deadtime.
Additionally, the discriminator signal triggers a monoflop, of which the output pulse width can be adjusted via V_{HitL}. The monoflop pulse triggers, in return, a fast Hit-Wired-Or, to which all pixels of the respective column are connected. At the bottom of the matrix a multiplicity logic receives those signals and filters for coincidence hits [163].
By the means of switching transistors every pixel can be en/disabled individually. The control of this is carried out by the same shift register used for the data readout. An SRAM cell, depicted in the lower part of figure 4.3 holds the disable bit. When the Load Disable Signal is activated the corresponding shift register value is written to the SRAM cell. However, disabling of the pixel, means only masking the SPAD output. The disable transistor switch is turned on, permanently forcing the input node to ground. The SPAD signals will no longer surpass the threshold of the discriminator. This passive masking scheme is a safe spacing alternative to an active one, which switches off the SPADs, as shown in section 4.3.3. The drawback, however, is that hot SPADs remain active and can cause extensive crosstalk particularly when the array is operated in a low light environment as in the DARWIN experiment.

4.2.2 Matrix Readout

The frame-wise readout of the matrix is performed using column-wise shift registers and a horizontal shift register that runs along the bottom of the matrix. In figure 4.4 a schematic of this readout scheme is shown. In the actual implementation each column hosts two interleaved shift registers and at the bottom of the matrix also two horizontal shift registers are employed. This doubles the readout speed compared to a single register per row and one horizontal one.

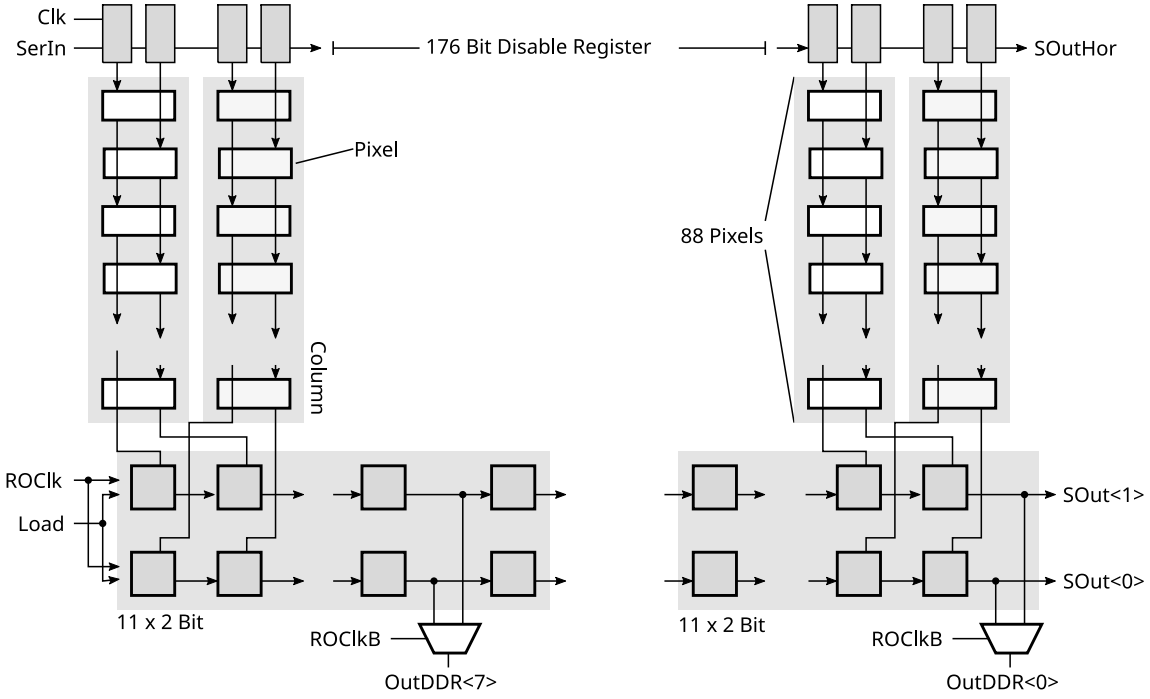

Figure 4.4: A schematic of the IDP2 matrix readout. Two interleaved shift registers per column transfer the pixel data to the bottom of the matrix. With the latter, two horizontal shift registers further transfer the data presented in the last row, to the output pads. With 8 parallel intercepting double data rate ports, which is a multiplexer controlled with the inverse readout clock, a faster readout can be achieved.

The pixels in a column are alternately connected to one of the two shift registers, making it, in total, 44 pixel stages with two outputs at the bottom of the column. The outputs of the columns are distributed on two serial shift registers made of 88 stages running along the bottom of the matrix. By activating the ROLoad signal, the data of the undermost row is loaded in the shift register and ready to be clocked to the serial outputs $\mathrm{SOut}\langle 1:0\rangle$ with the ROClk signal.
For further enhancement of the readout speed, eight intermediate data outputs are present, which are named $\mathrm{OutDDR}\langle 7:0\rangle$. These are distributed along the double row shift register after every eleventh stage. A multiplexer chooses which of the two lines is to be sampled, which is controlled by the inverse data clock signal ROClkB. Effectively a double data rate register is created, where in each clock cycle both data bits are presented on the output. In theory, when clocking the shift register at a 100 MHz and utilizing the parallel outputs, a frame rate of 200 kHz is reached.
Finally, at the top of the matrix a horizontal 176-bit long shift register is implemented, used for the matrix configuration. As mentioned in the previous section, through the column wise shift registers the disable bits are transferred to the pixel. To program the whole matrix 44 programming cycles of the shift register are needed.

4.2.3 Slow Control

The array's slow control includes three digital signal multiplexers, one analog multiplexer and four Digital to Analog Converters (DAC), which are configured via a shift register. Each part of the slow control consumes seven bits for configuration making the shift register 56-bit long. The digital signal multiplexers are used to monitor internal digital signals, such as, for example, the

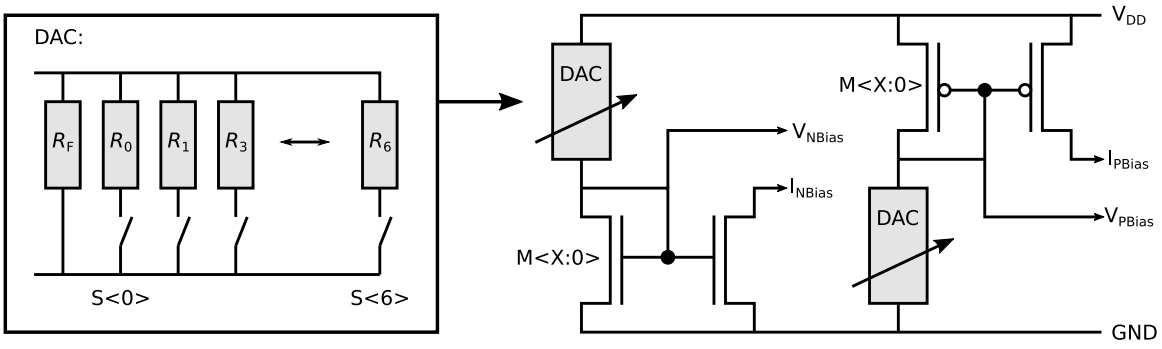

Figure 4.5: **Left:** The DAC consists of seven switchable and one permanent resistor connected in parallel.**Right:** Two examples of circuits using the DAC from the left side, to create bias voltages or currents for analog NMOS or PMOS transistors used within the IDP2 array. By further adding MOS transistors in parallel, indicated by M$\langle X:0\rangle$ the bias can be finely adjusted in the hardware.

output of the very same shift register or those of the multiplicity logic. One can freely select one of eight signals to output. The analog multiplexer, on the other hand, is used to output one of eight current or voltages biases set up by the DACs. With the latter, two biases needed in the pixel electronics are provided and the other two are for the multiplicity logic. A schematic of a DAC can be seen on the left side of figure 4.5.
A DAC comprises seven switchable resistors, R_0 to R_6, and one fixed resistor $R_\mathrm{F} = 1.15\,\mathrm{M\Omega}$ in parallel. Here $R_0 = R_\mathrm{F}$ and the resistors are fabricated out of poly silicon. Towards the higher order selection bit, the value of the resistors drops with $R_i = R_1/2^i$, so that, for example, $R_6 = R_0/64$. The switches are closed by setting the corresponding bit. On the right side of figure 4.5 the principle of using the DAC to create bias voltages and currents for NMOS and PMOS transistors can be seen. By having multiple transistor stages of the current mirror, which is indicated by M$\langle X:0\rangle$ one can further adjust the biases in the hardware.

4.3 DARWIN Test Array and Process Variations

Within this work a dedicated test array for the DARWIN experiment was developed, which is described in this section. The purpose of this array is to test if Digital SiPMs can meet the most basic constraints of the DARWIN experiment. The following list recaps on these constraints, which were discussed in detail in section 2.4:

- The dark count rate at liquid Xenon temperatures ($T = 165\,\mathrm{K}$) has to be $\leqq 0.01\ \mathrm{Hz\,mm^{-2}}$.
- The quantum efficiency at wavelengths of 178 nm has to be $\geqq 20$ %.
- Highest possible fill factor.
- Low power dissipation of roughly a few $1\,\mathrm{mW\,cm^{-2}}$.

The dark count rate and the quantum efficiency at $\lambda = 178\,\mathrm{nm}$ are intrinsic parameters of the SPAD and both were not sufficient at the time of the design of this array. The dark count rate at liquid Xenon temperatures was measured with the IDP2 and is about $35\,\mathrm{Hz\,mm^{-2}}$ (see section 6.4). The quantum efficiency, on the other hand, is for this extremely short wavelength,

mostly zero [157]. However, both can be optimized and within the submission of this array these issues were tackled by process variations developed by the manufacture and, are described in the next subsection.
The high fill factor and the low power dissipation can be greatly influenced by a smart pixel design and a tailor-made readout architecture. In the design of the test array great emphasis is placed on both parameters but, at the same time the readout architecture should be simple and reliable for the characterizations of various process variations of the SPADs. Again, this array is intended to test the basic constraints and a dedicated readout architecture for the S1 and S2 signals is clearly the matter of successor arrays. The DARWIN test array is depicted in the middle of figure 4.6, it is composed of 19×19 pixels and has an overall size of 6.1×5.9 mm^2.

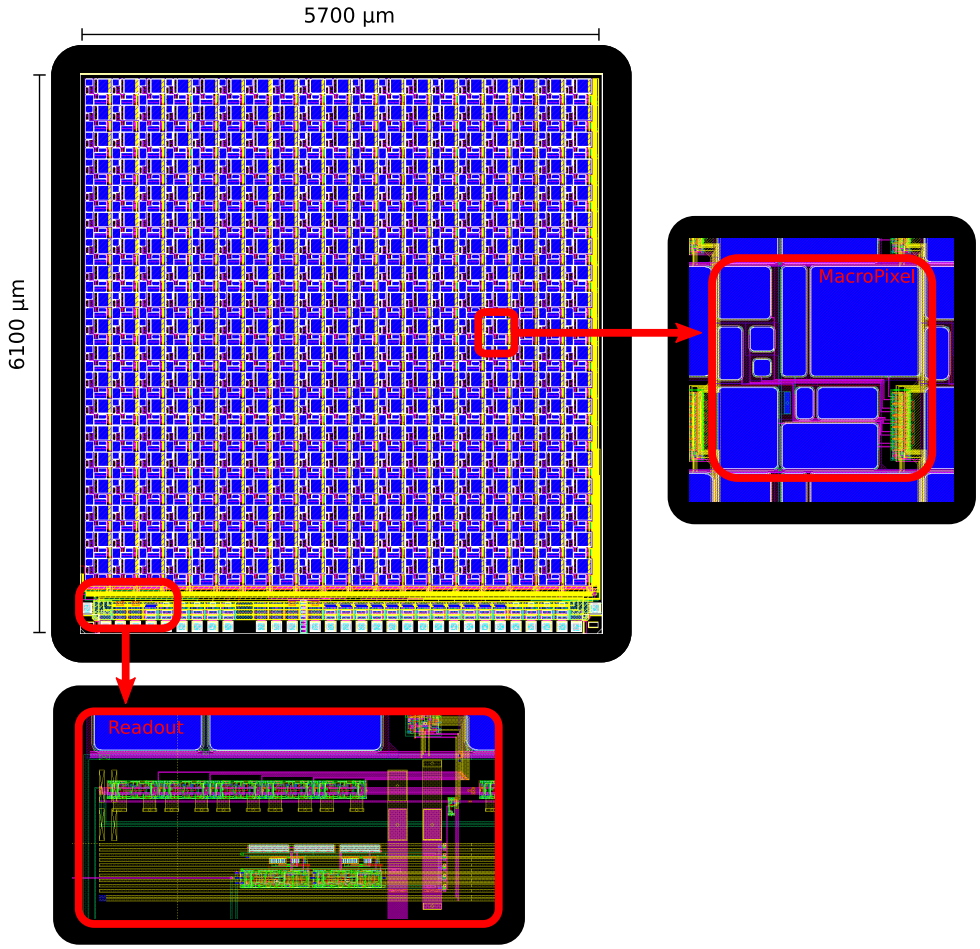

Figure 4.6: In the middle a picture of the DARWIN Test array is visible. To its right a zoomed in view to the Macropixel structure is visible, which consists of ten SPADs and one readout electronics. The SPADs are marked in blue while the readout electronics are highlighted by a green box. On the bottom a part of the layout of the readout electronics is depicted.

The so-called macro pixel, which is depicted on the right side of figure 4.6, is the key feature to optimize the fill factor. It comprises ten SPADs of different geometry, which are shown in blue, but only one readout circuit, which can be seen on the lower right. On the one hand, minimizing the electronics inside the pixel is a straight-forward way to a improve the fill factor. On the other hand, the SPAD size plays a central role to further increase it. Large area SPADs offer a high fill

factor, but very few measurements on these were undertaken, especially at lowest temperatures. Their behavior in terms of noise is unknown and this should be investigated with a variety of SPAD sizes included in the macro pixel. The number of ten SPADs is arbitrary and does not necessarily match the number of SPADs in the future macro pixel.
The readout architecture is data driven and composed of pure CMOS logic to achieve both a low power dissipation and simplicity. A small fraction of the layout can be seen in the lower part of figure 4.6. The functionality is very simple, it is composed of only a few logic building blocks and works the following way: The readout becomes active when a SPAD inside a macro pixel emits a signal and delivers the binary address of the hit pixel, otherwise its idle. In principle, power is then only consumed in the short active period and therefore the overall power consumption should be well below 1 mW.
In the following sections an overview of the macro pixel with all its different SPADs will be given and the impact of the SPAD geometries on fill factor will be discussed. Then, the SPAD front-end circuitry and readout electronic of the macro pixel will be described. Lastly an overview of the peripheral electronics and the slow control is given.

4.3.1 Process Variations

Within the submission of the DARWIN test array process variations of the SPADs were undertaken by the manufacturers at IMS. The aim is it to tackle the two most constraining SPAD parameters for the DARWIN experiment. The first is the dark count rate at liquid xenon temperatures and the second is to enhance the PDE for xenon scintillation light with a $\lambda = 178\,\mathrm{nm}$ (see section 2). In total, eight wafers with technology variances were fabricated.
Operated at liquid xenon temperatures $\mathrm{T} = 165\,\mathrm{K}$, SPADs mainly suffer from tunneling noise (see section 3.6.5). With its strong dependency on the electric field inside the SPAD, a central step to reduce it is to lower the peak field strength inside the depletion region of the SPAD (see section 3.6.3). A reduction in noise of several orders of magnitude was already demonstrated in [132] or [128]. In total three wafers with reduced peak fields were fabricated which were, characterized by means of the DARWIN test array. These three wavers are referred to as process variation 1, 2 and 3 in the latter sections of this work. Process variation 2 has, by far the lowest peak field followed by 1 and finally 3. The absolute value of the peak fields is not known.
For the PDE at UV light, variations in the entrance window of the SPAD and the top most p-implant of the SPAD are done. The top most protective layer of the SPADs covers the bare silicon surface (see section 3.5). It is thinned down to some 10 nm to minimize absorption in it [165]. The p-implant of the SPAD must also be thinned, since most of the UV light will be absorbed in the vicinity of the surface and the charge-carriers will most likely recombine (see section 3.5). In the so-called PureB Process [166] a layer of Boron of about 1 nm thickens is placed on top of the bare silicon, replacing the p-implant. UV photons are absorbed more likely in the vicinity of the surface, where the multiplication area now is, and are detected. Four wafers with UV sensitive enhancements are fabricated, including further steps not reported here. However, the measurement of these were beyond the scope of this work and a detailed description has to be postponed to a future publication.

4.3.2 Macropixel: Layout

The macro pixel is intended as a test structure for different SPAD sizes and is an initial step towards a key structure for a future high fill factor array. The latter means having several SPADs and only a small readout electronic. A picture of its layout is depicted on the left side of figure 4.7. The macro pixel has a size of $290 \times 290\ \mu\mathrm{m}^2$ and comprises ten SPADs, of which

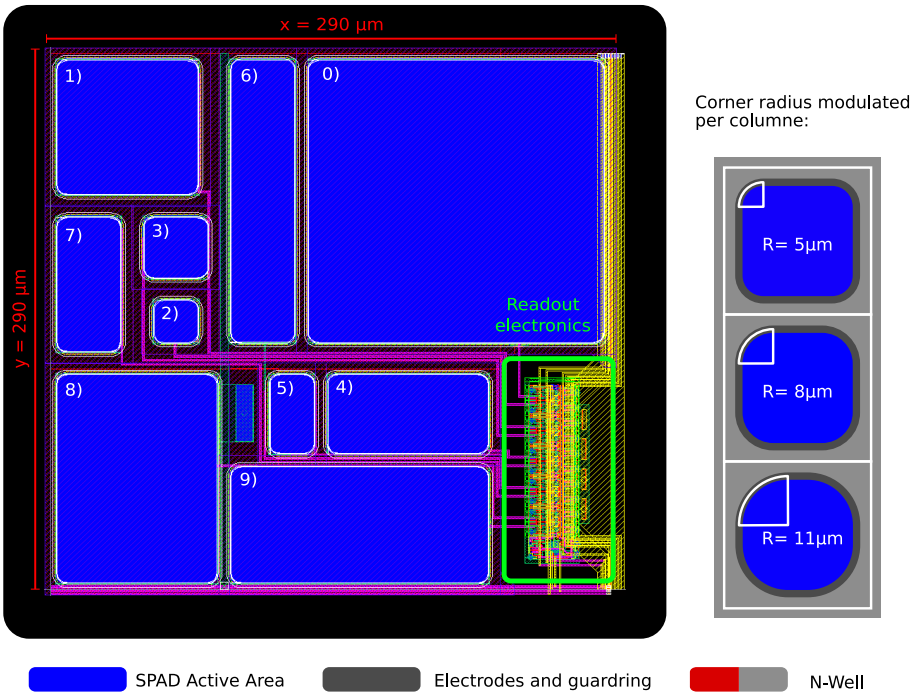

Figure 4.7: **Left:** Layout of the Macropixel, which is comprised of ten SPADs, where the active area is marked in blue and one readout electronics marked with a green frame. **Right:** Three different corner radii of the SPADs, which are implemented column wise. The N-Well on the left side is shown in faint red, whereas on the right side it is depicted in gray for a better clarity.

the active area is marked in blue, and one readout electronics marked with a green frame. Each SPAD cell is marked with a number, which corresponds to the order in which they are connected to the readout electronics.
The SPADs are square shaped, which allows a dense packaging, minimizing dead area [167]. They have rounded corners and the active area is surrounded by a guard-ring (see section 3.2) which is depicted as a white frame in figure 4.7. Furthermore, the SPADs are placed in a common high voltage n-well, which minimizes their pitch. The n-well is marked in faint red in figure 4.8 and spans the area of the macro pixel only leaving free the space of the readout electronics. The bias voltage for the SPADs is supplied via a single wide contact in the center of the n-well. However, as this macro pixel is mostly intended as a test structure the packaging is not yet fully optimized. To examine if the SPAD corner radius has an effect on the noise performance, their corner radii are modulated. Three different corner radii are implemented and change per column of the matrix. A schematic of the resulting SPADs is shown in the lower right of figure 4.7. With a rounder corner, the electrical field could be more uniform, avoiding high field regions, which in turn lead to a higher tunneling noise at low temperatures (see section 3.6). However, at room temperature it has already been proven that there is no difference between very round corners and more squared shape SPADs [168].
The size and aspect ratio of the ten SPADs housed inside the macro pixel are listed in the table shown on the left side of figure 4.8. The list is sorted by the SPAD size, with the smallest SPAD first and the largest last. Having ten different SPAD allows the dark count rate to be measured as a function of the size with a fairly fine gradation. As already mentioned in the previous section, in future arrays the number of SPADs can differ. On the right side of figure 4.8 the

corresponding fill factor of the SPADs are visible. From small SPAD sizes the fill factor increases rapidly, until an active area of about 0.01 mm^2, where the fill factor is about 80 %. Above this size the fill factor converges slowly towards 100%.

Nr.	SPAD size X x Y [µm]	Aspect ratio [%]
2	30.0 × 30.0	100
5	30.0 × 50.0	60
3	40.0 × 40.0	100
7	40.0 × 80.0	50
4	90.0 × 50.0	56
6	40.0 × 160.0	25
1	80.0 × 80.0	100
9	140.0 × 70.0	50
8	90.0 × 120.0	75
0	160.0 × 160.0	100

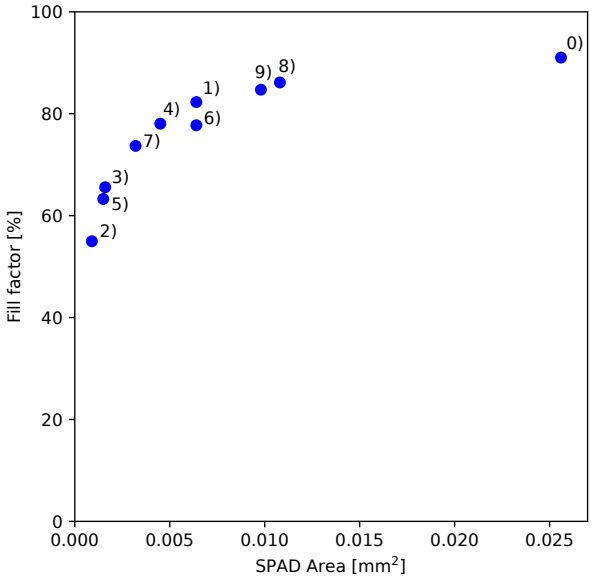

Figure 4.8: **Left:** List of the sizes and the aspect ratio of the ten SPADs shown on the left of figure 4.7. **Right:** Fill factor of the ten SPADs of the macro pixel. The numbering corresponds to the one in the list on the left. For increasing SPAD sizes the fill factor converges towards 100%.

It is clear that large SPAD sizes with their high fill factor are preferable for the DARWIN experiment (see section 2.4.3). From the theoretical point of view there is nothing against the use of large SPADs. According to the discussion in section 3.6 the dark count rate at a constant over voltage and temperature should only depend on the area of the SPAD. So, replacing several small SPADs with only one large SPAD will not impair the overall noise.
In practice, however, there are two effects that worsen the noise performance, making small SPADs more preferable, at least at room temperature: First, SPADs of this technology, having a large active areas above 0.007 mm^2, were shown to have a dark count rate more than proportional to the area [90]. A deviation of up to one order of magnitude was measured for sizes above 0.015 mm^2. So that in the worst case, small SPADs reach the required noise level of the DARWIN experiment but large ones are significantly above, which limits the usable size and therefore the fill factor.
Secondly, the number of so called hot SPADs, SPADs with significantly higher noise than the average SPAD (see section 3.6.6), increases with the SPAD size [90]. These hot SPAD have to be switched off to operate the array at its genuine noise performance. Apparently, switching off SPADs means losing active area and, in return, effectively reducing the fill factor. Especially for large SPADs this effect can be quite drastic. Consequently, using a smaller SPAD size may lead to a overall higher fill factor of the array, so that there is somehow an optimal SPAD size. However, with the IDP2 it was also observed that the number of hot SPADs decreases at lower temperature (see section 6.5), which shifts this optimal SPAD size towards higher SPAD sizes.
With this SPAD test structure both, the dark count rate and the number of hot SPADs can be measured as a function of the size and shape to determine the optimal size and shape for a future array.

The last part is the readout electronics of the macro pixel, which is also a crucial part for the fill factor and is shown in figure 4.9. The circuitry has the dimensions of 55×125 µm^2 and is placed outside the shared n-well of the SPADs. Its functionality is minimal to reduce the amount of electronics. It comprises only three basic blocks, of which the description follows the section after the next: 1) An array of ten SPAD front ends, one for each SPAD, including the quench and recharge circuit for the SPAD readout. A turquoise frame highlights this block. 2) A ten bit Enable Register for turning off or on the individual SPADs, marked with a green frame. 3) A SPAD signal processing and control block, which sends the SPAD hit signal further to the peripheral readout logic and is marked with a red frame. In contrast to the SPAD packaging an aim was also to create a dense layout for a good estimate on the area it occupies and hence a reasonably good calculation of the fill factor.

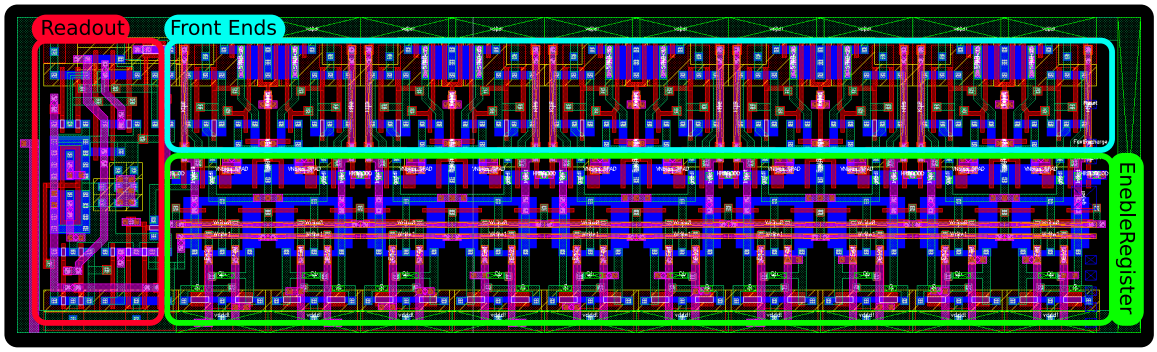

Figure 4.9: Picture of the layout of the electronics included in a Macropixel. It comprised three basic blocks: 1) Ten front ends, one for each SPAD, which read out the SPAD signal and are highlighted by a turquoise frame. 2) The 10-bit Enable Register for turning on and off individual SPADs, which is marked by a green frame. 3) The signal processing, highlighted with a red frame, which sends the SPAD hit signal to the peripheral readout.

4.3.3 Macropixel: SPAD Front-End

The SPAD front-end includes a quench and recharge circuit with active feedback, which has the main purpose to reduce afterpulsing (see section 3.3). However, the front-end circuitry is designed as a test platform so that there is also the possibility to quench the SPAD purely passively and compare both schemes. Furthermore, it allows the individual SPAD to be permanently switch off, which is especially helpful for hot SPADs. These not only enhance the arrays overall noise but also induce crosstalk (see section 6.5). The schematic of the front-end electronics, including a timing diagram of the important control signals and the SPAD anode voltage, which is the terminal where it is read out, is shown in figure 4.10.
The SPAD bias voltage is applied at its cathode. In idle mode, where the transistor switches M7 and M2 are open and M1 closed, the SPAD anode is at ground potential. The current source M6 recharges the anode node, with a discharge current adjustable via V_{R}. The anodes direct connection to the subsequent circuitry, which is not suited for operation voltages above the supply voltage V_{DD}, makes it necessary to keep the excess bias of the SPAD V_{Ex} below V_{DD}. When a photon hits the SPAD the voltage at its anode rises swiftly to the value of the applied excess bias. When the threshold voltage $V_{\mathrm{Th}} \approx 0.8\,\mathrm{V}$ of the inverter INV1 is surpassed, its output (HitB) switches to low and the subsequent inverted INV2 restores the genuine polarity of the SPAD signal again. The latter then triggers the hit Wired-Or, to which all ten front ends are

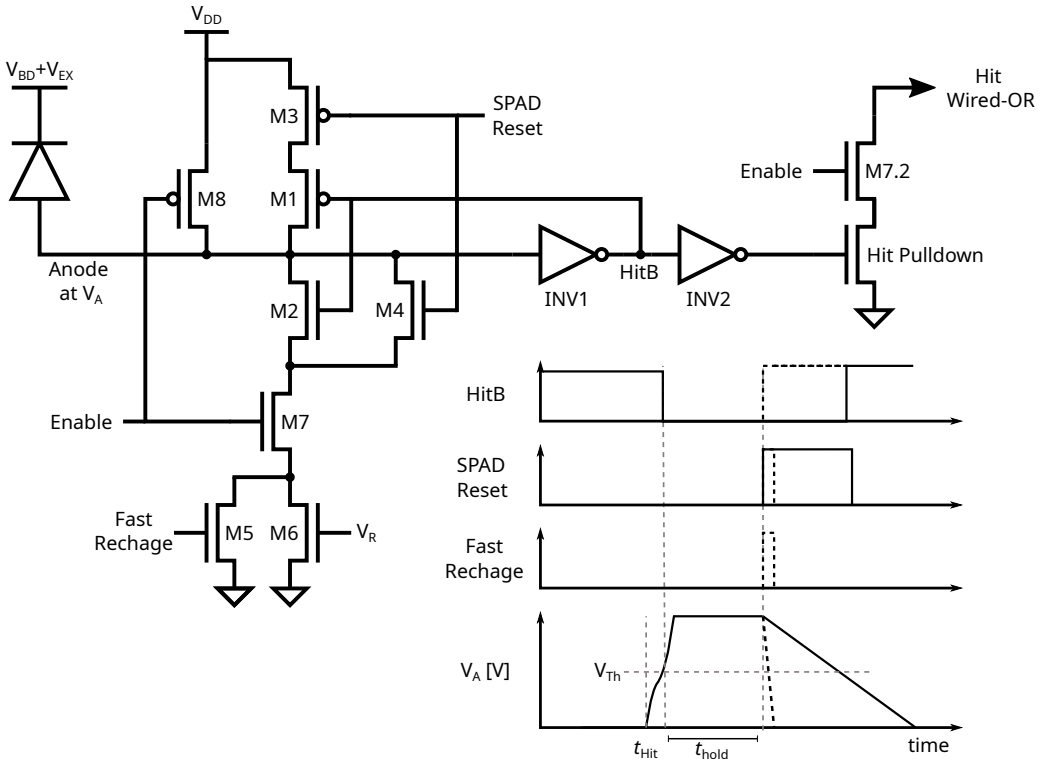

Figure 4.10: Schematics of one of the SPADs front end electronics in the Macropixel. A timing diagram of the control signals and the anode voltage for the active quenching, with fast (dashed) and slow recharge (solid) is shown. Active feedback is triggered by the HitB signal, which closes M1 and opens M2 to switch the SPAD off. Setting SPAD Reset discharges the SPAD anode again, which can be done fast, with the large current of M5, or more slowly with a constant current by M6. For a purely passive quench the SPAD Reset signal is set permanently. M8 and M7 are employed to disable the SPAD permanently.

connected, flagging to the Macro Pixel electronics that there is a hit.
At the same time the output of INV1 (HitB) triggers the active feedback. The transistor switch M2 is opened and M1, in return, closed. Consequently, the anode is charged up to the supply voltage V_{DD} and the SPAD, which is biased with at $V_{\mathrm{Ex}} < V_{\mathrm{DD}}$, is switched off. The SPAD stays in this state until the predefined hold time has elapsed and a reset is performed. Within the hold time afterpulsing i.e. release of trapped charge carriers, cannot cause a secondary avalanche. The hold time is variable and is set by the FPGA controlling the array.
For the reset of the SPAD the SPAD Reset signal is set, which opens M3 and closes M4, so that the anode node is discharged with a constant current by M6. Furthermore, there is the possibility to perform a fast recharge with a large current by switching on the transistor switch M5 (fast reset signal) during the reset. This process is displayed by the dashed line in the timing diagram.
To operate the SPAD in the purely passive quenching scheme (see section 3.3) the SPAD Reset signal is permanently set, which opens M3 and disables the feedback mechanism. The current source M6 acts as a quenching resistor, whereas the recharge time can be adjusted via V_{R}. In principle, afterpulsing can also be masked in this configuration by choosing a recharge time longer than the afterpulsing time constant. The release of the trapped charge-carriers then happens while the anode voltage is slowly recharging and is still above the threshold of the INV1 (see section 3.7.1).

Finally, the switches M7 and M8 are employed to enable or disable the individual SPADs of the macro pixel. When the enable signal is unset M8 is opened and M7 is closed, so that the anode is charged up to V_{DD} and the SPAD is permanently switched off. At the same time, M7.2 is also opened and the connection to the Hit Wired-Or is disabled.

4.3.4 Macropixel: Readout electronics

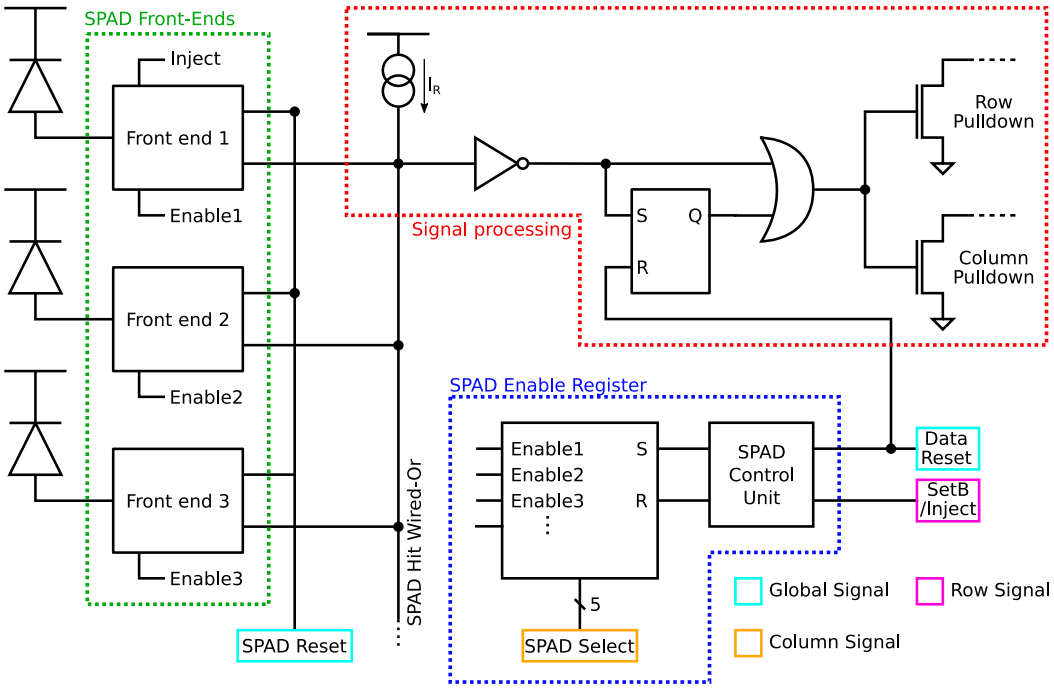

Figure 4.11: A schematic of the readout electronics of the Macropixel. The front-end electronics of the SPADs (green frame), where only three are shown, digitize the SPAD signal. The signal processor (red frame) saves the common SPAD hit signal and routed it to a row and column-wise Wired-OR, connected to the peripheral logic. The ten-bit Enable Register (blue frame) inhabits the enable bit of each SPAD. Data Reset and the SetB/Inject signals are for two tasks: 1) Reset the logic after a hit 2) Programming of the Enable Register. The double occupancy reduces the number of signal buses.

The readout electronics in the Macro Pixel is designed to occupy as little space as possible to guarantee a high fill factor. An essential step towards this was to merge all SPAD signals and treat them as one. This is actually possible since in the DARWIN experiment spacial resolution down to the SPAD level is not required (see section 2.4.3). The common hit signal is then processed by a single block of electronics, which notifies the periphery that there was a hit in the macro pixel. In figure 4.11 the schematic of the macro pixel circuitry is shown. It consists of the three following blocks which are marked with colored frames inside the schematic: 1) A block of ten front-ends for the SPADs (green) 2) the hit signal processing block (red) 3) the SPAD masking register (blue). For the sake of clarity not all ten front-ends are displayed.
All of the ten SPAD front-ends are connected to a common Hit wired-or and the SPAD hit signals from it are buffered by an inverter. Apart from SPAD Hit signals with an electrical inject signal, connected to the first front-end, hit signals can be simulated. On one side the inverter sets a hit flip-flop on the other side its output signal is bypassed to trigger an OR gate, to which the

hit flip-flop is also connected. The Or-Gate steers the row and column-wise wired-ORs, which notify the periphery that there has been a hit in this macro pixel. This bypass scheme allows the macro pixel to operate with or without hit flip-flop.
When the Data-Reset signal is permanently set by the FPGA the hit flip-flop is disabled. Consequently, by the means of the hit wired OR the SPADs front-ends directly control the row and column-wise hit buses. With this, the genuine signal lengths of the SPADs can be measured in active and passive quench mode (see section before) and thus also the amount of afterpulsing. So, for the active quenching the minimal hold time can be determined, while for passive quenching the minimal recharge time can be evaluated to minimize afterpusling and both schemes compared (see previous section). The fast discharge (see previous section), however, can only be tested by the means of a single active macro pixel, since the Fast Discharge signal is global. A SPAD hit during its activation causes a high current, which may harm the SPAD.
When on the other hand, Data Reset is controlled by the FPGA, clearing the hit flip-flop also after a certain hold time, it is possible to mask afterpulsing with the macro pixel electronics itself. With this, in principle a minimal SPAD front-end with a poly silicon resistor for passive quenching can be sufficient for a future array, which strongly reduces the number of steering signals and electronics inside the macro pixel.
The mask register, which comprises ten SRAM cells, provides the enable bits for the ten individual front-ends. To program the mask register a individual SRAM cell has first to be addressed with the 5-bit wide SPAD Select bus, which is distributed column-wise. For the actual programming, a small logic block is employed in which the Data reset and the SETB/Inject signals are reused to reduce the number of bus lines in the matrix. With the Data Reset signal it decided which selected SRAM cell is set (1) or unset (0). By setting the Set/Inject signal the actual programming of the selected SRAM is performed.

4.3.5 Readout Architecture

The readout architecture for the DARWIN Test Array should be, on the one hand, reliable and simple to create a fail-save basis for the extensive test at low temperatures. On the other hand, a first step towards a readout for the DARWIN Experiment should be made in terms of basic principle and power consumption. The chosen architecture is asynchronous, data driven and implemented with pure CMOS logic. The overall amount of logic is very low and compries mostly logic CMOS gates, so that it should be more or less fail-save and no static currents are flowing. Data driven means the readout is only active when a hit occurs. Consequently, the power consumption in idle mode should be dominated by leakage current of the CMOS logic. Under photon radiation the power consumption should be proportional to the rate of detected photon signals.
The functionality of the readout is as follows: When the Macropixel flags a hit signal the readout architecture outputs a one-bit Matrix-Hit signal used as trigger signal for the readout FPGA and a binary x/y address of the corresponding macro pixel. The binary address is 10-bit wide as the actual matrix comprises 19×19 macro pixels. Additional photons arriving while the readout is active are not processible and an error signal is flagged. In principle, this could be a suitable approach for reading out the low flux S1 signal in the DARWIN experiment (see section 2.4.2).
A schematic of the readout logic is shown in figure 4.12. For the sake of clarity, the size of the depicted matrix is reduced to 3×3 macro pixels, for which the logic is, however, exactly the same as for the actual one. Furthermore, only the x address processor is shown in detail while the one in y direction, which is identical, is depicted as a white box.
At the bottom of the matrix four horizontal wired-ORs are present ($\mathrm{AX}\langle 1:0\rangle$ and $\mathrm{AXB}\langle 1:0\rangle$), with which the x address is deduced. Correspondingly, another four vertical Wired-ORs are

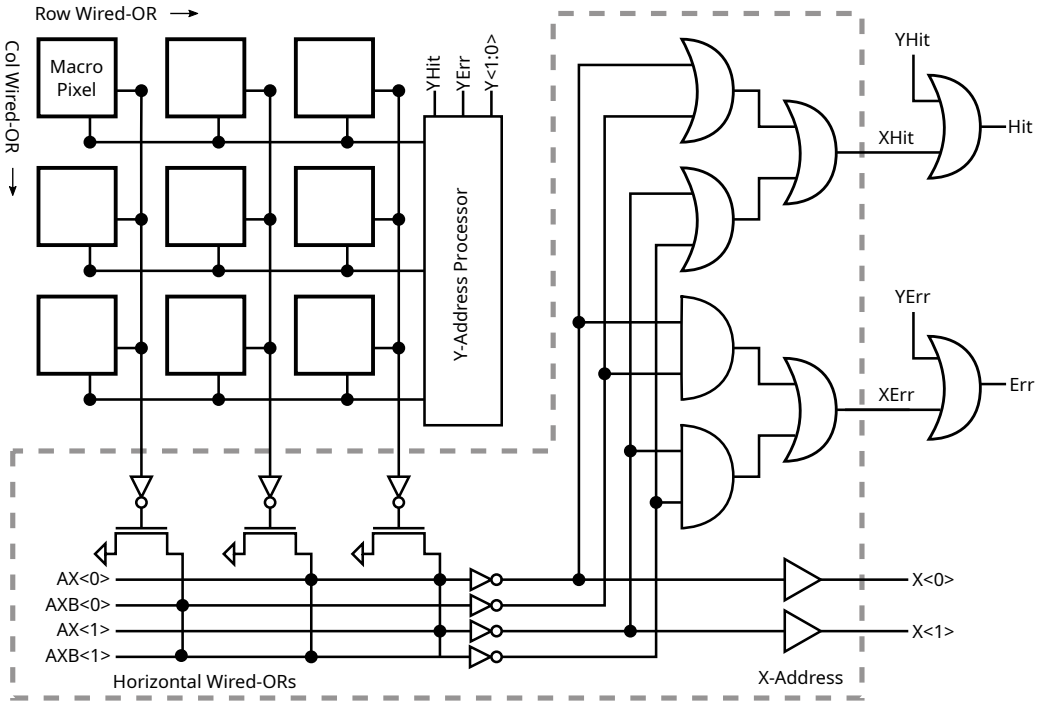

Figure 4.12: Schematic of the readout logic of an 3×3 macro pixel matrix. It outputs the binary x/y address of a hit Macro Pixel. Only the x address processor is shown in detail as the one in y direction is identical. The column- and row-wise hit buses in the matrix are connected to four horizontal and four vertical wired or at the bottom and the right side of the matrix. With the signals present on the wired-Ors the hit and error signals and the address is deduced.

present on the right side of the matrix, deducing the Y address. Two of this horizontal wired-ORs correspond to the actual address bits ($AX\langle 1:0\rangle$), while the other two ($AXB\langle 1:0\rangle$) are the so-called inverse address bits, which are needed for the error and hit signals formation. When a macro pixel is hit the row and column-wise hit buses inside the matrix are triggered. At the bottom and the right side of the matrix these hit signals are buffered and trigger a pull down, which is connected to some of the four vertical and horizontal wired-ORs. The connection pattern corresponds to the binary number of the row/column address. The column least significant address is on the left side and increments by one for each column to the right. So, for example, the column in the middle of the matrix in figure 4.12 has the binary address "01" and is connected to the horizontal Wired-OR $AX\langle 0\rangle$ and $AXB\langle 1\rangle$. The corresponding numbering of the rows starts on the top side of the matrix and the connection scheme is equal.
The signals of horizontal and vertical wired-ORs are buffered (by inverters), which trigger the further logic to deduce the Matrix-Hit signal, the Error and the x/y address signal outputs. The Matrix-Hit signal is the logical OR of all four address wired-ORs and will be output as soon as any of horizontal or vertical the wired-ORs are activated. The Error signal on the other side is the logical AND of one address bit and its corresponding inverse. Since, for a single hit, the binary number connection patter permits both to be active at once and if both are active a coincidence hit occurred. Finally, the row and column address corresponds to the buffered value of $AY\langle 1:0\rangle$ and $AX\langle 1:0\rangle$, respectively.
After a hit was detected by the FPGA the Matrix is cleared, which is done according to the description in the previous section.

4.3.6 Slow Control

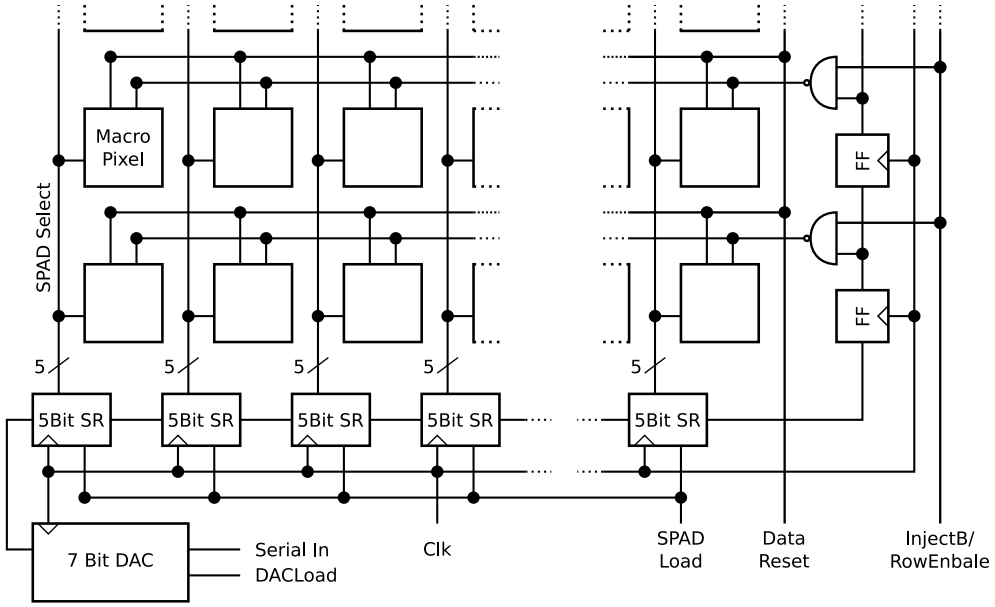

Figure 4.13: Schematic of the slow control shift register, which is 127-bit long. The starting point is a 7-bit DAC. The rest controls the matrix: In each column a 5-bit bus selects which SPAD to program in the matrix. The shift register running along the rows control the row-wise 1-bit buses. The 1-bit stages value in combination with the Data Reset Signal and SETB/Inject signal is used to either Enable or Disable the selected SPADs or not program the row at all.

The arrays macro pixel matrix and one DAC, which the bias voltage of the current source for the recharge of the SPAD can be adjusted, are configured via a 127-bit long shift register. Configuring of the macro pixel matrix means programming the mask register in the macro pixel, which selects which SPAD are to enabled or disabled (see section 4.3.4). The programming of the mask register is done exclusively via horizontal and vertical bus signals, so that no additional electronics is needed in the macro pixel. The pixel matrix is then programmed in an X-Y programming scheme, with which the all macro pixels can be programmed at once as well as column- or row-wise or even individually. Programming works as follows: Along each column runs a 5-bit bus, which is used to select the SPAD to program. With the Set/Inject it is selects whether the row is programmed or not and the Data Reset is used to decide if the SPAD is enabled or disabled.
In figure 4.13 a schematic of the shift register and its location in the array can be seen. The starting point of the shift register is the 7-bit DAC, which is identical to the one used in the IDP2 (see section 4.2.3). The DAC is programmed with the data in the shift register when the DAC-Load signal is flagged. At the bottom of the matrix a 5-bit shift register stage is present for each column, with which the SPAD is selected. The data is transferred to the SPAD select buses when the SPAD-load signal is activated. On the right side of the matrix a 1-bit stage per row is present, for the SET/Inject signal, to decide which row to program. The Data-Reset signal on the other side is a global signal common to all macro pixels. When setting the Inject/Set signal the selected SPADs are programmed. After programming the matrix, the shift register has to be set to a default state, in which the last 19 bits are high in order to be able to perform an electrical inject.

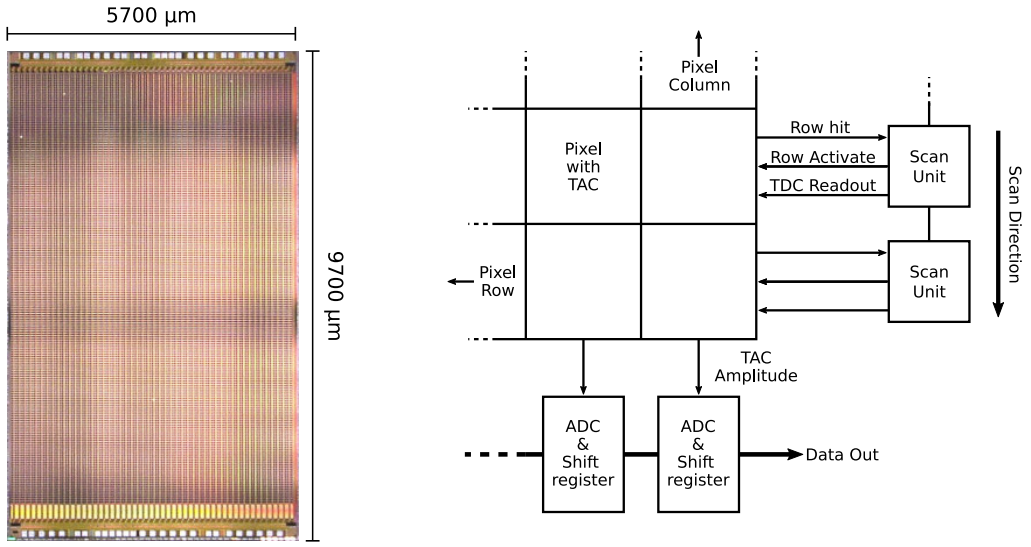

Figure 4.14: **Left:** Image of the time-resolved single photon camera **Right:** Schematic of the frame-wise readout. In each pixel a Time-to-Amplitude Converter (TAC) is included, measuring the photon timing. During readout a chain of Scan Units scan the Matrix row-wise for hits, starting in the top-most row. Empty rows are skipped, ones with hits are individually selected for readout. An ADC for each pixel of a row in the bottom of the matrix reads out the TAC's amplitude. A shift register then transfers the data out.

4.4 Time-Resolved Single Photon Camera

With its excellent intrinsic time resolution, which is well below 100 ps [168], the SPAD is highly suitable for time-resolved single photon imaging. Knowing the precise timing of an incident photon is a quality gaining more and more importance in a wide variety of physics experiments and commercial applications. For example, in particle physics the timing is utilized for particle identification [169]. In biology, cells are monitored with fluorescent lifetime imaging [164]. Finally, in the automotive industry the distance to the vehicle in front is determined with a photon time of flight measurement [170].
Within this work a time-resolved single photon camera was developed, which can be seen on the left side of figure 4.14. It comprises 174×100 pixels with a size of 50×57 µm^2. In each pixel, a circuit for measuring the photon arrival is present. It is an analog Time-to-Amplitude Converter (TAC), where the timing information is converted to a voltage level saved on a capacitor [171]. A very compact circuit was developed, which fits effortlessly into the pixel and enables a high amount of active sensing area to be kept and thus a fill factor of about 50 %.
The readout of the pixel timing information is frame-wise and zero suppressed. A schematic of the employed readout architecture is shown on the right side of figure 4.14. At the start of a programmable integration time window the TACs in all pixels are enabled and measure the arrival time of an incident photon. The subsequent digitization of the capacitor voltage level happens row wise, whereas rows not carrying a hit information are skipped. A chain of scan units asynchronously selects rows with hits for the read-out. The hit scan is linear, starts from the top most row and propagates down to the bottom of the matrix.
At the end of each column a Wilkinson ADC is present [172], digitizing the voltage level of the pixel of the currently-selected row. For this the capacitor is discharged and the elapsed time is recorded. A shift register running along the bottom of the matrix shifts out the timing informa-

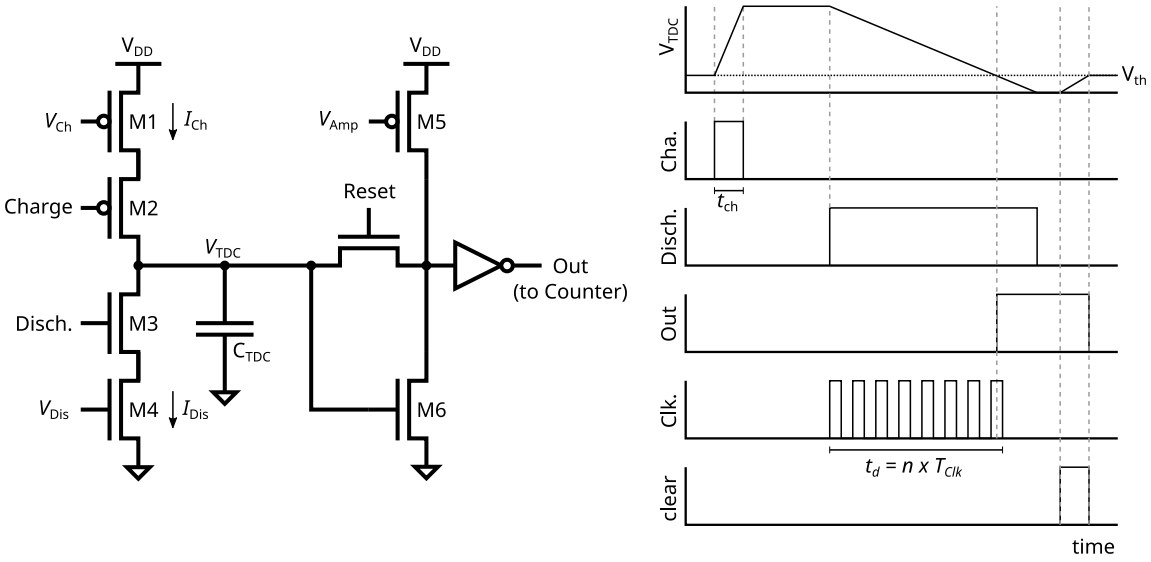

Figure 4.15: **Left:** Schematic of the TACs circuitry. M1 and M4 are the current sources, which are enabled by M2 and M3 respectively, for charging and discharging the capacitance C_{TDC}. The gain stage (M5,M6) acts as cooperator for the discharge process. When the clear signals is set M6 becomes diode connected and recharges C_{TDC} to the same working point as before the measurement. **Right:** Timing diagram of one measurement cycle with the TAC. The counter for measuring t_{d} is not displayed.

tion to the periphery.
With the large number of pixels, the excellent fill factor and the TAC's programmable input window a vast variety of use cases should be covered: A low flux of photons can be monitored with good detection efficiency over a large time. At the same time, with the zero suppressed readout low photon occupancy measurements can be made at a high frequency to gather a high amount of statistics in a reasonable time. On the other hand, it is also possible to handle a very intensive light burst in a short time.
Within this section the TAC, the pixel electronics, and the matrix readout will be discussed. The characterization of this chip, however, was beyond the scope of this work.

4.4.1 In Pixel Time-to-Amplitude Converter

For the precise measure of the arrival time of a photon, an analog Time-to-Amplitude converter (TAC) is employed. Such circuits offer an excellent time resolution of several 10 ps [173] and have the advantage of being small in implementation size [174]. The main drawback, however, is that a certain conversion time elapses to digitize the analog voltage level, which can be in the order of some micro seconds [171]. A fully digital time measurement circuit, by comparison, needs only a few clock cycles to digitize the arrival time but consumes a significantly higher amount of electronics and space [175]. A schematic of the employed TAC circuit is shown on the left side of figure 4.15. As it comprised only 13 transistors the fill factor of the pixel is, as already mentioned above, in the order of 50 %. On the right side of figure 4.15, the time measurement and readout sequence of the TAC is illustrated at hand of a timing diagram.
The central part of the circuit is the capacitor C_{TAC}. On activation of the charge signal, the transistor switch M2 is closed and the capacitor is charged with the current I_{Ch}. Upon the

deactivation of the charge signal M2 is opened again and a fixed voltage level settles on the capacitor, which is a measure of the time elapse since the start of the charge process.
In the next step, the voltage level is digitized making use of the Wilkinson ADC principle [172], where the discharge time of C_{TAC} is measured. On activation of the discharge signal, which closes the transistor switch M3, a digital counter is started, which is incremented on each clock strobe. When the discharge is completed, which is flagged by a comparator, the counter is stopped. The comparator is a simple gain stage, which switches its output to low when the voltage on C_{TAC} drops below its threshold voltage V_{th}. The threshold voltage can be adjusted via the bias voltage of the current source M5.
On completion of the discharge the Reset signal is activated and clears the TAC. The gain stage transistor M6 becomes diode connected, so that the capacitor is charged roughly to the threshold voltage of the comparator.
Finally, from the digitized timing information the genuine timing of the input signal has to be determined, by means of

$$t_{\mathrm{ch}} = \frac{n \cdot T_{Clk}}{k} \tag{4.1}$$

where, t_{ch} is the timing of the input signal, n is the number of elapsed clock strobes, T_{Clk} the period of the counter clock and $k = I_{\mathrm{ch}}/I_{\mathrm{Dis}}$ the so-called stretching factor, given by the ratio of discharge and charge current [171]. With a large stretching factor, a moderate clocking frequency is sufficient to recover the timing with a high counter resolution. The latter is determined by the accuracy of the counters least significant bit (LSB) and can be written as $LSB = T_{CLK}/k$ [171], [176]. For example, a clock frequency of 100 MHz and a stretching factor $k = 1000$ corresponds to an LSB accuracy of 10 ps. Apparently, such a fine resolution is only reasonable when the TAC's own noise is in the same order or lower. Furthermore, a relatively long conversion time is required, which reduces the readout speed. However, accuracy can always be traded for speed by reducing the stretching factor.
The intrinsic time-resolution of the TAC itself is determined by the current sources for the charge and discharge process. What is most important is that it is time dependent and degrades for higher charge and discharge times. The current noise of M2 and M4 is integrated on the capacitor over the duration of the charge and discharge process [177], introducing a jitter in the comparator's output signal. The longer the current integration is the higher this jitter becomes. According to [178] the timing resolution, which is then determined by the output jitter, is somewhat proportional to the square root of the conversion time.

4.4.2 Pixel Electronics

The center piece of the pixel electronics is clearly the TAC. The surrounding logic is then designed to support a fast readout speed by flagging the periphery directly if there is a hit to readout or not. The Pixel logic is shown in figure 4.16.
The SPAD is passively quenched and AC coupled, so that the n-well of the readout logic and the SPAD can be shared (see section 4.2.1). The SPAD signal is digitized by a discriminator (see section 4.1), which sets the Hit flip-flop when the accumulation signal is active. The hit signal propagates further to the TAC and starts the charge process. A pull-down transistor also connected to the hit flipflops output, is activated. The Row Hit wired-or notifies the end of row logic that there was a hit in at least one pixel of the row.Finally, at the same time the closing of the accumulation time window the TAC capacitor charging is stopped.
When the row is activated for the readout, carried out by the very same end of row logic, the pixel output logic is granted control over the column-wise TDCDoneB wired-OR. In case the pixel has not recorded a timing information, the pull-down transistor is instantaneously activated, indi-

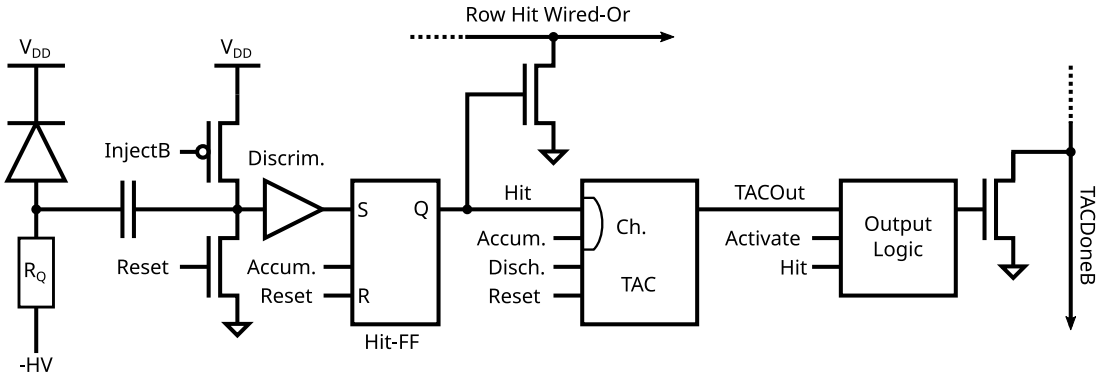

Figure 4.16: Schematic of the electronics inside a pixel. The SPAD is AC coupled to a discriminator digitizing its signal. When the accumulation signal is set, a hit signal is buffered by a hit flip-flop. Its output triggers the Row Hit wired-Or and starts the TACs ramp, which is stopped when the accumulation signal is disabled. The output logic controls the column-wise TACDone Wired-OR, on the rows activation for readout. If a hit was recorded, the pull down is activated on the completed discharge, otherwise it is directly triggered.

cating to the end of column logic that no discharge time has to be measured. Otherwise the TAC capacitor is discharged when the Row Discharge signal is set and the pull-down transistor is triggered on completion of the discharge.
As a final step, the reset has to be performed. It is done shortly and for a predefined time before the next photon accumulation, bringing all TACs to a comparable operation point. This reduces the systematical errors of the individual frames. During the reset the Hit flip-flop is unset, the discriminator input is discharged and the TACs capacitor will be charged to a predefined voltage level (see previous section).
Finally, a dedicated disable logic for the SPAD, like for the IDP2 (see section 4.2), is not absolutely necessary and was rejected in favor of the system complexity. A disable logic is mostly used to switch off hot SPADs, which are SPADs with enhanced dark count rate compared to the average ones. Potentially, they could cause an excess number of rows carrying a hit, which would, in return, compromise the readout speed. However, hot SPADs, of the implemented SPAD size, have an average dark count rate of about 5000 Hz (see section 6.5). For typical time windows of 10 to 100 ns only a very small fraction will have a dark count, so the readout speed is not compromised.

4.4.3 End of Row Logic

To enhance the frame rate of the time-resolved single photon camera, a zero suppressed readout was implemented. Only rows in which pixels actually carry a timing information are read out, while empty ones are skipped. The rows are asynchronously scanned with a chain of so-called scan units, which are inspired by [179], [180]. The scan units are placed at the end of each row, making the decision of reading out or skipping. A schematic of one scan unit is shown in figure 4.17.
The Scan In signal can be seen as a token. Inserted at the top-most scan unit it traverses through the whole chain. Scan units where the Row Hit signal is set, stop the token, while those where no hit is present, pass it. On a stop the Row activate signal is set and the output logic of each pixel in the row gains control over column-wise TACDoneB wired-OR (see previous section).

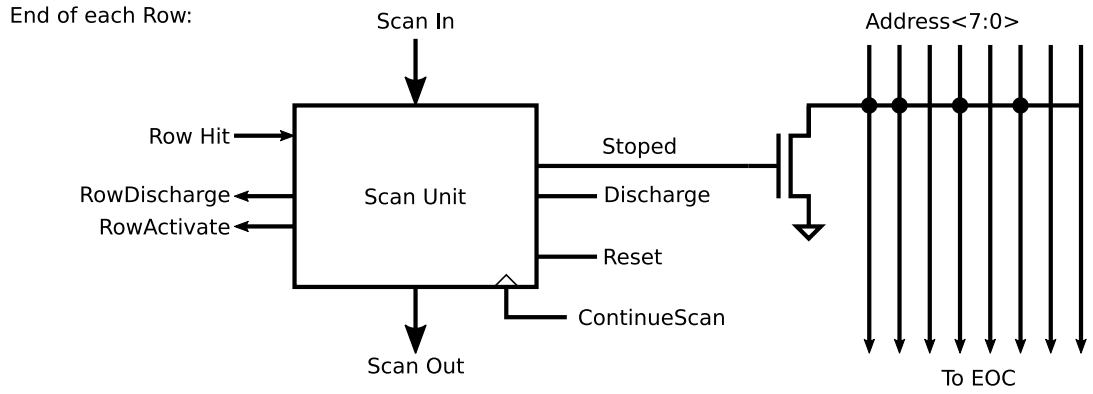

Figure 4.17: The row wise hit scan is done by scan units, where one is schematically shown here. The Scan In is connected to the Scan out of the previous row. If the Scan In signal, also called scan token, is set and a hit is present in the row, its address is outputted on the address bus and the row can be readout. In case no hit is present in the row, or ContinueScan is activated after a readout, the Scan In signal is passed to Scan Out and arrives at the next stage.

Simultaneously, the address of the row is transferred on the 8-bit address bus. With the pull-down connected to the bus in the way that the decimal address of the row is represented as a binary number. The address is read in by the end of column logic at the bottom of the matrix. For the readout of the TAC, the discharge signal is set. Although it is a global signal, it is only passed further to the pixels of the current active row, in the form of the Row-Discharge signal. On the completion of the discharge, the ContinueScan signal is set, allowing the scan token to be passed to the next scan unit. The ContinueScan input is edge triggered, to prevent the token falling through several scan units by accident.
When the token finally has passed through all scan units the readout is finished. With this the detector can be reset to record the next frame. On the reset the flip-flops for continuing the scan are reset and, moreover, the pull-up current sources for the row-wise hit Wired-ORs are activated.

4.4.4 End of Column Logic

Upon the selection of a row for the readout, the discharge of the TAC capacitor is carried out. The elapsed time up to the completion of the discharge process is measured by a digital counter at the end of each column. In figure 4.18 a schematic of the counter, its enable logic and the data transfer logic of one column is shown.
The column wise TACDoneB Wired-Or, which is directly controlled by the pixels of the selected row, is connected to a clock gate logic. While the TDCDoneB is inactive the clock is passed through the logic towards the counter. When the discharge is completed the TAC prompts the TACDoneB signal and the clock transmission is stopped. This happens only during the clock's low state, so that clock spikes are prevented. Furthermore, a pixel of the selected row carrying no hit directly sets the TDCDoneB wired-Or, so that the counter will not start at all.
The clock gate logic also outputs its Enable-State, which is, in turn, used to flag the periphery that the readout is completed. The enable output is connected to a horizontal readout-finished wired-Or, which is common to all counter stages. When all individual counters are disabled the wired-Or recharges, informing the periphery that readout of the row is finished.
As a counter a 10-bit ripple counter is employed, which is simple and straight forward to imple-

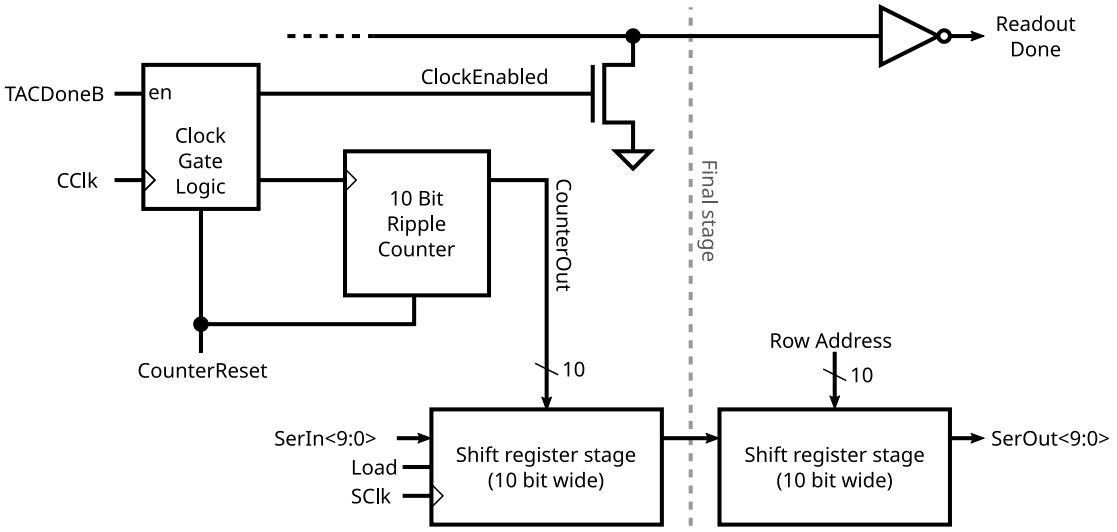

Figure 4.18: Schematic of the logic at the end of each column of the matrix. The counter clock is fed through the clock gate logic as long as TACDoneB is not set. Otherwise the 10-bit ripple counter stops counting and the digitized discharge time is loaded into a 10-bit wide shift register stage. The shift register, consisting of 101 stages, runs along the bottom of the matrix. In its first stage the address of the row is loaded. Readout Done is flagged when all counters are finished.

ment. As a synchronous data access is not required here, the cascaded delay is of no concern. The clock frequency of the counter is intended to be 100 MHz and hence, the maximum record able discharge time is 10 µs. A 10 ns accumulation time window can then be read out with an accuracy of 10 ps (see TAC section).
The counter data is transferred to a 10-bit wide shift register stage by flagging the load signal. The shift register runs along the bottom of the matrix, collects the data of a readout row and transfers it to the periphery. The first stage of this shift register is for the address of the current row. Correspondingly, ten output pads are present to transfer the data parallel as it is to an FPGA. While the data is shifted out, the next row can already be selected and digitized, which enhances the readout speed.

4.4.5 Slow Control

As in the IDP2 array a shift register was used to control the slow control part of the time-resolved single photon camera (see section 4.2.3). With a length of 56-Bit, configuration data is supplied to a Digital MUX, which is used for monitoring some internal digital signals, an analog multiplexer for internal analog signals and at last six DACs. The latter are identical to those used in the IDP2 and control the TACs bias voltages for the charge and discharge current source, the comparator bias and another three bias voltages needed within the array, which were left out of the discussion.

5. Setup for Cryogenic Measurements

Characterizing a large number of DARWIN test array at various low temperatures demands a dedicated cryogenic measurement setup, which provides the needed low temperature in a straightforward way and keeps it constant over the duration of the measurement. The temperature stability of the system is a key parameter for conserving the SPAD's operation point. The latter is defined through the excess bias voltage applied on the SPAD and varies with temperature as the value of the breakdown voltage does (see section 3.4).
Within this work, a cryogenic measurement system based on a vacuum liquid nitrogen bath cryostat, for the characterization of the DARWIN test array, was implemented. The setup consists of the cryostat with a vacuum vessel, in which the DARWIN Test Array is mounted on a carrier printed circuit board (PCB). Steering signals for the array are provided by a control PCB sitting outside it in the lab. The remote connection is then established by a custom-made cabling system with a vacuum tight feed through. Finally, with the firmware and the measurement software the array is controlled and data is taken. Moreover, the software monitors parameters like power consumption and temperature, and controls the voltage sources to set the different bias voltages. The resulting setup is nearly fully automated making it possible to measure several of the DARWIN Test arrays in a consistent way with moderate time exposure. However, the implementation of this system is due to the promising results gained with a much simpler cryogenic approach. The first test of Digital SiPMs at lower temperature were actually performed with a thermal insulating vessel, holding a cooling mixture to provide a low temperature. The Digital SiPM array was then submerged in the bath to reach its temperatures.
The starting point of this chapter is the description of the simple cryogenic setup, which includes the utilized cryogenic substances such as the readout electronics. The main part of this chapter will then be the description of the dedicated cryogenic setup.

5.1 Simple Approach

For the first characterization of Digital SiPMs at low temperatures, a simple cryogenic setup was chosen, which is shown in figure 5.1. The aim was to keep the material budget low, have a short preparation time and have a fast insight into the low temperature behavior of Digital SiPMs. For this, a simple cooling bath cryostat, which is shown in the upper part of figure 5.1, was utilized. In the lower part of figure 5.1 the associated readout electronics with the SPAD array is shown. The array used for the first experiment at cold temperature is the IDP2 array, a single photon camera explained in the previous chapter.
An open glass Dewar, which is a thermal insulating vessel, hosts the cooling bath, which consists of a liquid or solid cooling substance. The bath temperature is maintained until the bath substance is fully evaporated, melted or sublimated. Various temperatures are then exclusively provided by using different cooling baths. Common cooling substances are liquefied or solidified gases, like liquid Nitrogen, and mixtures of them with some organic solvents, like ethanol, and will be discussed in more detail in the next subsection. In addition, with this cryostat, all measurements had to be done at room conditions, so that it was not possible to implement an active temperature stabilization.
To measure at cold temperatures, the array then has to be brought into close thermal contact with the bath. For this, on one side a T-shaped carrier board for the IDP2 was utilized, with which the rest of the readout electronics can be separated for the cooling bath and stay at room

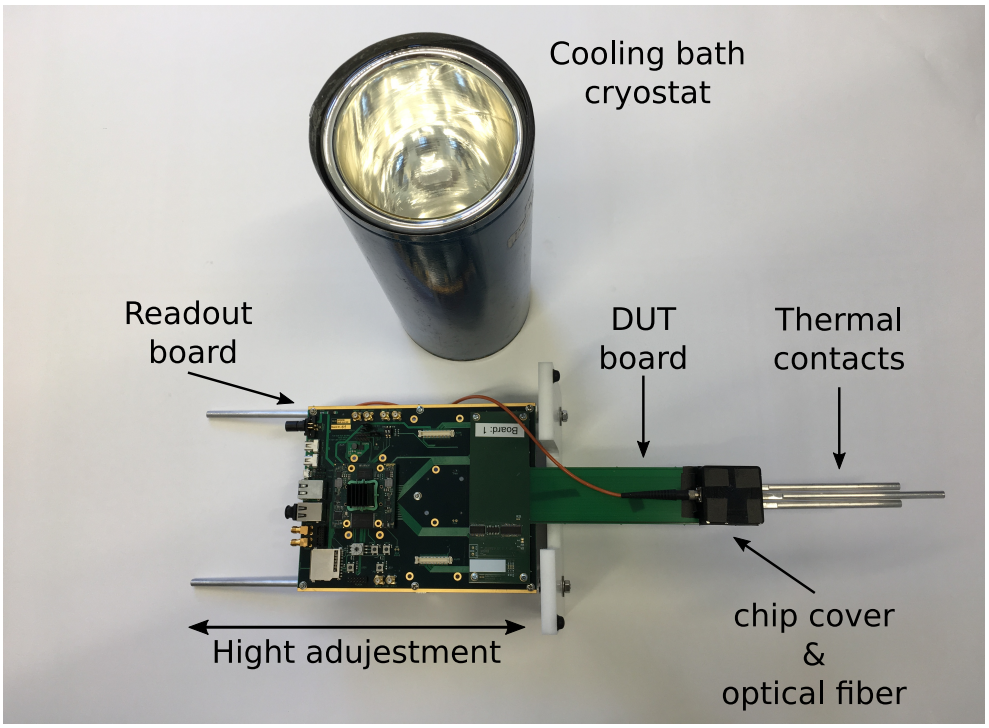

Figure 5.1: The cryogenic and readout setup for the first measurements of a SPAD array (IDP2) at low temperatures. In the upper part the open glass Dewar is visible for hosting the cooling bath, while in the lower part the measurement setup for the SPAD array is visible.

temperature. On the other side the aluminium rods, acting as thermal contacts to the bath, are attached to the T-shaped carrier board so that the array does not need to be immersed in the liquid. Especially solvents like acteton, dissolve the epoxy resin with which the array is glued onto the carrier PCB and destroy the setup.
The array itself is glued with epoxy resin on an aluminum holder, which is screwed to the tip of the T-shaped carrier board and is not visible in figure 5.1. Furthermore, a PT-100 thermometer is placed on the aluminum holder right beside the array to measure the platform temperature. The aluminum rods are then attached to the back of the aluminum holder. The array is covered by a 3D-printed light cover to shield it from ambient light. At the same time, the cover hosts a light fiber, coupled to the array, in order to measure its light sensitivity at low temperature. A laser-diode emitting red light is positioned at room temperature in the lab and is coupled to the other end of the light fiber. Inside the light cover of the array, a mirror made of aluminum foil directs the light from the fiber to the array. The carrier board, which was developed in the work group, before the start of this work, is plugged on the readout board which controls and reads out the array. The readout board is, in addition, mounted on a rack, which stabilizes the overall setup when put on the cryostat.
For measurement the T-shaped DUT board is then inserted into the Dewar and the rack of the readout board is positioned on top of the vessel. With the help of the rack also the height above the cooling bath can be adjusted, so that the thermal contact between the bath and chip is worsened and intermediate temperatures are reached. Further elements for the temperature adjustment, like a restive heater, did not work properly. Gas convection inside the cryostat lead to fluctuations in temperatures, which could not be balanced by regulation. Nevertheless the temperature stability was sufficient for the measurement, which is described in the next section.

During the measurement, the glass Dewar opening was covered by polystyrene for thermal isolation and light-tight blankets were wrapped around the electronics and the vessels opening to shield the array from the ambient light of the lab. However, both are left out of figure 5.1 for the sake of clarity.
The readout board was developed as freely programmable steering platform for all kinds of SPAD arrays, within the work group [181]. It hosts a Xilinx Zynq-FPGA providing the necessary signals to control the array and readout the output data. The firmware is saved on an SD memory card and is loaded within the boot process of the FPGA. The read out process of the IDP2 (single photon camera) is frame-wise as described in section 4.2.2. The FPGA set up a certain and controllable illumination time window, in between which the buffer in the pixel logic of each SPAD is enabled and can record a single photon hit. Afterwards the whole array is read out row by row, using the parallel ports to enhance the readout speed. The readout time of a single frame is controllable (see next section) and is set to be about 50 µs, since, in the first test at lower temperatures, setup and hold time violations where observed, which made it necessary to lower the readout speed. The time in between the frames corresponds to the dead time of the IDP2.
The FPGA also controls the slow control and shift register with which individual SPADs are masked. Furthermore, the FPGA tracks the temperature of the array once per second. For this, the PT-100 thermometer mounted next to the array is read out by a ltc2990 IC, which communicates over I2C link with the FPGA and sends the data, when the FPGA requests it. The connection to the readout software for data collection and controlling the FPGA is established via TCP.

5.1.1 Firmware and Software

The firmware for the Xilinx Zynq-FPGA was developed in the work group and its central module is a sequencer. The sequencer controls the outputs to the array and reads in the inputs coming from it, according to the commands given to it. Commands are sent from the computer and are saved in a ram on the FPGA. From the RAM the sequencer, one after the other, take the commands and process them. Processing is done within one clock cycle of the 112 MHz system clock. Commands are, for example, to read in the inputs, set specific outputs, repeat prior commands several times or wait for a certain time. With these the steering sequence is created to readout a frame of the IDP2 (see section 4.2.2), whereas the wait command can be utilized to reduce the frequency of the readout, since at low temperatures setup and hold time might change.
The software was then written in C++ within this work, and is mostly controlled via a central GUI created within the QT framework [182]. Its main purpose was to send the steering patters, which were mostly hard encoded, to the sequencer on the FPGA. Steering patterns for the readout of the matrix, for programming the slow control and for programming the enable register (see section 4.2) are provided in the software and sent to the FPGA via TCP.
A central image class acts as receiver for the read out frame data sent from the FPGA via TCP. In this class the binary frames are integrated to an image, where the number of hits in each pixel is represented as integer number. This image is then sent to the main GUI, where it is displayed as a color map. After a measurement, the image data is written to the disk.
Furthermore, the software controls the voltage sources for the SPAD bias via GPIB. Additionally, the temperature of the experimental platform is read out once a second with the PT100 thermometer mounted in close proximity to the array and described above. The tracked temperature covering the period of the measurement is then written to the disk after each measurement.

Substance	Cooling agent	Bath temperature T
Water	Liquid Nitrogen	273 K
Ethanol	Dry Ice	201 K
Dry Ice	-	195 K
Acetone	Liquid Nitrogen	179 K
Ethanol	Liquid Nitrogen	157 K
Liquid Nitrogen	-	77 K

Tab. 5.1: List of the cooling baths with the used cooling agent for their creation and their respective temperatures.

5.1.2 Cooling Bath

A cooling bath housed in an insulated vessel, which is at room pressure, is a simple way to reach and maintain a low temperature in an experiment. A cold solid or liquid substance is put into the vessel, which has a sublimation or melting temperature well below room temperature. As it changes the phase to gas or liquid it withdraws energy from the bulk material and therefore the critical temperature of the transition is maintained until the phase transition is completed. By adding liquid solvents to the used cooling agent also bath temperatures can be varied so that a broad variety of baths with different low temperatures can be created. In table 5.1 a list of all substances used for measuring the IDP2 at cold temperatures, is shown.
The first and easiest way to create a cooling bath is to use liquefied or solidified gas. Liquid nitrogen and frozen carbon dioxide, called dry ice, are easy to access and, at room pressure, they provide baths with the respective temperature of boiling point of liquid nitrogen at $T = 77\,\mathrm{K}$ and the sublimation point of dry ice at $T = 195\,\mathrm{K}$.
The next cooling baths, which were utilized, were mixtures of solid and liquid compounds. The starting point is a liquid, which is partly frozen out with liquid nitrogen. The solid part melts, withdraws energy form the liquid, and therefore the temperature of the liquid part is kept at the melting point of the solid until it is completely melted. Care has to be taken during the freeze out process. If too much liquid nitrogen is added the liquid freezes out completely. In this case the bath temperature drops even below the melting point of the solid and it has to rise again until it starts melting, which is quite time consuming. The liquid substances used were, water, acetone and ethanol, which are all easy to access. They yield bath temperatures of $T = 273\,\mathrm{K}$, $T = 179\,\mathrm{K}$ and $T = 157\,\mathrm{K}$, respectively. A more comprehensive list of cold bath mixtures can, for example, be found in [183].
The third kind of cooling bath was provided by mixing dry ice with a substance that increases its sublimation temperature. In this case the choice was limited to ethanol, which yielded a bath temperature of $T = 201\,\mathrm{K}$. Further substances were not accessible.
By using of these cooling baths and by adjusting the height of the array above the cooling bath (see previous section) in total 19 measurements at different temperatures were possible. Although the creation of the cooling bath was quite cumbersome and time consuming an astonishingly good temperature stability was reached. The array temperature, which was measured with the PT-100 directly next to it, increased by only about $\Delta T = 1\,\mathrm{K}$ in 20 min, which was also the time a complete dark count rate measurement took.

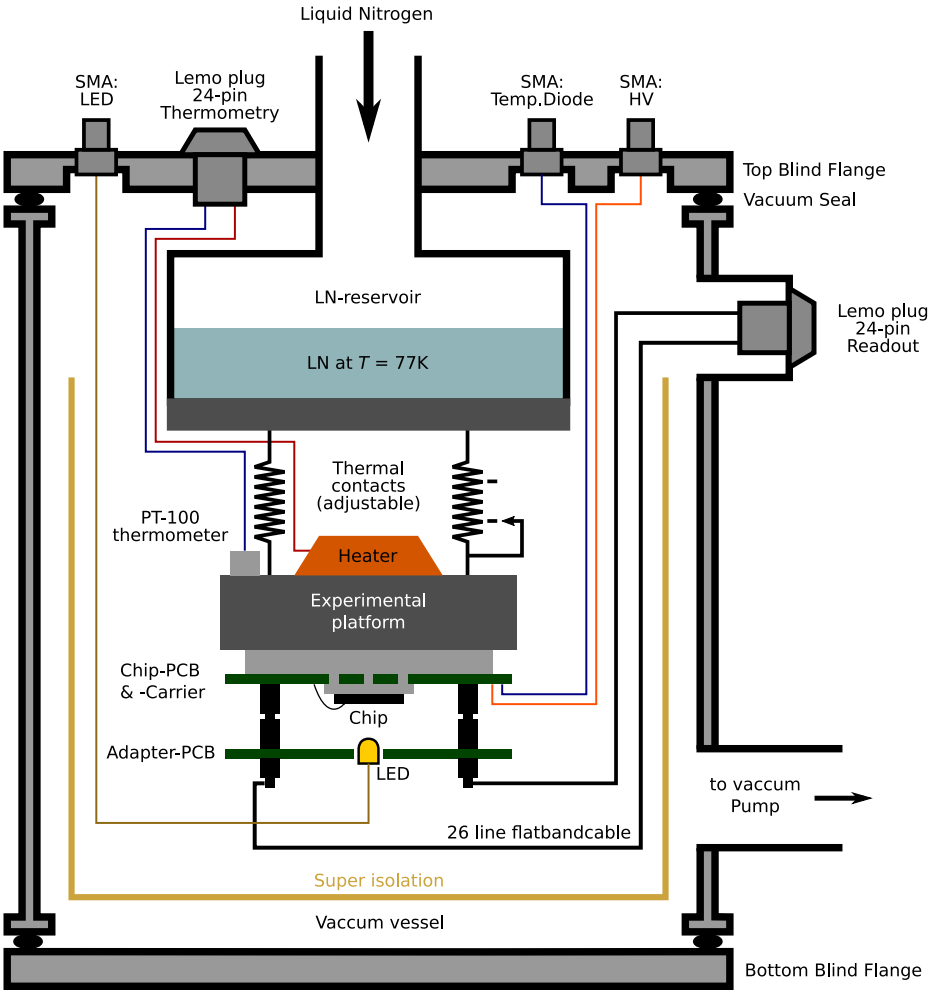

Figure 5.2: Schematic structure of the liquid nitrogen cryostat. The outer part is the vacuum vessel with its blind flanges. The cooling stage, sitting inside the vacuum, consists of the experimental platform and the liquid nitrogen reservoir. The PT-100 thermometer and the heater are used for the temperature control of the platform to which the experimental setup is attached.

5.2 Cryogenic Setup

A sophisticated cryogenic measurement setup forms the foundation for the characterization of the DARWIN Test array (see section 4.3) at various low temperatures. In this setup, liquid nitrogen is used as a cooling agent. With the employed active temperature regulation any temperature between $T = 300\,\mathrm{K}$ and $T = 100\,\mathrm{K}$ can be setup and maintained over a long period of time. This is a important requirement to gain consistent results for several reruns of the measurements with different process variations of the DARWIN test array (see section 4.3).
The basic components of the cryostat are a vacuum vessel with a vacuum pump system and the cooling stage operated inside the vacuum. These parts were provided by the group of Prof. Dr. Christian Enss at the University of Heidelberg. This group is specialized in the low temperature properties of amorphous solids and low temperature radiation detectors working according to the calorimetric principle [34]. The cryostat was extended to fit the needs of the experiment in terms of signal lines. This means, additional cables and a vacuum-tight electrical connection

were installed. A schematic of the cryostat structure is shown in figure 5.2.
The vacuum vessel, the cryostat outer part, is shown in gray and is cylindrical shaped with a length of 1 m and a diameter of 0.2 m. The bottom and the top of the vessel are closed with blind flanges. On the top blind flange, the cooling stage is attached and it can be completely removed from the vacuum vessel by detaching the flange. The vacuum is provided and maintained by a pump system consisting of a rotary valve pump with a turbo molecular pump as second stage, reaching a pressure well below 10^{-5} mbar. The vacuum thermally isolates the cooling stage from the outside and prevents air humidity from condensing on the array.
The cooling stage, the cryostat inner part, consists of a liquid nitrogen reservoir and an experimental platform in thermal contact with it, where the DARWIN test array is mounted. Rescue foil, also known as super isolation foil, is wrapped around the cooling stage to isolate it from thermal radiation coming from the vacuum vessel, which is at room temperature. The reservoir inner part stays at room pressure and liquid nitrogen is filled into it via a feedthrough mounted on the top blind flange.
For the setup of various temperatures, a PT-100 thermometer and a heater are attached to the back of the experimental platform, which are read out and biased by a PID-controller. The thermal contact between the reservoir and the experimental platform is chosen to be relatively weak. Therefore, the platform temperature can be adjusted with moderate power consumption of the heater and, subsequently, the lifetime of the cooling bath is increased. Four brass screws, with the diameter of 3 mm make up the basic thermal contact. However, it was found that this contact allows a minimal temperature of only $T = 120$ K. Below this temperature the parasitic heat input from the setup and outside, surpasses the cooling power coming from the reservoir and the temperature becomes unstable. In order to reach lower temperatures, the thermal contact was enhanced by attaching an additional aluminum wire, which extends the temperature range down to $T = 100$ K.
The DARWIN test array is mounted on an aluminum holder to which also its corresponding carrier printed circuit board (PCB) is screwed. The aluminum holder is, in turn, screwed tightly to the experimental platform. Some vacuum grease applied to the back of the holder to guarantee a good thermal contact to the platform. A more comprehensive description of the carrier PCB can be found in the next section.
To operate the array in total 22 digital signals, 3 bias voltages and one power and ground line are needed. As already mentioned above additional cables had to be installed into the cryostat to provide this number of electrical connections. Two ribbon cables with 26 lines carry the 22 digital signals such as the power and ground lines. A vacuum-tight 24-pin LEMO connection system then connects the two cables from the inside, to the two on the outside of the cryostat, where the readout board controlling the array is situated. Inside the cryostat, both cables run along the liquid nitrogen reservoir to precool them and decrease the parasitic heat load on the experimental platform. The signals on the two cables (inside and outside) are distributed as follows: one ribbon cable is used for the array input signals, while the other one is used for the array output signals to prevent cross talk between these. Furthermore, on the ribbon cable every second signal line is permanently connected to ground to prevent cross talk between the individual signal lines. An additional adapter PCB then establishes the connection between the ribbon cables and the carrier PCB as the latter possess a different connection system. Again, the PCBs are described in the next section.
The total length of the ribbon cabling system is about $L \approx 1$ m, but high-speed data transmission is not required in this experiment, so that signal integrity was sufficient. Signal rise and fall times were below 10 ns. During the measurement at high temperatures ($T >$240 K) the measured hit rate was below 100 kHz while at lower temperatures it is in the order of 1 Hz or well below. Only at room temperatures, when measuring hot SPADs, crosstalk in the address

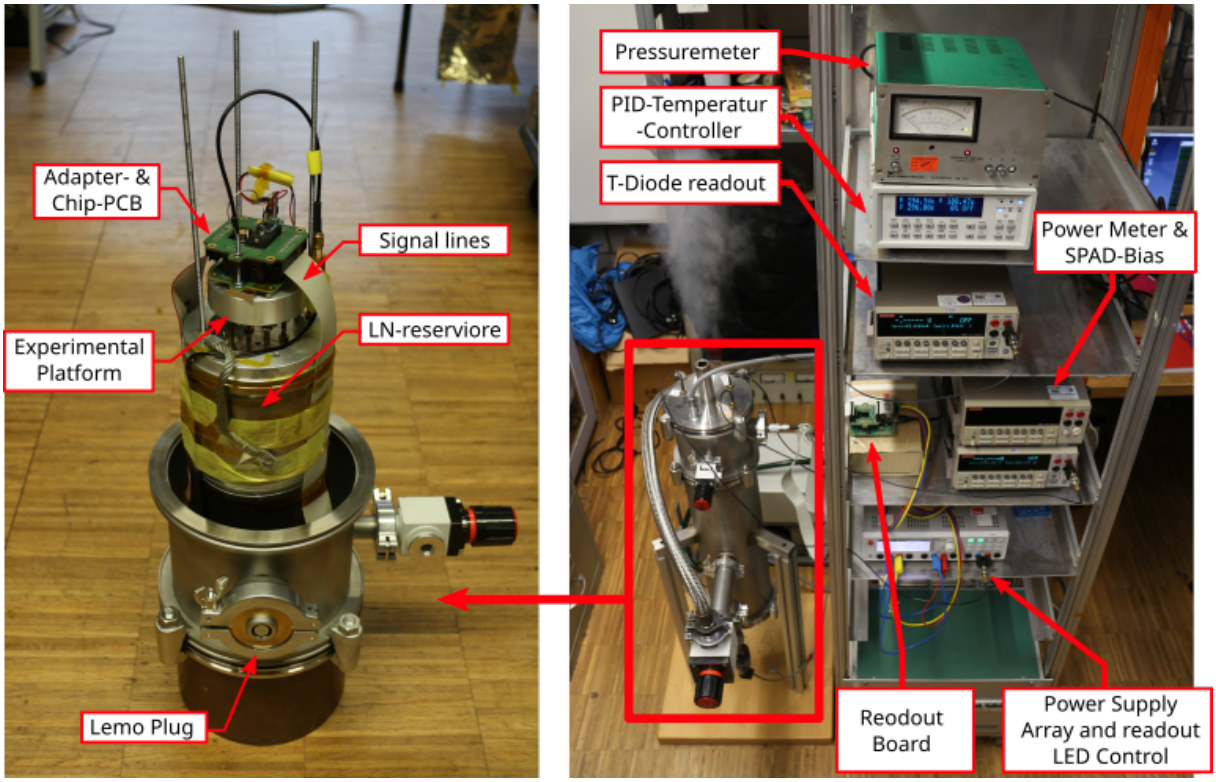

Figure 5.3: **Left:** Photograph of the cryostat inner part where the signal cables, the liquid nitrogen reservoir and the experimental platform are visible. **Right:** Image of the complete measurement setup in operation. The cryostat is situated beside a rack where all instrumentation is placed on. The central part is the readout board which controls and reads out the array in the cold. The rest are devices for setting up and measuring the temperature on the platform, for adjusting the various bias voltage, and for providing the power supply.

lines occurred, which was afterwards corrected in software as only single SPADs are measured at room temperatures.
For the remaining bias signals, meaning the SPAD bias voltage, the thermometer diode on the array and the LED mounted in front of the array, SMA feedthrough connection on the top blind flange are used. The LED emits yellow light, and was tested beforehand in Prof. Dr. Enss group and was proven to work down to liquid Helium temperatures of $T = 4.2\,\mathrm{K}$. The LED is mounted on a 3D printed holder, which is screwed to the adapter board. The main purpose of it was to illuminate the array during the breakdown voltage measurement. Finally, the heater and the PT-100 thermometer, are connected via a separated LEMO connector on the top flange, which was already installed and is exclusively intended for this purpose.
In figure 5.3 on the left side a photograph of the cryostat inner parts can be seen, where the signal cables, the liquid nitrogen reservoir and the experimental platform, are visible. On the right side a picture of the complete measurement setup in the lab is visible. The cryostat is placed beside a rack where all necessary instruments are placed on. The Central part is the readout board, which controls and reads out the SPAD array on the carrier board inside the cryostate via the discussed cabling system. Recorded data on the readout board is transmitted to the measurement computer via FTDI, which will be described in detail in the following section. Most of the other devices of the measurement setup can be controlled with the measurement software via GPIB. The setup is nearly fully automated, apart from the refill of the liquid nitrogen reservoir,

which has to be done manually. Furthermore, parameters like the power consumption and the current temperature in the cryostat are recorded on a regular basis of 1 s and are written to disk during a measurement.
For the power supply for the readout board and SPAD array, two voltage sources (Agilent/Keysight E3620) were utilized which are, apart from the pressure meter, the only devices not controllable via GPIB. The power consumption of the array is measured with a current meter (Keithley Model 2000), connected in series to the supply voltage line of the array. The high voltage SPAD bias and the LED bias voltage are controlled with a dual-channel source measure unit (Keithley SMU 2600).
The platform temperature is set up and read out with a PID-controller (Lakeshore 333) and the temperature stability is measured to be about $\Delta T = 0.1\,\mathrm{K}$. The temperature of the array is monitored with the on-chip temperature diode (see section 4.3). A source measure unit (Keithley SUM 2400) applies a current bias to the diode and simultaneously measures the voltage. The temperature calibration can then be done by means of the measured platform temperature.

5.3 Readout Electronics

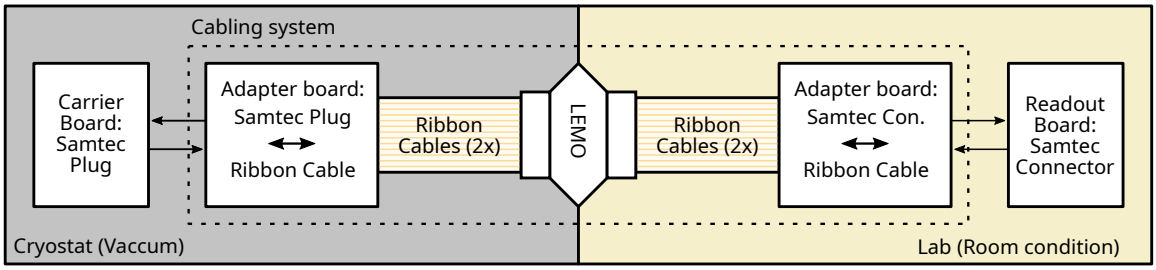

Figure 5.4: Schematic of the readout electronics used for the measurements at low temperatures. The chip carrier board is mounted inside the cryostat, while the readout board, controlling the ASIC, is outside. The cabling system then establishes the remote connection.

For the readout of the DARWIN test array at cryogenic temperatures, new readout electronics are used, which replace the old one used for the IDP2 (see section 5.1). For the latter the firmware programming is quite complicated and within the work group a much more lightweight solution was present, which was developed in the course of the PETA project [184].
This system consists of a readout board housing the readout FPGA and carrier board on which the DARWIN Test Array can be mounted. It offers the following advantages: 1) The firmware running on the readout board is very lightweight and straight forward to adapt 2) the data transmission is based upon a fast and versatile FTDI USB 3.0 interface, which has a high data throughput 3) The size of the existing carrier board fits perfectly with the experimental platform of the cryostat, so that only minor adaptions to the PCB had to be made.
In the course of this work the existing PETA readout setup was adapted and extended to read out the DARWIN test array in the cryostat. In figure 5.4 a schematic overview of the resulting readout electronics is shown, where the following adaptions and extensions were made: The existing carrier PCB was redesigned, so that it can be mounted in the cryostat. Two adapter PCB were designed to make the carrier PCB and the readout board compatible with the cabling system of the cryostat. The latter, consisting of ribbon cables, that possess ribbon cable plugs, while the carrier and readout boards have Samtec plugs. For the existing readout board in the lab, the firmware was rewritten and a new software for controlling the FPGA from the PC was developed.
In the following subsections the three different PCBs employed in this setup are described.

5.3.1 Printed Circuit Boards

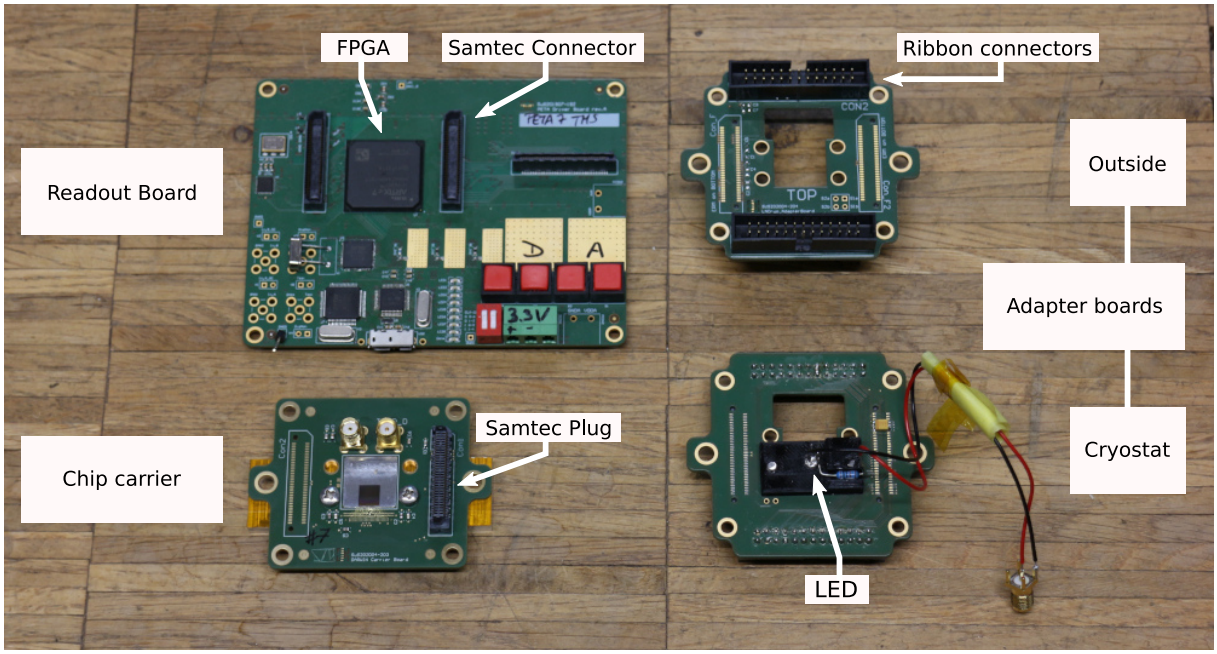

Figure 5.5: Shown are all PCB used for the readout of the SPAD array in the cold. In the upper half the readout board is shown left and its corresponding adapter board on the right, both are situated at room temperatures. In the lower left the chip carrier and on the right side its adapter board can be seen, which are mounted in the cryostat. The adapter boards make the carrier and readout board compatible with the cryostat cabling system.

In figure 5.5 the readout board (upper left), the carrier PCB (lower left) and the two adapter boards (right) are shown, which were, apart form the readout board, all designed within this work.
The readout board hosts the FPGA (Xilinx Artix 7, mounted in the middle), which creates the control signals for the array and processes the hit signal coming from the array. These signals are routed to the Samtec connector of type ERF8 placed on the right side of the FPGA. The connector on the left side, on the other hand, carries only PETA specific signals that cannot be used for this array. The carrier board, which can be seen on the lower left side of the figure 5.5, possesses the corresponding Samtec plug on the right side, so that it is possible to connect both boards directly for test purposes. The connector on its left side, carries no signals and therefore it is not necessary to soldered it onto the board.
The data transmission from the FPGA to the PC is established via a fast USB 3.0 interface IC of type FTDI FT601. In order to maximize the bandwidth, the connection is unidirectional and only data from the FPGA is transmitted to the PC. The control of the FPGA and also programming of the firmware is, on the other hand, done with another USB-controller IC of type FTDI FT2232H. This IC is a USB to JTAG converter and is connected to the JTAG ports of the FPGA. On the one hand the measurement computer can program the firmware on the FPGA via JTAG and on the other hand it can be used during normal operation to send configuration data to the FPGA. Configuration data consists of data for the slow control and for the FPGA internal registers described in the next section. Both ICs, the FT601 and the FT232, are connected to the USB-Hub IC on the board to have only one common USB connection from the PC to the readout board. All three ICs are located below the FPGA and can be seen on the upper left side

of figure 5.5, but are not labeled, for the sake of clarity.
The only disadvantage of the readout board was that its power supply voltage for PETA chip did not fit to the DARWIN test array. The PETA chip requires $V_{DD} = 2.5\,V$, while the CMOS-technology of the DARWIN Test array requires $V_{DD} = 3.3\,V$. The supply voltage is directly regulated on the readout board, but there was no possibility to replace this regulator with another. However, the lower supply voltage of $V_{DD} = 2.5\,V$ did not compromise any of the array's functionality and all measurements were, in the end, performed with this lower supply voltage. At the end of this thesis a new revision of the board was designed in the group, which will then replace the current board for future measurements.
The adapter boards are then used to make the carrier and readout board which, are equipped with Samtec connectors and plugs, compatible with the ribbon cable plugs of the cabling system. Both adapter boards are shown on the right side in figure 5.5. The large clearance hole in the middle, acts as the mounting point for the LED and is used to feed through the SMA cables connected to the carrier board. The LED is glued on a black 3D printed plastic holder, which is screwed on the PCB.
To design only one adapter board PCB, top and bottom are equipped with solder pads for the Samtec plugs and connectors and the ribbon connectors. In order not to mix up signals the plugs and connectors have to be mounted as follows: The readout board requires the Samtec plug, which is soldered on the top side of the first adapter board, while the connectors for the carrier board are soldered on the bottom side of the second adapter board. Connectors for the ribbon cables are always soldered to the top side. This leads to different orientations of the adapter boards on the inside and outside of the cryostat. This is shown in figure 5.4 where they are positioned so that they fit onto the corresponding board on their left side.
Later, additional suppression capacitors of 1 pF were soldered to some selected signal lines to shield them from observed high frequency pick-up signals. The mounting point is the back of the ribbon connectors on the adapter board, which is close to the receiver side. These signals are the hit and error signals (see section 4.3.4), which are most important for the readout FPGA, and the data clock signal for the slow control (see section 4.3.6). This measure improved the signal integrity, and since the capacity of the cables is also quite high it did not lowered the transmission frequency.

5.3.2 Carrier Board

The carrier board is the mounting point for the array in the cryostat and can be seen in figure 5.6. It hosts only a few passive electrical components, which are all placed on the top side, because the back faces towards the experimental platform of the cryostat. As described in the previous subsection all electrical signals for the array, including power and ground connections are routed through the Samtec plug on the right side. During the measurement it is replaced by a dummy plug. The two SMA connector on the top side are used for the SPAD bias voltage and the integrated temperature diode. Suppressor capacitors ($\sim$10 nF) are connected to the supply voltage line, the SPAD bias line and the temperature diode to shield them from high frequency pick-up signals.
When the carrier board is placed inside the cryostat, a good thermal contact between the experimental platform and the SPAD array has to be provided. Therefore the array is mounted on an aluminum holder, which offers a significantly higher thermal conductivity than the fiber glass the PCB consists of. The holder has a small platform in the middle, which fits directly into the clearance hole in the middle of the PCB. In addition, the part of the aluminum holder which is in direct contact with the PCB, is covered with Kapton tape to electrically insulate it from it.
Initially, epoxy resin was used to glue the ASIC onto the aluminum holder. However, during

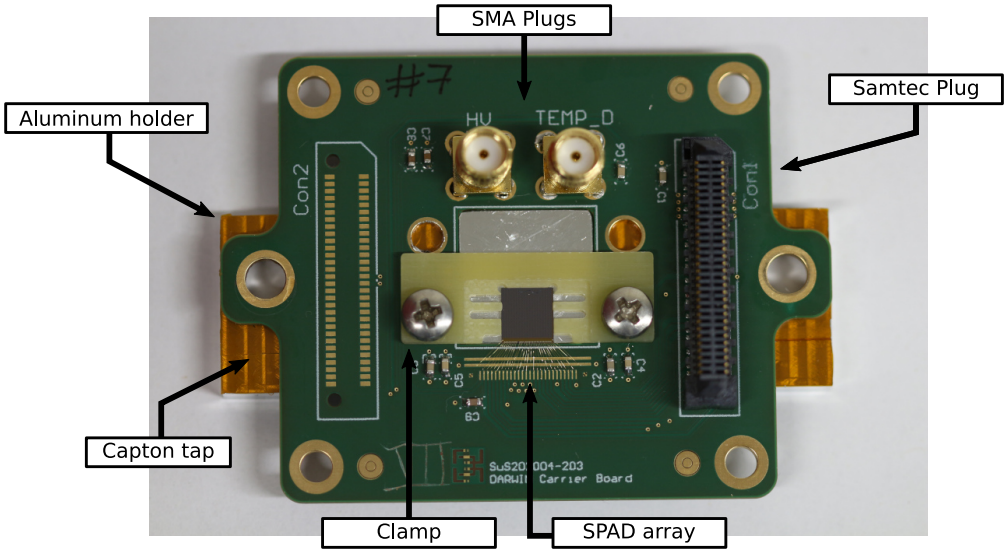

Figure 5.6: Image of the assembled chip carrier board. Below the PCB the aluminum holder, which is partly covered with Kapton tape, can be seen. In the middle there is the electrically connected DARWIN test array with the clamp, attaching it to the aluminum holder.

the cool down of the cryostat several arrays broke. The reason for this is the large difference in the coefficient of the thermal expansion (CTE) of aluminum and silicon. The CTE of silicon is around an order of magnitude lower than that of aluminum thus causing too much tension on the array [185], [186]. A solution for this, which is commonly used in low temperature experiments, is to clamp the silicon dye onto the aluminium holder, which allows both materials to stay in close thermal contact but still move without exerting any tension on each other.
The clamp, holding the array, is seen as a yellow frame surrounding the array in figure 5.6. Below the array a drop of silicon grease (Korasilon) was added to ensure a good thermal contact to the array and the platform. The clamp was designed and fabricated, with the help of Dr. A. Reiser, a member of the Work Group of Prof. Dr. Christian Enss. The base material is a fiber glass compound also used for printed circuit boards. The two bars, which are on the left and right side of the array, act like leaf springs and press the array against the aluminum holder. In order to not harm any electronic structure on the array, the overlap with the array is about 100 µm, which corresponds to the size of its blank silicon margin. Another great advantage of the clamp was that defect arrays were easy to exchange.

5.4 Firmware and Software

The last missing part to gain a full overview of the employed measurement setup is the description of the Firmware running on the FPGA, directly controlling the ASIC, and the software on the PC, which then communicates with the FPGA. The firmware on the FPGA is very lightweight and has mainly the function to program the slow control register on the array and send collected hit data to the computer. The software, on the other hand, has been optimized to automate the measurements as much as possible to reduce the workload of the many successive dark count rate measurements.

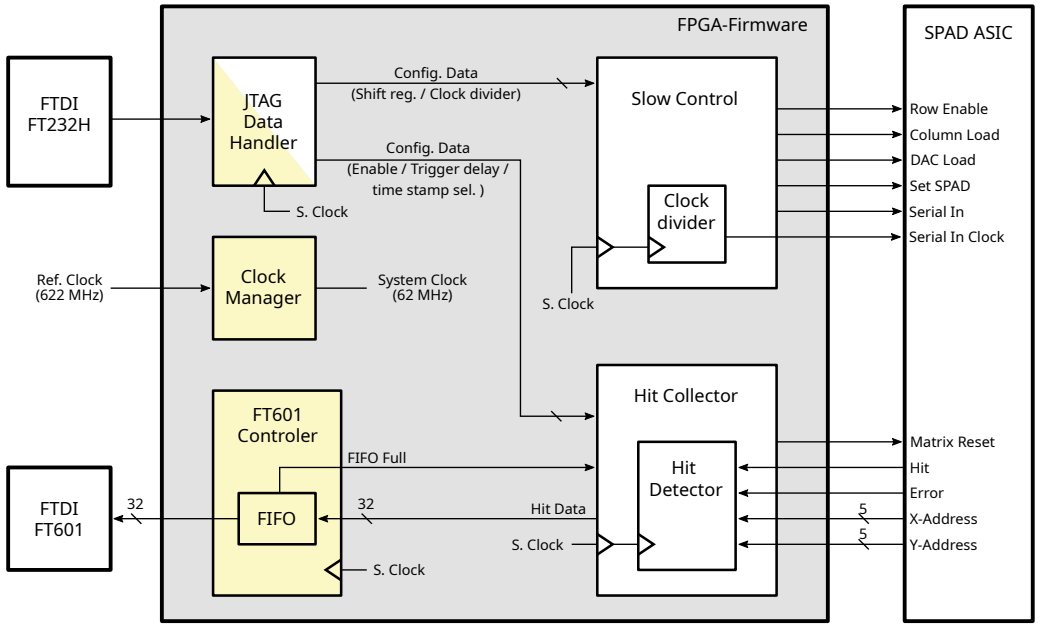

Figure 5.7: Block diagram of the firmware and the connection to the array is shown. In the upper part the JTAG data input and the module for the slow control is visible, while in the lower part the readout and data transferred to the PC is shown. The modules marked in dark yellow are taken from the PETA project.

5.4.1 Firmware

The firmware is written in system Verilog, based on a template of the PETA firmware, and is designed to be lightweight and simple. A block diagram of the firmware is shown in figure 5.7, with the blocks highlighted in yellow taken from the PETA project. The major tasks are to control the array slow control, to read out the data coming from the chip, to send it to the PC and provide configuration data for the firmware, which is done with four modules: 1) The slow control block programs the array shift register. 2) The hit collector detects the hit signal coming from the array. 3) A JTAG register consumes configuration data for the slow control and the firmware data written transfer from the computer 4) The output FIFO acts as a data buffer for the fast FTDI USB interface IC, which transfers data to the computer. Apart from that, one clock generator module is present for clock management.
The clock generation module contains a mixed-mode clock manger (MMCM) primitive [187], which is fed by an external high frequency reference clock with a frequency of 622 MHz. The reference clock signal is in the MMCM module divided by a factor of ten to 62 MHz and is then fed to all modules. This value was actually the default clock frequency of some module of the PETA project. Since individual hit signals have a width of about 300 ns (see section 6), which results in a maximum hit output rate of about 3 MHz, it was not required to enhance this rate. Configuration data for the firmware modules and the slow control of the DARWIN Test array is exclusively sent from the PC via the FTDI FT232H IC into the FPGA using the JTAG-Protocol. In the JTAG-Data Handler module the JTAG data is accessed with a BSCAN2 primitive [187] and copied by the internal state machine. Upon a completed transmission, the data is distributed to its final destination. For this the input data string is separated into one part belonging to the slow control, and into one for the read out module. These bit strings are then compared to the present data and, in case of a change, an update signal in combination with the new data is sent to the corresponding module. The slow control module programs the 121-bit long shift register

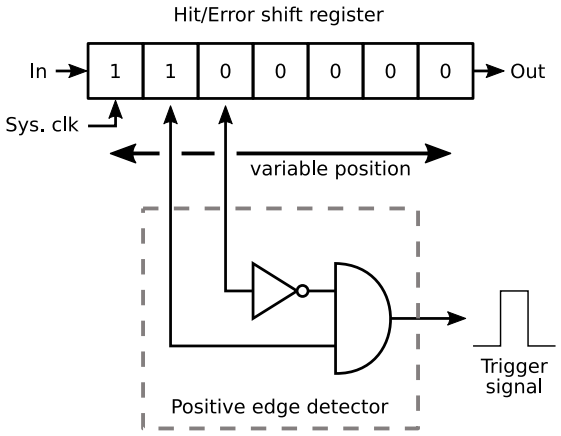

Figure 5.8: Positive edge detector for the hit and error signals as implemented in the firmware. The shift register, where the signals are clocked in, are used to create a delayed trigger signal by setting the inputs at a variable stage of the register.

of the DARWIN Test array. A state machine creates the clock signal for programming the arrays serial register and simultaneously outputs the required 121-bit of data serially. Finally it creates the necessary signal pattern to program the DAC or the matrix (see section 4.3.6). Programming can be done with variable speed since the timing can shift towards lower temperatures and, for example, setup or hold times can be violated. For this a clock divider module is utilized, which outputs an enable signal when the value of an internal 16-bit counter is equal to an externally set 16-bit value (send via JTAG). Only when the enable signal is flagged can the state machine proceed to the next state, which effectively reduces its operational speed without affecting synchronism with the system clock.
The Hit Collector reads out the asynchronous hit and error signals coming from the array. These are searched for with a positive edge trigger, of which the output signal has an adjustable delay. The latter was necessary since the address bits had a delay with respect to the hit or error signal, in the order of 15 ns. On the rising edge of the trigger signal the internal state machine then samples the 10-bit address of the firing macro pixel, adds a time stamp to the address and writes the data directly into the output FIFO.
The schematic of the logic of the edge detector is in figure 5.8. The hit, error and the address signals of the array are clocked into shift registers to synchronize them with the system clock. The positive edge detector performs a logic AND between two neighboring stages of the shift register, whereas the input coming from the right stage is inverted and corresponds to the value one clock cycle delayed. If there is a change from 0 to 1 a hit occurred and a pulse is output. The position of the inputs of the positive edge detector can be freely chosen and therefore a delay to the actual hit event is created, which can be up six clock cycles.
On a positive edge of a hit or error signal a 20 bit time stamp is generated. The time stamps is a 20-bit long bit string extracted from a 64-bit counter, running at system clock speed. The subsection of the counter output register which is extracted, is adjustable via the JTAG configuration data. When a higher bit address is selected the least significant bit of the time stamp bit has less accuracy but the wrap-around time is increased and vice versa for a lower position. Finally, the 20-bit time-stamp and the 12-bit address are concatenated into a 32-bit wide register, which is then written in the output FIFO (1024 words wide) of the FT601-Control module as long as the FIFO full signal is not flagged. The length of the hit bit-string is chosen to match the width of the output buffers of the FT601 IC. The latter collects the data in the FT601-Control module output FIFO and transfers individual 32-bit data words via the fast USB 3.0 interface, to the computer. The transmission rate can be up to $300\,\mathrm{MB\,s^{-1}}$, which is more than sufficient for this experiment, where hit rates of some 100 kHz have to be measured at least at room temperature.

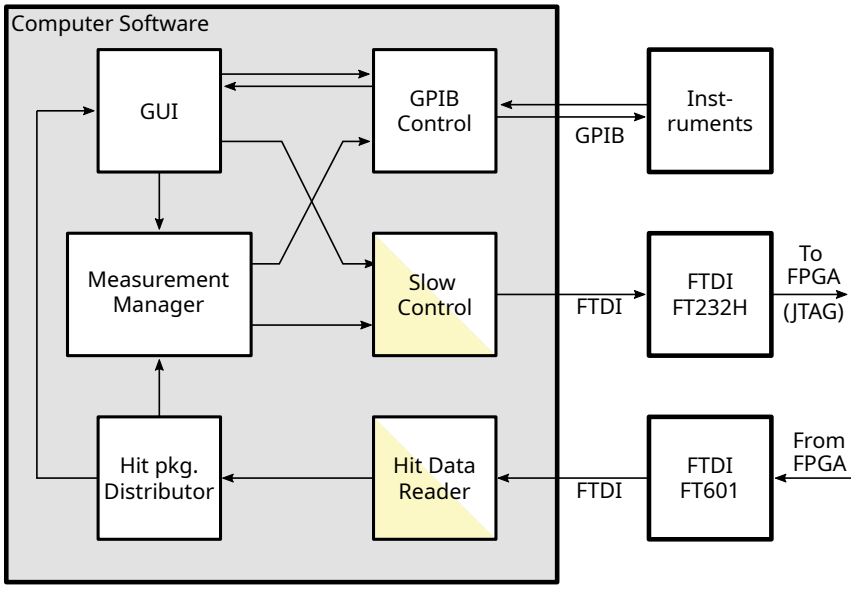

Figure 5.9: Block diagram of the software. The blocks marked partly in yellow are taken from the PETA project.

5.4.2 Software

The main purpose of the software is to be a reliable platform for the great number of dark count rate measurements that need to be performed with the DARWIN test arrays. It has been optimized to automate the measurements as much as possible. One of its main features is, for example, that several successive measurements can be configured with different parameters and then are performed automatically. The software is written in C++, is multi-threaded so that four threads work in parallel and has a Graphical User Interface (GUI) which is based on the QT framework [182]. A block diagram of the software is shown in figure 5.9. The arrows visualize the data flow between the different blocks and the blocks marked partly in yellow, include methods for the communication with the FPGA taken, which are from the PETA project.
The central control element is the GUI. With it, control settings of all kinds can be made: The pixel matrix can be configured and the SPADs of the macro pixel can be enabled or disabled. Parameters like, DAC value, slow control clock speed and readout delay can be adjusted. Furthermore, permanent reset, fast recharge signals (see section 4.3.3) and finally the Hit Collector on the FPGA can be enabled or disabled (see previous section). The slow control class holds all the configuration data for the matrix and the FPGA and sends it, on a change in them, via the JTAG interface chip FTDI FT232H to the FPGA. On the startup the latter class also programs the firmware on the FPGA. Furthermore, via the GUI the measurements to perform are configured and the instruments can be controlled.
Hit data detected by the FPGA is transferred via the fast FTDI USB 3.0 interface to the computer, when the software requests it. Every 100 µs a thread inside the reader class requests the transfer and reads a whole burst of hit data. Each hit consists of a 32-bit strings and is put in a hit container class on its arrival. This class holds the hit string and with its methods the hit address, the time stamp and the Error bit of the hit bit string can be accessed fast. The individual hit containers, in return, are put into a hit package and, after a finished data transfer, the hit package is put in an output queue. The latter is emptied every 100 ms by the hit package distributor.
From the hit package distributor the hit packages are distributed to all other classes. A copy

of them is directly sent to the GUI, where the hit rate and location can be monitored with an intensity map of the array and a rate histogram where the number of hits is plotted against time. During a measurement, the packages are collected and merged to a single large one. To identify which package belongs to an individual measurement, an ID is assigned to them on arrival and the first and last package is marked like this. Preceding the enabling of the hit collector, the FPGA sends a unique start bit-string as well as stop bit-string, on disabling. The same ID is assigned to all packages between the start and the stop string. When no measurements are done, hit package are deleted to prevent memory overflow.
Measurements are configured in the GUI. The aim was to take several successive measurements with different parameters and SPADs. For this purpose, a list of measurements can be created, the parameters for each measurement can be set and when the start button is pressed, all measurements are performed one after the other. The basis of this class builds the QT model/view architecture. This architecture is intended to manage the relation between data and its manner of presentation during run time [188]. The measurement parameter-container is hidden behind an abstract model class, which accesses the data when it is requested over the GUI. The individual measurements are displayed in a list, where they can be added and deleted. Once added, their parameters can be adjusted over a separate editor window. With it, the cryostat temperature, the measurement time, the SPADs to measure and the SPAD bias, can be adjusted. Furthermore, it is also programmable if all macro pixels are to be measure at once or if chunks of it like 3x3 pixels, should be measured.
For the actual measurement, the list of individual ones is sent to the measurement manager where they are done, one after the other. A separate thread performs the measurement so that the data collection carried out in the main thread, is not disturbed. In the beginning of the measurement the matrix is configured, the bias voltages set, and the hit package distributor is informed to collect the packages. Then the Hit collector module on the FPGA is enabled via the slow control class, and a timer for measurement started. The timer's accuracy is actually limited to 100 ms and in addition, the transfers of the enable bit via JTAG introduced an additional delay. This however, does not distort the dark count rate determination: At room temperature the dark count rate is high and with the time stamp of the individual hits the measurement length can be determined within 1 µs accuracy. At low temperatures where almost no hits occur and hours of measurement time are required, a delay of even a few seconds is neglectable.
The measurement thread waits until the central data class has collected the last hit package, which is labeled with the stop sequence. Then all hits of the completed hit packages, including those with a set error bit, are written to disc. In addition, all measurement parameters and the tracked temperature and power consumption are written to disk. A new directory is created for each measurement, which is labeled with the time and date so that it cannot be overwritten by default. Time and date can be used as identifier, since all measurements are also logged in a lab book with date and time. The final data analysis is done completely offline with a data frame work written in python, of which the functionality is partly described in section 6.2.
The last part is the GPIB controller, which controls the instruments for setting bias voltages as well as the temperature inside the cryostat. Furthermore, power consumption and temperature is recorded once per second and is displayed in the GUI. All instruments can be controlled via the main GUI, but also the measurement manager has access to the instruments. The GPIB controller is made thread-safe so that power and temperature tracking wont interfere with the setting of parameters in the measurement class or form the GUI. For this a simple event loop is implemented, where request for changes of parameters of an instrument are added in a queue. Then the requested actions are performed, one after the other, by the thread. Read-in values like the temperature or the power consumption are then put into an output queue belonging to the instrument for which the change was requested, and the requester is notified that the result is ready.

6. Digital SiPMs at Various Low Temperatures

Within this chapter the results of the characterization of Digital SiPMs at low temperatures are shown. The aim is it to investigate the suitability of this kind of light detector for the DARWIN experiment, where the detector must be operated at cryogenic temperatures of $T \approx 165\,\mathrm{K}$.
With the IDP2, an array not optimized for cryogenic operation, a first insight into the behavior of Digital SiPMs at low temperatures, was obtained. The temperature profile of the dark count rate was successfully recorded and showed that the dark count rate at cryogenic temperatures has to be lowered to meet the constraints of the DARWIN experiment. Furthermore, effects were observed like the so-called hot SPADs, which are SPADs with significantly higher noise than a average SPAD, actually become average SPADs at lower temperatures and can be used for photon detection. Moreover, photon emission of current drawing electronics was observed, which has to be omitted to operate the array at its genuine noise performance.
Based on these results the DARWIN test array, a dedicated prototype to the DARWIN experiment, was developed. Three process variations (wafer-wise) have been implemented by our vendor to reduce the dark count rate at low temperatures. The test array also houses ten SPADs of different shapes and sizes to observe how the dark count rate and also the number of hot SPADs, scale with the SPAD geometry. Finally, it was observed that the noise is independent of the SPAD geometry so that large ones with a high fill factor, can be used. However, the effective fill factor, which is the residual fill factor after turning off the hot SPADs, shows that there is an optimal size since large SPADs have also have more hot SPADs. This optimal size increases with temperature, as the number of hot SPADs decreases.
The following section describes the data acquisition of the IDP2 as well as the DARWIN test array while the subsequent section describes the methods of the data analysis. Then the results of the IDP2 are shown, which are the breakdown voltage, the dark count rate, the hot SPADs and the photon emission effect. Finally, the results of the DARWIN test array are discussed. In the beginning the breakdown voltage is described and the dark count rate of the process variations. Then, in detail, the effect of the SPAD size on the dark count rate and the number of hot SPADs at low and high temperatures are described. Lastly, the correlated noise and its impact on the DARWIN experiment is briefly discussed and the so-called start up effect of the SPADs is described.

6.1 Data Acquisition

This first section describes in detail the data acquisition for the IDP2 and the DARWIN Test array. It briefly summarizes which cryogenic setup was used, in which format the arrays output their data and how the arrays are configured for the measurement. Then it shortly describes how the breakdown voltage is measured and finally the dark count rate measurements are discussed with particular reference to the data accumulation time.

6.1.1 IDP2: Single Photon Camera

Cryogenic Setup: A first extensive insight into Digital SiPMs with the IDP2 at various low temperatures was obtained with the bath cryostat described in section 5.1. The cryogenic setup was quite simple and only a short preparation time was needed for its setup. Various cooling mixtures were used, delivering predefined bath temperatures, which were, to some extent ad-

justable by varying the height of the array above the bath. In total it was possible to take measurements at 19 different temperatures. During these, a decent temperature stability was obtained. An average drift of 1 K per (∼20 min) was observed, which was mostly enough to perform a characterization at a single temperature. However, producing the different cooling baths was time consuming and cumbersome. As a consequence of this inconvenient behavior of the cryogenic setup, a full dark count rate characterization was only done for a single array. Nevertheless, at room temperature and liquid nitrogen temperatures a second array confirmed the measured dark count rates.

Array Output Data: During a dark count rate measurement with the IDP2, binary single photon images, also called frames, including the one bit hit information of each SPAD, are recorded. The accumulation time per frame is programmable and the total measurement time is therefore the product of the number of frame and the accumulation time per frame. To reduce the amount of accumulated data, for each measurement all recorded frames are summed up and only a single integrated image, including an integer number of the accumulated hits for each SPAD, is saved to disk.

Breakdown Voltage: The breakdown voltage was determined by means of the excess bias voltage dependent dark count rate measurement, which is described next.

Dark Count Rate: At each temperature the dark count rate was measured at various SPADs bias voltages. Starting from shortly below the breakdown voltage the bias voltage was gradually increased until the dark count rate started to increased rapidly (see section 6.4). Approximately 20 bias voltage steps were made per temperature. The breakdown voltage was extracted from the resulting voltage dependent noise curves measurement, according to the description in the next section.

At the various temperatures and bias voltages, the following frame numbers and integration time windows were chosen: At room temperatures the dark count rate was about 45 Hz for the average SPADs and the hot SPAD rate was roughly two orders of magnitude higher. A frame integration time of 6.6 µs was chosen to prevent saturation of the hot SPADs. To gather a decent amount of statistics for the average SPADs, a total number of 1500000 frames were accumulated so that the measurement time was 1 s. From room temperature the dark count rate then decreased exponentially, to 2 Hz at $T = 273$ K. Therefore, the total measurement time was increased to 7.5 s at $T = 280$ K and 15 s at $T = 273$ K. However, the high number of frames of 1500000 was kept and only the integration time increased to also measure the hot SPAD rate free from saturation. The dark count rate of these decreases only one order of magnitude in this temperature range. For temperatures below $T = 244$ K, the decrease in dark count rate was much weaker and the number of hot SPADs started to decrease (see section 6.5). The average SPAD dark count rate at $T \approx 240$ K was about 1 Hz and decreased to 0.3 Hz at liquid nitrogen temperatures of $T = 77$ K. For this range the number of recorded frames was 50000 and the integration time per frame was 2 ms, making it a measurement time of 100 s.

6.1.2 DARWIN Test Array

Cryogenic Setup: The dark count rate of the DARWIN Test Array was measured with the vacuum liquid nitrogen cryostat described in section 5.2. With this setup, measurements at low temperature with long time exposure and high temperature stability, are possible. Any desired temperature between $T \approx 296$ K and $T \approx 100$ K is adjustable. To cover the whole range in a reasonable amount of time, measurements are made at 11 different temperatures with an interval of $\Delta T = 20$ K.

In total eight DARWIN test array were fully characterized. Two arrays from each of the three wafers were utilized, which were fabricated using experimental process variations implemented

to improve the dark count rate at low temperatures (see section 4.3.1). A further two arrays were utilized originating from a wafer made in the standard process, which is the established SPAD processing of our manufacturer, IMS. Gathering the data for each of the eight arrays took about one year, including also time lost due to defects and destroyed arrays and time investment in optimization of the measurement software.

Array Output Data: During a dark count rate measurement only one SPAD out of ten in the macro pixel was switched on, the remaining ones were switched off. Those SPADs have a different size and aspect ratio (see section 4.3.4). The DARWIN Test array delivers a 10-bit x/y-address of the hit macro pixel and, in case of a coincidence hit, an error signal is output (see section 4.3.5). The FPGA adds a 20-bit time-stamp (see section 5.4.1) to the address before transferring the data to the computer. The LSB accuracy of the time-stamp is variable and set according to the measurable length, so that the timer did not overflow. Every detected hit, including the timing information, is stored to disk, to investigate any time dependent effects of the rate. Error signals are also written to disk to evaluate cross talk and monitored online to omit rate saturation effects. Accumulation of the dark counts then happened in a defined exposure time-window set up on the measurement computer (see section 5.4.2).

Array Settings: The versatile front-end circuitry of the macro pixels had several operating modes (see section 4.3.4), of which a entire characterization was beyond the scope of this work. During operation, the circuitry was configured as follows: The hit flip-flop was permanently disabled and the front-end was set to the passive quench mode (see section 4.3.3). With active feedback, the reset signal triggered by the FPGA, sometimes did not work and the array became stuck in operation. The reason for this is not entirely clear, as such behavior cannot be observed when only an individual macro pixel is activated and operated with active quenching feedback. The SPAD adjustable recharge current (see section 4.3.3) was configured at room temperature, so that the output signal length (see section 4.3.4) was about 300 ns, to prevent excessive error signals. This corresponds to the minimal delay of the readout circuitry in the periphery (see section 4.3.5) and no shorter signal is obtained when the current is further increased. At temperatures below $T \approx 200\,\mathrm{K}$ a afterpulsing pile-up effect occurred. A sudden increases in the detected rate was observed, which was considerably worse under illumination. It is assumed that the after pulsing probability at this temperature is so high that afterpulses are the origin of new afterpuslses and so the rate rapidly increases. This effect was reduced by increasing the recharge current. The signal length increases to about 1 µs, so that most of the afterpulsing is masked by the recharge process (see section 3.7.1).

Break down Voltage: When a new array was installed in the cryostat, the breakdown voltage was determined for the entire temperature range (before measuring the dark rate), using additional light from the LED (see section 5.2).

Excess Bias Voltage: Dark count rate measurements were performed at constant excess bias of $V_{\mathrm{Ex}} = 1\,\mathrm{V}$. The low dark count rate at low temperatures making long exposure times necessary, made excess bias voltages sweeps, like for the IDP2, unfeasible. The choice to measure at a relative low excess bias of $V_{\mathrm{Ex}} = 1\,\mathrm{V}$ had various reasons: First, the maximal applicable excess bias, or more precis the signal height, is limited to the supply voltage due to SPAD front-end electronics of the DARWIN test chip (see section 4.3.3). Also, the supply voltage was reduced to $V_{\mathrm{DD}} = 2.5\,\mathrm{V}$(see section 4.3.3) so that the maximal excess bias was $V_{\mathrm{Ex}} = 1.7\,\mathrm{V}$. Finally, with our determination of Breakdown voltage a offset of about 0.8 V is introduced compered to the breakdown voltage measured with the IV-curve (see section 6.2.1). So the excess bias is actually higher, but since the offset is not exactly known and may vary with temperature, it was decided to stick with our definition. A IV-Curve measurement method is in planing to be more comparable to other SPADs.

Second, the PDE at low temperatures is unknown and might increase with decreasing tempera-

tures (see section 6.3.2). However, very little is known of the PDE changes at low temperatures and has to be evaluated in near future. Nevertheless, Digital SiPMs at room temperatures show a relatively good PDE already at low bias voltages (see section 6.3.2). If the present bias voltage is not sufficient for the PDE, voltage can be increased (with a change of the readout board), which is at low and high temperatures accompanied by a moderate increase in noise (see section 6.9.1). Finally, and perhaps not directly comparable: SiPMs with optimizations in VUV light, from different vendors, already reach their maximal PDE at relative low voltages ($V_{\mathrm{Ex}} = 2 - 3\,\mathrm{V}$) [189]. Since comparable optimization steps are made (see section 4.3.1), it might be also the case for digital SiPMs. However, these arrays are still in manufacture and on their arrival have to be tested for noise, which might be worse due to the more complex manufacture, and the QE.

Dark Count Rate: At room temperatures the readout was saturated, due to the high rates of the individual SPADs (particularly the large ones). Consequently, the macro pixels were measured one after the other or in groups of 3×3. Here, the count rate for the smallest and largest SPAD was 20 Hz and 600 Hz, respectively. A measurement time of 2 s per macro pixel was chosen to perform the measurement in a moderate time. For decreasing temperatures, up to $T = 240\,\mathrm{K}$, the dark count rate dropped about one order of magnitude per 20 K. Subsequently, for $T = 280\,\mathrm{K}$ saturation of the rate stopped and all macro pixels were measured at once. The measurement time was 1 min at $T = 280\,\mathrm{K}$ and 10 min at $T = 260\,\mathrm{K}$, which resulted in a reasonable number of dark counts per SPAD.

Below $T = 240\,\mathrm{K}$ tunneling noise becomes dominant and the impact of the process variations became visible. Process variation 1 and 3 showed only an improvement of the rate of half an order of magnitude compered to the standard process, so that the exposure times stayed in the same order of magnitude. At $T = 220\,\mathrm{K}$ the smallest and largest SPAD of the array, made in the standard process, have roughly a value of 2 mHz and 75 mHz, respectively. The measurement time of the SPADs is chosen to be about 30 min. Tunneling noise has a lower temperature dependency and below $T = 220\,\mathrm{K}$ the count rate decreased about an order of magnitude per 60 K. Up to $T \approx 160\,\mathrm{K}$ a measurement time of 30 min was still sufficient. Below and down to 100 the measurement time, however, had to be increased to 1 h for the larger SPADs (SPAD 0,1,6,8,9) and 1.5 h for the smaller ones (SPAD 2,3,4,5,7) (see section 4.3.2).

Process variation 2, on the other hand, showed a reduction in tunneling noise of more than an order of magnitude better than arrays made in the standard process. For those low noise arrays, tunneling becomes dominant at a lower temperature of $T = 220\,\mathrm{K}$, correspondingly, the measurement time has to be increased already at higher temperatures. At $T = 220\,\mathrm{K}$ the smallest SPADs had a dark count rate of about 0.3 mHz and the largest ones 8 mHz. The dark count rate also roughly decreased one order of magnitude per 60 K. Up to $T = 200\,\mathrm{K}$ the measurement time was 30 min. From 180 K to 160 K it was about 1 h, and below, even increased to 3 h. At 140 K, for example, a medium sized SPAD had a dark count rate of 60 µHz, so that even with 3 h measurement time only a few SPADs accumulated at least one hit. However, increasing the measurement time was barely feasible as it took already 30 h for 10 SPADs for a single temperature.

Excess Bias Sweep: To investigate the bias voltage dependency of the dark count rate in a modest time exposure, voltage sweeps at distinct temperatures of $T = 160\,\mathrm{K}$ and $T = 260\,\mathrm{K}$ were performed with a small, medium and large SPAD (3,1,8). In both cases, 10 steps with voltages from $V_{\mathrm{Ex}} = 0.4\,\mathrm{V} + V_{\mathrm{BD}}$ to $V_{\mathrm{Ex}} = 1.8\,\mathrm{V} + V_{\mathrm{BD}}$ were measured. It has to be mentioned again that for all dark count rate measurements, the arrays supply voltage was $V_{\mathrm{DD}} = 2.5\,\mathrm{V}$ due to the voltage regulation on the FPGA board (see section 5.3.1), so that higher excess bias voltages cannot be reached.

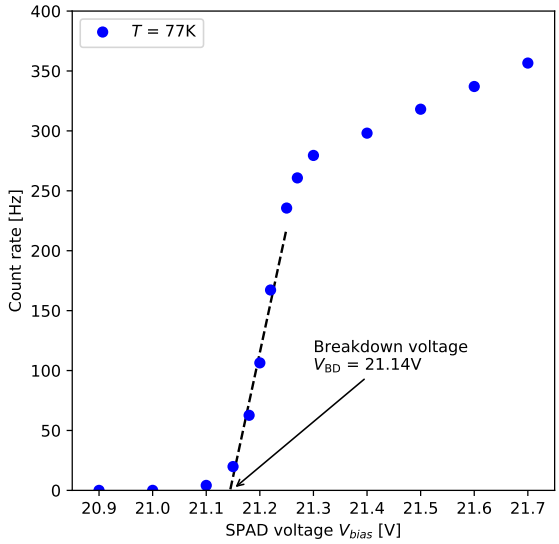

Figure 6.1: Typical rate measurement of the IDP2. When the bias voltage approaches the breakdown voltage the SPADs become active. The rate swiftly increases which is caused by small variations in between the breakdown voltages of the SPADs. The observed rate settles when all SPADs are active. The breakdown voltage is defined as zero crossing point of a linear regression (black dashed line) of the steep rate onset, to which the arrow points.

6.2 Data Analysis

This section describes the analysis of the acquired data on the basis of the rate measurements described in the previous section. The entire analysis is done offline within a custom-made python framework. First, the breakdown voltage for the various temperature has to be determined. Then the dark count rate has to be evaluated at all temperatures, including the extraction of the number of hot SPADs. It has to be noted, that error bars are mostly not shown in the plots of this chapter, since the errors were quite small. However, errors have not been neglected during the course of this work and are included in the discussion when necessary.

6.2.1 Breakdown Voltage Determination

The breakdown voltage V_{BD} is one of the key parameters to operate SPADs at a comparable operational point, at different temperatures. It decreases towards lower temperatures and has to be re-evaluated for each measurement temperature (see section 3.4). Within this work the determination of the breakdown voltage is based on evaluating the average count rate of the SPADs in the array during a voltage sweep from below, to a certain excess above, the breakdown voltage. The measured count rate is either from dark counts or is induced by additional light from an LED. Other methods, like the evaluation of the onset of current flow (I-V curve) during a voltage sweep as described, for example, in [103], were not possible since the available current meters are not sensitive enough.
A typical result of a bias voltage sweep performed with the IDP2 at $T = 77\,\mathrm{K}$ is shown in 6.1. Initially, the observed rate is zero until the breakdown voltage is reached. The count rate starts to increase rapidly since there are small variations in the breakdown voltages of the individual SPADs. When all SPADs are biased above breakdown, the rate flattens out. The further increase of the count rate is caused either by increase of photon detection efficiency (see section 3.5) when light is utilized or by the increasing dark count rate (see section 3.6). According to our definition, the breakdown voltage is then the zero crossing of a linear regression of the steep slope.
Naturally, this method introduces an offset with respect to the actual breakdown evaluated with an I-V curve. The SPAD signal has first to surpass the threshold voltage of the front ends CMOS logic in order to be detected. For the DARWIN test array, where the SPAD input is directly connected to a CMOS inverted (see section 4.3.3), the offset is equal to its threshold voltage of

about 0.8 V. Therefore the DARWIN Test array is actually operated at $V_{\mathrm{Ex}} \approx 1.8\,\mathrm{V}$. However, in this work the excess bias is specified using our definition. With the IDP2, the SPADs are AC coupled (see section 4.2.1) and the offset additionally depends on the input capacitance of the discriminator (capacitive voltage divider). Actually, a difference between the breakdown voltage of the IDP2 and the DARWIN test array made in the standard process of $\Delta V = 1.5\,\mathrm{V}$ was observed (see section 6.7). Both arrays are made with the same processing, so this deviation is attributed to the AC coupling scheme.

6.2.2 Noise Evaluation

The dark count rate of the IDP2 and the DARWIN Test Array at various temperatures are evaluated by means of the following method: The average value of the dark count rate of the average SPADs is extracted by fitting an appropriated probability density function to the dark count rate distribution. So-called hot SPADs, having a significantly higher dark count rate than the average SPADs, are excluded from the evaluation. Depending on the amount of the statistics, i.e. the number of accumulated hits, the average rate is determined using either a Gaussian or Poisson regression and afterwards normalized to the active area of the SPAD (including their rounded corners, see section 4.3.2). A normalization that allows a comparison of the dark count rate of SPADs of different sizes. The dark count rate at different temperatures is, in turn, made at equal excess bias voltages. In figure 6.2 examples for the noise evaluations of the DARWIN Test array are shown. A Gaussian regression used at a temperature of $T = 260\,\mathrm{K}$ is shown on the left, while on the right there is an example of a Poisson regression at $T = 160\,\mathrm{K}$.

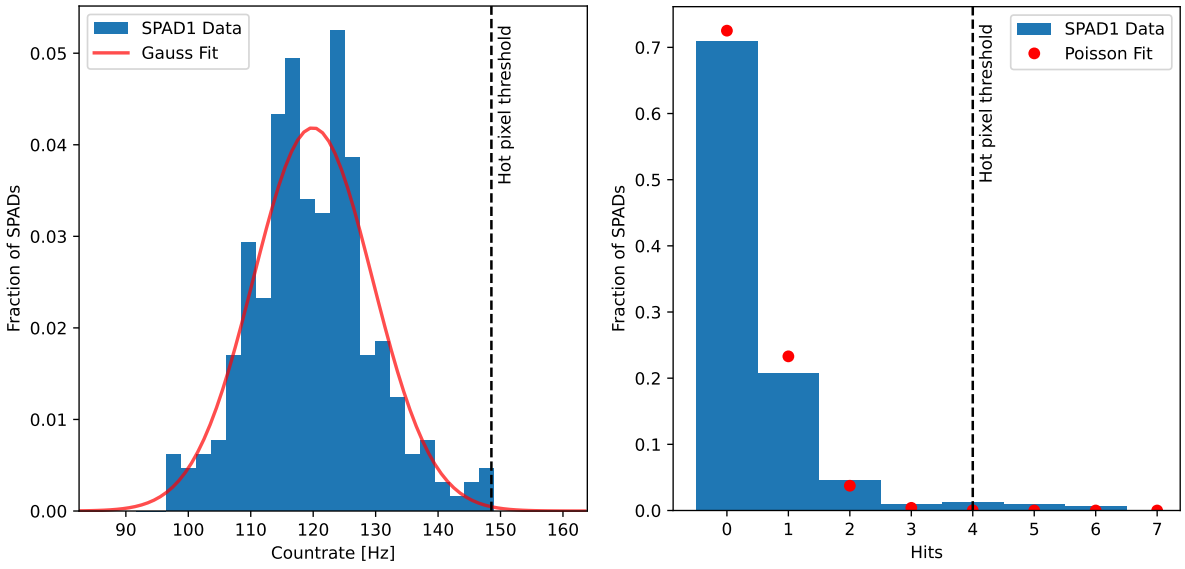

Figure 6.2: **Left:** Noise evaluation at $T = 260\,\mathrm{K}$ in with a Gauss regression of the normalized dark count rate distribution. The histogram comprises the dark count rate of the individual SPADs gained by dividing the SPAD number of accumulated hits by the measurement times. **Right:** Noise evaluation at $T = 160\,\mathrm{K}$ with a Poisson regression of normalized dark count rate distribution. The histogram comprises the number of hits accumulated by the individual SPADs. The dashed lines are the thresholds above which the SPAD are classified as "hot".

For temperatures between $T = 296\,\mathrm{K}$ and $T = 240\,\mathrm{K}$, the dark count rate is high and decreases swiftly from $25\,\mathrm{kHz\,mm^{-2}}$ to $50\,\mathrm{Hz\,mm^{-2}}$, regardless of the SPAD size (see section 6.8). Within

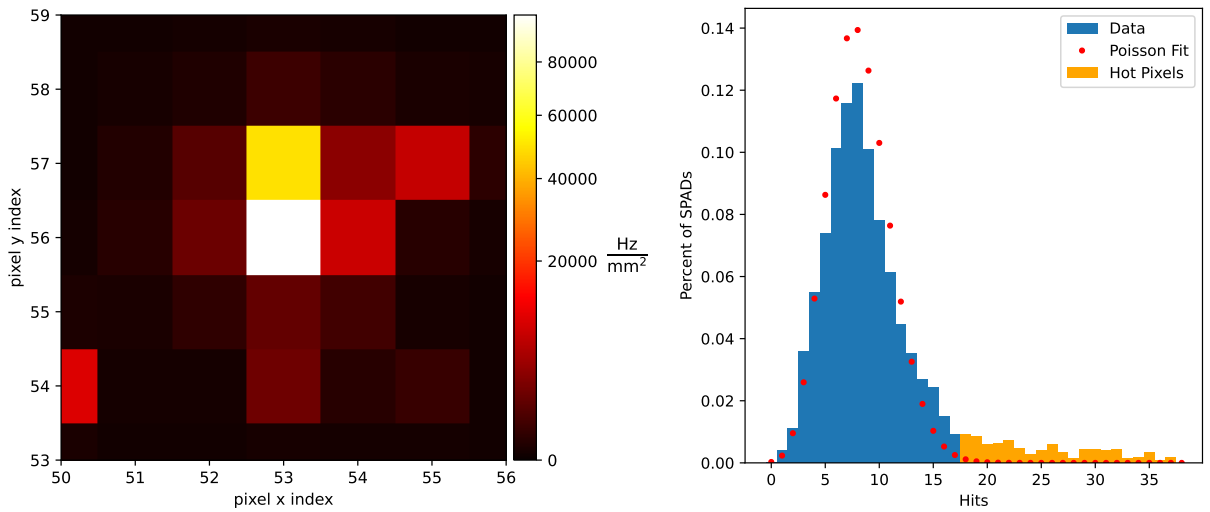

Figure 6.3: **Left:** Dark count rate intensity map with a very active hot SPAD in the center, which enhances the count rate of the direct neighbors by cross talk. **Right:** Dark count rate distribution with a tail (orange) introduced by crosstalk, caused by hot SPADs. SPADs in the tail are initially average ones but are misidentified as hot.

this temperature range the dark count rate distribution is well described with a Gaussian regression. The rate histogram comprises the dark count rate of the individual SPADs, determined by dividing the number of accumulated hits of the SPADs by the measurement time. SPADs having a count rate above three sigma of the Gauss curve, indicated by the black dashed line, are flagged as hot SPADs. Their number is extracted to investigate it as a function of temperature. Due to their high rate within the depicted range, no hot SPAD is visible. However, a logarithmic plot, showing the whole rate range can be found, for example, in figure 6.17.
At temperatures below $T = 240\,\mathrm{K}$ to $T = 220\,\mathrm{K}$ the dark count rate becomes very low and the low statistic regime is reached. This means that, then during the measurement time roughly less than 10 hits per SPAD is accumulated. For example, for the DARWIN array at lowest temperatures a significant number of the SPADs had shown zero hits, even though the measurement time was about 3 h. A Poisson distribution, which can be seen on the right side of figure 6.2, describes the data well and the mean value of the regression divided by the measurement time corresponds to the dark count rate. The histogram comprises the number of accumulated hits of the individual SPADs. The number of hits above which a SPAD is classified as hot, is when intensity of the Poisson distribution drops below 0.15%, shown as a black dashed line on the right side of figure 6.2. Since, the lack of a 3 sigma criteria, as for a Gauss distribution, an empirical value was chosen after inspecting several dark count rate distributions. Above this threshold the SPADs definitely do not contribute much to the mean value of the distribution and can therefore be seen as hot. Overall, the introduced systematic error is assumed to be small.
Three important comments on the IDP2 data analysis, which do not relate to the DARWIN Test Array: First, extraction of the rate at a certain excess bias voltage V_{Ex} is done with a spline extrapolation of the voltage-dependent dark count rate curve. Second, photon emission from the readout electronics impairing the dark count rate of the lower part of the matrix. For the evaluation of the mean dark count rate, only the upper half meaning, 44×88 pixels of the matrix were analyzed. Finally, hot SPADs lead to a significant amount of cross talk in the surrounding SPADs, which is shown in for one example hot SPAD on the right side of figure6.3. This effect can be observed until the number decreases significantly at lower temperatures ($T \approx 160\,\mathrm{K}$).

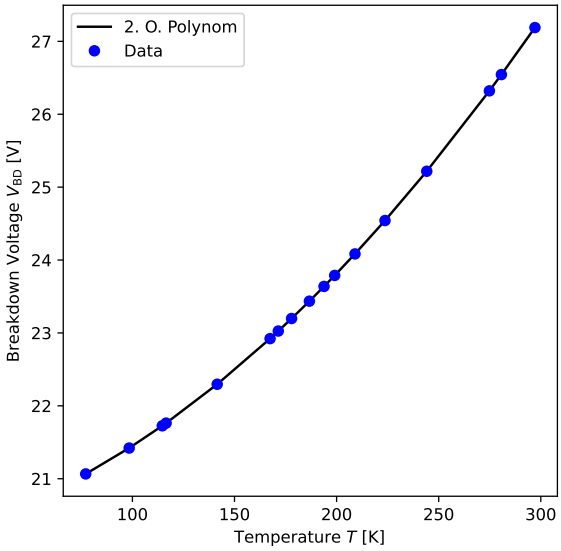

Figure 6.4: Breakdown voltage as a function of the temperature (blue dots). The black line is a polynomial fit of the second order to extrapolate the breakdown voltage at various temperatures.

The artificially enhanced count rate caused a tail in the noise distribution, which leads to an overestimation of the number of hot SPADs. An example for this at $T = 240\,\mathrm{K}$ is shown on the right side of figure 6.3, the orange tail corresponds to the SPADs which are wrongly marked as hot SPADs. To extract a more reasonable number of hot SPADs, all average SPADs are masked first (offline in the python analysis software). Then the noisiest SPADs, with the surrounding eight SPADs, are masked in sequence until no SPADs remain. The number of hot SPADs is only incremented when the iteration passes an unmasked SPAD. Apparently, with this method, neighboring hot SPADs are counted as one, which introduces a systematic error. However, the number of neighboring hot SPADs is small and, for the IDP2, the greatest interest lies in the temperature dependency of the hot SPADs.

6.3 IDP2: Breakdown Voltage and Sensitivity

The IDP2 was the starting point of the measurement series of Digital SiPMs at lower temperatures. The first quantity that has to be determined is the breakdown voltage since the excess bias defines the operation point of the array. Furthermore, it was also tested that the array is still sensitive to light at low temperatures.

6.3.1 Breakdown Voltage

Since the breakdown voltage decreases with temperature (see section 3.4) it is inevitable for the operation of the array, and the noise characterization, that it has to be evaluate for various temperatures. In figure 6.4 the breakdown voltage for various temperature is shown. The black line corresponds to a polynom fit of the second order, which has no physical meaning and is used for calibration purposes and to determine the temperature coefficient. The breakdown voltage decreases with temperature since the mean free path of the charge-carrier, drifting inside the depletion region of the SPAD, increases. Consequently, a lower field is needed to perform impact ionization. The exact shape of the breakdown voltage temperature profile is, however, difficult to predict because the SPAD doping profile, which defines the electric field and is unknown to the author, plays an important role in it.
Within the measured temperature range it decreases by about 6 V between $T \approx 296\,\mathrm{K}$ and $T \approx$

77 K. In the beginning it decreases nearly linear, while at lower temperatures of $T = 200\,\mathrm{K}$, the curve flattens. The temperature coefficient, which is important for the stability of the operation point against temperature fluctuations [100], is $40\,\mathrm{mV\,K^{-1}}$ at $T = 296\,\mathrm{K}$. At lower temperatures of $T = 160\,\mathrm{K}$ it decreases to $25\,\mathrm{mV\,K^{-1}}$. Both are fairly small so neither the photo detection efficiency (see next section) nor dark count rate changes much for moderate temperature fluctuation.
Finally, the method used within this work to determine the breakdown voltage, introduces another systematic error not described in section 6.2.1. Not considered until now, was the variation of the threshold voltage of the CMOS logic, on which our definition of the breakdown voltage depends. It increases towards lower temperatures (see, for example, [190]), slightly changing the shape of the curve. However, typically, the temperature coefficient of threshold voltages are in the order of a few $1\,\mathrm{mV\,K^{-1}}$ [191]. So, at $T = 77\,\mathrm{K}$ the threshold voltage is about 200 mV higher than at room temperature, which is still a rather small effect.

6.3.2 Light Sensitivity

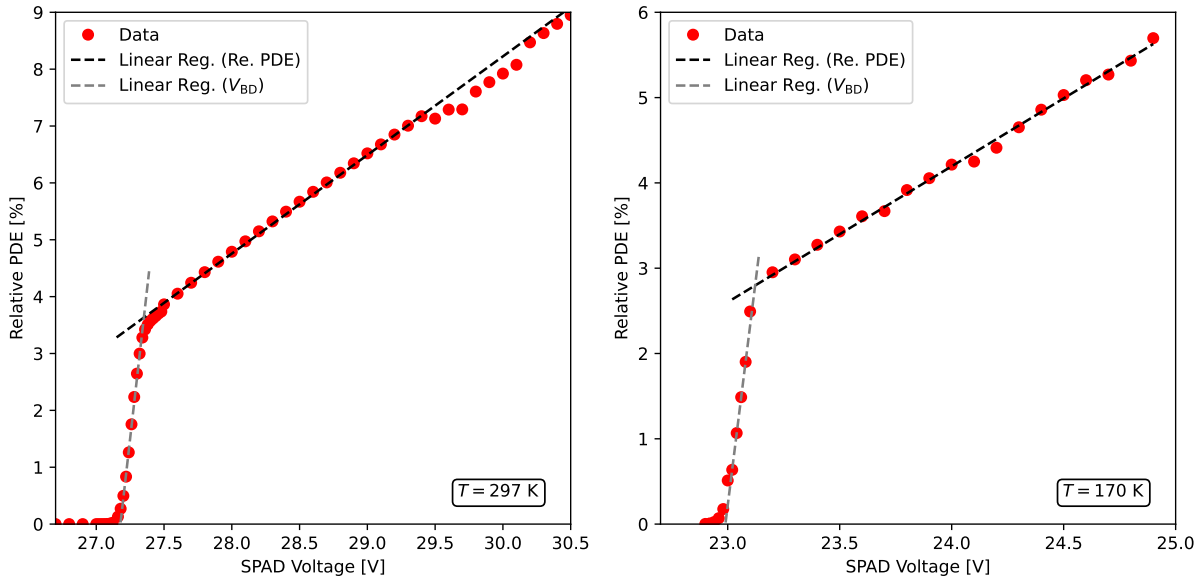

Figure 6.5: Relative PDE of the IDP2 at $T \approx 297\,\mathrm{K}$ (left) and $T \approx 170\,\mathrm{K}$ (right). When the bias voltage surpasses the breakdown voltage the PDE increase until all SPADs are active (gray line). Afterwards the rate settles and the further increase is due to the increasing avalanche trigger probability, which is found to be relatively linear. At $T \approx 297\,\mathrm{K}$ the relative PDE increases about 1.7%/V, while its about 1.6%/V at $T \approx 170\,\mathrm{K}$.

During the course of this work it was not possible to determine the absolute value of photon detection efficiency (PDE), since no calibrated reference detector to measure the absolute number of photons was available. However, tests of the light sensitivity at room temperature and low temperatures were preformed to ensure that photons are detected and whether the photon detection efficiency as function of excess bias changes with temperature.
For this, The IDP2 was uniformly illuminated with a laser diode of $\lambda = 642\,\mathrm{nm}$ wavelength. The diode was situated in the lab, at room temperature, and a light fiber was utilized to lead the light to the array at cold temperatures. The diode was switched on simultaneous to the start of a new frame (see section 5.1) and was switched off again after the accumulation time of the frame was over (see section 4.2.1). In total 20000 frames where recorded. The intensity of the

laser was adjusted to be low so that, in total, 800 to 1000 photon hits were recorded per SPAD at $V_{\mathrm{Ex}} = 1\,\mathrm{V}$. The integration time at $T = 170\,\mathrm{K}$ was 5 µs per frame. With these settings the probability of double photon hit in a SPAD is very low. Furthermore, dark counts plays a minor role in this measurement, since the rate is 0.06 Hz per SPAD at $T \approx 170\,\mathrm{K}$ (see next section) while the total measurement time is 100 ms. For $T = 297\,\mathrm{K}$ a integration time 2.5 µs, which was accidentally set, is longer than intended and, was noticed long after the measurement. However, the hot SPADs were excluded of the analysis and the dark count rate of the SPADs is 45 Hz at $V_{\mathrm{Ex}} = 1\,\mathrm{V}$ and increased to 75 Hz at $V_{\mathrm{Ex}} = 3\,\mathrm{V}$. The total integration time was 50 ms so about two to four dark counts are included in the recorded frames which is negligible.
The relative PDE is then determined by dividing the average number of photons detected, by the total number of the frames. The resulting relative PDE, as function of the SPAD voltage, can be seen in figure 6.5 at $T = 297\,\mathrm{K}$ (left) and $T = 170\,\mathrm{K}$ (right). Error bars are not included since the relative error of the single measurement is mostly in the order of 1%. The data points between $29.5\,\mathrm{V} > V > 29.5\,\mathrm{V}$ at $T = 297\,\mathrm{K}$ suffer from a systematic error of the laser or the measurement setup.
For both curves at lower voltages a rapid increase of the relative PDE can be observed, which corresponds to the breakdown process of the individual SPADs. One after the other, they are turned on and when all SPADs are biased above breakdown, the rate settles. The linear regression (gray curve) applied to the steep increases shows again how the breakdown voltage is determined (see section 6.2.1).
After the initial breakdown process is completed, a linear and moderate increase in the relative PDE can be observed. At $T = 297\,\mathrm{K}$ (left) a slope of $1.7\%/V$ is found, while above $V = 30.1\,\mathrm{V}$ the slope decreases. Overall the curve is in agreement with the expected behavior. The increase in PDE with the bias voltage is mostly given by the increasing avalanche trigger probability of the SPAD (see section 3.5). The trigger probability as a function of the bias voltage, can be approximated by a limited exponential growth [192], which increases strongly at lower bias voltages until it starts to converge to 100% at high bias voltages. Therefore, the PDE especially at low bias voltages can be described well with a linear regression.
It was also possible to compare the relative increase in PDE with SPADs of same manufacture and comparable size, of which the quantum efficiency is reported in [90]. At a wavelength of $\lambda = 642\,\mathrm{nm}$ and at $V_{\mathrm{Ex}} = 2\,\mathrm{V}$ a quantum efficiency of roughly 10% is found, which increases to 15% at $V_{\mathrm{Ex}} = 4\,\mathrm{V}$ and 20% at $V_{\mathrm{Ex}} = 6\,\mathrm{V}$. This corresponds to a linear increase in the quantum efficiency with a slope of 2.5%/V. With the IDP2 having a fill factor of roughly 55% the increase in the PDE (QE time fill factor, see section 3.5) is about 1.4%/V, which is in agreement with the observed value. However, to compare the measurements in more detail a PDE measurement has to be made. Furthermore, the excess bias voltage of the IDP2 and the reported SPADs are not directly comparable. Although their manufacture is same there is a difference in the breakdown voltage was found ($\Delta V = 2\,\mathrm{V}$), which is assumed to be mostly introduced by our method of its determination (see section 6.2.1). The IDP2 is therefore operated at a higher excess bias.
At $T = 170\,\mathrm{K}$ (right) also a linear behavior is observed, so the SPADs are actually sensitive to light at low temperatures, and a slope of $1.6\%/V$ was determined. This value is comparable to the one at room temperature, so the relative increase in PDE dose not significantly change between these temperature. However, the absolute PDE might have change. Unfortunately, the PDE as a function of the temperature is to the authors knowledge broadly unknown since only little quantification was reported until now. It seems to increase a little towards lower temperatures (see section 3.5) and from a simplified qualitative view on the physics this seems feasible. With decreasing temperatures the mobility of the carrier-changes increases and, also the mean-free length, so that they can gain more energy on comparable long paths. Consequently, impact ionization is more effective. Maybe measurement with blue light of $\lambda = 450\,\mathrm{nm}$ would

have been more preferable, since here the SPADs are most sensitive a change would have been more obvious [90]. Here, at $V_{\mathrm{Ex}} = 2\,\mathrm{V}$ a QE of 25% is found, which increases to 45% at $V_{\mathrm{Ex}} = 4\,\mathrm{V}$, ($\sim 10\%/\mathrm{V}$). This was however, beyond the scope of this work.
Nevertheless, the QE at blue light at room temperature is encouraging and show that Digital SiPMs are sensitive at low bias voltages, which keeps the dark count rate at moderate level. In principle, Digital SiPMs can be utilized in the DARWIN Experiment without optimization for VUV light. Instead a wavelength shifting window can be installed (see section 2.4.4), so that the Xenon scintillation light is shifted to $\lambda \approx 400\,\mathrm{nm}$. Here, a PDE of 25% can be reached, when the SPADs have a quantum efficiency of 35%, reached at a low excess bias, and a fill factor of 70%.

6.4 IDP2: Dark Count Rate

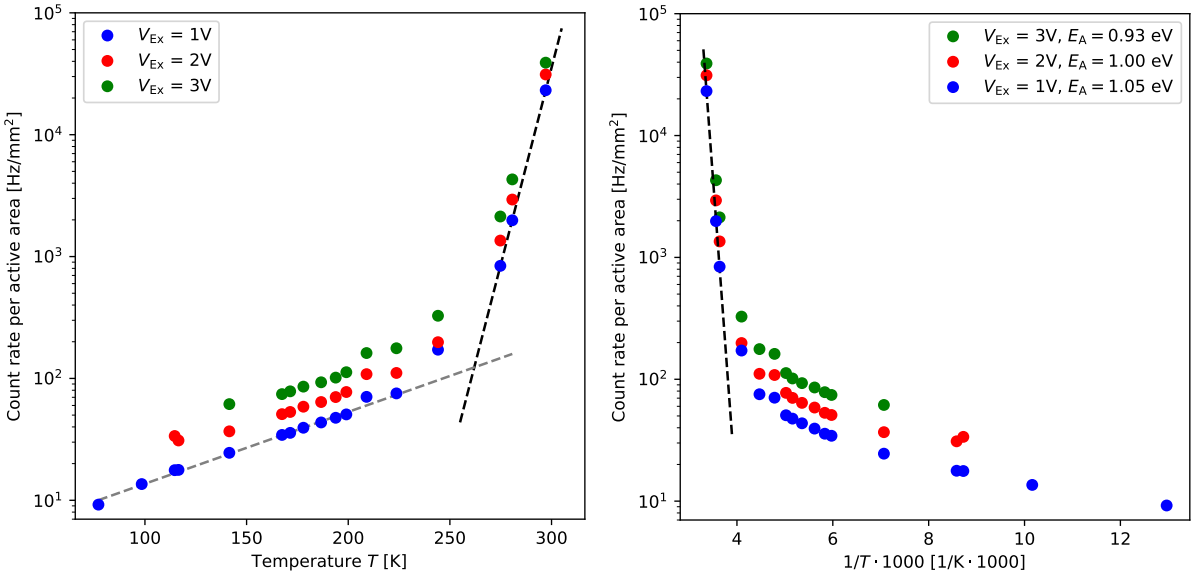

Figure 6.6: **Left:** Dark count rate at various temperatures and excess bias voltages. Two noise contributions can be discriminated decreasing both exponentially with temperature can be seen; Thermal generation at higher temperatures (black dashed line) and tunneling noise at lower temperatures (gray dashed line). The black and gray dashed lines correspond to a fit of exponential function to one of each part for the extrapolation of noise values. **Right:** Arrhenius plot of the dark count rate shown left. The activation energy is evaluated by using equation 6.1.

With the IDP2, the first dark count rate characterizations of Digital SiPMs at low temperatures, were carried out. The expectation was for two noise contribution dominating at different temperatures. These are thermal generation noise (see section 3.6.1) at high temperatures and tunneling noise (see section 3.6.3) at low temperatures. The aim was to observe what temperature profile the thermal generation rate follows, i.e. whether it is dominated by diffusion noise (see section 3.6.2) or generation via defect centers (SRH generation rate) (see section 3.6.1). Diffusive noise is more advantageous since it decreases more rapidly with temperature than SRH generation rate. At some low temperatures the thermal generation rate falls below the tunneling noise. Tunneling noise is only weakly dependent on temperature and represents a lower limit for the dark count rate. Since the SPADs of the IDP2 are not optimized for low temperature usage, tunneling noise was expected to be above the DARWIN limit of $0.01\,\mathrm{Hz\,mm^{-2}}$ (see section 2.4.3). On the left side of figure 6.6 the dark count rate of the IDP2 at various temperatures and at $V_{\mathrm{Ex}} = 1\,\mathrm{V}$ (blue), $V_{\mathrm{Ex}} = 2\,\mathrm{V}$ (red) and $V_{\mathrm{Ex}} = 3\,\mathrm{V}$ (green) is shown. As already described in

section 6.2.2, the hot SPADs are excluded from the noise analysis and the dark count rate is normalized to the active area of the SPADs. The dashed gray and black lines are exponential functions fitted to the data to extrapolation the dark count rate at temperatures beyond the measured ones. For the sake of clarity, these fits are only shown for the blue data point. The data points at low temperatures for the red and green curve are not shown because here it was not possible to apply voltages above $V_{\mathrm{Ex}} = 2\,\mathrm{V}$ or $V_{\mathrm{Ex}} = 2\,\mathrm{V}$ as they were above the dynamic voltage range. This effect will be discussed in detail in the next subsection. Again, errors are not shown because they are in the range of a few 1%.
The dark count rate comprises two exponential curves, which can be attributed to the dominance of thermal generation noise (black dashed curve) at high temperatures and tunneling noise (grey dashed curve) at low temperatures. Coming from room temperatures, the dark count rate decreases swiftly with about 1 order of magnitude per 20 K. Up to the temperature of $T = 250\,\mathrm{K}$, when tunneling becomes dominant, the dark count rate has decreased from an initial value of $23\,\mathrm{kHz\,mm^{-2}}$ at room temperature to $90\,\mathrm{Hz\,mm^{-2}}$.
On the right side of figure 6.6 the corresponding Arrhenius plot, which is used to determine whether the thermal generation noise is dominated by SRH generation noise or diffusive noise [193]. The Arrhenius equation is written as

$$R(T) = A \cdot \exp\left(-\frac{E_{\mathrm{A}}}{k_{\mathrm{B}}T}\right) \tag{6.1}$$

where, A is a temperature independent constant, E_{A} is the activation Energy and k_{B} the Boltzmann-Constant. While the SRH generation rate $R_{\mathrm{S}}(T) \propto n_{\mathrm{i}} \propto \exp(-E_{\mathrm{G}}/2k_{\mathrm{B}}T)$ (eq. 3.7), with $E_{\mathrm{G}} = 1.12\,\mathrm{eV}$ as band gap energy of silicon, the diffusive noise $R_{\mathrm{D}}(T) \propto n_{\mathrm{i}}^2 \propto \exp(-E_{\mathrm{G}}/k_{\mathrm{B}}T)$ (eq. 3.8). Consequently, fitting the noise with equation 6.1 yield $E_{\mathrm{A}} \approx 0.56\,\mathrm{eV}$ when SRH generation is dominant and $E_{\mathrm{A}} \approx 1.12\,\mathrm{eV}$ when diffusive noise is dominant.
The activation Energy at $V_{\mathrm{Ex}} = 1\,\mathrm{V}$ is determined to be $E_A = 1.05\,\mathrm{eV}$ ($\pm 5\%$), which is close to the band gap energy of $E_{\mathrm{G}} = 1.12\,\mathrm{eV}$. Clearly, the main source of noise for the average SPAD are charge-carriers entering the space charge region by diffusion. This corresponds to with the results found in [123], where it was shown that only hot SPADs follow the temperature dependency of the SRH generation rate. For higher excess bias voltages, the activation energy shrinks by a small fraction, so that it is at $V_{\mathrm{Ex}} = 3\,\mathrm{V}$ about 10% lower. This is quite a minor decrease but could be a hint for an increase in afterpulsing, of which the time constant extends towards lower temperatures and the probability increases for higher excess bias voltages.
Below $T = 250\,\mathrm{K}$ tunneling becomes the dominant source of noise, which is less dependent on temperature but still decreases exponentially with it. This decrease can, on the one hand, be attributed to the reduction of the electric field inside the SPAD as the breakdown voltage decreases with temperature. On the other hand, the band gap increases towards lower temperatures (see section 3.6.3). From $T = 200\,\mathrm{K}$ down to $T = 77\,\mathrm{K}$ the measured rate decreases by half an order of magnitude. For increased bias voltages the temperature exponent remains about the same, so that the temperature dependency of the tunneling rate at least does not change visibly.
Finally and most important for the DARWIN experiment, is the dark count rate at liquid Xenon temperatures of $T = 165\,\mathrm{K}$. At $V_{\mathrm{Ex}} = 1\,\mathrm{V}$ the dark count rate is about $35\,\mathrm{Hz\,mm^{-2}}$ and increases to $75\,\mathrm{Hz\,mm^{-2}}$ at $V_{\mathrm{Ex}} = 3\,\mathrm{V}$. Apparently, these values are three orders of magnitude above the constrained value of $0.01\,\mathrm{Hz\,mm^{-2}}$ (see section 2.4.3). However, this result is quite a promising start: To optimize the dark count rate at liquid Xenon temperatures only tunneling noise has to be lower, which is accomplished by lowering the SPAD peak electric field (see section 4.3.1). The diffusive noise contribution decreases very rapidly with temperature and will not influence the dark count rate at $T \approx 160\,\mathrm{K}$. The extrapolation of the noise curve shown on right in figure 6.6 evaluates to a diffusive rate of $5 \times 10^{-6}\,\mathrm{Hz\,mm^{-2}}$ at $T \approx 160\,\mathrm{K}$.

6.4.1 Excess Bias Dependency

With the dark count rate of the IDP2 measured as a function of the excess bias voltage (see section 6.1.1) one majors observation was made: As mentioned briefly in the previous section, the voltage range in which the SPADs can be operated, is reduced. A maximum bias voltage was found, above which the count rate increases rapidly and the SPADs become inoperable, which may reduces the achievable photon detection efficiency (PDE, see section 3.5) at lower temperatures. The second observation made was that tunneling noise increases approximately exponentially with the bias voltage.
In figure 6.7 the dark count rate as function of the excess bias voltages at $T = 77\,\mathrm{K}$ and $T = 167\,\mathrm{K}$ is shown. The black dashed lines are linear regressions of the logarithmic dark count rates between $0.2\,\mathrm{V} > V_{\mathrm{Ex}} > 1.8\,\mathrm{V}$ at $T = 77\,\mathrm{K}$ and between $0.2\,\mathrm{V} > V_{\mathrm{Ex}} > 3\,\mathrm{V}$ at $T = 167\,\mathrm{K}$. The steep increase of the dark count rate at excess bias voltages close to zero, corresponds to the turn-on process of the SPAD in the array, which are all active at a voltage of about $V_{\mathrm{Ex}} \approx 0.2\,\mathrm{V}$ (see section 6.2.1).

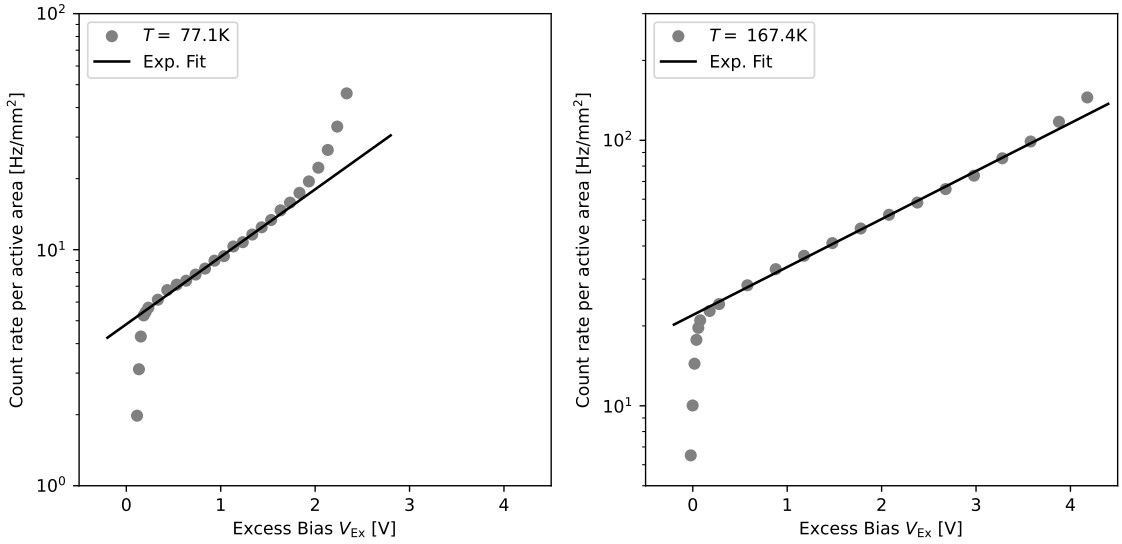

Figure 6.7: Dark count rate as function of the excess bias at $T = 77\,\mathrm{K}$ (left) and at $T = 167\,\mathrm{K}$ (right). The dashed lines are linear regression of the logarithmic data. At both temperatures the dark count rate depends exponentially on the excess bias. On the left side above $V_{\mathrm{Ex}} \approx 1.8\,\mathrm{V}$ the dark count rate deviates from the exponential behavior since the afterpulsing probability is strongly increased. At higher temperatures (right) the voltage range is larger and up to $V_{\mathrm{Ex}} \approx 3\,\mathrm{V}$ can be applied without a significant amount of afterpulses.

At $T = 77\,\mathrm{K}$, shown on the lower left, the count rate increases approximately exponentially with increasing excess bias voltages until $V_{\mathrm{Ex}} \approx 1.8\,\mathrm{V}$ where it starts to deviate from this initial behavior. The exponent is moderate, such that between $V_{\mathrm{Ex}} \approx 0.2\,\mathrm{V}$ and $V_{\mathrm{Ex}} \approx 1.8\,\mathrm{V}$ the dark count rate increases from $5\,\mathrm{Hz\,mm^{-2}}$ to $15\,\mathrm{Hz\,mm^{-2}}$ and thus triples. However, more qualitative statements on the shape of tunneling noise as a function of the voltage, are difficult. Tunneling depends on the present peak electric field (see section 3.6.3), which in turn is defined by the doping profile of the SPAD and modulated by the excess bias (see section 3.4).
Above $V_{\mathrm{Ex}} \approx 1.8\,\mathrm{V}$ the dark count rate increases rapidly and, at $V_{\mathrm{Ex}} \approx 2.2\,\mathrm{V}$ the array becomes inoperable. Inoperable means that the current consumption of the SPADs increases rapidly to some $1\,\mathrm{mA}$, which is normally barely measurable, and the recorded frame are partly incomplete.

The bias voltage has to be lowered below breakdown and the enable bits of the SPADs have to be reprogrammed to be operable again. This behavior is also reported for SiPM arrays operated at low temperature [72]. A divergence of afterpulsing (see section 3.7.1) is assumed to cause the rapid rate increase. This means, the afterpulsing probability is so high that the subsequent afterpulses of a primary event, again cause afterpulsing. Afterpulsing depends on the applied excess bias voltage as, with it, the number of charge carriers traversing the depletion region during an avalanche, increases (see section 3.7.1). So, it increases with the bias voltage until it diverges. In [72] it was also proven that, by decreasing afterpulsing, the SiPMs are operable at higher excess bias voltages.
Towards higher temperatures the time constant of the released charge carriers decreases so that more of them leave the depletion region of the SPAD when it is still recharging. Thus those carriers have a lower chance to trigger the SPAD again (see section 3.7.1), the afterpulsing probability lowers and the maximal applicable excess bias voltage increases. This can be seen on the right side of figure 6.7, where the dark count rate as function excess bias voltages at $T = 167\,\mathrm{K}$ is shown. Voltages of $V_{\mathrm{Ex}} > 3\,\mathrm{V}$ can be applied and only above $V_{\mathrm{Ex}} = 4\,\mathrm{V}$ does the dark count rate start to deviate from the exponential behavior. Towards higher bias voltages the array again becomes inoperable. In principle, at $V_{\mathrm{Ex}} \approx 3\,\mathrm{V}$ a sufficient PDE can be reached (see section before). On the other hand the voltage range can be increased by utilizing a more sophisticated SPAD front end with which afterpulsing can be suppressed (see section 3.7.1) and higher bias voltages can be reached. However, such a circuitry consumes more space and decreases the fill factor.
Finally, the exponent extracted with the linear regression of the logarithmic data is a little lower than at $T = 77\,\mathrm{K}$. The dark count rate doubles between $V_{\mathrm{Ex}} \approx 0.2\,\mathrm{V}$ ($23\,\mathrm{Hz\,mm^{-2}}$) and $V_{\mathrm{Ex}} \approx 1.8\,\mathrm{V}$ ($47\,\mathrm{Hz\,mm^{-2}}$). The change of the exponent is assumed to be caused by two reasons: Liquid nitrogen and liquid xenon temperatures are roughly 90 K apart, in between this range on one side the band gap increases and on the other side the breakdown voltage decreases (see section 3.4), lowering the field, so that the exponent changes (see section 3.6.3).

6.5 IDP2: Hot SPADs

Hot SPADs are SPADs having a significant higher dark count rate than the average SPAD. Switching them off is essential not only to operate the array at its genuine noise level but also to lower the crosstalk-induced signals in the neighboring SPADs, which actually decreases the usable active area and thus the fill factor (see section 3.5). However, it has been observed that, at lower temperatures, hot SPADs literally freeze out and become average SPADs. A beneficial behavior for the DARWIN experiment, as at $T \approx 160\,\mathrm{K}$ fewer hot SPADs have to be switched off and the fill factor is effectively higher compared to room temperature.
Being "hot" is caused by defects or impurities inside the depletion region causing a high SRH generation rate (see section 3.6.6). As for the average SPADs their dark count rate decreases with temperature and, at a certain point, SRH noise falls below the tunneling noise level, making them indistinguishable from the average SPADs and therefore also usable for photo detection. On the left side of figure 6.8 this behavior is illustrated by means of the dark count rate as function of temperatures of two hot SPADs (yellow and red dots). In addition, the dark count rate of one average SPAD (green dots) and one hot SPAD, which does not freeze out is shown (blue dots). The latter is assumed to suffer from structural damage, which may causes an significantly increased peak field so that tunneling is strongly enhanced. However, the fraction of these defective SPADs is very low so that after the freeze out only a small residual fraction is left. The average SPADs, as already discussed in the previous section, are dominated by diffusive noise at higher temperatures, which is $R(T) \propto n_{\mathrm{i}}^2$. For these tunneling noise becomes dominant

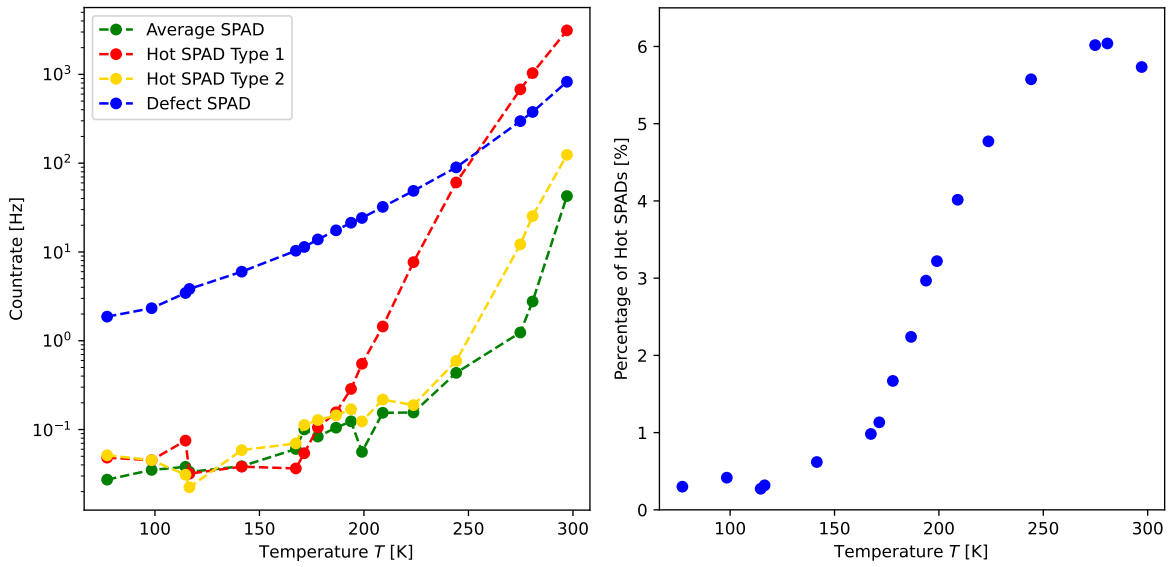

Figure 6.8: **Left:** Temperature dependent dark count rate of three hot SPADs (red, yellow, blue) and one average SPAD (green). The freeze out temperature of the red curve is lower than the one of the yellow curve, which is due to the higher amplitude. The hot SPAD, in blue, will not freeze out as it has some structural damage. **Right:** Temperature dependent fraction of hot SPADs. The initial value of 6% starts to decrease at $T = 250\,\mathrm{K}$ until at $T = 150\,\mathrm{K}$ only a residual fraction remains.

for $T < 250\,\mathrm{K}$.
The dark count rate of the hot SPAD shown in red, is about three orders of magnitude higher than that of the average SPAD. In addition, the SRH generation rate depends less on temperature ($R(T) \propto n_\mathrm{i}$, see previous section). The combination of both leads to the hot SPAD freezing out at $T \approx 180\,\mathrm{K}$. Moreover, hot SPADs with lower noise can be found, like, for example, the one shown in yellow. Its dark count rate is only slightly above the average one, and its SRH generation rate is not yet fully dominated. Hence, the temperature dependency is somehow between that of SRH and diffusive noise. Both effects lead to a freeze out at $T \approx 240\,\mathrm{K}$. Consequently, the freeze out temperature, is on the one hand a product of the weaker temperature dependency of the SRH noise, but on the other hand it very much depends on the initial magnitude of the dark count rate at room temperature. Moreover, with decreasing tunneling noise the freeze out process should in turn be shifted towards lower temperatures.
The fraction of hot SPADs as function of temperatures is shown on the right side of figure 6.8. The number of hot SPADs was determined according to the method described in section 6.2.2. It decreases uniformly which means that the dark count rate of the hot SPADs is quite broadly and uniformly distributed, which is also shown later in this section (see right side of figure 6.9). At room temperature and down to $T = 250\,\mathrm{K}$ about 6% of the total number of SPADs are "hot". Since the number of hot SPADs is low and the IDP2 has a relatively high pixel density with reasonably small SPADs, it is assumed that a low density of single point-like defects, equally distributed over the silicon dye, cause hot SPADs.
Below $T = 250\,\mathrm{K}$ the freeze out process starts, where hot SPADs with low noise freeze out first (yellow points on the left side of figure 6.8). One after the other they freeze out until $T \approx 170\,\mathrm{K}$ turn to an average SPADs and the curve starts to converge towards a very low residual value ($< 1\%$), consisting mainly of hot SPADs, which have suffer from a structural defect (blue curve on the left side of figure 6.8).

The temperature profile of the Hot SPADs dark count rate and their dark count rate distribution were also investigated in more detail. The temperature dependency is observed with an extraction of the activation energy (see section before) per SPAD [123]. The resulting histogram of the activation energies is shown on the left side of figure 6.9. On the right sideof figure 6.9 a scatter plot is shown, where their activation energy is plotted against the dark count rate of all SPADs at room temperature. In both plots it is highlighted at which activation energies, the hot SPADs can be found. Not highlighted is the kind of hot SPAD shown in blue on the left side of figure 6.8. Their noise level can have any value above the average one, which is not further shown here but results in activation energies spreading over the whole observed range. Furthermore, the activation energy from SPADs suffering from crosstalk induced by the hot SPADs (see section 6.2.2), are also marked.

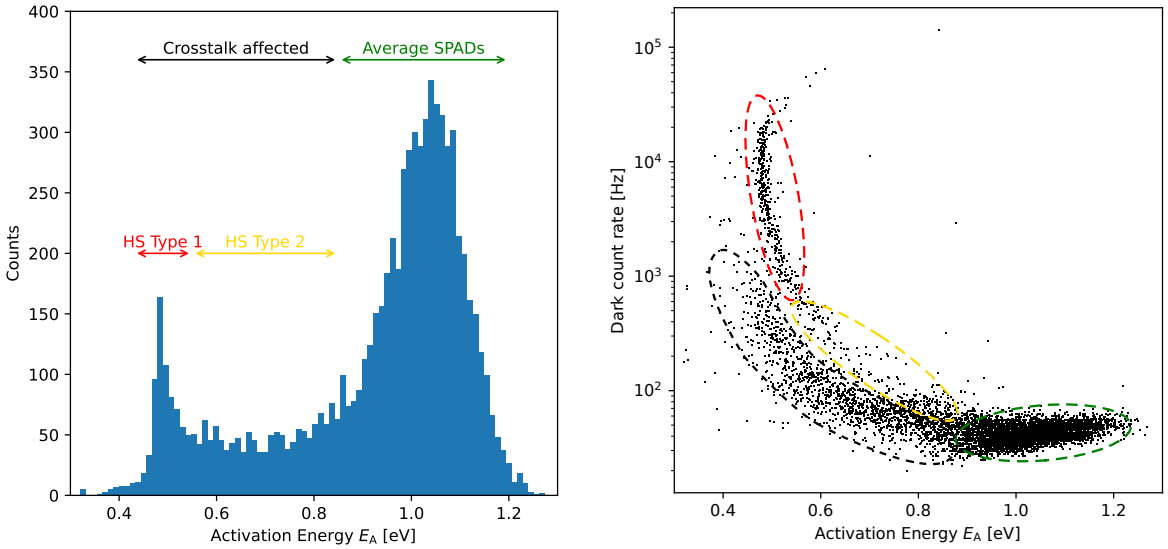

Figure 6.9: **Left:** Histogram of the SPADs individual activation energy. Energy ranges in which the hot SPADs shown in figure 6.8 are marked with equivalent color. Further the activation energy of the crosstalk affected SPADs is shown. **Right:** Scatter plot of the activation energy of the SPADs and their corresponding dark count rate at room temperature and $V_{Ex} = 1.0\,V$. The groups of SPADs marked in the histogram on the left side are also highlighted with corresponding colors.

In the activation energy histogram, on the left side of figure 6.9, two distinct peaks and a broad underground in between are visible. The larger of both peaks is centered at an activation energy of E_A =1.05 eV, which is very close to the band gap energy of $E_G = 1.12\,eV$. This activation energy corresponds to the diffusive noise of the average SPADs, which are visible as a dark area in the lower right in the scatter plot.
The broad underground in between the two peaks is partly caused by the hot SPADs with the lower noise amplitude (yellow curve in figure 6.8) and the crosstalk-affected SPADs. When the SRH generation rate is not fully dominant the activation energy is in between that of the average and hot SPADs. Their dark count rate is marked with the yellow frame on the right side of figure 6.9. The second lower peak is centered around E_A =0.44 eV, which is close to $E_G/2 = 0.56\,eV$. These are the SPADs for which SRH generation noise at higher temperature is dominant. In the scatter plot on the right side of figure 6.9, they are marked with a frame in red. With their dark count rate significantly higher than the average SPADs, they are clearly the hot SPADs. Their dark count rate is uniformly distributed over about two orders of magnitude and

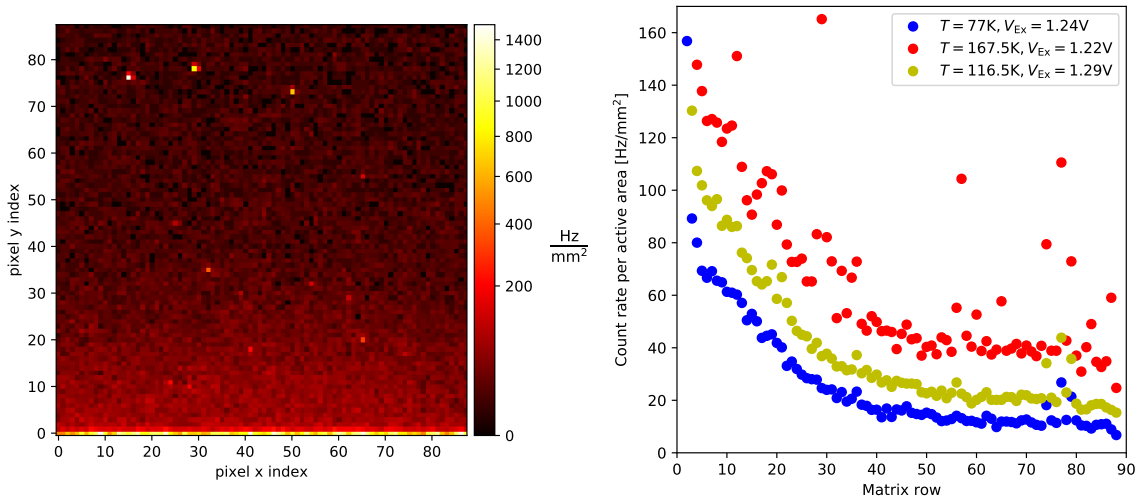

Figure 6.10: **Left:** Dark count rate intensity map at $T = 77\,\mathrm{K}$ and $V_{\mathrm{Ex}} = 1.0\,\mathrm{V}$. Pixels in the lower part of the matrix have an increased dark count rate caused by photon emitted by circuitry situated at the bottom of the matrix. **Right:** Mean dark count rate per row (including hot SPADs) at different temperatures but same excess bias voltage. Photon emission does not depend on temperature as the shape of the curves are the same.

reaches a maximum value of about $1 \times 10^4\,\mathrm{Hz}$. This distribution causes the uniform decrease of their number with temperature. How it exactly forms is, however, beyond of the scope of this work.
Finally, the SPADs affected by crosstalk possess activation energies in the whole region below 0.8 eV. On the right side of the figure 6.9, they are marked with a black frame. A large fraction actually show the same activation as the hot SPADs but have a significantly lower rate. Crosstalk has become the dominant noise source and, as the dark count rate of the hot SPADs follows the SRH temperature dependency, the crosstalk-affected SPADs mimic this behavior. For SPADs situated further away or in the vicinity of less noisy SPADs posses an activation energy somewhat below 0.8 eV. The crosstalk effect is quite far reaching and significant as it affects about 10% of all SPADs, making it inevitable that the hot SPADs are switched off.

6.6 Photon Emission of the Readout Electronics

During the operation of the IDP2 at lower temperatures of $T < 200\,\mathrm{K}$, it was observed that photons emitted by the readout electronics increase the dark count rate of a part of the pixel matrix. On the left side of figure 6.10 an intensity plot of the dark count rate pixel matrix at liquid nitrogen temperatures of $T = 77\,\mathrm{K}$ is shown. Towards the bottom half of the matrix, the count rate increases rapidly and is highest in the bottom row, below which the readout logic is situated. The circuitry causing the emission, is the wired-OR receiver for the multiplicity logic (see section 4.2). It is an analog circuit which draws a constant current and cannot be switched off completely. The current, however, was, for all measurements set to the possible minimum via the slow control.
On the right side of figure 6.10 the mean dark count rate (including the hot SPADs) of the rows is shown at different temperatures. The increase in count rate is visible up to half of the matrix, which corresponds to an absorption length of the photons of about $\mathcal{O}(1\,\mathrm{mm})$. Subsequently, a large portion of the emitted photons possess an infrared wavelength, which penetrates far into the

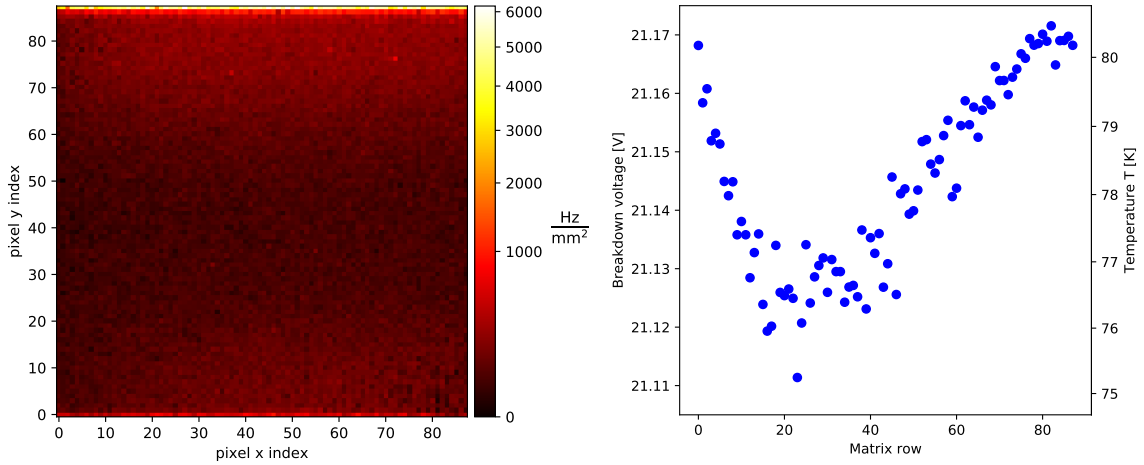

Figure 6.11: **Left:** Dark count rate intensity map at $T = 77\,\mathrm{K}$ and $V_{\mathrm{Ex}} = 1.0\,\mathrm{V}$. Photon emission background was induced by clocking the shift register at the top of the matrix during data accumulation. **Right:** Mean breakdown voltage per row, which can be used to evaluate the local temperature on the array.

silicon and is in agreement with the description in section 3.7.3. However, the emission intensity and spectrum, at least in the observed range, are not affected by increasing temperatures. The shape of all three noise curves, measured at different temperatures but with same excess bias. Only an offset separates the individual curves, which is due to the increase in dark count rate towards higher temperatures.

It was also possible to induce photon emission by utilizing the shift register above the top-most row, which is used to shift in the enable bits of the individual SPADs (see section 4.2.2). During data accumulation it is normally idle but in this case it was clocked at a frequency of 50 MHz. On the left side of figure 6.11 the resulting intensity map is visible. Photon emission now disturbs also the upper part of the matrix. Consequently, only current drawing circuits actually emit photons. To omit this effect at low temperatures, it is essential to keep the activity of the surrounding logic very low or somehow physically isolated from the SPADs. To further quantify the magnitude of the photon emission, a power dependent measurement has to be taken. This was, however, beyond the scope of this work.

Finally, as a byproduct of this investigation, a simple method for determining the local temperature on the array, was developed. The breakdown voltage, which was measured, and is known for the whole temperature range (see section 6.3), can be used to determine the temperature present in a single row or even down to the pixel level. Initially, this method was used to rule out excessive heat dissipation as the cause of the dark count rate increase. Obviously, the observed sharp increase in the dark count rate requires a rather drastic increase in temperatures of $\sim$100 K, which, in turn, increases the breakdown voltage to a level well above the applied bias voltage.

On the right side of figure 6.11 the result of temperature evaluation whilst the shift register was clocked, is shown. At a lower temperature the breakdown voltage has a temperature coefficient of about $\sim 25\,\mathrm{mV\,K^{-1}}$ (see section 6.3), which is sufficient to determine the local temperature with an accuracy of $\Delta T = 1\,\mathrm{K}$. So the difference of the temperature towards the upper and lower margin of the matrix, which is about $\Delta T \approx 5\,\mathrm{K}$, can be resolved.

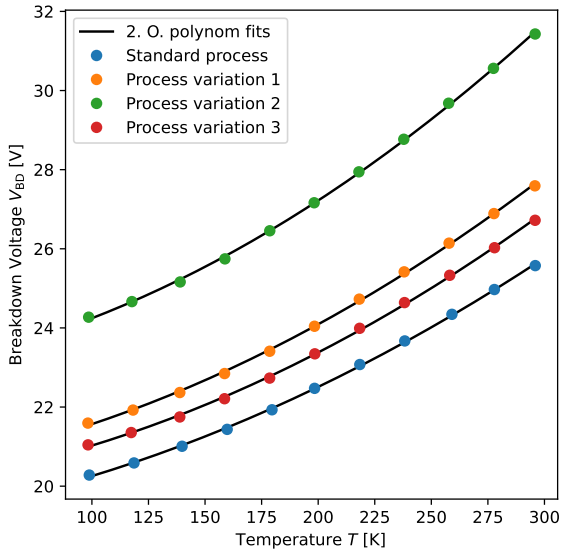

Figure 6.12: Breakdown voltage as a function of the temperature for the arrays made in the standard process as well as in the three process variations, which have lower electric peak fields (see section 4.3.1). Process variation 2 has the lowest peak field, followed by 1, 3 and, lastly, the standard process. The breakdown voltage increases, the lower the peak field inside the SPAD is (see section 3.4). Black lines are second order polynomial fits for calibration purpose and to determine the temperature coefficients.

6.7 DARWIN Test Arrays: Breakdown Voltage

As for the IDP2, the first thing to measure with the DARWIN test array is the break voltage as a function of the temperatures to reach a comparable operation point of the array, since it decreases with temperature. In figure 6.12 the breakdown voltage for the arrays made in the standard process as well as in the three process variations (see section 4.3.1), is shown. The temperature profile of all breakdown voltage curves is linear at high temperatures but flattens towards lower temperatures, which is also in agreement with the curve observed for the IDP2 (see section 6.3). The black curves are second order polynome fits, that have no physical meaning. They are fitted for calibration purpose and to extract the temperature coefficients. At first, between the SPADs no significant difference in the breakdown voltage was found, so its average value was taken. Then, Each data point is the average value of the two measured arrays of the same manufacture (see section 6.1.2). The difference between the breakdown voltages of the two arrays is around 50 mV. Consequently, the variations of the breakdown voltage introduced during manufacture, is low and multiple arrays can be biased by a common SPAD bias line without causing large fluctuations in the operation point (see example found in [103]). This is especially important when a large detection plane of the DARWIN cryostat has to be covered with digital SiPMs, with a low number of cables (see section 2.4.3).
The breakdown voltage of the standard process is about $V_{\mathrm{BD}} = 25.6\,\mathrm{V}$ at room temperature and decreases by about 5.3 V to a value of $V_{\mathrm{BD}} = 22.3\,\mathrm{V}$ at 100 K. The temperature coefficients, which are important for the stability of the operation point against temperature fluctuations (see section 6.3), at $T = 296\,\mathrm{K}$ is $37\,\mathrm{mV\,K^{-1}}$ and at $T = 160\,\mathrm{K}$ it is $23\,\mathrm{mV\,K^{-1}}$, which is quite low.
The absolute value of the breakdown voltage at room temperature for a standard process array is about 1.5 V lower than that of the IDP2 (see section 6.3), which is made in the same process. The difference is most likely due to the IDP2 AC coupling of the SPAD (see section 6.2.1). The temperature profile, the absolute decrease between $100\,\mathrm{K} < T < 296\,\mathrm{K}$ and the temperature coefficients, are on the other hand, in line with the value found for the IDP2. Consequently, it is assumed that the IDP2 is actually operated at higher excess bias voltages. In future experiments the breakdown voltage determination has to be updated to a standard method such as measuring the I-V curve (see section 6.2.1) to avoid these errors and have a comparable value to arrays found in literature.

Within the process variations in the manufacture of the arrays, the electric peak field inside the depletion region was reduced to lower tunneling noise . Process variation 2 has by far the lowest peak field, followed by 1, and, lastly 3, but the absolute value is unknown (see section 4.3.1). With decreasing field peak, which is accompanied with a increase in the width of the depletion region, the breakdown voltage increases (see section 3.4). So, the respective breakdown voltage of process variations 1 and 3 are, at room temperature, by about 1 V and 2 V higher than the standard process. Yet they still have roughly the same absolute variation in the temperature range of $100\,\mathrm{K} < T < 296\,\mathrm{K}$ and the temperature coefficient are also roughly the same as for the standard process.
Process variation 2 on the other hand, which has the large reduction in the peak field, has the highest breakdown voltage. Its absolute decrease, which is 7.2 V, in the temperature range of $100\,\mathrm{K} < T < 296\,\mathrm{K}$ is higher. The temperature coefficients are also increased but the difference is quit minor. At $T = 296\,\mathrm{K}$ a value of $51\,\mathrm{mV\,K^{-1}}$ is found, which decreases to $31\,\mathrm{mV\,K^{-1}}$ at $T = 160\,\mathrm{K}$. Its natural that for a SPADs with reduced peak field the temperature coefficients are higher, which can be understand as follows: With the reduction of peak field the depletion region of the SPAD is widened (see section 3.4). For decreasing temperatures the mean free path of the charge-carriers increases and a lower field is required to reach the breakdown condition. For a wider depletion region the field depends less on the applied voltage compered to thin one and so the break voltage change is larger.

6.8 DARWIN Test Arrays: Dark Count Rate

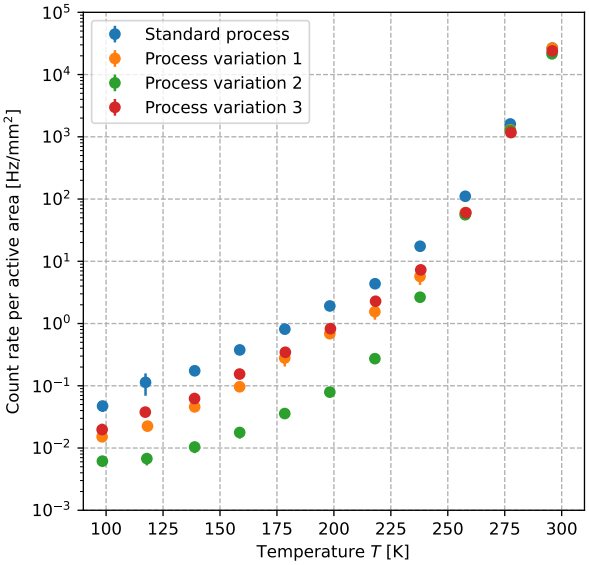

Figure 6.13: Dark count rate temperature profile of the DARWIN Test array fabricated in the standard process and those three process variations. The rate is normalized to the active area of the SPADs and the excess bias voltage is kept constant at $V_{\mathrm{Ex}} = 1\,\mathrm{V}$. Although, all process variations show a reduced tunneling noise contribution, it is lowest for process variation 2, since it has the lowest peak in electric field.

One of the most important goals within the submission of the DARWIN Test array was to reduce the dark count rate at liquid xenon temperatures ($T \approx 160\,\mathrm{K}$). At this temperature tunneling noise is dominant (see section 6.4), which strongly depends on the electric peak field in the SPAD. To reduce it an optimization campaign was started by our manufacturer, in which three arrays with, a different reductions of the peak field were created and called process variation 1,2 and 3 (see section 4.3.1). Process variation 2 has, by far, the lowest peak field, followed by 1 and lastly 3. In figure 6.13 the dark count rate normalized to active area for arrays made with these process variation and the one made in the standard process as a function of the temperature at $V_{\mathrm{Ex}} = 1\,\mathrm{V}$, can be seen. (Excess bias choice see section 6.1.1.) Each data point is the average value of the dark count rate found for the 10 different SPADs of the macro pixels. Although

they differ in size and shape, their count rate normalized to the active area is very comparable, which will be discussed in the next section. The errors, which is the standard deviation of the mean values, are barely visible in the log scale. Furthermore, the dark count rate shown here is from the second round of characterized arrays. However, the first run showed very comparable results, but the values scattered more throughout the temperature range as the measurement procedure was still in optimization.
As observed for the IDP2 (see section 6.4) the dark count rate as a function of temperature comprises two noise contributions scaling exponentially with the temperature: At higher temperatures thermal generation noise is dominant, which causes the initial steep decrease. At the lower temperature, below $T \approx 240\,\mathrm{K}$, tunneling noise becomes dominant, which depends less on temperature. Here also the effects of the process variations become visible.
At liquid Xenon temperatures of $T \approx 160\,\mathrm{K}$, process variation 1 and 3 show a dark count rate reduction about a factor of two and four, respectively, compared to the standard process. A rate of $0.4\,\mathrm{Hz\,mm^{-2}}$ ($\pm 10\%$) was found for the standard process and $0.2\,\mathrm{Hz\,mm^{-2}}$ ($\pm 10\%$) and $0.1\,\mathrm{Hz\,mm^{-2}}$ ($\pm 15\%$) for the process variations 1 and 3, respectively. However, the most significant reduction is achieved with process variation 2, which was expected as it also has the lowest peak field. The dark count rate is more than an order of magnitude lower than that of the standard process. At $T \approx 160\,\mathrm{K}$, a rate of $0.02\,\mathrm{Hz\,mm^{-2}}$ ($\pm 20\%$) was found, which is in the same order of magnitude as the constrained $0.01\,\mathrm{Hz\,mm^{-2}}$ of the DARWIN experiment (see section 2.4.3). So, already in this first optimization attempt it was possible to massively reduce the tunneling noise contribution for Digital SiPMs. In the next step, it is necessary so measure the PDE of those SPADs in the visible range of light as well as then they are optimized for VUV light to investigate if there are any changes introduced by the process variation. Furthermore, it has to be evaluated if the noise is already low enough for DARWIN experiment and which PDE is, in the end, required. Eventually, the excess bias has to be increased to gain a larger PDE, so that the noise also increases. However, the latter increases relatively moderate with the excess bias, which can be seen in the next section. Also, a second round of optimizations should in principle be possible, where the tunneling is decreases only about a small portion, which was, for example, reached with process variations 1 and 3.
When approaching lower temperatures, the dark count rate of all arrays of different processing decreases further. In general, tunneling reduces, for all arrays, by about one order of magnitude per 60 K. Process variation 2 deviates from this behavior below $T \approx 140\,\mathrm{K}$. However, statistics, even with measurement times of 3 h, were very poor, so that a further decrease may not be resolvable. At the lowest temperatures measurable with the current setup $T \approx 100\,\mathrm{K}$ a dark count rate of well below $0.01\,\mathrm{Hz\,mm^{-2}}$ is found, which makes digital SiPMs also very attractive for liquid argon-based rare event search experiments [73], which have a temperature of $T \approx 87\,\mathrm{K}$ inside the cryostat.

At higher temperatures, where thermal generation dominates, the dark count rate of all the arrays made with process variations as well as the standard process, is comparable. On the left side of figure 6.14 the Arrhenius plot (see section 6.4) is shown for the process variation 2. The Arrhenius equation (see eq. 6.1) was fitted to the data (black dashed line) with which an activation Energy of $E_\mathrm{A} = 1.02\,\mathrm{eV}$ ($\pm 5\%$) was determined. So the dark count rate of the average SPADs at high temperatures, is dominated by diffusive noise. At room temperatures an average value of about $25\,\mathrm{kHz\,mm^{-2}}$ is measured. The rate then decreases to $60\,\mathrm{Hz\,mm^{-2}}$ at $T = 260\,\mathrm{K}$, which corresponds roughly to a decrease of about one order of magnitude per 20 K.
Finally, the dark count rate as a function of temperature of a standard process array, can be compared to that of the IDP2 (see section 6.4). Their manufacture is the same but it has to be noted that the determined breakdown voltage for the IDP2 is due to its AC Coupled SPADs about 1.5 V higher than for the DARWIN test array (see previous section). It is assumed that

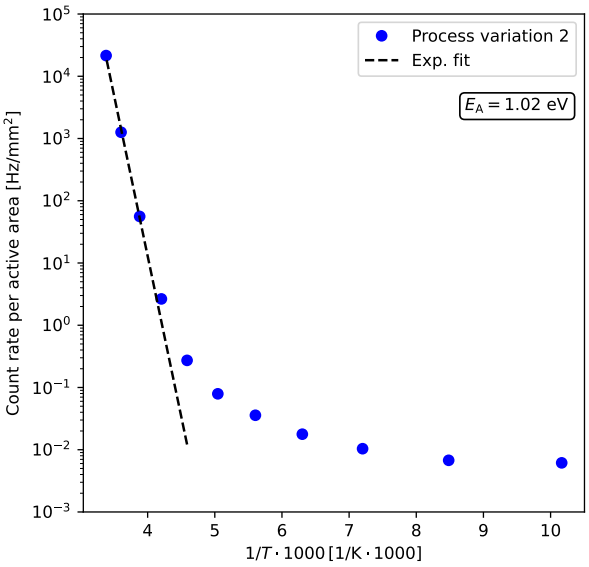

Figure 6.14: Arrhenius plot of the dark count rate of an array made in process variation 2 at $V_{Ex} = 1\,V$, with a fit of the Arrhenius equation (eq. 6.1) shown as black dashed line. An activation energy of $E_A = 1.02\,eV$ ($\pm 5\%$) was found, indicating that diffusive noise is the dominant noise source at higher temperatures.

the actual breakdown voltage is equal and consequently the IDP2 is operated with a 1.5 V higher excess bias.

For the IDP2 and the DARWIN Test array, at higher temperatures diffusive noise dominates (see section 6.4), so the temperature dependency of the noise is comparable. At room temperatures the dark count rate of both is comparable ($\sim 20\,kHz\,mm^{-2}$), although their effective excess bias voltage is different. This can, on the one hand, be explained by the relatively weak dependency of diffusive noise rate on the excess bias (see figure 6.16), which increases mostly due to the increase in the avalanche trigger probability (see section 3.6.2). Furthermore, diffusive noise very much depends on the quality of manufacture of the SPADs [116]. For example, just a few more defects in the interface of the silicon dioxide layer on top of the SPAD (see section 3.5) can increase the dark count rate. These defects act as generation centers for electron hole pairs (see section 3.6.1), which then defuse into the depletion region. Since, the manufacturing of both arrays is 4 years apart, small variations in manufacture cannot be excluded.

At low temperatures the DARWIN Test arrays made in the standard process show a lower tunneling noise than the IDP2. At $T \approx 160\,K$ and at $V_{Ex} = 1\,V$ a dark count rate of the IDP2 was measured to be $35\,Hz\,mm^{-2}$, while for the standard process of the DARWIN Test array its is only $0.4\,Hz\,mm^{-2}$. The difference is at least partly caused by the unequal excess bias voltage. However, for the DARWIN array the maximal applicable bias voltage is 1.7 V (see next section), so a value can only be extrapolated. For the IDP2, a value of $11\,Hz\,mm^{-2}$ is extrapolated at 1.5 V less excess bias voltage (see section 6.4.1). However, tunneling is a quite complex function of the applied voltage (see section 3.6.3) and the tunneling level might be even lower at this voltage.

Furthermore, the IDP2 was manufactured 4 years prior to the DARWIN Test array. The manufacture optimizes Digital SiPMs mainly for room temperature operation where tunneling is negligible. So, over the years some parameters eventually changed or fluctuated in processing, which reduced tunneling noise by accident. Finally, there might be a higher amount of afterpulses for the IDP2. However, the effect of afterpulsing on frame wise readout architecture of the IDP2 is not entirely clear. In between the frames there is a dead time of about 50 µs (see section 5.1) and the accumulation time, in which only a single dark count can be detected, is about 1 ms at liquid Xenon temperatures (see section 6.1.2).

6.9 Effect of SPAD size and shape

The macro pixel test structure comprises 10 SPADs with different active areas and aspect ratios (see section 4.3.2). With these, the dark count rate as a function of size and shape, can be investigated. Particularly the large SPADs are of special interest for the DARWIN experiment as they offer a high fill factor of $> 80\%$. However, at the beginning of this work it was not clear whether the dark count rate is proportional to the area, so that several small SPADs can be replaced with one large one, or if another unknown effect inflates their rate. Furthermore, for large SPADs also the number of hot SPADs increases (see section 4.3.2). Hot SPADs need to be switched off to operate the array at its genuine noise performance. This, in return, decreases the active area and thus, effectively, the fill factor, making smaller sizes preferable. An, optimal SPAD size exists, for which the fill factor is highest after switching all hot SPADs off. In addition, the number of hot SPADs decreases towards low temperatures (see section 6.5), which increases the optimal SPAD size.
In this section, first the dark count rate is investigated as a function of the SPAD size and shape. Then the number of hot SPADs is evaluated also as a function of the SPAD size and temperature and a model present, with which the optimal SPAD size at various temperatures, can be evaluated. All demonstrated by an array made with the process variations 2, since all others, if not otherwise stated, behave very similarly.

6.9.1 Dark count rate

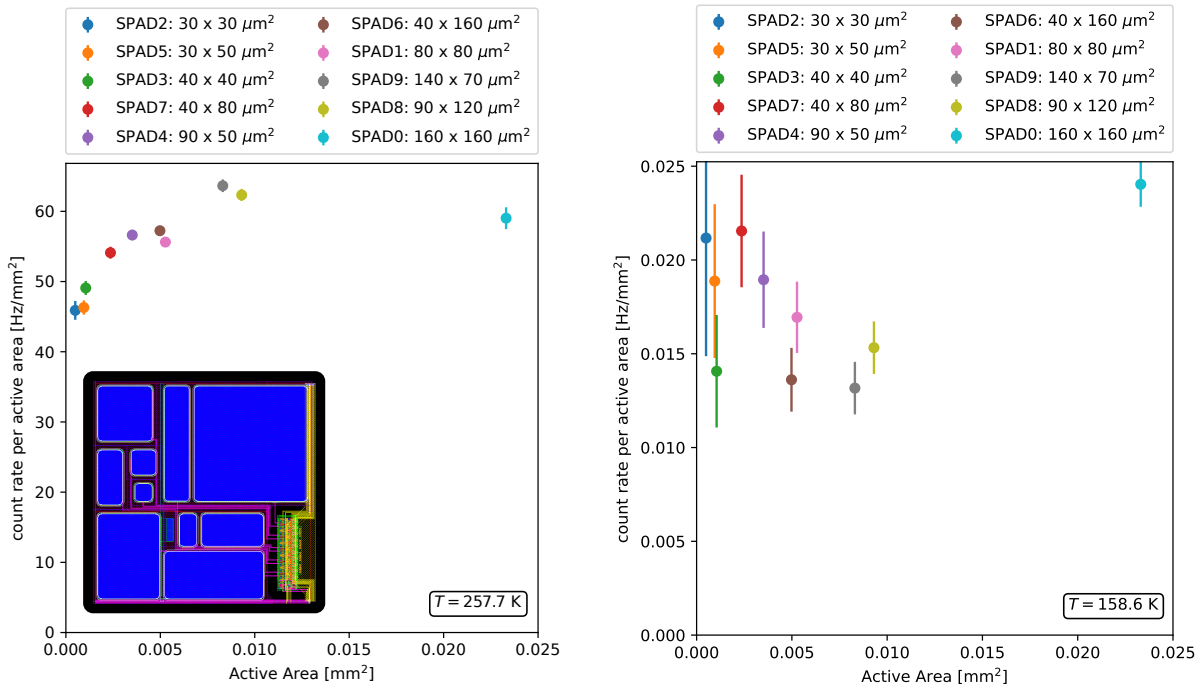

Figure 6.15: Dark count rate normalized to the active area of the ten SPADs of different shape and size, as function of the active area at $V_{\mathrm{Ex}} = 1\,\mathrm{V}$. On the left side at temperatures $T \approx 260\,\mathrm{K}$, where thermal generation is dominant, and on the right side at $T \approx 160\,\mathrm{K}$ where tunneling noise is the dominant. A picture of the macro pixel is included to visualize the relative SPAD size. At higher temperatures, the dark count rate scales with size. At lower temperatures no such behavior is observed, but it might be masked due to the error.

In figure 6.15 the dark count rate, normalized to the active area, is plotted against the active area of the SPADs at $V_{\mathrm{Ex}} = 1\,\mathrm{V}$ for $T \approx 260\,\mathrm{K}$ (left) and $T \approx 160\,\mathrm{K}$ (right). The plotted errors correspond to the standard error of the mean (the standard deviation divided by the square root of the number of good SPADs). For this discussion it is necessary how accurate the mean is. The standard deviation on the other side highlights the dispersion of noise of the SPADs.
At first, the variation of the corner radius (see section 4.3.2) of the SPAD had no observable influence on their dark count rate, so that the standard corner radius of 5 µm can continue to be used.
At higher temperatures of $T \approx 260\,\mathrm{K}$, shown on the left side of figure 6.15, the SPAD dominant noise source is diffusive noise. Although the rate is normalized to the area, there is a slight increase of the dark count rate visible towards larger sizes. Between the smallest and the largest, which has an area ten times larger than the small, an increase in rate of about 25% is observable, which is same for all process variations and visible up to the temperature of $T \approx 220\,\mathrm{K}$. The SPAD shape, on the other hand, does not make any difference. SPAD 1 and 6 (purple and brown data point) have almost the same area, differing only by about 5%, but due to a smaller aspect ratio, SPAD 6 has 25% more circumference. However, their rate is not significantly different. The small deviation between these, is most likely introduced by systematic error of the Gauss fit. Since there are only 361 SPADs, which have differences in the rate causing a certain standard deviation, the choice of the binning and the fit interval can introduced a variation of the mean in the order of 2%. This was, especially, worse for the larger SPADs since many hot pixels are present and accordingly less average SPADs are in the average distribution. Furthermore, the smaller number of average SPADs in the noise distribution is also the cause for the larger error for the SPAD0.
Overall, the difference between the sizes is rather small and in addition seems mostly to affect the small SPAD sizes, so in principle there is nothing to prevent the use of larger SPADs. However, why the dark count rate scales with sizes is, not entirely clear. Diffusive noise is caused by minority charge-carriers, which diffuse into the depletion region (see section 3.6.2). In principle, this can happen at any place in the diode where, no or only a small, potential separates them from the depletion region. Therefore, a broad variate of possibilities for diffusion exists, which can originate from the silicon surface, electrical contacts, or any structure inside the SPAD or its surrounding [116]. The guard-ring structure surrounding the SPAD, however, can be excluded as it causes a diffusive noise contribution scaling with circumference, which is already excluded. Another possible cause could be that their area is overestimated, of which the physical size of the active area is actually smaller than assumed.
On the right side of figure 6.15, the dark count rate as a function of the SPAD size is shown for $T \approx 160\,\mathrm{K}$. The statistics is much lower than at room temperatures, even though the measurement time was with an hour much longer. The accuracy is limited to 10% for the large SPADs and about 30% for the smaller ones. However, for this work the resolution is sufficient since of most interest is the order of magnitude of the noise.
At those temperatures tunneling noise dominates and no significant increase is visible towards large sizes. Also, tunneling noise almost exclusively depends on the electric field peak inside the depletion region of the SPAD (see section 3.6.3). As there is no significant deviation, meaning at least an order of magnitude, between the SPADs, the field distribution inside the SPADs is assumed to be relatively homogeneous and the peak field fairly comparable. So, at low temperatures, the SPAD noise is mostly independent of the SPADs size as well as the shape and large SPADs can be utilized in terms of noise in future arrays. To gain more accurate insight in their behaivor, a significant increase in measurement time, of about a factor of ten, is required, which was beyond the scope of this work.
It was further investigated if their is any difference in the dark count rate as function of the

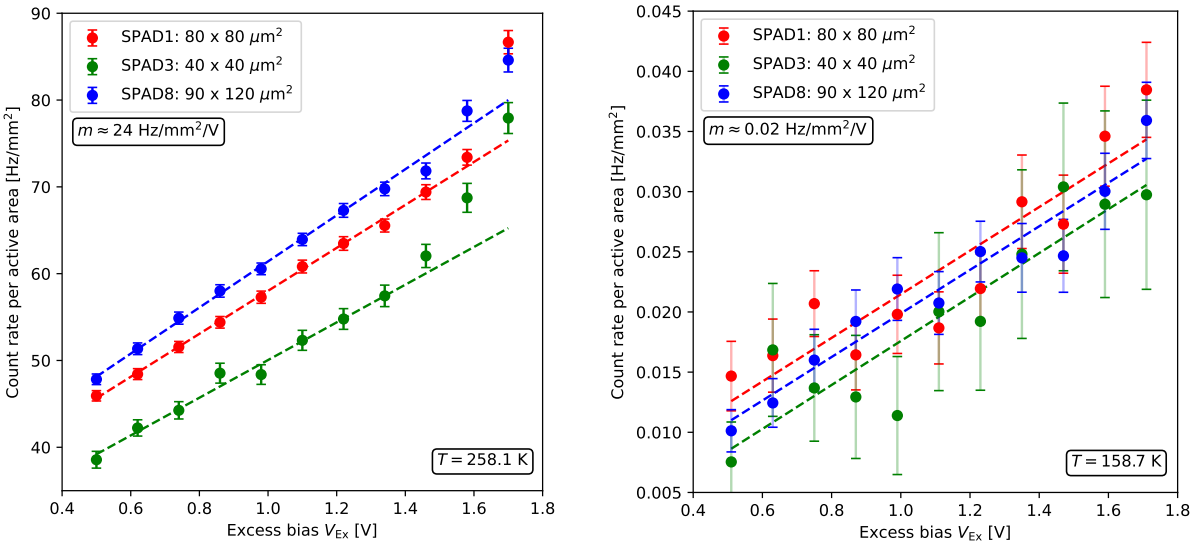

Figure 6.16: Dark count rate normalized to the active area as a function of the applied excess bias voltage, for a small, a medium and a large SPAD (process variation 2) at $T \approx 260\,\mathrm{K}$ (left) and $T \approx 160\,\mathrm{K}$ (right). The dashed lines are linear regressions. At $T \approx 260\,\mathrm{K}$ their slopes are comparable and the offset described at the beginning of this section is visible. At $T \approx 160\,\mathrm{K}$ the error is fairly large, but all SPADs show the roughly the same increase an no large offset is visible.

excess bias for the difference SPAD sizes. These measurements were made by means of a small (3), a medium (1) and a large SPAD (8) at $T \approx 260\,\mathrm{K}$ and $T \approx 160\,\mathrm{K}$, which is plotted in figure 6.16. The dashed lines correspond to linear regressions of the data points.
It should be noted that the maximal applicable excess bias voltage is about $V_{\mathrm{Ex}} = 1.7\,\mathrm{V}$. On the one hand, taking into account the offset of 0.8 V introduced by the breakdown voltage determination method (see section 6.2.1), at this excess bias the SPAD signal amplitude is already is close to the arrays supply voltage, which is limited by the readout board to $V_{\mathrm{DD}} = 2.5\,\mathrm{V}$ (see section 5.3.1). The front end does not allow SPAD signals with larger amplitude then the supply voltage (see section 4.3.3), so that above this excess bias the front end is assumed to become inoperable and the rate somehow increases, which is not completely visible in the plots for the sake of clarity. On the other hand, the operational voltage could be limited in a comparable way as for the IDP2. Here, a high afterpulsing probability is assumed to increase the noise very rapidly. Since, the dark count rate is increasing visible at high temperatures before $V_{\mathrm{Ex}} = 1.7\,\mathrm{V}$ (left side of figure 6.16), where also a short recharge time of the SPAD is chosen (see section 6.1.2) this effect cannot completely be excluded.
At at $T \approx 260\,\mathrm{K}$, shown on the left side of figure 6.16, for the three SPADs of different size an linear increase of the dark count rate is observed. The diffusive noise increases with the applied excess bias voltage mostly due to the increasing avalanche trigger probability inside the SPAD (see section 3.6.2). This is in agreement with the sensitivity measurements, shown in section 6.3.2, where the detected photon rate also increases fairly linear with the applied excess bias voltage (see section 6.3.2). However, the slope for all SPADs is very comparable and increase with $(24 \pm 1)\,\mathrm{Hz\,mm^{-2}\,V^{-1}}$. The offset found between the SPADs dark count rate corresponds to the one observed on the left side of figure 6.15. So, the different SPAD sizes also have no influence on the dark count rate as function on the excess bias voltage.
At lower temperatures of $T \approx 160\,\mathrm{K}$, shown on the right side of figure 6.16, a increase in the dark

count rate is visible but the error, especially for the small one, is large. Compared to the error shown on the right side of figure 6.15, it is even larger, which is due to a shorter measurement time of only 30 min per voltage step. The increase of the rate is approximately linear and fits to the error margin of most of the data points. Its exact profile is, however, not resolvable within this small voltage range and could also be exponential with a moderate exponent (compare section 6.4.1). An significant difference in the offset of the linear regression is not visible and might be masked by the error. However, the slope of the different SPADs sizes are roughly the same and is about $(0.020 \pm 0.003)\,\mathrm{Hz\,mm^{-2}\,V^{-1}}$, which is fairly moderate.
Clearly with respect to the dark count rate, no large deviations from expected proportionality to the area were found, and furthermore, no dependency on their shape was observed. Consequently, large SPADs, also with more sophisticated shapes, like hexagonal ones, having a lower margin area and therefore a higher fill factor compered to square SPADs, can be used at high temperatures as well as at low temperatures.

6.9.2 Hot SPADs

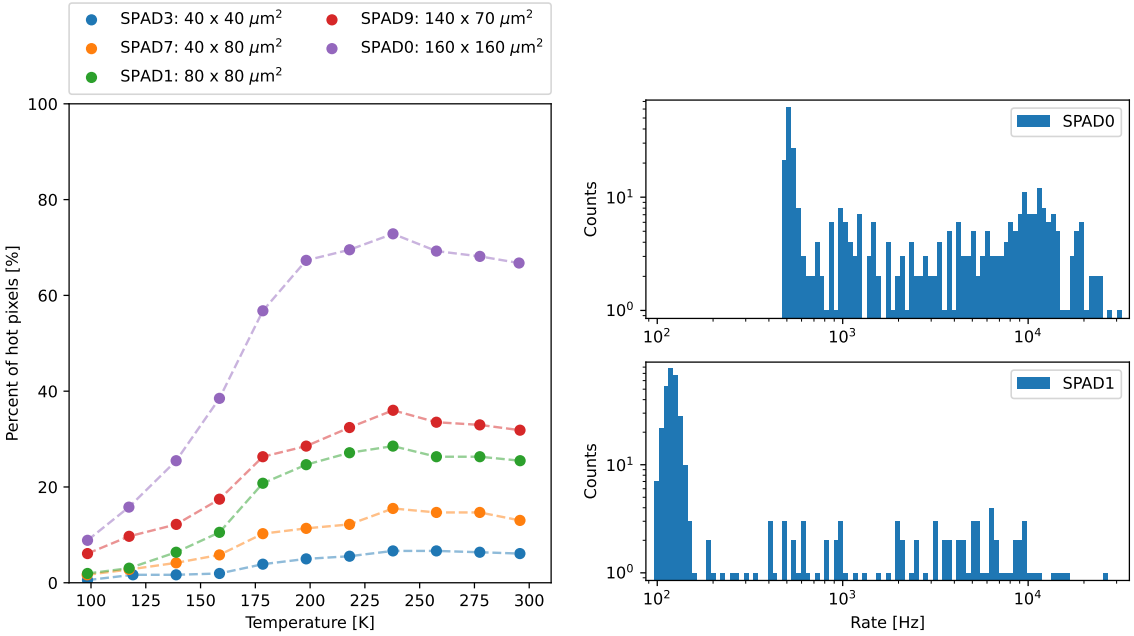

Figure 6.17: **Left:** Fraction of hot SPADs as function of temperature for various SPAD sizes (Process variation 2). The freeze out process (see section 6.5) starts at $T \approx 200\,\mathrm{K}$. **Right:** Example of the dark count rate distributions of SPAD0 and SPAD1 at room temperature. The peak shows the average SPADs while the broad part of the distribution are the hot SPADs.

On the left side of figure 6.17 the fraction of hot SPADs is shown for various SPAD sizes as a function of temperature. The fraction of hot SPADs clearly scales with size. For example, at room temperature between the medium size SPAD1 and the large SPAD0 it increases from 20% to 70%, with SPAD0 being four times larger than SPAD1. SPAD3, on the other hand, has about the size of the SPADs of the IDP2 and the observed fraction of 5% is in line with the 6% found for the IDP2 (see section 6.5). The absolute error of the faction of hot SPADs is approximately ±2% for the large SPADs and ±1% for the small ones.
Towards lower temperatures, the freeze out process of the Hot SPADs is observed, which is very comparable to the one of the IDP2 (see section 6.5). The fraction of hot SPADs decreases

uniformly with temperature, since the dark count rate of hot SPADs of the DARWIN Test array are also uniformly distributed, which can be seen on the right side of figure 6.17. Two examples of dark count rate distributions (not normalized to area) at room temperature for a medium size SPAD (SPAD1, bottom), and the largest one (SPAD0, top), are shown. In both distributions a peak at lower count rates is visible, representing the average SPADs. Above this peak a broad, uniform distribution of hot SPADs is observed, which is more highly populated for the large SPAD. However, a maximal rate of roughly 1×10^4 Hz can be found, which is mostly independent of SPAD size and in agreement with the value found for the IDP2 (see right side of figure 6.9). Consequently, as for the IDP2 (see section 6.5) it is assumed that mostly single point like defects situated inside the depletion region of the SPAD causing their "hot" behavior, making it irrespective of SPAD size. Furthermore, manufacture seems to introduces the same and a fairly constant amount of defects, since the data of the DARWIN test array and the IDP2 are comparable.
Overall the freeze out process starts at $T \approx 200$ K and is irrespective of SPAD size. Compared to the IDP2, the start temperature of the freeze out is about $\Delta T = 50$ K lower (see section 6.5), which is due to the lower tunneling noise limit of the DARWIN Test array (see section 6.8). Secondly, the start temperature of the freeze out process is given as follows: The average thermal generation noise, above which a SPAD must be situated to be a hot SPAD, increases proportional with the SPAD size (see previous subsection). Tunneling noise forming the freeze out boundary for hot SPADs (see section 3.6.6), is also proportional to the size. Consequently, the hot SPADs of all SPAD have a comparable relative noise level above the corresponding tunneling level and therefore freeze out at roughly the same temperature.
Finally, the SPADs are free of crosstalk-induced tail, which was observed for the IDP2 (see section 6.2.2). In the DARWIN array, crosstalk is very unlikely, because SPADs in adjacent macro pixels are separated by 290 µm (see section 3.7.2), since only one of the 10 SPADs in a macro pixel is activated during a measurement.
Obviously, at room temperature, it is not practical to use large SPAD sizes, since for SPAD0 70% of them have to be switched off to operate the array at its genuine noise performance. The loss in active area, and therefore fill factor, is too drastic, making smaller sizes preferable. An optimal SPAD size was observed, for which the overall fill factor, after switching off all hot SPADs is largest. Moreover, as the number of hot SPADs decreases with temperature, this optimal size increases, which is most advantageous for the DARWIN experiment. It enables a larger effective fill factor, which is the residual fill factor of the array when all hot SPADs are switched off. To determine this optimal size the fraction of hot SPADs as function of the size was modeled and thus the effective fill factor was calculated.
A Poisson-model, which assumes the defect denisty to be very low and the defects are equally distributed , is utilized to describe the fraction of hot SPADs as function of the SPAD size. The probability to have a k defects in the SPAD is described by an Poisson-distribution [194]. Mostly the IDP2 (see section 6.5) confirms this assumption. Its has a large number of pixels, which are reasonable small and only a fraction of hot SPADs at room temperatures of 6%, so that the defect density is low and they are observed to be equally distributed. The fraction of hot SPADs as function of the size, is then written as

$$P_{\mathrm{b}}(k \geq 1, A) = 1 - \exp\left(-DA\right) \tag{6.2}$$

where k is the number of defects, A is the active area of a SPAD and D is the defect density [194]. On the left side of figure 6.18 a fit of this model to the fraction hot SPADs of an array made with process variation 2, is shown at room temperatures and at lower temperatures of $T \approx 160$ K and $T \approx 100$ K. The fit describes the data at room temperature as well as those at lower temperatures, reasonably well. So, the defect density is low, mostly single defects cause the SPADs to be "hot"

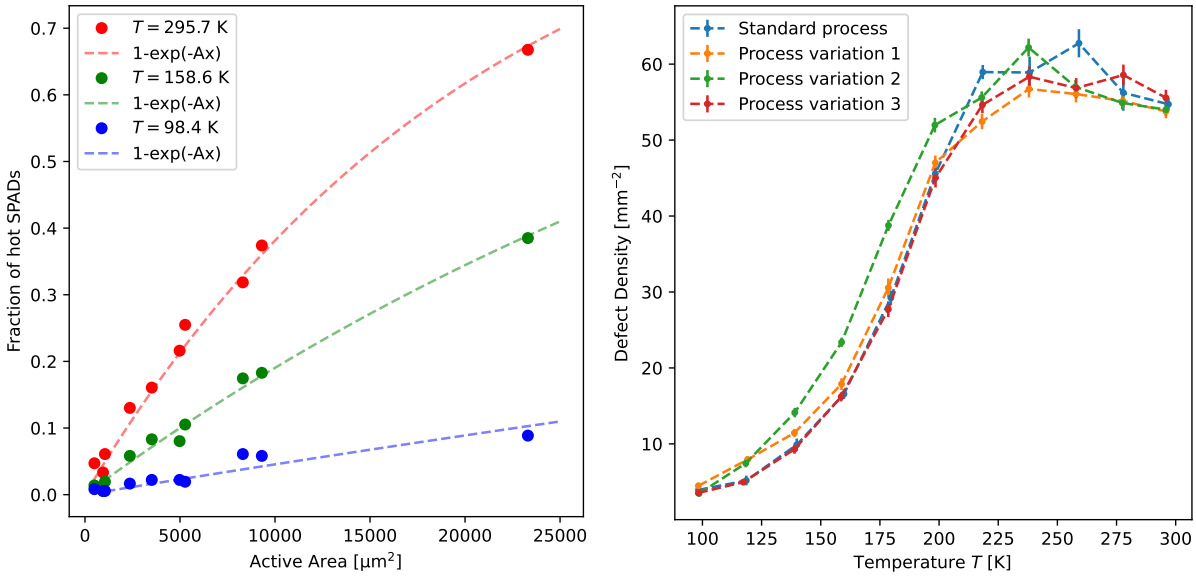

Figure 6.18: **Left:** Fit of the Poisson-model (eq. 6.2) to the fraction of hot SPADs (figure 6.17) as function of the SPAD size at $T \approx 296\,\mathrm{K}$ (red), $T \approx 160\,\mathrm{K}$ (green) and $T \approx 100\,\mathrm{K}$ (blue) for a array of process variation 2. **Right:** Defect density D obtained from the model fit as function of the temperature for arrays fabricated in the standard process and with process variation 1,2 and 3.

and no additional effect is introduced because of the size. Finally, the number of hot SPADs for all sizes, decreases uniformly with temperature, since the model fit describes the data well also at low temperatures. The reduced defect density towards low temperatures should not be confused with a vanishing of the defects, as only their noise contribution drops below the tunneling noise level. The defect density is determined to be around $D = (54 \pm 2)\,\mathrm{mm}^{-2}$ at room temperatures, $D = (24 \pm 1)\,\mathrm{mm}^{-2}$ at liquid Xenon temperatures, and decreases to $D = (5.0 \pm 0.5)\,\mathrm{mm}^{-2}$ at $T \approx 100\,\mathrm{K}$.
On the right side of figure 6.18 there is the defect density extracted with the Poisson model as a function of temperature. The defect density is the average from the two data sets, which were accumulated for each process variation (see section 6.1.2). At room temperatures all arrays of the different processing show a comparable defect density of roughly $D \approx 54\,\mathrm{mm}^{-3}$. Consequently, the manufacture with the process variations, does not introduce further defects. Towards lower temperatures at $T = 200\,\mathrm{K}$ it decreases so that it reaches a value of $D \approx 20\,\mathrm{mm}^{-3}$ at liquid Xenon temperatures. However, since process variation 2 shows the most significant reduction of the tunneling noise level (see section 6.8), a slightly higher defect density is observed compared to the others. At $T \approx 160\,\mathrm{K}$ a defect density of $D \approx 24\,\mathrm{mm}^{-3}$ is observed while with the other arrays it is about $D \approx 17\,\mathrm{mm}^{-3}$.
The so-called effective fill factor, which was already introduced above, is defined as the residual fill factor after all hot SPADs are switched off. It can be written as

$$FF_\mathrm{e}(A,T) = P_\mathrm{g}(D(T),A) \cdot FF(A). \tag{6.3}$$

where, P_g is the fraction of good SPADs, which is $P_\mathrm{g} = 1 - P_\mathrm{b}$ (see eq. 6.2), $D(T)$ is the temperature dependent defect density and FF is the fill factor of the SPADs (see section 4.3.2). In figure 6.19 the effective fill factor at three different temperatures, for the defect density determined with an arrays made with process variation 2, is shown. The dashed line in gray is the

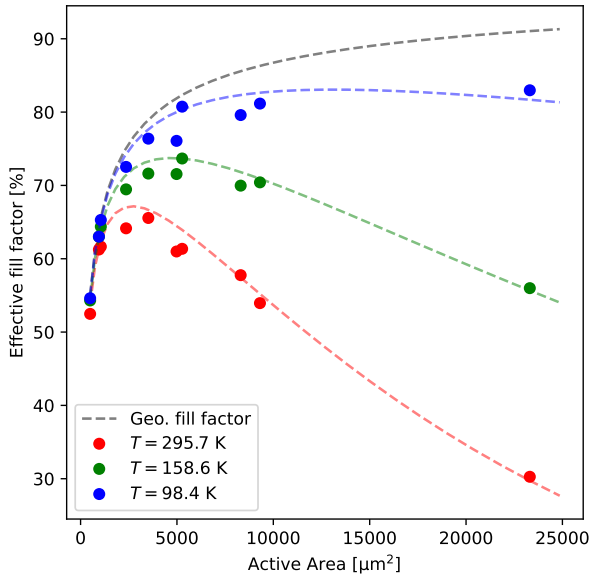

Figure 6.19: Effective fill factor (FF_e) as a function of the size of the active area of the SPAD at $T \approx 296\,\mathrm{K}$ (red), $T \approx 160\,\mathrm{K}$ (green) and $T \approx 100\,\mathrm{K}$ (blue) for a array made with process variation 2. The dashed gray line is the fill factor as a function of the active area. The data points are obtained by multiplying their fill factor with the fraction of good SPADs (figure 6.17). The colored dashed lines at the respective temperature are calculated from equation 6.2 with a defect density obtained from figure 6.18.

calculated geometrical fill factor FF as function of SPADs active area. The colored dashed lines are the effective fill factor at different temperatures as a function of the SPAD size calculated from equation 6.3 where the defect density is from the model fit (see right side of figure 6.18). The data points on the other sides are the values for the ten SPADs of the macro pixel, which were calculated with the help of the measured fraction of hot SPADs (see figure 6.17) multiplied with their geometrical fill factor (gray curve). The data points tend to be slightly below the curve this has two reasons: First, the fit shown on the left side of figure 6.18 has the tendency underestimate the farction of hot SPADs about one to two percent, at least for the smaller SPADs. Second, the data points below the line belong mostly to the rectangular ones. The fill factor of these is slightly lower than for the square ones. Since, the gray line represents the geometrical fill factor for rectangular SPADs a small systematic error is introduced. Overall, the defect density determined with the Poisson model (see eq. 6.2) shows a reasonably good agreement with the data.
At room temperature (red curve) a distinct maximum of the effective fill factor is visible for a certain SPAD area, which shifts to larger sizes for lower temperatures. While at room temperature with a $60 \times 60\ \mu\mathrm{m}^2$ SPAD, an effective fill factor of 65% is reachable, at liquid Xenon temperatures a SPAD size of $80 \times 80\ \mu\mathrm{m}^2$ can be used and the effective fill factor is 74%. This corresponds then to the SPAD size best utilized for a future DARWIN Digital SiPM array. With lower temperatures, the effective fill factor converges towards the geometrical fill factor since most of the hot SPADs are frozen out and, for example, at $T \approx 100\,\mathrm{K}$ a effective fill factor above 80% can be reached.

6.10 Power Consumption

A low power consumption is a key feature of a light detector to prevent excessive heating of the liquid Xenon target in the DARWIN cryostat (see section 2.4.3). For this purpose, the DARWIN Test array is equipped with a data-driven readout architecture (see section 4.3.5). Here, power is only consumed when a hit in the matrix happened, so that the power consumption should scale approximately linear with the rate of photons detected.
For the measurement of the power consumption as a function of the photon rate, the SPADs were biased with $V_{\mathrm{Ex}} = 1\,\mathrm{V}$ and the detector was irradiated with the LED (see section 5.2). The

LED bias voltage was increased step-wise, and at each voltage step the rate was measured for a duration of 20 s. Error signals are included into the analysis so as not to overestimate the power consumption. However, the fraction of error signals is mostly about 1% and only increased to 10% at the highest rate for the largest SPAD. The power consumption of the array is then obtained by multiplying the supply voltage $V_{DD} = 2.5\,V$ with the measured current consumption of the readout electronics. The latter is recorded continuously and measured once per second (see section 5.2). In figure 6.20 the power consumption at $T \approx 160\,K$ as a function of the detected photon rate for SPAD0, which is the largest one of the ten (see section 4.3.2), from an array manufactured with process variation 2, is shown. The line in red corresponds to a linear regression of the data points.

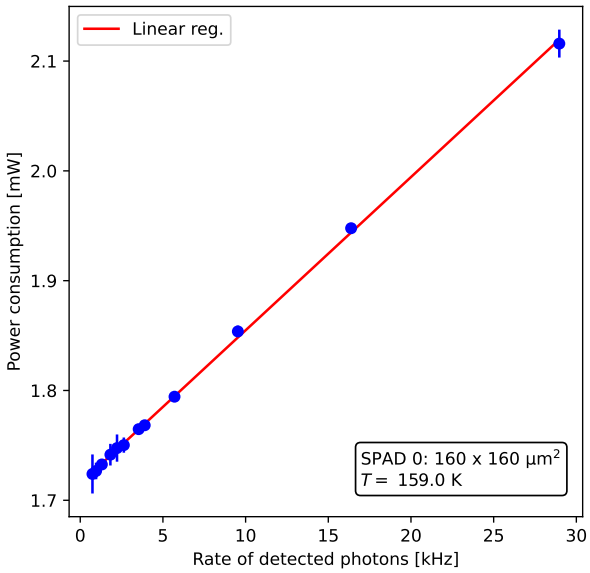

Figure 6.20: Power consumption as a function of the detected photon rate for SPAD0 at $V_{Ex} = 1\,V$. The line in red is a linear fit, which has a slope of $14\,\mu W\,kHz^{-1}$ and a y-intercept (idle power consumption) of 1.7 mW.

The power consumption scales linear with the rate of detected photons and its determined slope is only $14\,\mu W\,kHz^{-1}$ ($\pm 1\%$), which corresponds to an energy consumption of about 14 nJ per detected signal. The y-intercept of the fit corresponds to the idle power consumption at zero detected rate and is 1.7 mW.

The most significant contribution to the power consumption per detected signal is attributed to the charger process of the cables used to remotely connect the array inside the cryostat with the readout board (see section 5.2). The array has, in total, 12 output signals, which are the hit signal, the error signal and ten for the x/y address of the hit macro pixel. A ribbon cable carries these signals, which is roughly 1.5 m long and each of the twelve lines is assumed to have a capacitance in the order of 150 pF. One charge process then consumes an energy of about 1 nJ (with $E = C \cdot V^2$). The next significant contributor is the readout electronics of the DARWIN Test array. A signal of a macro pixel triggers 10 wired-ORs, which have a length of 5 mm and are assumed to have a capacitance of a few 1 pF. Furthermore, a minimal block of logic processes the signals on the wired-OR and drive the lines to the pads, of which the power consumption is assumed to be negligibly small. The overall dynamic power consumption of the readout is assumed to make up 10% of the total.

The contribution of the SPAD recharge process is, on the other hand, negligibly small. With a SPAD capacitance of roughly 100 fF [195], the recharge to an excess bias of $V_{Ex} = 1\,V$ consumes about 0.1 pJ. The power consumption of the ten SPADs with different geometry was also measured and no significant difference was found between these. Also, a change in temperature does not lead to significant change in the dynamic power consumption.

The idle power consumption is higher than the dynamic one. A static current of about 700 µA is measured in idle mode. However, the arrays readout is nearly all made of CMOS logic apart from, the wired-Ors transferring the hit signals, which all have no static power consumption. The only known part of the circuitry of the array drawing a constant current, is the DAC (see section 4.3.6), with which the recharge current of the SPADs is adjusted. It was determined to consume a constant current of about 1 µA, which a negligibly small contribution. Some portion will be lost to leakage current, but the overall amount of electronics on the array is small. On the readout board there is a voltage regulator connected to the array supply voltage line, which is assumed to consume about 100 µA. However, it is unknown whether the constant current mostly drawn by the arrays circuitry, by the readout board or even caused by a fault on the carrier board.
Nevertheless, a data-driven readout architecture is very suitable for the DARWIN experiment, since very little power is consumed per photon detected. In addition the event rate in the DARWIN experiment is low (see section 2.4.3) and the array can mostly remain in idle mode. Assuming the idle power consumption is in the same order in a future array with a size of $1 \times 1\text{cm}^2$ so that about 50 000 arrays cover the detector plane of the DARWIN Experiment ($\varnothing \approx 2.6\,\text{m}$), the total power consumption will be about 90 W. Even the contribution of the cables charge process can be kept low. They will have a significant capacitance, since they are about ten or more meter long, but when their number is kept low and the data transfers happens at a moderate frequency, which is allowed due to the low event rate, the power consumption can be low.

6.11 Correlated Noise

The main sources of correlated noise for a digital SiPM array, are optical crosstalk, afterpulsing, and photon emission by the readout electronics (see section 3.7). Optical crosstalk between SPADs is caused by photons emitted during an avalanche in one SPAD, which trigger a neighboring one. Afterpulsing is a phenomenon where charge-carriers of an avalanche are trapped in trap levels (see section 3.7.1) and, upon their release, which occurs with a certain lifetime, they can trigger an avalanche. Photons are emitted from the readout electronics when they draw current.
In this section, at first a more general discussion is undertaken, concerning the impact correlated noise in digital SiPMs arrays actually has on the DARWIN experiment. For the discussion, a moderate crosstalk and afterpulsing probability is assumed, which is so low that both processes cannot re-trigger themselves, making the array inoperable (see section 6.4.1). After this, a very basic measurement of the crosstalk probability at $T \approx 160\,\text{K}$ is present. This was made with the DARWIN test array. A quantification of afterpulsing, meaning measuring the time constant, was, however, beyond the scope of this work. The minimal hit signal length of the DARWIN Test array is, with 300 ns (see section 6.1.2), is to long to resolve it. Also, afterpulsing was not observed during the dark count rate measurements, since it was mostly masked by the long recharge time of the SPADs (see section 6.1.2). Finally, photon emission was, with the low power readout of the DARWIN test array (see section before), in contrast to the IDP2, not directly observable any more.

6.11.1 Impact on the DARWIN Experiment

Photon emission by the readout electronics is perhaps most concerning for DARWIN. When a static current flows or the circuitry is very active, a background is introduced which is not distinguishable from the dark count rate (see section 6.6). With the dark count rate also the accidental

3 fold coincident rate increases (see section 2.4.3), so that a minimum of three photons cannot be properly resolved. However, with a low power readout architecture it is strongly suppressed, making it key feature for a future array for the DARWIN experiment.
In contrast to photon emission by the readout, afterpulsing and crosstalk are always correlated to a primary SPAD signal, which has its origin in a dark count or a photon absorption. The result is, on the one hand, an increased dark count rate, which again decreases the energy threshold, and, on the other hand, a variation in the number of detected photons, which worsens the energy resolution (see section 2.4.3).
However, the dark count rate of the SPADs at $T \approx 160\,\mathrm{K}$, which is about $0.02\,\mathrm{Hz\,mm^{-2}}$ (see section 6.8), is so low that it is highly unlikely that a coincidence dark count occurs in the neighboring SPADs or a subsequent dark count occurs with a short delay in the same SPAD. Since, digital SiPM arrays offer position and time resolution, these afterpulsing or crosstalk events can be identified and rejected. Consequently, the actual uncorrelated dark count rate is not impaired.
In the S1 signal about 10^2 to 10^4 photons illuminate two large detector planes, each equipped with $\sim$ 50000 arrays (see previous section), making it nearly impossible that two photons hit neighboring SPADs or, with some delay, the same SPAD. Thus, it should be possible to detect and discard crosstalk and afterpulsing events in an recorded S1 event, so that the minimum resolvable number of photons defining the energy threshold is not distorted.
For an S2 event where 10^3 to 10^6 photons are emitted and focus on a small spot on the detector plane (see section 2.4.3), crosstalk introduces hits in neighboring SPADs, which are indistinguishable from actual photons. Consequently, an offset or fluctuations in the number of detected photons is introduced. Since the recoil energy is determined by the number of detected photons, it has to be evaluated how much a small variation in their number degrades the energy resolution.
The number of registered afterpulses, on the other hand, depends on the readout architecture of the utilized Digital SiPM array. So, for example, in an architecture where a certain delay between the detection of a photon and the extraction of the hit information from the pixel is present, afterpulsing may be masked in this delay.

6.11.2 Optical Crosstalk

Optical crosstalk is caused by photons emitted during an avalanche in one SPAD, that travel through the silicon and trigger a neighboring SPAD (see section 3.7.2). These photons create a secondary signal with a delay of some 1 ps to the primary one. The number of emitted photons depends on the current flowing through the depletion region during the avalanche. Furthermore, it mostly does not depend on temperature but increases for decreasing SPAD pitch. In conclusion it becomes worse for very dense arrays with large SPADs, as particularly for larger SPADs the current flow per avalanche is increased (see section 3.7.2).
Crosstalk is quantified as probability that, on a primary SPAD signal, a neighboring SPADs fires. In the DARWIN Test array, a crosstalk event with its very short delay, causes an error signal (flag for a coincident hit, see section 4.3.5). Therefore, the crosstalk probability is assumed to be proportional to the fraction of the error signals.
In a future array the SPADs will be densely packed and all SPADs of a macro pixel will be activated. So, to characterize crosstalk for this scenario, two SPADs per macro pixel were activated simultaneously during a dark count rate measurement. These two are located directly on the border to the next macro pixel. In figure 6.21 an part of the macro pixel matrix is shown where the red dotted lines highlights the border between the macro pixels and the green arrows marks which SPADs were switched on simultaneously. The number of dark counts and the corresponding error signals were recorded over a duration of 30 min at a temperature of $T \approx 160\,\mathrm{K}$ and $V_{\mathrm{Ex}} = 1\,\mathrm{V}$. During an ordinary dark count rate measurement, where only one SPADs in

the macro pixel are switch on, the average fraction of error signals is determined to be about $\sim 0.1\% \pm 0.02\%$. Therefore, it is assumed that an increase in the fraction of errors is mostly caused by crosstalk and the fraction of error is directly considered as the crosstalk probability (CTP). The CTP is indicated along the arrows in figure 6.21. Furthermore, all measurements were made with respect to SPAD1 as it situated on the edge of the macro pixel. At the same time, with a size of $80 \times 80\mu m^2$, it provides the maximal effective fill factor at $T = 160\,K$ (see section 6.9.2) and is therefore the chosen SPAD size for future arrays (see section 7.2.2).

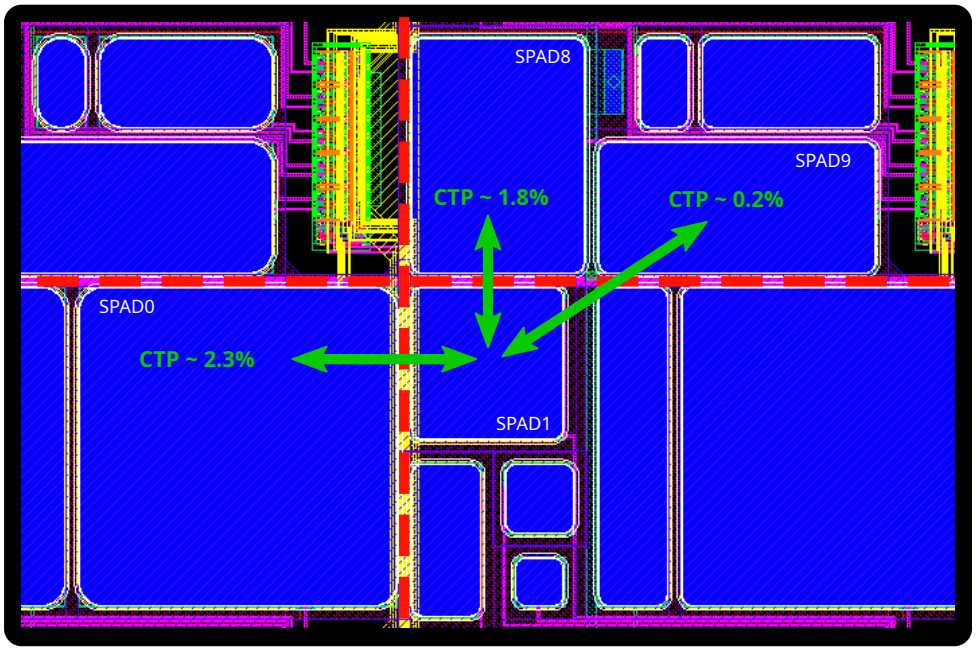

Figure 6.21: Picture of the layout of the DARWIN Test array showing an part of the macro pixel matrix. The red dotted lines highlight the border between neighboring macro pixels. The green arrows mark the SPADs, which are simultaneously switched on during a dark count rate measurement, to determine their crosstalk probability (CTP). The CTP is indicated along the arrows.

The fraction of error signals when the neighboring SPADs, SPAD1 and SPAD9, are activated, was found to be $1.8\% \pm 0.1\%$. The crosstalk probability between SPAD1 and SPAD8, which are diagonal neighbors, was measured to be $0.2\% \pm 0.02\%$, which is slightly above the default error fraction of 0.1%, but is overall negligible. When SPAD0 and SPAD1 are active at the same time (which are also direct neighbors), a quite comparable value of $2.3\% \pm 0.1\%$ can be found. This value is a little larger than the one for SPAD1 and SPAD9. However, SPAD0 is larger than SPAD8 and is much closer than SPAD9 so, to some extent diagonal crosstalk may enhance this value.
In the new digital SiPM array, described in the next chapter, a macro pixel structure with a square footprint and SPADs of the size of roughly $80 \times 80\mu m^2$, are used. When SPADs are situated at the corner of the macro pixel, like SPAD1 in figure 6.21, they have 2 direct neighbors and one diagonal one. The latter neighbor should be negligible and thus the resulting crosstalk probability for the direct neighbors adds up to an overall crosstalk probability of $\sim 4\%$. SPADs with only one direct neighbor, have a reduced chance of $\sim 2\%$.
The 4% crosstalk probability found for the optimal SPAD size is low but still significant. However, as described before, in the S1 signal of the DARWIN experiment, the crosstalk signals can be identified. In an S2 signal it needs to be evaluated how this actually influences the en-

ergy resolution. In principle, crosstalk could also be reduced with measures like, for example, implementing optical trenches between the SPADs or further separating them. However, such measures, should be avoided, since they reduce the fill factor or introduce additional processing, which may affect the dark count rate.

6.12 SPAD Start-Up Behavior

While operating the DARWIN test array below temperatures of $T \approx 220\,\mathrm{K}$ it was observed that on its start-up, which means enabling the output of the SPAD bias voltage source to bias the SPADs above breakdown, the dark count rate is very high and drops with time. In figure 6.22 the dark count rate (whole array including hot SPADs) for the first 5 min after the start-up is depicted for SPAD1 (process variation 3) at $T \approx 160\,\mathrm{K}$ and $T \approx 120\,\mathrm{K}$ and $V_{\mathrm{Ex}} = 1\,\mathrm{V}$. It has to be noted that the investigation of this effect was performed over the whole period of array characterization. Therefore, in the following a collection of data from several arrays with different process variations is shown, since no significant changes were observed for the different manufacture. Furthermore, all are shown by means of SPAD1, since also between the SPADs no significant difference was observed. Also hot and average SPADs, follow the same behavior.

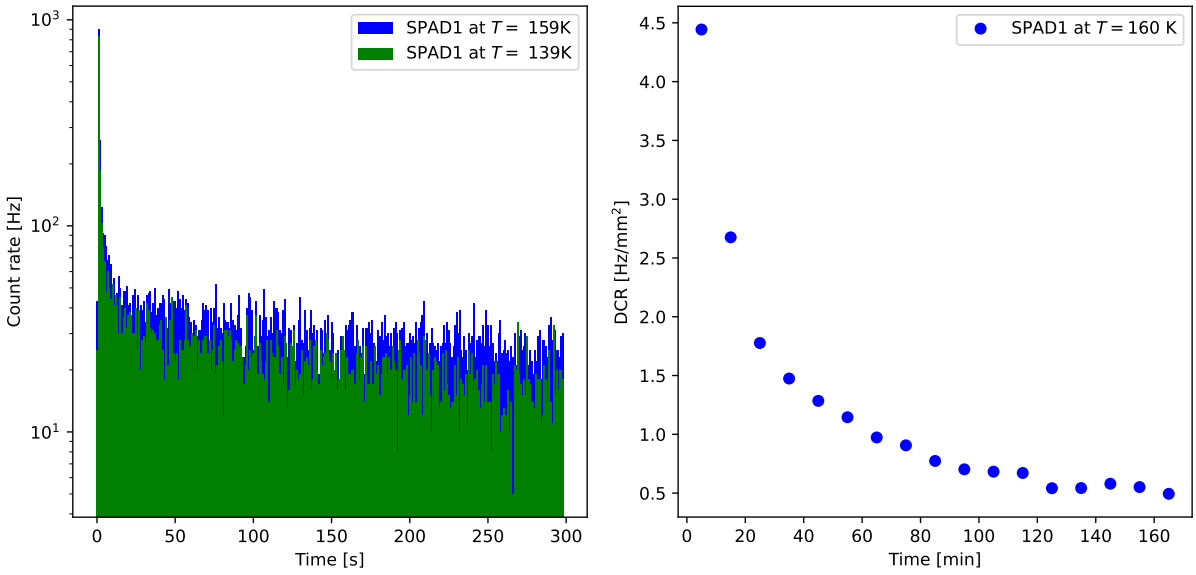

Figure 6.22: **Left:** Measured dark count rate of the array (process variation 3, hot SPADs included) at $T \approx 140\,\mathrm{K}$ and $T \approx 160\,\mathrm{K}$ during the start up, meaning increasing the SPAD voltage from zero bias to above the breakdown voltage ($V_{\mathrm{Ex}} = 1\,\mathrm{V}$). A first rapid decrease in rate is observed which goes over into a second, more moderate, decrease. **Right:** Average dark count rate per 10 min of a 3 h measurement at $T \approx 160\,\mathrm{K}$ started shortly after the first steep decrease in the start-up effect (process variation 3, hot SPADs excluded). It takes about 2 h until the dark count rate reaches its true value.

The initial dark count rate is high and decreases by about one order of magnitude within a few 1 s. However, the SPADs genuine noise performance has not yet been reached since a second fall in dark count rate follows which has a much longer time constant than the first. This second fall was monitored over a period of 3 h at $T \approx 160\,\mathrm{K}$ and the average dark count rate for 10 min slices was evaluated for it, which is shown on the left side of figure 6.22. It takes about 2 h until the dark count rate reaches its actual or true level.

It is not clear where this effect originates from, but it seems to be comparable to afterpulsing (see section 3.7.1). In the unbiased state, where the p/n-junction inside the SPAD is in thermal equilibrium and the depletion region very small, so that charge carriers can occupy most trap levels inside the SPAD. When the bias voltage above breakdown is suddenly applied and the SPADs p/n-junction driven out of thermal equilibrium, the trapped charge-carriers are released with a certain life time and can trigger an avalanche. The life-time of those traps, however, must be in the order of seconds for the first initial drop. Secondly, the life-time does not seems to increase with decreasing temperature as it does for afterpulsing, which can be seen on the left side of figure 6.22.
The second decrease must then be another kind of defect level, having a much longer life-time. However, it is not known if such defect level exist in silicon. Furthermore, the dark count rate as a function of time, as shown on the right side of figure 6.22, has to be evaluated for several temperatures, to see how it evolves with temperature. However, due to a lack of time, in the end of this work, such a characterization was not possible any more.
Nevertheless, this effect can be avoided when the SPAD bias is constantly switched on, whereas the bias voltage is not needed to be above breakdown. While measuring the array in the cryostat the bias voltage was mostly set to 20 V during idle time. Also, lower voltages were possible without triggering the start-up effect, as long as the diode was not forward biased.

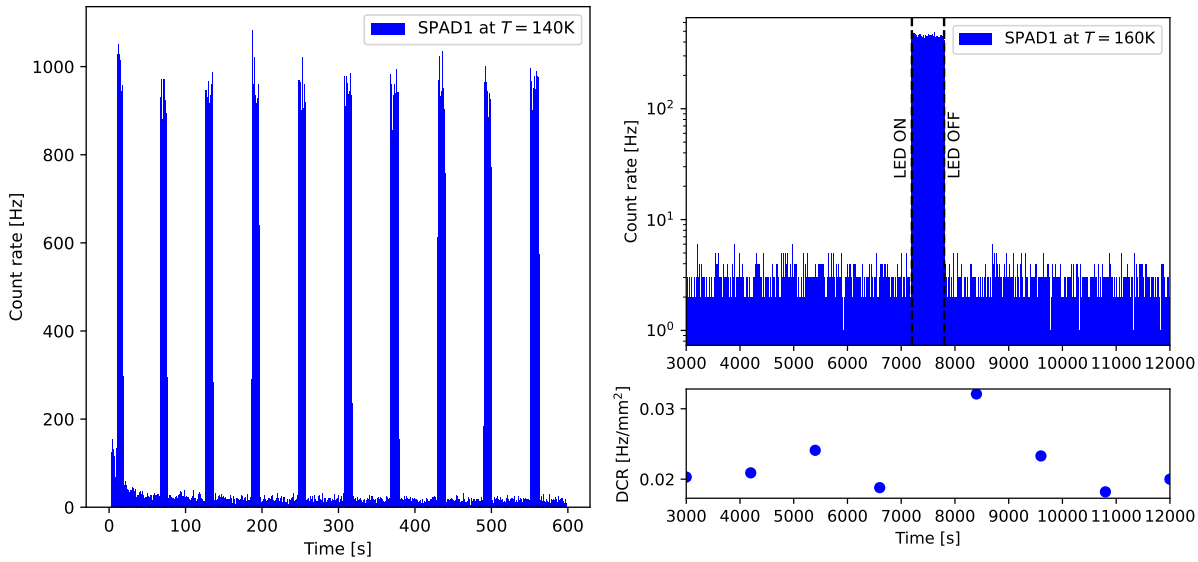

Figure 6.23: **Left:** The dark count rate at $T \approx 140$ K of the array (standard process) was measured for 10 min and every 50 s the LED was switched on for 10 s to test if a decrease in quantum efficiency causes the start up effect. **Right:** Excerpt of a dark count rate measurement (process variation 2) at $T \approx 160$ K where after 2 h the LED was turned on for 10 min. Afterwards again 2 h where measured to test if the LED introduces this effect.

Since it is not clear where this effect originates from, it was further tested that the quantum efficiency (QE) of the SPADs is not affected. Or, more precisely, that the decrease in dark count rate is not caused by a decease in avalanche trigger probability (see section 3.5). For this, the start-up process was trigger, the dark count rate measured for 10 min and after every 50 s the LED in front of the array (see section 5.2) was switched on for 10 s. The measurement was done with SPAD1 (standard process) at $T \approx 140$ K and its result is visible on the left side of figure 6.23. First, over the duration of 10 min no decrease in the photon count rate was visible. Secondly, the first illumination was done during the first steep decrease and only a small offset

in the count rate was introduced. If the QE were to decrease with time, the number of detected photons in the following illumination cycles, would noticeably decrease, since the dark count rate more than halves.
It was further investigated if illumination actually introduces this effect, since during the photon detection charge carriers traverse through the space charge region more frequently than in dark conditions. At $T \approx 160\,\mathrm{K}$ Light was shined on the array made in process variation 2 for about 10 min. Before and afterwards the dark count rate was monitored for 2 h. An extract from this measurement is shown on the right side of figure 6.23. On the upper side the count rate is shown and marked where the LED was turned on, while on the lower side the average dark count rate of 20 min intervals is shown. The standard deviation of the average dark count rate for the two hours is evaluated to be $0.005\,\mathrm{Hz\,mm^{-2}}$ and therefore no significant increase in the dark count rate is observed directly after switching off the LED.

7. New Digital SiPM Array for DARWIN

With the results gained at liquid Xenon temperatures of $T = 165\,\mathrm{K}$, which are an excellent dark count rate, an ultra low power consumption and the effective fill factor of 75% (see previous sections), it was demonstrated that Digital SiPMs are a promising candidate for the light read out in the DARWIN experiment. Although the quantum efficiency at VUV light as essential parameter still has to be evaluated the next step is to approach a realistic readout for a Digital SiPM array for DARWIN. In this last chapter, first of all the requirements for a realistic readout are listed and the proposed architecture described. Then the implementation, which is currently in the last steps of its finalization, will be described. Starting with the optimized macro pixel, the readout architecture, followed by the digital control block, are described. Finally, its properties are summarized and the possible performance in the DARWIN experiment is discussed briefly.

7.1 Requirements and Architecture

What is important for a new readout architecture for the DARWIN experiment (see section 2.4) is the ability to resolve the number of photons of the direct scintillation light (S1) signal and charge collection (S2) signal (see section 2.4). The latter is most challenging, as the energy range of events of interests is between $\sim$10 keV for a WIMP up to 2.5 MeV for neutrino-less double beta ($0\nu\beta\beta$) decay. Within some 1 µs a burst of 10^3 up to 10^6 photons, respectively, is emitted in close vicinity to the detector plane [32], [71]. For the new array, the list of basic constraints, defined in section 4.3, has to be expanded with the following points :

- Resolve a low flux (S1) and short very intense burst (S2) of photons
- Single photon time resolution of $\sim 10\,\mathrm{ns}$.
- Low event rate of a few Hz.
- Low amount of cables inside the cryostat.

In figure 7.1 a schematic of the new array is shown, which has the dimensions of $\sim 1 \times 1\ \mathrm{cm}^2$. The pixel matrix comprises 32×32 macro pixels, which are for clarity, not all depicted. The greatest emphasis of the design is laid on a high fill factor followed by a low power dissipation. For the first, a optimized macro pixel is utilized, which reaches the highest possible fill factor by housing several SPADs, which are read out by only one minimal block of electronics. Furthermore, the overall amount of readout electronics such as the I/O pads is kept low. The latter, in $\mathcal{O}(10)$, occupies only a small fraction of the array width, as shown in figure 7.1. This measure also keeps the number of cables low, which is then further reduced by sending the accumulated hit data serial through a daisy chain of N arrays.
For a low power dissipation, a data driven readout architecture is utilized, which is able to process coincidence hits within a short burst of photons. Here, macro pixels buffer a hit until they are read out. Hit scanners at the end of the column and row, build a scan unit, which extracts the addresses of the hit pixels one after the other. The extracted hit data, including a time stamp, which is recorded once per column with an accuracy of 10 ns, is then buffered by a FIFO, before it is serially output through the daisy chain of arrays.

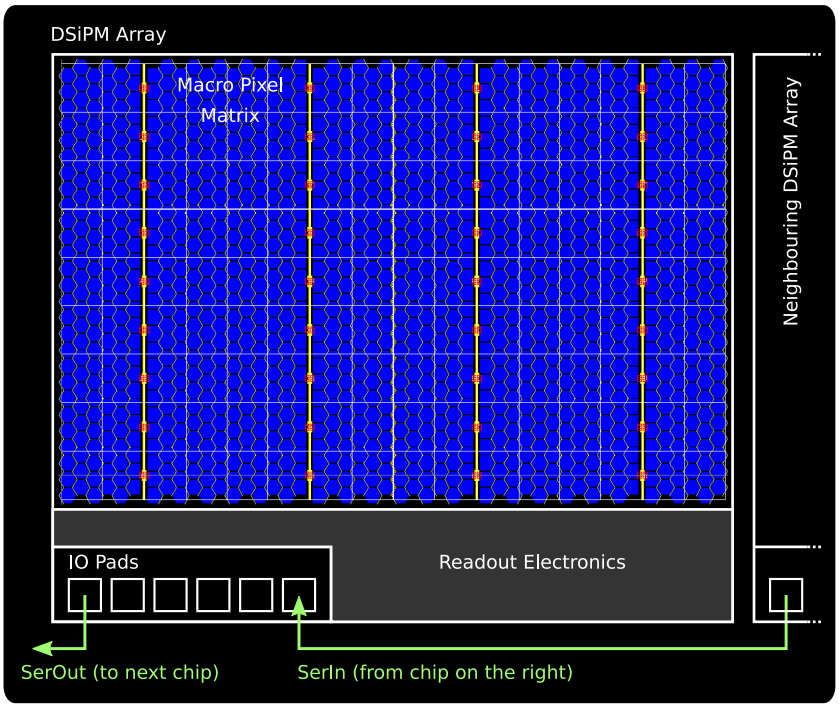

Figure 7.1: Illustration of the new high fill factor Digital SiPM array for DARWIN. Its dimensions are $\sim 1 \times 1$ cm^2 and it consists of 32×32 Macro Pixels. The SPADs in the pixel matrix are shown in blue, while the electronics is yellow. The readout block and the block of I/O pads are schematically depicted in gray and black, respectively.

7.2 Implementation

The new Digital SiPM array for the DARWIN experiment will be made in the CMOS technology by the IMS in Duisburg (see section 4). While the macro pixel is a full costume design, the readout will be synthesized from System Verilog code.

7.2.1 Macro Pixel: Electronics

A schematic of the electronics of a macro pixel, which are similar to the predecessor one (see section 4.3.3), is shown in figure 7.2. Mainly the number of transistors in the front end has been reduced, promoting a high fill factor, and components have been updated to match the new readout architecture.
Beginning with the description of the new functionality, which partially anticipates description of the overall readout of section 7.4. Hit signals from the SPAD front-ends are merged and send to a hit flip-flop. The positive edge of the hit signal sets the flip-flop and the column hit signal is activated. The hit scanner at the end of the columns is then notified about the hit in this column and selects the column for the read out by activating the SendRow signal. On selection, the pixel gains control over the Row Hit signal, with which the hit scanner at the end of the rows can deduce its row address. After this the macro pixel is cleared by a short pulse of the Data Reset signal. The flip flop is edge triggered, so that even if the hit bus is still high due to recharging SPADs it cannot be retriggered. Thus, the readout can proceed fast to the next column.

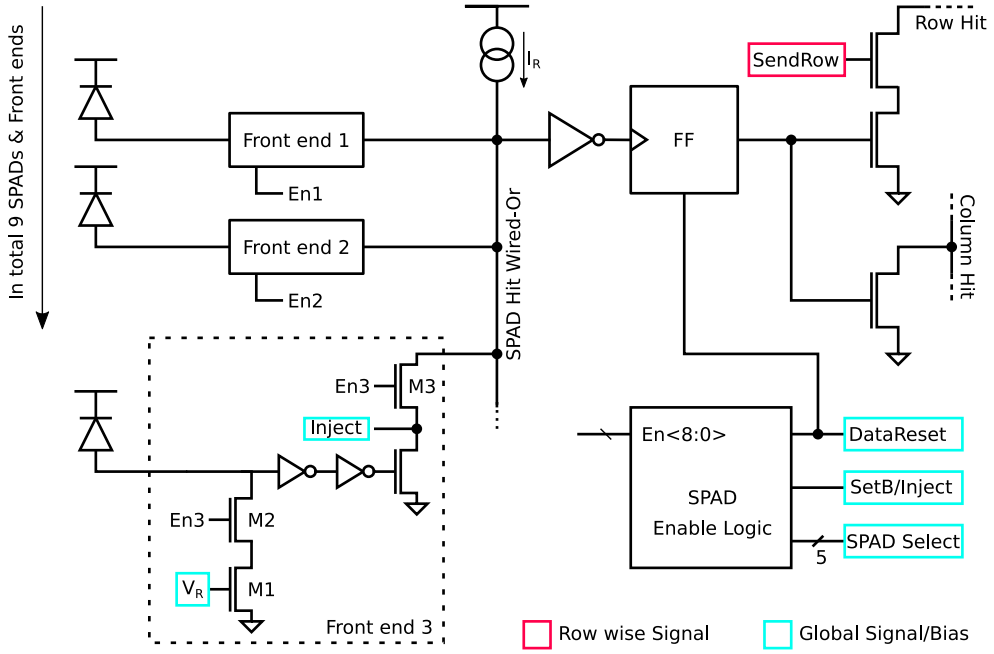

Figure 7.2: Schematic of the new macro pixel electronics, which is similar to the one of section 4.3.3. The number of transistors in the front-end, which is shown in detail on the lower left, was reduced by omitting the active feedback. Furthermore, the hit flip-flop is now edge triggered and a switch for the row bus has been added.

A schematic of one front-end circuit is shown on the lower left side of figure 7.2. For layout reasons, described in the next section, the number of SPADs and their corresponding front-ends is reduced to nine. The active feedback scheme of the predecessor front end is intended to lower afterpulsing (see section 4.3.3) and was omitted in this case, which reduces the number of transistors from 17 to eight. Afterpulsing should be no problem for the new readout architecture. There is a latency of at least $\mathcal{O}(50\,\text{ns})$ between a photon detection and the pixel address deduction. Within this latency any subsequent hits will not be detected. However, in case the time constant of afterpulsing at lower temperatures, is longer than the latency, additional hits can be masked by increasing the SPADs discharge time (see section 3.7.1). Furthermore, a subsequent hit in the same macro pixel is, especially for the S1 signal, most unlikely, so afterpulsing can also be identified in the data analysis.
In this minimal front end, the SPAD is passively quenched (see section 3.3) via the current source transistor M1. The recharge current is adjusted with the bias voltage V_R. Furthermore, the SPAD is disabled by a single NMOS switch (M2). When M2 is turned off it acts as high impedance so that the SPAD anode node cannot recharge [195]. At the same time, with M3, the access to the hit bus is disabled.
Finally, the SPAD enable logic is adopted form the predecessor array (see section 4.3.4).

7.2.2 Layout

The object of the macro pixel layout is to reach a very high fill factor and optimize the signal routing. The result is a unit of 4×1 Macro Pixels, which is shown in figure 7.3. With the electronics, visible as a yellow block, consuming $\sim 5\%$ of the pixel area, its geometrical fill factor

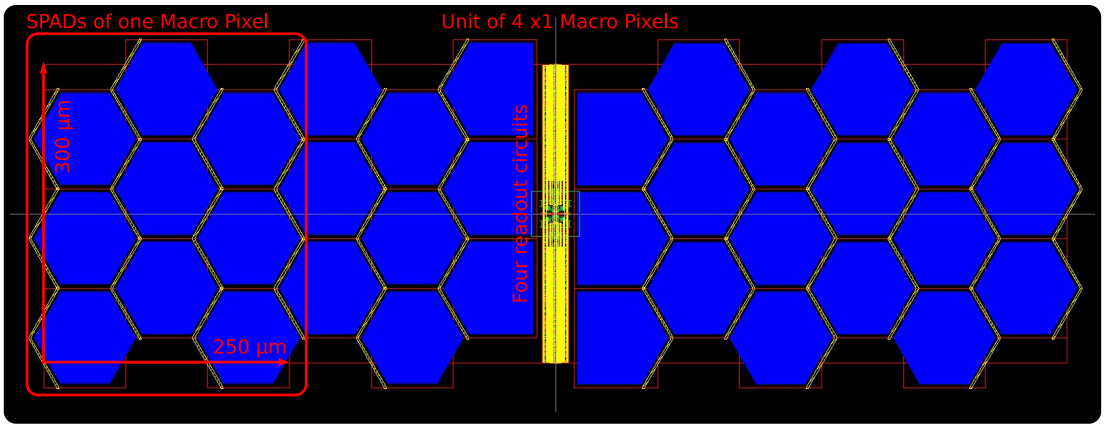

Figure 7.3: Layout of the key structure for a high fill factor: A unit of 4×1 Macro Pixels. Each Macro Pixel posseses nine SPADs of hexagonal shape, depicted in blue, which are read out by one block of readout electronics. The units of electronics are stacked and abutted, forming a joined block visible in yellow in the middle.

is $\sim 80\%$. The effective fill factor, which results from disabling the hot SPADs, is $\sim 70\%$.
Each of the four macro pixels consists of nine SPADs, showed in blue, which are read out by one block of electronics. The nine SPADs have a square arrangement to yield a comparable spacial resolution in x- and y-direction and have the dimension of 250×300 µm^2. Having nine SPADs per Macro Pixels is a good compromise between the pixel density, which is 12 mm^{-2}, and their fill factor.
The conspicuous hexagon shape of the SPADs is chosen to promote an even higher fill factor compared to square SPADs, since the edge area is smaller. A SPAD has the dimension of about 100×80 µm^2, which is close to but slightly above the optimal size of 80×80 µm^2 found at $T = 160$ K (see section 6.9.2). It was favorable for the layout to increase the height of the SPADs so that a single block of electronics fits into the half of the SPAD block height. The decrease in the effective fill factor, however, was $< 1\%$ (see section 6.9.2).
Visible in yellow in figure 7.3 are the four blocks of electronics belonging to the four macro pixels, which form a small channel in the middle of the macro pixel unit. Two electronics of directly neighboring SPAD blocks are stacked above each other. Then the two circuits of the macro pixels from the opposite side, are abutted. With this, the vacant area between SPADs and the electronic is halved compared to a block of two stacked electronics. The minimal distance between neighboring electronics is very small compared to the required spacing between the HV n-well of the SPAD and the electronics. Furthermore, the channel of electronics makes the routing of the $\mathcal{O}(10)$ signals very simple.

7.2.3 Matrix Readout

In an event in the DARWIN experiment a small amount of scintillation light (S1) and short intense light pulse from the charge collection (S2) is emitted (see section 2.4). To resolve both a low-power data-driven readout architecture is chosen. In this architecture the macro pixel stores a photon hit (1 bit) until it is read out. A hit scanner unit searches for the hit pixels in the matrix and, one after the other, extracts their x/y-address. The advantage of this scheme is that for a low flux of photons the readout is only active on demand and the power consumption is low. Simultaneously, to resolve a short intense pulse of light, the pixel matrix acts as a large

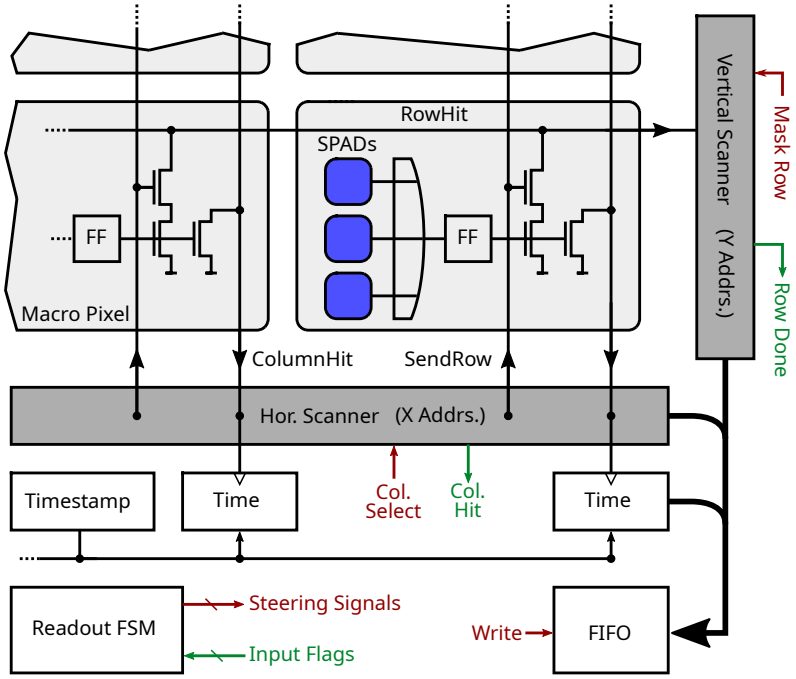

Figure 7.4: Simplified schematic of the macro pixel matrix readout. A horizontal scanner searches for columns with hit macro pixels and then is prompted by the FSM to select one. A vertical scanner extracts the y-address of the hit pixels in the column. For each pixel its x/y-address and column time stamp is written in the FIFO.

data buffer, which is then read out in the long period between subsequent events.
The readout architecture is shown in figure 7.4, hit scanning is done by a scanner in x- and one in y-direction, which are controlled by the readout finite state machine (FSM). When a photon hits a macro pixel the hit flip-flop is set and the Column Hit signal activated. Subsequently, the horizontal scanner is notified that there is a hit in this column and simultaneously the arrival time of the photon is recorded. A 12-bit time-stamp is taken once per column with an accuracy of 10 ns. A column-wise time-stamp is a good compromise between time granularity and consumed space. A pixel-wise time-stamp, for example, compromises the fill factor as further electronics has to be added to the macro pixel.
To extract the address, the readout FSM prompts the horizontal scanner to select a column. The selection follows a pattern, where the column with the highest address is always selected (see [196]). An alternative could have been a scanner comparable to the one implemented for the time-resolved single photon camera (see section 4.4.3). However, it proved to be more complex to control and therefore was dismissed.
The scanner sends the Send Row signal for the most significant column and outputs its address. At the same time, the corresponding Row Hit signals are activated, which are processed by a vertical scanner, also following the search pattern described above. One after the other, it deduces the y-address, which is, in combination with the x-address and the corresponding column time-stamp, written in a FIFO of the depth $\mathcal{O}(16)$ words. The FIFO acts as a buffer between the matrix readout and the further serial data transmission (see next section). After writing the data of one pixel its corresponding Row Hit signal is masked (inside the row scanner) so that the latter can proceed to the next row. When the column is fully read out its pixels are cleared and the next column can be processed. Overall, a single extraction of a macro pixel address consumes $\sim$50 ns at a clock frequency of 100 MHz.

7.2.4 Digital Control

For the digital control block a minimal interface is chosen to emphasis a high fill factor. In addition, the very low event rate of DARWIN of some 10 Hz not only permits reading out the accumulated hit data from the FIFO serial at a moderate transmission frequency of 100 MHz but also building a daisy chain of several arrays. A long shift register is formed, through which the data of the individual arrays propagate.

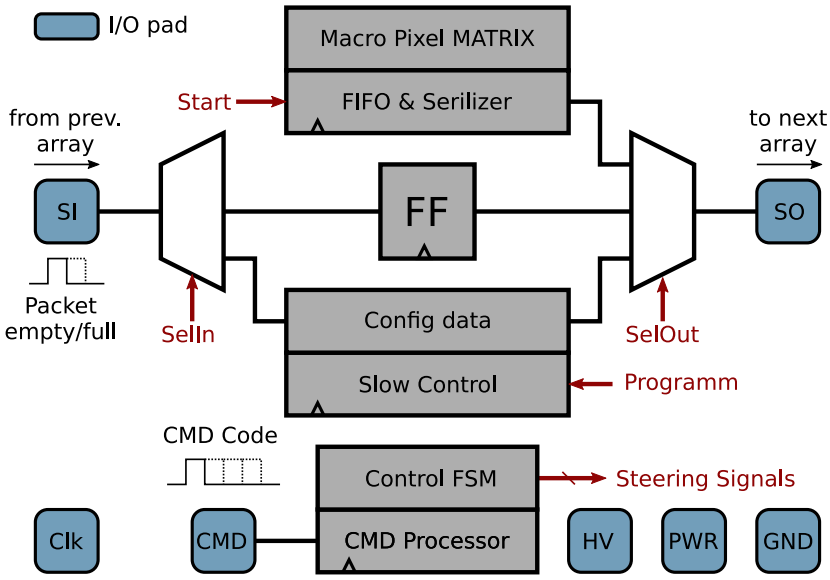

Figure 7.5: Schematic of the digital control block. The minimal interface consists of seven I/O pads. Commands given via the CMD input are processed by the CMD processor and start the control FSM. The latter provides the steering signals for all further blocks. The serializer outputs data, the slow control programs the matrix, and the in/out multiplexers direct the data stream. In idle state data is passed from the serial In (SI) via the flip-flop to the serial output (SO).

The digital control block is shown in figure 7.5. Only four digital I/O pads are needed for the control and readout (blue), while the remaining three are for power, ground and SPAD bias voltage. Furthermore, in a daisy chain of several arrays these four digital signals are sufficient to control the whole chain.
The digital control is steered via the clk (clock) and the CMD input, into which command words are fed in serial. The central blocks to process these commands are the command processor and the Control FSM. The latter samples the CMD input on the positive clock edge. Commands are encoded in a thermometer code and their start is flagged by a positive edge on the CMD input. For example, the sequence ”010” triggers a global chip reset, while ”01110” initiates a hit data transfer. The control FSM reacts to the specific command request by providing the steering signals for the following blocks. The serializer, which outputs the FIFO data serial, the slow control, which programs the pixel matrix and a register, which holds configuration and slow control data.
To prevent arrays from outputting their data simultaneously, data can only be injected into a packet. The start of a packet is flagged by a positive edge on the serial input (SI) followed by a bit, which is ”1” when the packet is full or ”0” when it is empty. For a data transmission the empty bit is toggled and the serializer is activated. The latter first outputs a 5-bit ID, which is unique for each array, followed by the hit data. Full packets, on the contrary, are passed through

the flip-flop to the serial output (SO).
To write or read the configuration register of a specific array in the chain, the configuration data package is preceded by the ID of the array. On a match, the data is written into the configuration register. The slow control for the matrix programming, is adopted form the predecessor array (see section 4.3.6).

7.3 Summary and Discussion

A new Digital SiPM array for the DARWIN Experiment was presented within this last chapter. This has the following properties at liquid Xenon temperatures of $T = 160\,\mathrm{K}$:

- Excellent dark count rate of $0.02\,\mathrm{Hz\,mm^{-2}}$ ($\sim$2 Hz per array).
- High geometrical and effective fill factor of $\sim 80\%$ and $\sim 70\%$.
- High spacial and time resolution of 300 µm and 10 ns.
- Low-power data-driven readout architecture.
- Low number of cables, with $\mathcal{O}(10)$ per module of N arrays.
- Simple mechanics for equipping the detector planes.

Within this last section the array light collection ability with respect to the brought energy range of the DARWIN experiments will be briefly discussed as it is a crucial parameter for DARWIN's energy resolution (see section 2.4).
First of all, the S1 signal will most likely be well resolve with this architecture. For WIMPs and $0\nu\beta\beta$ decay, between 10 and 10^4 photons [4] are emitted isotropically somewhere in the liquid xenon volume. These are then detected on two detector planes each covered with $\sim$ 50000 arrays (see section 2.4). What is more challenging is the S2 signal, where not only the number of emitted photons cover a wide range but more importantly, the emission happens in close vicinity to the upper detector plane (see section 2.4.2). When the collected charge enters the gas phase an isotropic burst of 10^3 photons for a WIMP of $\sim$10 keV, 10^5 for a 100 keV γ-event and up to 10^6 photons for a $0\nu\beta\beta$ decay [32], [71], is emitted. (Numbers are based on measurements with PMTs with a QE of (35%) [6]. For the discussion we assume the same PDE for Digital SiPMs.) For the array in the center of gravity of a WIMP S2 signal, we estimate that it faces a moderate photon flux of $2\,\mathrm{mm^2}$. With a pixel density of $12\,\mathrm{mm^2}$ (see section 7.2.2) WIMPS S2 signals are well resolved. For a γ event, however, the flux increases to 20 $\mathrm{mm^2}$. During the S2 signal most of the detected hits are buffered in the pixels and read out afterwards, so that about 50% of the photons are lost due to subsequent hits in already-triggered pixels. Hence, in this energy range, the array suffers from saturation, which even worsens at higher energies.
However, this problem could be solved by one of the two following approaches: Firstly, as already demonstrated for PMTs, which also suffer from saturation in this energy range, is extrapolation of the photon number from the saturated signal [71]. The photon flux drops with increasing distance to the center of gravity, so that it is well resolved in a certain distance.
The second approach, is increasing the FIFO depth. The FIFO primary purpose is to be a data buffer between the matrix and the serial readout. However, by utilizing the extraction speed of $\sim$50 ns and a large FIFO depth, around the order of the pixel number, many hits can be extracted from the matrix during the event. Hence, the probability is lower that idle pixles have subsequent hits. Nevertheless, enlarging the FIFO consumes space and compromises the fill factor.

In conclusion, the new DARWIN array is quit promising approach for a future light detector for DARWIN, which fulfills many of its constraints. The next steps are to examine the arrays behavior in operation by means of a sophisticated simulation with a realistic photon distribution. This helps to understand the saturation effect and shows the quality of extrapolation with respect to the energy resolution. Furthermore, the minimum size of the FIFO can be evaluated. Choosing the better of both solutions will then lead to a light detector for next and ultimate generation of liquid noble gas dark matter search experiments.

8. Summary and Outlook

This work involved the comprehensive study of digital SiPM arrays at low temperatures to evaluate their suitability as light detectors for liquid noble gas based rare event search experiments, such as the DARWIN experiment. Within this study, a dedicated digital SiPM prototype array was developed for DARWIN, which attempts to fulfill the basic constraints of a light detector for this experiment. These are a low noise ($\sim 0.01\,\mathrm{Hz\,mm^{-2}}$) at cryogenic temperatures, a high VUV light sensitivity ($\lambda \leq 178\,\mathrm{nm}$) and a high amount of active area.
The first low temperature measurements were made with a digital SiPMs array called IDP2, which is a single photon camera and not at all optimized for cryogenic usage. A simple cryogenic setup was implemented in which low temperatures were provided by cooling baths. The temperature profile of the dark count rate was recorded and though the noise level at liquid Xenon temperatures of $T \approx 165\,\mathrm{K}$, was with $35\,\mathrm{Hz\,mm^{-2}}$, too high for DARWIN, it was a promising starting point. Only the low temperature noise contribution, the so-called tunneling noise, had to be reduced. This is usually done by lowering the electric peak field inside the SPAD. Furthermore, two interesting effects were observed: Firstly, photons are emitted from the current drawing part of the readout circuitry impairing the noise at low temperatures. Secondly, the number of hot SPADs, these are SPADs with a particularly high dark count rate which have to be turned off, decreases at low temperatures and effectively increases the active area.
In the next step a dedicated test array for the DARWIN experiment was implemented, for which a low power dissipation and a high fill factor, were targeted. For the latter, a macro pixel test structure was implemented, which was the center piece of the array. It comprised 10 SPADs of different sizes and shapes, which were read out by only one minimal block of electronics. Every SPAD could be switched off with a dedicated masking bit. With the ten different SPAD geometries, the dark count rate could be measured very gradually as a function of the geometry. Especially large SPADs were of most interest since they offered a high fill factor but the noise performance was mostly unknown at the start of this work.
With a fully data-driven readout architecture for the pixel matrix, a low power dissipation ought to be achieved. This prevents excessive heating of the liquid xenon and, at the same time, suppresses the photon emission of the surrounding circuitry.
To tackle the high dark count rate at liquid xenon temperatures our manufacturer, the IMS in Duisburg, agreed to improve the tunneling noise with an optimized SPAD manufacturing process. It was attempted to reduce the electric peak field inside the SPAD by means of three wafer-wise process variations. Moreover, optimizations to make the SPAD directly sensitive to the liquid Xenon scintillation light of $\lambda = 178\,\mathrm{nm}$ were made. However, their manufacture was delayed and so the test of the quantum efficiency has had to be postponed.
For the low temperature characterization of the arrays made with the different process variation, a dedicated cryogenic measurement setup was implemented. It is a highly automated setup, which allows long-term measurements at a very stable temperature in a straightforward way. The noise level of the best process variation was found to be as low as $0.02\,\mathrm{Hz\,mm^{-2}}$, which is in the same order as DARWIN requires. The SPAD noise was not found to be proportional to the size of the SPAD and is independent of the shape. In addition, the number of hot SPADs reduces with temperature, so an optimal SPAD size was found, for which the fill factor is effectively highest when all hot ones are turned off. At $T \approx 160\,\mathrm{K}$ the optimal size is $80 \times 80\ \mu\mathrm{m}^2$, offering an effective fill factor of 75% while the geometrical one is $> 80\%$.
The power consumption of the readout architecture ism, in idle mode, about 1.7 mW and has a

contribution which depends on the signal rate. A linear increase in the power consumption was observed, which has a slope of $15\,\mu W\,kHz^{-1}$. This confirms that a data driven approach is most suitable for DARWIN.
As a final step, an array, with realistic readout architecture for DARWIN, was developed. The emphasis is, again, a high fill factor and a low power dissipation. Furthermore, the aim is it to make it suitable for the S1 and S2 signal of the DARWIN experiment by being capable of processing multiple hits. The central part for a high fill factor is the optimized macro pixel, which is $300 \times 300\ \mu m^2$ in size and is equipped with nine SPADs with a size close to the optimal one at $T \approx 160\,K$. The array offers a single photon time resolution of 10 ns, has a special resolution of about 300 µm and is controllable via a minimalist interface thus reducing the number of cables and requiring, less space, on the array, for bond pads.
Overall, digital SiPM arrays are a very promising candidate for the DARWIN experiment. They offer low noise, a high temporal- and spatial-resolution, and a high fill factor. The mechanics to cover a large area is simple as the number of cables is small, and only a few passive electrical components such as a carrier substrate, are required. With silicon being very radio pure and the low amount of material place in the cold, little radio activity is introduced. Finally, digital SiPMs are suitable for mass production which may result in lower costs. However, the PDE at VUV light is still a problem which urgently needs to be resolved. The next steps, when the delayed arrays arrive, is to measure the PDE with the optimization in the cold. Then the noise has to be re-evaluated, since the required steps to make them sensitive, are extensive interventions in the SPAD structure.
However, an alternative approach to using digital SiPMs for DARWIN directly, without any optimization for the VUV sensitivity, is to install them on the S2 plane. With a window, covered with wavelength-shifting material mounted in front of them, the genuine wavelength of the liquid Xenon scintillation light is shifted into the visible range of light. Here, digital SiPMs are very sensitive. Furthermore, the noise for the S2 signal might be less constrained since the scintillation light from the collected charge is a short and intense pulse of many photons.

List of Own Contributions

- The IDP2, a single photon camera, was characterized at low temperatures with the focus on its noise performance. A simple cryogenic setup was implemented where different cooling baths were utilized to provide various stable low temperatures. The array, its readout electronics and the firmware were already present at the start of this work, so that only the software was written.

- A dedicated DARWIN Test Array was developed. This was done as part of an engineering run in which several new digital SiPM arrays were implemented to expand the use-field of digital SiPMs, i.e., to address other experiments. The work group provided designs for the entire wafer and manufacturing was done exclusively for the group. In addition to the DARWIN Test array, the author implemented a Time-Resolved Single Photon Camera.

- To measure the DARWIN Test array at various low temperatures a more sophisticated cryogenic measurement setup was implemented. A liquid nitrogen cryostat was borrowed from the Work Group of Prof. Dr. Enss and was equipped with a new cabling systems to make it compatible with the array.

- The former readout electronics of the IDP2 were replaced by a more versatile readout board present in the group (PETA Project). To adapt the hardware to the needs of the DARWIN

test array, and make it compatible with the cabling system in the cryostat, a adapter board and a carrier board were designed.

- A new firmware and software, partly based on the existing one for the PETA project, were implemented for the new readout electronics. The aim was it to automate the upcoming large number of characterization measurements, as much as possible.
- In total, eight DARWIN Test arrays originating from four different wafers, manufactured with optimizations of the tunneling noise, were characterized with focus on the noise performance. The data analysis was done offline with a custom-made data framework written in Phython.
- The author's last task was to participate in the development of the new digital SiPM array for the DARWIN Experiment: A first iteration of the macro pixel circuitry and layout was developed, which was later finalized in the group. The concept of the readout was proposed and then implemented in System Verilog, for synthesis.

Bibliography

[1] C. Collaboration, "Search for dark matter and unparticles in events with a Z boson and missing transverse momentum in proton-proton collisions at sqrt(s) = 13 TeV," *Journal of High Energy Physics*, vol. 2017, no. 3, p. 61, Mar. 2017, ISSN: 1029-8479. DOI: 10.1007/JHEP03(2017)061. arXiv: 1701.02042.

[2] T. Fermi-LAT *et al.*, "Searching for Dark Matter Annihilation in Recently Discovered Milky Way Satellites with Fermi-LAT," *The Astrophysical Journal*, vol. 834, no. 2, p. 110, Jan. 2017, ISSN: 1538-4357. DOI: 10.3847/1538-4357/834/2/110. arXiv: 1611.03184.

[3] T. M. Undagoitia and L. Rauch, "Dark matter direct-detection experiments," *Journal of Physics G: Nuclear and Particle Physics*, vol. 43, no. 1, p. 013 001, Jan. 2016, ISSN: 0954-3899, 1361-6471. DOI: 10.1088/0954-3899/43/1/013001. arXiv: 1509.08767.

[4] J. Aalbers *et al.*, "DARWIN: Towards the ultimate dark matter detector," *Journal of Cosmology and Astroparticle Physics*, vol. 2016, no. 11, pp. 017–017, Nov. 2016, ISSN: 1475-7516. DOI: 10.1088/1475-7516/2016/11/017.

[5] E. Aprile *et al.*, "XENON1T dark matter data analysis: Signal reconstruction, calibration, and event selection," *Physical Review D*, vol. 100, no. 5, p. 052 014, Sep. 2019, ISSN: 2470-0010, 2470-0029. DOI: 10.1103/PhysRevD.100.052014.

[6] D. Mayani, "Photomultiplier Tubes for the XENON1T Dark Matter Experiment and Studies on the XENON100 Electromagnetic Background," 2016. DOI: 10.5167/UZH-130030.

[7] D Renker and E Lorenz, "Advances in solid state photon detectors," *Journal of Instrumentation*, vol. 4, no. 04, P04004–P04004, Apr. 2009, ISSN: 1748-0221. DOI: 10.1088/1748-0221/4/04/P04004.

[8] V. C. Rubin and W. K. Ford Jr., "Rotation of the Andromeda Nebula from a Spectroscopic Survey of Emission Regions," *The Astrophysical Journal*, vol. 159, p. 379, Feb. 1970, ISSN: 0004-637X, 1538-4357. DOI: 10.1086/150317.

[9] M. Bartelmann and P. Schneider, "Weak Gravitational Lensing," *Physics Reports*, vol. 340, no. 4-5, pp. 291–472, Jan. 2001, ISSN: 03701573. DOI: 10.1016/S0370-1573(00)00082-X. arXiv: astro-ph/9912508.

[10] M. Bradač *et al.*, "Revealing the properties of dark matter in the merging cluster MACSJ0025.4-1222," *The Astrophysical Journal*, vol. 687, no. 2, pp. 959–967, Nov. 2008, ISSN: 0004-637X, 1538-4357. DOI: 10.1086/591246. arXiv: 0806.2320.

[11] W. A. Dawson *et al.*, "Discovery of a Dissociative Galaxy Cluster Merger with Large Physical Separation," *The Astrophysical Journal*, vol. 747, no. 2, p. L42, Mar. 2012, ISSN: 2041-8205, 2041-8213. DOI: 10.1088/2041-8205/747/2/L42. arXiv: 1110.4391.

[12] G. Bertone *et al.*, "Particle dark matter: Evidence, candidates and constraints," *Physics Reports*, vol. 405, no. 5-6, pp. 279–390, Jan. 2005, ISSN: 03701573. DOI: 10.1016/j.physrep.2004.08.031.

[13] P. Collaboration *et al.*, "Planck 2015 results. XIII. Cosmological parameters," *Astronomy & Astrophysics*, vol. 594, A13, Oct. 2016, ISSN: 0004-6361, 1432-0746. DOI: 10.1051/0004-6361/201525830. arXiv: 1502.01589.

[14] M. Milgrom, "A modification of the Newtonian dynamics as a possible alternative to the hidden mass hypothesis," *The Astrophysical Journal*, vol. 270, p. 365, Jul. 1983, ISSN: 0004-637X, 1538-4357. DOI: 10.1086/161130.

[15] J. E. Felten, "Milgrom's revision of Newton's laws - Dynamical and cosmological consequences," *The Astrophysical Journal*, vol. 286, p. 3, Nov. 1984, ISSN: 0004-637X, 1538-4357. DOI: 10.1086/162569.

[16] C. Alcock *et al.*, "The MACHO Project: Microlensing Results from 5.7 Years of Large Magellanic Cloud Observations," *The Astrophysical Journal*, vol. 542, no. 1, pp. 281–307, Oct. 2000, ISSN: 0004-637X. DOI: 10.1086/309512.

[17] S. D. M. White *et al.*, "Clustering in a neutrino-dominated universe," *The Astrophysical Journal*, vol. 274, pp. L1–L5, Nov. 1983, ISSN: 0004-637X. DOI: 10.1086/184139.

[18] J. L. Feng, "Dark Matter Candidates from Particle Physics and Methods of Detection," *Annual Review of Astronomy and Astrophysics*, vol. 48, no. 1, pp. 495–545, Aug. 2010, ISSN: 0066-4146, 1545-4282. DOI: 10.1146/annurev-astro-082708-101659. arXiv: 1003.0904.

[19] G. G. Raffelt, "Astrophysical Axion Bounds," *arXiv:hep-ph/0611350*, vol. 741, pp. 51–71, 2008. DOI: 10.1007/978-3-540-73518-2_3. arXiv: hep-ph/0611350.

[20] K. N. Abazajian *et al.*, "Light Sterile Neutrinos: A White Paper," *arXiv:1204.5379 [astro-ph, physics:hep-ex, physics:hep-ph, physics:nucl-ex, physics:nucl-th]*, Apr. 2012. arXiv: 1204.5379 [astro-ph, physics:hep-ex, physics:hep-ph, physics:nucl-ex, physics:nucl-th].

[21] G. Gelmini and P. Gondolo, "DM production mechanisms," *arXiv:1009.3690 [astro-ph, physics:hep-ph]*, Sep. 2010. arXiv: 1009.3690 [astro-ph, physics:hep-ph].

[22] G. Jungman *et al.*, "Supersymmetric Dark Matter," *Physics Reports*, vol. 267, no. 5-6, pp. 195–373, Mar. 1996, ISSN: 03701573. DOI: 10.1016/0370-1573(95)00058-5. arXiv: hep-ph/9506380.

[23] "Search for dark matter production associated with bottom quarks with 13.3 fb−1 of pp collisions at $\sqrt{s}$ = 13 tev with the atlas detector at the lhc," Aug. 2016.

[24] L. E. Strigari, "Galactic Searches for Dark Matter," *Physics Reports*, vol. 531, no. 1, pp. 1–88, Oct. 2013, ISSN: 03701573. DOI: 10.1016/j.physrep.2013.05.004. arXiv: 1211.7090.

[25] V. Collaboration *et al.*, "Dark Matter Constraints from a Joint Analysis of Dwarf Spheroidal Galaxy Observations with VERITAS," *Physical Review D*, vol. 95, no. 8, p. 082 001, Apr. 2017, ISSN: 2470-0010, 2470-0029. DOI: 10.1103/PhysRevD.95.082001. arXiv: 1703.04937.

[26] J. I. Read, "The Local Dark Matter Density," *Journal of Physics G: Nuclear and Particle Physics*, vol. 41, no. 6, p. 063 101, Jun. 2014, ISSN: 0954-3899, 1361-6471. DOI: 10.1088/0954-3899/41/6/063101. arXiv: 1404.1938.

[27] J. D. Lewin and P. F. Smith, "Review of mathematics, numerical factors, and corrections for dark matter experiments based on elastic nuclear recoil," *Astroparticle Physics*, vol. 6, no. 1, pp. 87–112, Dec. 1996, ISSN: 0927-6505. DOI: 10.1016/S0927-6505(96)00047-3.

[28] S. M. Griffin *et al.*, "Multi-Channel Direct Detection of Light Dark Matter: Target Comparison," *Physical Review D*, vol. 101, no. 5, p. 055 004, Mar. 2020, ISSN: 2470-0010, 2470-0029. DOI: 10.1103/PhysRevD.101.055004. arXiv: 1910.10716.

[29] J. Billard *et al.*, "Implication of neutrino backgrounds on the reach of next generation dark matter direct detection experiments," *Physical Review D*, vol. 89, no. 2, p. 023 524, Jan. 2014, ISSN: 1550-7998, 1550-2368. DOI: 10.1103/PhysRevD.89.023524. arXiv: 1307.5458.

[30] Particle Data Group *et al.*, "Review of Particle Physics," *Progress of Theoretical and Experimental Physics*, vol. 2020, no. 8, p. 083C01, Aug. 2020, ISSN: 2050-3911. DOI: 10.1093/ptep/ptaa104.

[31] R. Bernabei *et al.*, "Final model independent result of DAMA/LIBRA–phase1," *The European Physical Journal C*, vol. 73, no. 12, p. 2648, Nov. 2013, ISSN: 1434-6052. DOI: 10.1140/epjc/s10052-013-2648-7.

[32] J. Aalbers *et al.*, "A Next-Generation Liquid Xenon Observatory for Dark Matter and Neutrino Physics," *arXiv:2203.02309*, Mar. 2022. arXiv: 2203.02309 [astro-ph, physics:hep-ex, physics:nucl-ex, physics:physics].

[33] SuperCDMS Collaboration *et al.*, "Search for Low-Mass Weakly Interacting Massive Particles with SuperCDMS," *Physical Review Letters*, vol. 112, no. 24, p. 241 302, Jun. 2014. DOI: 10.1103/PhysRevLett.112.241302.

[34] C. Enss, Ed., *Cryogenic Particle Detection* (Topics in Applied Physics v. 99). Berlin ; New York: Springer, 2005, ISBN: 978-3-540-20113-7.

[35] R. Agnese *et al.*, "Projected sensitivity of the SuperCDMS SNOLAB experiment," *Physical Review D*, vol. 95, no. 8, p. 082 002, Apr. 2017, ISSN: 2470-0010, 2470-0029. DOI: 10.1103/PhysRevD.95.082002.

[36] W Rau, "SuperCDMS SNOLAB - Status and Plans," *Journal of Physics: Conference Series*, vol. 1342, no. 1, p. 012 077, Jan. 2020, ISSN: 1742-6588, 1742-6596. DOI: 10.1088/1742-6596/1342/1/012077.

[37] N. J. T. Smith, "The SNOLAB deep underground facility," *The European Physical Journal Plus*, vol. 127, no. 9, p. 108, Sep. 2012, ISSN: 2190-5444. DOI: 10.1140/epjp/i2012-12108-9.

[38] M. Mancuso *et al.*, "Searches for Light Dark Matter with the CRESST-III Experiment," *Journal of Low Temperature Physics*, vol. 199, no. 1, pp. 547–555, Apr. 2020, ISSN: 1573-7357. DOI: 10.1007/s10909-020-02343-3.

[39] A. Aguilar-Arevalo *et al.*, "Results on Low-Mass Weakly Interacting Massive Particles from an 11 kg d Target Exposure of DAMIC at SNOLAB," *Physical Review Letters*, vol. 125, no. 24, p. 241 803, Dec. 2020, ISSN: 0031-9007, 1079-7114. DOI: 10.1103/PhysRevLett.125.241803.

[40] V. Chepel and H. Araújo, "Liquid noble gas detectors for low energy particle physics," *Journal of Instrumentation*, vol. 8, no. 04, R04001–R04001, Apr. 2013. DOI: 10.1088/1748-0221/8/04/r04001.

[41] DEAP Collaboration *et al.*, "Search for dark matter with a 231-day exposure of liquid argon using DEAP-3600 at SNOLAB," *Physical Review D*, vol. 100, no. 2, p. 022 004, Jul. 2019. DOI: 10.1103/PhysRevD.100.022004.

[42] P. A. Amaudruz *et al.*, "Measurement of the scintillation time spectra and pulse-shape discrimination of low-energy β and nuclear recoils in liquid argon with DEAP-1," *Astroparticle Physics*, vol. 85, pp. 1–23, Dec. 2016, ISSN: 0927-6505. DOI: 10.1016/j.astropartphys.2016.09.002.

[43] DarkSide Collaboration *et al.*, "Low-Mass Dark Matter Search with the DarkSide-50 Experiment," *Physical Review Letters*, vol. 121, no. 8, p. 081 307, Aug. 2018. DOI: 10.1103/PhysRevLett.121.081307.

[44] LUX Collaboration *et al.*, "Results from a Search for Dark Matter in the Complete LUX Exposure," *Physical Review Letters*, vol. 118, no. 2, p. 021 303, Jan. 2017. DOI: 10.1103/PhysRevLett.118.021303.

[45] E. Aprile *et al.*, "Dark Matter Search Results from a One Ton-Year Exposure of XENON1T," *Phys. Rev. Lett.*, vol. 121, no. 11, p. 111 302, Sep. 2018. DOI: 10.1103/PhysRevLett.121.111302.

[46] M. Schumann *et al.*, "Dark matter sensitivity of multi-ton liquid xenon detectors," *Journal of Cosmology and Astroparticle Physics*, vol. 2015, no. 10, pp. 016–016, Oct. 2015, ISSN: 1475-7516. DOI: 10.1088/1475-7516/2015/10/016.

[47] XENON Collaboration *et al.*, "The XENON1T dark matter experiment," *The European Physical Journal C*, vol. 77, no. 12, p. 881, Dec. 2017, ISSN: 1434-6044, 1434-6052. DOI: 10.1140/epjc/s10052-017-5326-3.

[48] L. Baudis *et al.*, "Neutrino physics with multi-ton scale liquid xenon detectors," *Journal of Cosmology and Astroparticle Physics*, vol. 2014, no. 01, pp. 044–044, Jan. 2014, ISSN: 1475-7516. DOI: 10.1088/1475-7516/2014/01/044. arXiv: 1309.7024.

[49] D.-M. Mei and A. Hime, "Muon-Induced Background Study for Underground Laboratories," *Physical Review D*, vol. 73, no. 5, p. 053 004, Mar. 2006, ISSN: 1550-7998, 1550-2368. DOI: 10.1103/PhysRevD.73.053004. arXiv: astro-ph/0512125.

[50] Y. Zhang *et al.*, "Corrected Values for Boiling Points and Enthalpies of Vaporization of Elements in Handbooks," *Journal of Chemical & Engineering Data*, vol. 56, no. 2, pp. 328–337, Feb. 2011, ISSN: 0021-9568, 1520-5134. DOI: 10.1021/je1011086.

[51] X. Collaboration *et al.*, "Removing krypton from xenon by cryogenic distillation to the ppq level," *The European Physical Journal C*, vol. 77, no. 5, p. 275, May 2017, ISSN: 1434-6044, 1434-6052. DOI: 10.1140/epjc/s10052-017-4757-1. arXiv: 1612.04284.

[52] P. A Breur, "Backgrounds in XENON1T," Ph.D. dissertation, 2019, ISBN: 9789463234757.

[53] G. Plante, "The XENON100 Dark Matter Experiment: Design, Construction, Calibration and 2010 Search Results with Improved Measurement of the Scintillation Response of Liquid Xenon to Low-Energy Nuclear Recoils," Ph.D. dissertation, Columbia University, 2012. DOI: 10.7916/D89P37MT.

[54] EXO Collaboration *et al.*, "Improved measurement of the $2\nu\beta\beta$ half-life of ^{136}xe with the exo-200 detector," *Physical Review C*, vol. 89, no. 1, p. 015 502, Jan. 2014. DOI: 10.1103/PhysRevC.89.015502.

[55] E. Aprile *et al.*, "Simultaneous Measurement of Ionization and Scintillation from Nuclear Recoils in Liquid Xenon for a Dark Matter Experiment," *Physical Review Letters*, vol. 97, no. 8, p. 081 302, Aug. 2006. DOI: 10.1103/PhysRevLett.97.081302.

[56] T. Doke, "Fundamental properties of liquid argon, krypton and xenon as radiation detector media," in *Experimental Techniques in High-Energy Nuclear and Particle Physics*, WORLD SCIENTIFIC, Nov. 1991, pp. 537–577, ISBN: 978-981-02-0867-7. DOI: 10.1142/9789814355988_0010.

[57] J. Jortner *et al.*, "Localized Excitations in Condensed Ne, Ar, Kr, and Xe," *The Journal of Chemical Physics*, vol. 42, no. 12, pp. 4250–4253, Jun. 1965, ISSN: 0021-9606, 1089-7690. DOI: 10.1063/1.1695927.

[58] S. Kubota *et al.*, "Recombination luminescence in liquid argon and in liquid xenon," *Physical Review B*, vol. 17, no. 6, pp. 2762–2765, Mar. 1978. DOI: 10.1103/PhysRevB.17.2762.

[59] I. T. Steinberger and U. Asaf, "Band-Structure Parameters of Solid and Liquid Xenon," *Physical Review B*, vol. 8, no. 2, pp. 914–918, Jul. 1973, ISSN: 0556-2805. DOI: 10.1103/PhysRevB.8.914.

[60] L. Althueser *et al.*, "GPU-based optical simulation of the DARWIN detector," *arXiv:2203.14354 [astro-ph, physics:physics]*, Mar. 2022. arXiv: 2203.14354 [astro-ph, physics:physics].

[61] T. Takahashi *et al.*, "Average energy expended per ion pair in liquid xenon," *Physical Review A*, vol. 12, no. 5, pp. 1771–1775, Nov. 1975. DOI: 10.1103/PhysRevA.12.1771.

[62] M. W. Goodman and E. Witten, "Detectability of certain dark-matter candidates," *Physical Review D*, vol. 31, no. 12, pp. 3059–3063, Jun. 1985. DOI: 10.1103/PhysRevD.31.3059.

[63] M. Yamashita *et al.*, "Scintillation response of liquid Xe surrounded by PTFE reflector for gamma rays," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 535, no. 3, pp. 692–698, Dec. 2004, ISSN: 0168-9002. DOI: 10.1016/j.nima.2004.06.168.

[64] J. Wulf, "Direct dark matter search with XENON1T and developments for multi-ton liquid xenon detectors," Ph.D. dissertation, Zurich U., 2018.

[65] E. Aprile *et al.*, "Observation and applications of single-electron charge signals in the XENON100 experiment," *Journal of Physics G: Nuclear and Particle Physics*, vol. 41, no. 3, p. 035 201, Mar. 2014, ISSN: 0954-3899, 1361-6471. DOI: 10.1088/0954-3899/41/3/035201. arXiv: 1311.1088.

[66] E. Aprile *et al.*, "Proportional light in a dual-phase xenon chamber," *IEEE Transactions on Nuclear Science*, vol. 51, no. 5, pp. 1986–1990, Oct. 2004, ISSN: 1558-1578. DOI: 10.1109/TNS.2004.832690.

[67] G. Plante *et al.*, "New measurement of the scintillation efficiency of low-energy nuclear recoils in liquid xenon," *Physical Review C*, vol. 84, no. 4, p. 045 805, Oct. 2011. DOI: 10.1103/PhysRevC.84.045805.

[68] S. Seltzer, *XCOM-Photon Cross Sections Database, NIST Standard Reference Database 8*, 1987. DOI: 10.18434/T48G6X.

[69] P. Barrow *et al.*, "Qualification tests of the R11410-21 photomultiplier tubes for the XENON1T detector," *Journal of Instrumentation*, vol. 12, no. 01, P01024–P01024, Jan. 2017, ISSN: 1748-0221. DOI: 10.1088/1748-0221/12/01/P01024.

[70] F. L. Rauch, "From Final Dark Matter Results and Background Shape Uncertainties in XENON100 to First Light in XENON1T," 2017. DOI: 10.11588/HEIDOK.00023239.

[71] E. Aprile *et al.*, "Energy resolution and linearity of XENON1T in the MeV energy range," *European Physical Journal C – Particles & Fields*, vol. 80, no. 8, pp. 1–9, Aug. 2020, ISSN: 14346044. DOI: 10.1140/epjc/s10052-020-8284-0.

[72] A. Gola *et al.*, "NUV-Sensitive Silicon Photomultiplier Technologies Developed at Fondazione Bruno Kessler," *Sensors*, vol. 19, no. 2, p. 308, Jan. 2019. DOI: 10.3390/s19020308.

[73] C. E. Aalseth *et al.*, "DarkSide-20k: A 20 tonne two-phase LAr TPC for direct dark matter detection at LNGS," *The European Physical Journal Plus*, vol. 133, no. 3, p. 131, Mar. 2018, ISSN: 2190-5444. DOI: 10.1140/epjp/i2018-11973-4.

[74] V. M. Gehman *et al.*, "Fluorescence efficiency and visible re-emission spectrum of tetraphenyl butadiene films at extreme ultraviolet wavelengths," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 654, no. 1, pp. 116–121, Oct. 2011, ISSN: 0168-9002. DOI: 10.1016/j.nima.2011.06.088.

[75] M. Capasso *et al.*, "FBK VUV-sensitive Silicon Photomultipliers for cryogenic temperatures," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 982, p. 164 478, Dec. 2020, ISSN: 0168-9002. DOI: 10.1016/j.nima.2020.164478.

[76] G. Gallina *et al.*, "Characterization of the Hamamatsu VUV4 MPPCs for nEXO," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 940, pp. 371–379, Oct. 2019, ISSN: 0168-9002. DOI: 10.1016/j.nima.2019.05.096.

[77] V. D'Andrea *et al.*, "The ABALONE Photosensor," *Journal of Instrumentation*, vol. 17, no. 01, p. C01038, Jan. 2022, ISSN: 1748-0221. DOI: 10.1088/1748-0221/17/01/C01038. arXiv: 2111.02924.

[78] D. Ferenc *et al.*, "The Novel ABALONE Photosensor Technology: 4-Year Long Tests of Vacuum Integrity, Internal Pumping and Afterpulsing," *arXiv:1703.04546 [astro-ph, physics:hep-ex, physics:physics]*, May 2017. arXiv: 1703.04546 [astro-ph, physics:hep-ex, physics:physics].

[79] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, N.J: Wiley-Interscience, 2007, ISBN: 978-0-471-14323-9.

[80] C. Kittel, *Introduction to Solid State Physics*, Global edition, [9th edition]. Hoboken, NJ: Wiley, 2018, ISBN: 978-1-119-45416-8.

[81] A. Spinelli and A. Lacaita, "Physics and numerical simulation of single photon avalanche diodes," *IEEE Transactions on Electron Devices*, vol. 44, no. 11, pp. 1931–1943, Nov./1997, ISSN: 00189383. DOI: 10.1109/16.641363.

[82] P. Seitz and A. J. P. Theuwissen, Eds., *Single-Photon Imaging* (Springer Series in Optical Sciences 160). Heidelberg ; New York: Springer, 2011, ISBN: 978-3-642-18442-0.

[83] G. Collazuol *et al.*, "Studies of silicon photomultipliers at cryogenic temperatures," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 628, no. 1, pp. 389–392, Feb. 2011, ISSN: 01689002. DOI: 10.1016/j.nima.2010.07.008.

[84] S. Cova *et al.*, "Avalanche photodiodes and quenching circuits for single-photon detection," *Applied Optics*, vol. 35, no. 12, p. 1956, Apr. 1996, ISSN: 0003-6935, 1539-4522. DOI: 10.1364/AO.35.001956.

[85] S. Sze and G. Gibbons, "Effect of junction curvature on breakdown voltage in semiconductors," *Solid-State Electronics*, vol. 9, no. 9, pp. 831–845, Sep. 1966, ISSN: 00381101. DOI: 10.1016/0038-1101(66)90033-5.

[86] A. Goetzberger *et al.*, "Avalanche Effects in Silicon p—n Junctions. II. Structurally Perfect Junctions," *Journal of Applied Physics*, vol. 34, no. 6, pp. 1591–1600, Jun. 1963, ISSN: 0021-8979, 1089-7550. DOI: 10.1063/1.1702640.

[87] L. K. Anderson *et al.*, "MICROWAVE PHOTODIODES EXHIBITING MICROPLASMA-FREE CARRIER MULTIPLICATION," *Applied Physics Letters*, vol. 6, no. 4, pp. 62–64, Feb. 1965, ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.1754166.

[88] A. Vilà *et al.*, "Geiger-Mode Avalanche Photodiodes in Standard CMOS Technologies," in *Photodetectors*, S. Gateva, Ed., Rijeka: IntechOpen, 2012, ch. 9. DOI: 10.5772/37162.

[89] E. Charbon, "Single-photon imaging in complementary metal oxide semiconductor processes," *Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences*, vol. 372, no. 2012, p. 20 130 100, Mar. 2014, ISSN: 1364-503X, 1471-2962. DOI: 10.1098/rsta.2013.0100.

[90] F. Villa *et al.*, "CMOS SPADs with up to 500 Mm diameter and 55% detection efficiency at 420 nm," *Journal of Modern Optics*, vol. 61, no. 2, pp. 102–115, Jan. 2014, ISSN: 0950-0340, 1362-3044. DOI: 10.1080/09500340.2013.864425.

[91] C. Niclass *et al.*, "Design and characterization of a CMOS 3-D image sensor based on single photon avalanche diodes," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1847–1854, Sep. 2005, ISSN: 0018-9200. DOI: 10.1109/JSSC.2005.848173.

[92] C. Piemonte, "A new Silicon Photomultiplier structure for blue light detection," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, New Developments in Radiation Detectors, vol. 568, no. 1, pp. 224–232, Nov. 2006, ISSN: 0168-9002. DOI: 10.1016/j.nima.2006.07.018.

[93] R. H. Haitz, "Mechanisms Contributing to the Noise Pulse Rate of Avalanche Diodes," *Journal of Applied Physics*, vol. 36, no. 10, pp. 3123–3131, 1965. DOI: 10.1063/1.1702936.

[94] D. Stoppa *et al.*, "Single-Photon Avalanche Diode CMOS Sensor for Time-Resolved Fluorescence Measurements," *IEEE Sensors Journal*, vol. 9, no. 9, pp. 1084–1090, Sep. 2009, ISSN: 1558-1748. DOI: 10.1109/JSEN.2009.2025581.

[95] S. Tisa *et al.*, "Fully-integrated CMOS single photon counter," *Optics Express*, vol. 15, no. 6, pp. 2873–2887, Mar. 2007, ISSN: 1094-4087. DOI: 10.1364/OE.15.002873.

[96] S. L. Miller, "Avalanche Breakdown in Germanium," *Physical Review*, vol. 99, no. 4, pp. 1234–1241, Aug. 1955. DOI: 10.1103/PhysRev.99.1234.

[97] W. Maes *et al.*, "Impact ionization in silicon: A review and update," *Solid-State Electronics*, vol. 33, no. 6, pp. 705–718, Jun. 1990, ISSN: 0038-1101. DOI: 10.1016/0038-1101(90)90183-F.

[98] E. Cartier *et al.*, "Impact ionization in silicon," *Applied Physics Letters*, vol. 62, no. 25, pp. 3339–3341, Jun. 1993, ISSN: 0003-6951. DOI: 10.1063/1.109064.

[99] C. Groves *et al.*, "The effect of ionization threshold softness on the temperature dependence of the impact ionization coefficient," *Semiconductor Science and Technology*, vol. 18, no. 7, pp. 689–692, Jun. 2003, ISSN: 0268-1242. DOI: 10.1088/0268-1242/18/7/316.

[100] N. Serra *et al.*, "Experimental and TCAD Study of Breakdown Voltage Temperature Behavior in $n+/p$ SiPMs," *IEEE Transactions on Nuclear Science*, vol. 58, no. 3, pp. 1233–1240, Jun. 2011, ISSN: 1558-1578. DOI: 10.1109/TNS.2011.2123919.

[101] F. Acerbi and S. Gundacker, "Understanding and simulating SiPMs," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, Silicon Photomultipliers: Technology, Characterisation and Applications, vol. 926, pp. 16–35, May 2019, ISSN: 0168-9002. DOI: 10.1016/j.nima.2018.11.118.

[102] C. R. Crowell and S. M. Sze, "TEMPERATURE DEPENDENCE OF AVALANCHE MULTIPLICATION IN SEMICONDUCTORS," *Applied Physics Letters*, vol. 9, no. 6, pp. 242–244, Sep. 1966, ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.1754731.

[103] N. Serra *et al.*, "Characterization of new FBK SiPM technology for visible light detection," *Journal of Instrumentation*, vol. 8, no. 03, P03019, Mar. 2013, ISSN: 1748-0221. DOI: 10.1088/1748-0221/8/03/P03019.

[104] C. Piemonte and A. Gola, "Overview on the main parameters and technology of modern Silicon Photomultipliers," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, Silicon Photomultipliers: Technology, Characterisation and Applications, vol. 926, pp. 2–15, May 2019, ISSN: 0168-9002. DOI: 10.1016/j.nima.2018.11.119.

[105] F. Zappa *et al.*, "Principles and features of single-photon avalanche diode arrays," *Sensors and Actuators A: Physical*, vol. 140, no. 1, pp. 103–112, Oct. 2007, ISSN: 09244247. DOI: 10.1016/j.sna.2007.06.021.

[106] N Otte, "The Silicon Photomultiplier - A new device for High Energy Physics, Astroparticle Physics, Industrial and Medical Applications," p. 9, 2006.

[107] A. Rochas, "Single photon avalanche diodes in CMOS technology," 2005. DOI: 10.5075/EPFL-THESIS-2814.

[108] R. McIntyre, "On the avalanche initiation probability of avalanche diodes above the breakdown voltage," *IEEE Transactions on Electron Devices*, vol. 20, no. 7, pp. 637–641, Jul. 1973, ISSN: 0018-9383. DOI: 10.1109/T-ED.1973.17715.

[109] W. Oldham *et al.*, "Triggering phenomena in avalanche diodes," *IEEE Transactions on Electron Devices*, vol. 19, no. 9, pp. 1056–1060, Sep. 1972, ISSN: 1557-9646. DOI: 10.1109/T-ED.1972.17544.

[110] I. Rech *et al.*, "Operation of silicon single photon avalanche diodes at cryogenic temperature," *Review of Scientific Instruments*, vol. 78, no. 6, p. 063 105, Jun. 2007, ISSN: 0034-6748. DOI: 10.1063/1.2743167.

[111] D. A. Neamen, *Semiconductor Physics and Devices: Basic Principles*, 2nd ed. Chicago: Irwin, 1997, ISBN: 978-0-256-20869-6.

[112] J. S. Blakemore, *Semiconductor Statistics*. New York: Dover, 1987, ISBN: 978-0-486-65362-4.

[113] W. Shockley and W. T. Read, "Statistics of the Recombinations of Holes and Electrons," *Phys. Rev.*, vol. 87, no. 5, pp. 835–842, Sep. 1952. DOI: 10.1103/PhysRev.87.835.

[114] R. N. Hall, "Electron-Hole Recombination in Germanium," *Phys. Rev.*, vol. 87, no. 2, pp. 387–387, Jul. 1952. DOI: 10.1103/PhysRev.87.387.

[115] G. Lutz, *Semiconductor Radiation Detectors*. Berlin, Heidelberg: Springer Berlin Heidelberg, 2007, ISBN: 978-3-540-71678-5 978-3-540-71679-2. DOI: 10.1007/978-3-540-71679-2.

[116] D. McGrath *et al.*, "Dark Current Limiting Mechanisms in CMOS Image Sensors," *Electronic Imaging*, vol. 30, no. 11, pp. 354–1–354–8, Jan. 2018, ISSN: 2470-1173. DOI: 10.2352/ISSN.2470-1173.2018.11.IMSE-354.

[117] E. O. Kane, "Theory of Tunneling," *Journal of Applied Physics*, vol. 32, no. 1, pp. 83–91, Jan. 1961, ISSN: 0021-8979. DOI: 10.1063/1.1735965.

[118] W. Bludau *et al.*, "Temperature dependence of the band gap of silicon," *Journal of Applied Physics*, vol. 45, no. 4, pp. 1846–1848, Apr. 1974, ISSN: 0021-8979. DOI: 10.1063/1.1663501.

[119] L. Esaki, "New Phenomenon in Narrow Germanium $p\ensuremath{-}n$ Junctions," *Physical Review*, vol. 109, no. 2, pp. 603–604, Jan. 1958. DOI: 10.1103/PhysRev.109.603.

[120] A. Schenk, "Rigorous theory and simplified model of the band-to-band tunneling in silicon," *Solid-State Electronics*, vol. 36, no. 1, pp. 19–34, Jan. 1993, ISSN: 0038-1101. DOI: 10.1016/0038-1101(93)90065-X.

[121] *Tunneling Phenomena in Solids Lectures presented at the 1967/NATO Advanced Study Institute at Risodbenddbend, Denmark*. 1969, ISBN: 978-1-4684-1752-4.

[122] G. A. M. Hurkx *et al.*, "A new recombination model for device simulation including tunneling," *IEEE Transactions on Electron Devices*, vol. 39, no. 2, pp. 331–338, Feb. 1992, ISSN: 1557-9646. DOI: 10.1109/16.121690.

[123] E. A. G. Webster and R. K. Henderson, "A TCAD and Spectroscopy Study of Dark Count Mechanisms in Single-Photon Avalanche Diodes," *IEEE Transactions on Electron Devices*, vol. 60, no. 12, pp. 4014–4019, Dec. 2013, ISSN: 1557-9646. DOI: 10.1109/TED.2013.2285163.

[124] M. Ghioni *et al.*, "Large-area low-jitter silicon single photon avalanche diodes," in *Integrated Optoelectronic Devices 2008*, R. Sudharsanan and C. Jelen, Eds., San Jose, CA, Feb. 2008, p. 69001D. DOI: 10.1117/12.761578.

[125] J. Frenkel, "On Pre-Breakdown Phenomena in Insulators and Electronic Semi-Conductors," *Physical Review*, vol. 54, no. 8, pp. 647–648, Oct. 1938. DOI: 10.1103/PhysRev.54.647.

[126] G. Vincent *et al.*, "Electric field effect on the thermal emission of traps in semiconductor junctions," *Journal of Applied Physics*, vol. 50, no. 8, pp. 5484–5487, Aug. 1979, ISSN: 0021-8979. DOI: 10.1063/1.326601.

[127] G. Hurkx *et al.*, "A new recombination model describing heavy-doping effects and low-temperature behaviour," in *International Technical Digest on Electron Devices Meeting*, Dec. 1989, pp. 307–310. DOI: 10.1109/IEDM.1989.74285.

[128] K. Ozaki *et al.*, "Characterization of New Silicon Photomultipliers with Low Dark Noise at Low Temperature," *Journal of Instrumentation*, vol. 16, no. 03, P03014, Mar. 2021, ISSN: 1748-0221. DOI: 10.1088/1748-0221/16/03/P03014. arXiv: 2007.13537.

[129] C. Piemonte *et al.*, "Performance of NUV-HD Silicon Photomultiplier Technology," *IEEE Transactions on Electron Devices*, vol. 63, no. 3, pp. 1111–1116, Mar. 2016, ISSN: 1557-9646. DOI: 10.1109/TED.2016.2516641.

[130] D. P. Palubiak and M. J. Deen, "CMOS SPADs: Design Issues and Research Challenges for Detectors, Circuits, and Arrays," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 20, no. 6, pp. 409–426, Nov. 2014, ISSN: 1558-4542. DOI: 10.1109/JSTQE.2014.2344034.

[131] M. Zarghami, "Characterization, calibration, and optimization of time-resolved CMOS single-photon avalanche diode image sensor," Ph.D. dissertation, Università degli studi di Trento, Trento, Sep. 2020.

[132] F. Acerbi *et al.*, "Cryogenic Characterization of FBK HD Near-UV Sensitive SiPMs," *IEEE Transactions on Electron Devices*, vol. 64, no. 2, pp. 521–526, Feb. 2017, ISSN: 1557-9646. DOI: 10.1109/TED.2016.2641586.

[133] T. Frach *et al.*, "The digital silicon photomultiplier — Principle of operation and intrinsic detector performance," in *2009 IEEE Nuclear Science Symposium Conference Record (NSS/MIC)*, Oct. 2009, pp. 1959–1965. DOI: 10.1109/NSSMIC.2009.5402143.

[134] A. C. Ulku *et al.*, "A 512 × 512 SPAD Image Sensor With Integrated Gating for Widefield FLIM," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 25, no. 1, pp. 1–12, Jan. 2019, ISSN: 1558-4542. DOI: 10.1109/JSTQE.2018.2867439.

[135] G. D. Watkins, "Defects in Irradiated Silicon: Electron Paramagnetic Resonance and Electron-Nuclear Double Resonance of the Si-," *Physical Review*, vol. 134, no. 5A, A1359–A1377, 1964. DOI: 10.1103/PhysRev.134.A1359.

[136] M. J. Madou, *Fundamentals of Microfabrication: The Science of Miniaturization*, 2nd ed. Boca Raton: CRC Press, 2002, ISBN: 978-0-8493-0826-0.

[137] H. Pettersson *et al.*, "Electrical and optical properties of molybdenum and tungsten related defects in silicon," *Semiconductor Science and Technology*, vol. 6, no. 4, pp. 237–242, Apr. 1991, ISSN: 0268-1242. DOI: 10.1088/0268-1242/6/4/002.

[138] A. Butcher *et al.*, "A method for characterizing after-pulsing and dark noise of PMTs and SiPMs," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 875, pp. 87–91, Dec. 2017, ISSN: 0168-9002. DOI: 10.1016/j.nima.2017.08.035.

[139] S. Cova *et al.*, "Trapping phenomena in avalanche photodiodes on nanosecond scale," *IEEE Electron Device Letters*, vol. 12, no. 12, pp. 685–687, Dec. 1991, ISSN: 1558-0563. DOI: 10.1109/55.116955.

[140] A. Jamil *et al.*, "VUV-Sensitive Silicon Photomultipliers for Xenon Scintillation Light Detection in nEXO," *IEEE Transactions on Nuclear Science*, vol. 65, no. 11, pp. 2823–2833, Nov. 2018, ISSN: 1558-1578. DOI: 10.1109/TNS.2018.2875668.

[141] S. Jahromi and J. Kostamovaara, "Timing and probability of crosstalk in a dense CMOS SPAD array in pulsed TOF applications," *Optics Express*, vol. 26, no. 16, pp. 20 622–20 632, Aug. 2018, ISSN: 1094-4087. DOI: 10.1364/OE.26.020622.

[142] J. Bude *et al.*, "Hot-carrier luminescence in Si," *Physical Review B*, vol. 45, no. 11, pp. 5848–5856, Mar. 1992. DOI: 10.1103/PhysRevB.45.5848.

[143] N. Akil *et al.*, "A multimechanism model for photon generation by silicon junctions in avalanche breakdown," *IEEE Transactions on Electron Devices*, vol. 46, no. 5, pp. 1022–1028, May 1999, ISSN: 1557-9646. DOI: 10.1109/16.760412.

[144] N. Akil *et al.*, "Photon generation by silicon diodes in avalanche breakdown," *Applied Physics Letters*, vol. 73, no. 7, pp. 871–872, Aug. 1998, ISSN: 0003-6951. DOI: 10.1063/1.121971.

[145] A. Lacaita *et al.*, "On the bremsstrahlung origin of hot-carrier-induced photons in silicon devices," *IEEE Transactions on Electron Devices*, vol. 40, no. 3, pp. 577–582, Mar. 1993, ISSN: 1557-9646. DOI: 10.1109/16.199363.

[146] A. Nepomuk Otte, "On the efficiency of photon emission during electrical breakdown in silicon," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, New Developments In Photodetection NDIP08, vol. 610, no. 1, pp. 105–109, Oct. 2009, ISSN: 0168-9002. DOI: 10.1016/j.nima.2009.05.085.

[147] I. Rech *et al.*, "Optical crosstalk in single photon avalanche diode arrays: A new complete model," *Optics Express*, vol. 16, no. 12, pp. 8381–8394, Jun. 2008, ISSN: 1094-4087. DOI: 10.1364/OE.16.008381.

[148] W. Kindt *et al.*, "Optical Cross Talk in Geiger Mode Avalanche Photodiode Arrays: Modeling, Prevention and Measurement," in *28th European Solid-State Device Research Conference*, Sep. 1998, pp. 192–195.

[149] P. A. Childs *et al.*, "Evidence of optical generation of minority carriers from saturated MOS transistors," *Solid-State Electronics*, vol. 26, no. 7, pp. 685–688, Jul. 1983, ISSN: 0038-1101. DOI: 10.1016/0038-1101(83)90025-4.

[150] S. Tam and C. Hu, "Hot-electron-induced photon and photocarrier generation in Silicon MOSFET's," *IEEE Transactions on Electron Devices*, vol. 31, no. 9, pp. 1264–1273, Sep. 1984, ISSN: 1557-9646. DOI: 10.1109/T-ED.1984.21698.

[151] T. Gandhi, Ed., *Microelectronics Failure Analysis Desk Reference*, Seventh edition. Materials Park: ASM International, 2019, ISBN: 978-1-62708-245-7.

[152] J. C. Tsang *et al.*, "Picosecond imaging circuit analysis," *IBM Journal of Research and Development*, vol. 44, no. 4, pp. 583–603, Jul. 2000, ISSN: 0018-8646. DOI: 10.1147/rd.444.0583.

[153] G. Deboy and J. Kolzer, "Fundamentals of light emission from silicon devices," *Semiconductor Science and Technology*, vol. 9, no. 5, pp. 1017–1032, May 1994, ISSN: 0268-1242. DOI: 10.1088/0268-1242/9/5/004.

[154] J. Kölzer *et al.*, "Quantitative emission microscopy," *Journal of Applied Physics*, vol. 71, no. 11, R23–R41, Jun. 1992, ISSN: 0021-8979. DOI: 10.1063/1.350466.

[155] M. Lanzoni *et al.*, "Hot-electron-induced photon energies in n-channel MOSFETs operating at 77 and 300 K," *IEEE Electron Device Letters*, vol. 10, no. 5, pp. 173–176, May 1989, ISSN: 1558-0563. DOI: 10.1109/55.31711.

[156] I. Duisburg, "SPAD performance," p. 1, 2021.

[157] I. Duisburg, "SPAD-Based Sensors for Spectroscopy Applications," p. 2, 2021.

[158] P. P. Calò *et al.*, "SiPM readout electronics," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, Silicon Photomultipliers: Technology, Characterisation and Applications, vol. 926, pp. 57–68, May 2019, ISSN: 0168-9002. DOI: 10.1016/j.nima.2018.09.030.

[159] M. D'Incecco *et al.*, "Development of a Very Low-Noise Cryogenic Preamplifier for Large-Area SiPM Devices," *IEEE Transactions on Nuclear Science*, vol. 65, no. 4, pp. 1005–1011, Apr. 2018, ISSN: 1558-1578. DOI: 10.1109/TNS.2018.2799325.

[160] C. Degenhardt *et al.*, "Performance evaluation of a prototype Positron Emission Tomography scanner using Digital Photon Counters (DPC)," in *2012 IEEE Nuclear Science Symposium and Medical Imaging Conference Record (NSS/MIC)*, Oct. 2012, pp. 2820–2824. DOI: 10.1109/NSSMIC.2012.6551643.

[161] D. Bronzi *et al.*, "SPAD Figures of Merit for Photon-Counting, Photon-Timing, and Imaging Applications: A Review," *IEEE Sensors Journal*, vol. 16, no. 1, pp. 3–12, Jan. 2016, ISSN: 1558-1748. DOI: 10.1109/JSEN.2015.2483565.

[162] S. Gundacker and A. Heering, "The silicon photomultiplier: Fundamentals and applications of a modern solid-state photon detector," *Physics in Medicine & Biology*, vol. 65, no. 17, 17TR01, Aug. 2020, ISSN: 0031-9155. DOI: 10.1088/1361-6560/ab7b2d.

[163] I. Sacco, "Development of highly integrated PET/MR detector modules," 2016. DOI: 10.11588/HEIDOK.00022239.

[164] W. Becker, *Advanced Time-Correlated Single Photon Counting Applications*. Cham: Springer International Publishing, 2015, ISBN: 978-3-319-14929-5 978-3-319-14930-1 978-3-319-14928-8 978-3-319-35842-0.

[165] S. Herbert *et al.*, "Quantum Efficiency Determination of a Novel CMOS Design for Fast Imaging Applications in the Extreme Ultraviolet," *IEEE Transactions on Electron Devices*, vol. 59, no. 3, pp. 846–849, Mar. 2012, ISSN: 1557-9646. DOI: 10.1109/TED.2011.2177838.

[166] L. K. Nanver *et al.*, "Robust UV/VUV/EUV PureB Photodiode Detector Technology With High CMOS Compatibility," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 20, no. 6, pp. 306–316, Nov. 2014, ISSN: 1077-260X, 1558-4542. DOI: 10.1109/JSTQE.2014.2319582.

[167] C. Niclass *et al.*, "A 100-m Range 10-Frame/s 340 $\,\times\, $96-Pixel Time-of-Flight Depth Sensor in 0.18-$\mu\hboxm$ CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 2, pp. 559–572, Feb. 2013, ISSN: 1558-173X. DOI: 10.1109/JSSC.2012.2227607.

[168] D. Bronzi *et al.*, "Low-noise and large-area CMOS SPADs with timing response free from slow tails," in *2012 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, Bordeaux, France: IEEE, Sep. 2012, pp. 230–233, ISBN: 978-1-4673-1708-5 978-1-4673-1707-8 978-1-4673-1706-1. DOI: 10.1109/ESSDERC.2012.6343375.

[169] I. Fleck *et al.*, *Handbook of Particle Detection and Imaging*. Cham: Springer International Publishing, 2020, ISBN: 978-3-319-47999-6.

[170] M. Beer, "SPAD-basierte Sensoren für die laufzeitbasierte Distanzmessung bei hoher Hintergrundlichtintensität," Ph.D. dissertation, Dec. 2018.

[171] J. Kalisz, "Review of methods for time interval measurements with picosecond resolution," vol. 41, no. 1, pp. 17–32, Dec. 2003, ISSN: 0026-1394. DOI: 10.1088/0026-1394/41/1/004.

[172] P. Horowitz, *The Art of Electronics*, Third edition. New York, NY: Cambridge University Press, 2015, ISBN: 978-0-521-80926-9.

[173] P. Chen *et al.*, "A Low-Cost Low-Power CMOS Time-to-Digital Converter Based on Pulse Stretching," *IEEE Transactions on Nuclear Science*, vol. 53, no. 4, pp. 2215–2220, Aug. 2006, ISSN: 1558-1578. DOI: 10.1109/TNS.2006.876051.

[174] D. Stoppa *et al.*, "A 32x32-pixel array with in-pixel photon counting and arrival time measurement in the analog domain," in *2009 Proceedings of ESSCIRC*, Sep. 2009, pp. 204–207. DOI: 10.1109/ESSCIRC.2009.5325970.

[175] M. Gersbach *et al.*, "A Time-Resolved, Low-Noise Single-Photon Image Sensor Fabricated in Deep-Submicron CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 6, pp. 1394–1407, Jun. 2012, ISSN: 1558-173X. DOI: 10.1109/JSSC.2012.2188466.

[176] A. Rivetti, *CMOS: Front-End Electronics for Radiation Sensors* (Devices, Circuits, and Systems). Boca Raton, Fla.: CRC Press, 2015, ISBN: 978-1-4665-6311-7 978-1-4665-6310-0.

[177] T. Sepke *et al.*, "Noise Analysis for Comparator-Based Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 3, pp. 541–553, Mar. 2009, ISSN: 1549-8328, 1558-0806. DOI: 10.1109/TCSI.2008.2002547.

[178] K. Hansen *et al.*, "8-bit 5-MS/s Analog-to-Digital Converter for Pixel-Level Integration," *IEEE Transactions on Nuclear Science*, vol. 60, no. 5, pp. 3843–3851, Oct. 2013, ISSN: 0018-9499, 1558-1578. DOI: 10.1109/TNS.2013.2280660.

[179] P. Delpierre and J. J. Jaeger, "A sparse data scan circuit for pixel detector chips," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 305, no. 3, p. 627, Aug. 1991, ISSN: 0168-9002. DOI: 10.1016/0168-9002(91)90168-P.

[180] J. Hoff *et al.*, "PreFPIX2: Core architecture and results," in *2000 IEEE Nuclear Science Symposium. Conference Record (Cat. No.00CH37149)*, vol. 2, Lyon, France: IEEE, 2000, pp. 9/103–9/107, ISBN: 978-0-7803-6503-2. DOI: 10.1109/NSSMIC.2000.949879.

[181] *HDROB*, https://sus.ziti.uni-heidelberg.de/Projekte/HDROB/.

[182] *Qt | Cross-platform software development for embedded & desktop*, https://www.qt.io.

[183] R. E. Rondeau, *Slush Baths.* https://pubs.acs.org/doi/pdf/10.1021/je60028a037, May 2002. DOI: 10.1021/je60028a037.

[184] M. Ritzert, "Development and Test of a High Performance Multi Channel Readout System on a Chip with Application in PET/MR," 2014. DOI: 10.11588/HEIDOK.00017092.

[185] A. J. C. Wilson, "The thermal expansion of aluminium from 0 to 650 C," *Proceedings of the Physical Society*, vol. 53, no. 3, pp. 235–244, May 1941, ISSN: 0959-5309. DOI: 10.1088/0959-5309/53/3/305.

[186] P. Becker *et al.*, "The lattice parameter of highly pure silicon single crystals," *Zeitschrift für Physik B Condensed Matter*, vol. 48, no. 1, pp. 17–21, Aug. 1982, ISSN: 1431-584X. DOI: 10.1007/BF02026423.

[187] Xilinx, *UG470, 7 Series FPGAs Configuration User Guide*, Aug. 2018.

[188] *Model/View Programming | Qt Widgets 5.15.9*, https://doc.qt.io/qt-5/model-view-programming.html.

[189] G. Gallina *et al.*, "Characterization of SiPM Avalanche Triggering Probabilities," *IEEE Transactions on Electron Devices*, vol. 66, no. 10, pp. 4228–4234, Oct. 2019, ISSN: 1557-9646. DOI: 10.1109/TED.2019.2935690.

[190] N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A Systems Perspective* (The VLSI Systems Series), 2nd ed. Reading, Mass: Addison-Wesley Pub. Co, 1993, ISBN: 978-0-201-53376-7.

[191] L. Vadasz and A. Grove, "Temperature dependence of MOS transistor characteristics below saturation," *IEEE Transactions on Electron Devices*, vol. ED-13, no. 12, pp. 863–866, Dec. 1966, ISSN: 1557-9646. DOI: 10.1109/T-ED.1966.15860.

[192] M. Ghioni *et al.*, "Compact active quenching circuit for fast photon counting with avalanche photodiodes," *Review of Scientific Instruments*, vol. 67, no. 10, pp. 3440–3448, Oct. 1996, ISSN: 0034-6748. DOI: 10.1063/1.1147156.

[193] E. A. G. Webster *et al.*, "Transient Single-Photon Avalanche Diode Operation, Minority Carrier Effects, and Bipolar Latch Up," *IEEE Transactions on Electron Devices*, vol. 60, no. 3, pp. 1188–1194, Mar. 2013, ISSN: 1557-9646. DOI: 10.1109/TED.2013.2243152.

[194] G. S. May and S. M. Sze, *Fundamentals of Semiconductor Fabrication*. Hoboken (N. J.): John Wiley and Sons, 2003, ISBN: 978-0-471-23279-7.

[195] D. Bronzi *et al.*, "Fast Sensing and Quenching of CMOS SPADs for Minimal Afterpulsing Effects," *IEEE Photonics Technology Letters*, vol. 25, no. 8, pp. 776–779, Apr. 2013, ISSN: 1041-1135, 1941-0174. DOI: 10.1109/LPT.2013.2251621.

[196] P. Fischer *et al.*, "MEPHISTO – a 128-channel front end chip with real time data sparsification and multi-hit capability," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 431, no. 1, pp. 134–140, Jul. 1999, ISSN: 0168-9002. DOI: 10.1016/S0168-9002(99)00262-4.

Acknowledgements

I think a thank you is best said in your native language...
Als erstes möchte ich Herr Prof. Dr. Peter Fischer danken, für die Aufnahme als Doktorand in seiner Arbeitsgruppe. Danke für die Möglichkeit sehr frei und selbstbestimmt mit dieser großartigen Detektortechnologie zu arbeiten. Danke für die zahlreichen und konstruktiven Diskussionen, die Motivation und die Ratschläge.
Als zweites möchte ich meiner Partnerin Laura (und unserem Hund Benjamin) danken, die mich vor allem in der Schreib-Zeit, die durch Corona hauptsächlich Daheim statt fand, seelisch und moralisch unterstützt hat. Ohne dich hätte ich nicht durchgehalten, danke das du für mich da bist. Schreiben war für mich, ohne Ausnahme, die anstrengendste Phasen der Doktoranden-Zeit.
Auch danke an meine Mitmenschen an der Uni, ob ehemalig, noch da, aus der selben AG oder nicht. Sowohl fachliche, also auch der reinen Verstreuung zugetragen, waren die Unterhaltungen und Diskussionen immer sehr, wie man so schön sagt, fruchtbar. Diesbezüglich, ein spezieller Danke an folgenden Menschen, die mich bei meiner Arbeit besonders Unterstütze haben: Besten Dank Timo. Unsere gemeinsame Zeit im Labor im KIP war großartige und sehr erfolgreiche. Danke an die AG von Prof. Dr. Christian Enss uns in deren Laboren ein Platz zum Messen geschaffen zu haben. Danke Andreas Reiser, für das Bereitstellen des Stickstoff Kryostaten, einer der zentrale Gegenstände meiner Arbeit, und obendrauf die Unterstützung durch dein großes technischen Wissen. Danke David für die tolle gemeinsame Doktoranden Zeit in der AG und die gegenseitige Unterstützung. Danke Jan, nicht nur fürs Gegenlesen vieler Teile meiner Arbeit, sonder auch die Freundschaft über unsere gemeinsame Zeit in der AG hinaus. Danke auch an meinen ehemaligen Kollegen Flo fürs Gegenlesen und die Konstruktiven Kommentare. Danke an Daniel, du hast mich schon damals beim Schreiben meiner Bachlor Arbeit betreut. Deine Anmerkungen für mein Grundlagen Kapitel, waren (wie erwartet) äußerst Hilfreich.
Alles letzte Danke an meine Eltern und alle meine Freund:innen, die mich durch meine Doktoranden Zeit und vor allem die Schreibzeit begleitet haben. Die Ablenkungen vom Schreiben waren mir sehr willkommen.