Dissertation

submitted to the

Combined Faculty of Mathematics, Engineering and Natural Sciences

of Heidelberg University, Germany

for the degree of

Doctor of Natural Sciences

Put forward by

David Clemens Schimansky

born in: Speyer

Oral examination: January 10, 2024

Design of a Novel Readout ASIC for X-ray Diffraction Experiments at High-Energy Synchrotron Light Sources

Referees: Prof. Dr. Peter Fischer
Prof. Dr. André Schöning

Zusammenfassung

Das Ziel dieser Arbeit bestand in der Überprüfung der Umsetzbarkeit eines Auslese-ASICs, der die ambitionierten Anforderungen des X-Ray Integrating Detector (XIDer) Projekts erfüllt. XIDer befasst sich mit der Entwicklung eines hybriden 2D-Pixeldetektors für Röntgenbeugungsexperimente an Synchrotrons der vierten Generation wie die European Synchrotron Radiation Facility (ESRF) in Frankreich. Zu den Anforderungen zählt ein großer dynamischer Zählbereich bis zu $1 \times 10^{11}\,\mathrm{ph\,s^{-1}\,mm^{-2}}$, während der Detektor gleichzeitig einzelne Photonen auflösen können soll. Hinzu kommt eine hohe nötige Anpassungsfähigkeit an Experimente mit unterschiedlichen Voraussetzungen. Der geplante Energiebereich von 30 keV bis 100 keV erfordert außerdem den Einsatz von Verbindungshalbleitern wie Cadmiumtellurid und Cadmiumzinktellurid, die eine hohe mittlere Kernladungszahl aufweisen.

Der entwickelte ASIC erlaubt die parallele Auslese von Sensor-Pixelmatrizen mit integrierter Analog-zu-Digital-Umsetzung (ADU), Datenvorverarbeitung und -speicherung. Dabei setzt er auf neue Konzepte wie die digitale Integration, das Telegramm-Protokoll und ein zweistufiges Frontend, in dem eine kontinuierliche ADU implementiert ist.

Mit Fokus auf das analoge Frontend gibt diese Arbeit Einblicke in die Entwicklung des Auslese-ASICs, angefangen bei der Motivation gewählter Konzepte, bis hin zur Charakterisierung gefertigter Prototypen und daraus gezogener Schlussfolgerungen. Des Weiteren werden mehrere, an ESRF-Beamlines durchgeführte Messungen mit ASIC-Sensor-Prototypen vorgestellt und analysiert.

Abstract

The aim of this thesis was to verify the feasibility of a readout ASIC which fulfills the challenging requirements of the X-ray Integrating Detector (XIDer) project. XIDer is committed to the design of a 2D hybrid pixelated detector for X-ray diffraction experiments at accelerator-based fourth-generation X-ray sources like the European Synchrotron Radiation Facility (ESRF). The requirements include a wide dynamic photon counting range up to $1 \times 10^{11}\,\mathrm{ph\,s^{-1}\,mm^{-2}}$ with single photon sensitivity and a high versatility for many different measurement conditions. In addition, the energy range of 30 keV to 100 keV demands for the use of high-Z compound semiconductor sensor materials like cadmium telluride and cadmium zinc telluride. The proposed and implemented readout ASIC design follows a modularized approach to read out large sensor pixel matrices in parallel performing on-chip analog-to-digital conversion, data pre-processing and storage. It explores novel concepts like a pipelined continuous conversion front-end, the digital integration scheme and the telegram protocol.

This thesis presents the ASIC's design process from drafts to actual implementations. Design concepts, simulations and characterisation measurements of ASIC and ASIC-sensor assembly prototypes are explained, analyzed and discussed with an emphasis on the performance of the analog front-end.

Contents

1 Introduction

All over the world, accelerator-based X-ray light sources are being developed, built and maintained to push the boundaries of imaging condensed and living matter. In this endeavour, scientists seek to gain further insight into the structure of materials and organisms. Not only the static structure is of interest, but also its evolution over time as it undergoes changes in chemical reactions, phase transitions or other physical processes such as deformation due to mechanical stress. Modern facilities allow resolving structures down to the nanometer scale while illuminating the sample under study every few 100 ns. An example for such a facility is the European Synchrotron Radiation Facility (ESRF) in Grenoble, France. Under the name EBS, the ESRF completed the upgrade of its storage ring in August 2020 to become the world's first high-energy fourth-generation synchrotron radiation source with a brilliance unprecedented by any other facility of this type [1, 2]. Other facilities around the world such as APS in Lemont, USA [3], the SPring-8 in Sayo, Japan [4], PETRA-IV in Hamburg, Germany [5] or HEPS in Beijing, China [6] are following its example by implementing similar accelerator upgrades or by constructing new light sources based on the same concepts.

As the properties and capabilities of these X-ray light sources improve and grow, so do the requirements placed on instrumentation used to detect this radiation. Subsequently, new detectors have to be developed to surpass the performance of current systems. As a collaboration between Heidelberg University and the European Synchrotron Radiation Facility, the **XIDer** project (see chapter 5) is committed to the design of such an instrument. Its goal is to implement a versatile 2D detector for cutting edge high-energy X-ray diffraction experiments to be performed by scientists at the ESRF in the near future. As such, the detector must provide a very high dynamic range to sustain and process X-ray photon fluxes up to $1 \times 10^{11}\,\mathrm{ph\,mm^{-2}\,s^{-1}}$ while still providing single photon sensitivity [7]. This requires a detector with sufficiently low readout noise, not exceeding an equivalent noise charge (ENC) of a few hundred electrons. At the same time, the detector has to provide time resolving capabilities to follow the temporal structure of the X-ray beam down to a few 100 ns. And with a target X-ray energy range from 30 keV to 100 keV [8], the use of unconventional sensor materials is necessary. Last but not least, the system needs to be as versatile as possible to cater for many different experiments. To address this issue, it has to provide a high degree of flexibility in terms of image acquisition, data pre- processing and data readout capabilities. Innovative signal and data processing concepts like the custom-designed data flow control protocol *telegram* which is described in section 6.1.3 and 6.3.3.2 are essential for the success of this project.

The detector must be conceived as a modular device to allow building full systems of variable active detection areas of up to more than 40 cm × 40 cm. Each module is based on a 2D hybrid assembly consisting of a pixelated high-Z semiconductor sensor bump-bonded pixel-by-pixel to a small number of readout ASICs. In this architecture, each pixel has a corresponding on-ASIC channel counterpart such that the whole sensor matrix can be read out and processed in parallel. Resulting from experimental requirements, the pixel pitch in XIDer has been chosen as 100 µm. This choice not only results in an incident flux capability of $1 \times 10^{9}\,\mathrm{ph\,s^{-1}\,pix^{-1}}$ but it also imposes a challenging space constraint on the readout electronics. As a result, the ASIC is implemented in the TSMC 65 nm technology

which provides a reasonable compromise between good analog features and low space and power consumption.

The basic idea of the XIDer ASIC front-end is to use a concept that operates in between the two most used schemes for X-ray detection – photon counting and charge integration. We call this approach *continuous conversion* in which the signal charge is integrated and continuously converted to a digital value while the integration is still ongoing. This approach is similar to that chosen by projects like the MM-PAD [9]. Section 6.1.1 explains the procedure in detail. In addition, a novel idea called *digital integration* ([10]) as explained in section 5.4 is implemented.

This thesis aims to introduce the XIDer project and concentrates on the aspects which Heidelberg University and the author of this thesis have been and will be responsible for: the design and characterisation of XIDer's readout ASIC. With a focus on the analog front-end, it discusses the project feasibility from the ASIC point of view, presents chosen concepts and weighs them against different approaches. In addition, first prototypes that have been manufactured over the course of this thesis are presented. These range from bare ASICs to prototype assemblies with CdTe/CdZnTe (CZT) sensors that have been used in beamtime characterisation measurements at an ESRF beamline. Besides, the used test environment including software, firmware and PCBs as well as necessary protocols and stimuli to operate the ASIC are demonstrated and explained. At the end of this thesis, there is a conclusion providing a summary of the current state of the project, the author's contributions as well as an outlook of XIDer's future.

2 The European Synchrotron Radiation Facility

In order to provide a context for the XIDer project, this chapter includes a general introduction to synchrotron radiation with a focus on its application at the ESRF. It presents a few fundamentals of synchrotron light generation, discusses science with X-rays and gives an overview of the synchrotron light source community. The last sections of this chapter provide a closer look at the ESRF and its particular requirements. Since the XIDer project is dedicated to storage ring based synchrotron radiation facilities, this chapter excludes the discussion of sources based on free electron lasers.

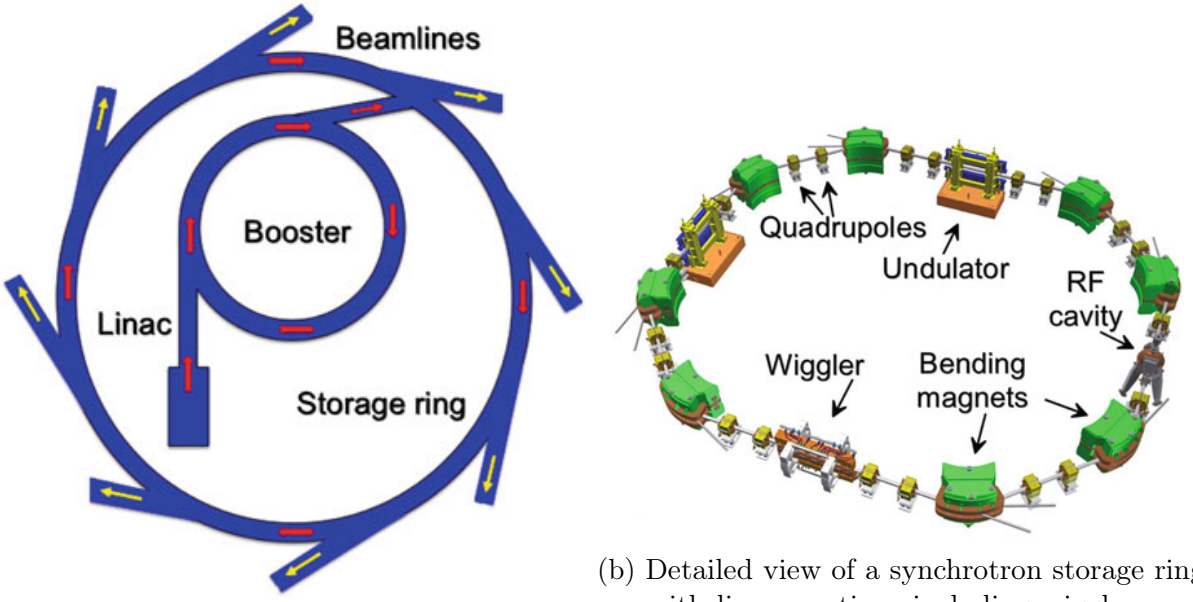
2.1 Synchrotron Radiation Light Sources

When a charged particle that is moving at a velocity close to the speed of light is deflected from its trajectory by an external force, it radiates electromagnetic radiation. In nature, this so-called synchrotron radiation can, for instance, be found in space where relativistic electrons face strong potential fields generated by objects like black holes [11] or pulsars [12].

While synchrotron radiation was considered a nuisance in early particle accelerators, in the mid of the 20th century, scientists found out that this kind of radiation offers a great potential for many different scientific areas that can profit from the production of intense and precise X-ray beams [13]. This revelation started a completely new research area committed to the design and construction of synchrotron light sources. With ever-improving new technologies, the boundaries of experimental techniques have been pushed further and further down to nanometer scales. The highly brilliant X-ray radiation generated in these facilities opens up new possibilities in research fields like condensed matter studies, medical physics and diagnostics, chemistry or biology among others. The applications range from analyzing atomic lattices to watching a protein change its structure in a biochemical reaction to investigating fossils and materials for their inner structure in a non-destructive way [14, 15]. If not mentioned otherwise, the following subsections are based on the sources [12], [13] and [16].

2.1.1 Basic Synchrotron Operation Principle

Since the construction of the first synchrotron radiation facility, their basic structure has not changed. Synchrotrons consist of two parts: an electron accelerator to provide electrons with velocities close to the speed of light as well as a storage ring to keep these electrons and force them on a circular trajectory via bending magnets to generate synchrotron light. This structure is drawn in figure 2.1a. The electron acceleration starts with an electron gun and a linear accelerator (LINAC). It acts as a pre stage for the booster, increasing the energy of the electrons up to a few MeV. In the booster, the electrons are accelerated further to reach their final energy of a few GeV. At this point, they are injected into the storage ring, an evacuated metal pipe in circular shape. Beamlines around the storage ring make use of the synchrotron light which is mainly radiated in a tangential direction to the electrons' trajectory. Then, after conditioning the X-ray beam with suitable optics,



(a) Basic synchrotron structure [12]

(b) Detailed view of a synchrotron storage ring with linear sections including wigglers and undulators [12]

Figure 2.1: Schematic views of a synchrotron

scientists illuminate the sample under study to conduct their experiment. Figure 2.1b provides a more detailed view of modern synchrotron storage rings. As depicted, modern facilities incorporate linear sections with wigglers and undulators. Their function will be explained over the course of this section. The radio-frequency (RF) cavities are used to recover the electrons' energy that is lost as they radiate synchrotron light along their orbit in the storage ring.

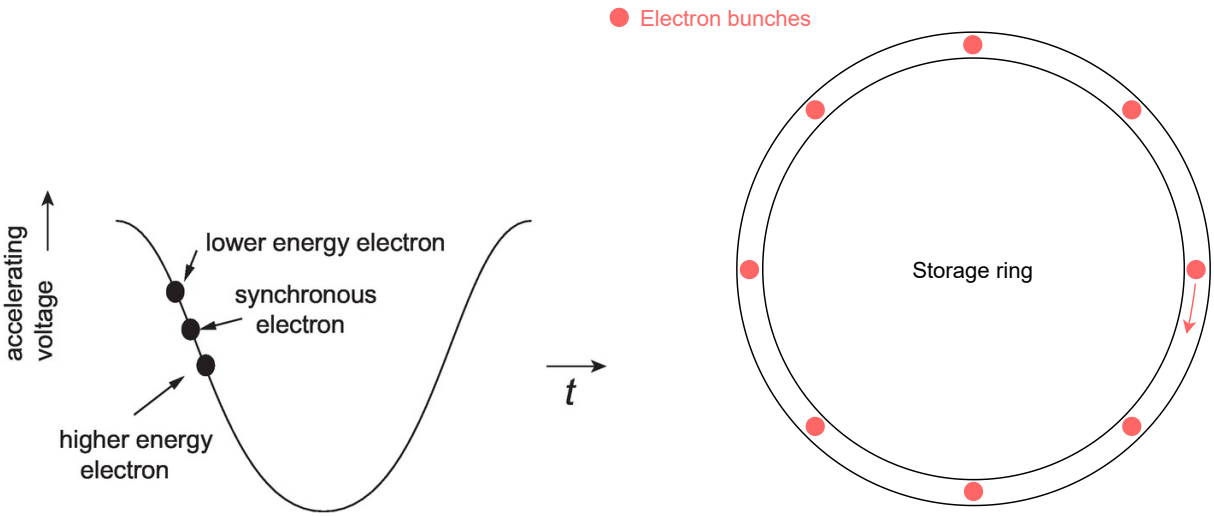
2.1.1.1 Electron Energy Preservation with RF Cavities

Applying Schwinger's formula [17], the radiated power P of a relativistic charged particle with mass m and energy E in a synchrotron with storage ring radius R is given as

$$P = \frac{2}{3}\frac{e^2 c}{R^2}\left(\frac{E}{mc^2}\right)^4 \tag{2.1}$$

where e is the elementary charge and c is the speed of light. As shown in this equation, this power is proportional to $1/m^4$ of the charged particle which explains why electrons are the best choice for building a synchrotron light source. Their rest mass energy of 511 keV is e.g. about 200 times smaller than that of a muon and about 1800 times smaller than that of a proton. As a result, muons and protons of the same energy radiate less power by a factor of 1.6×10^9 and 1×10^{13} respectively. The equation also shows an inverse proportionality to the radius of the storage ring. Thus, smaller rings lead to higher radiated power by the charged particle. However, they also require stronger magnetic fields to keep the electrons on the beam trajectory. With the revolution frequency $2\pi R/c$ taken into account, the charged particle's energy loss per turn can be calculated as

$$\Delta E = \frac{4\pi}{3}\frac{e^2}{R}\left(\frac{E}{mc^2}\right)^4 \tag{2.2}$$



(a) RF voltage applied to an RF cavity. [16] (b) Electron beam bunching

Figure 2.2: RF cavities and electron beam bunches

This corresponds to the amount of energy that has to be restored by the RF cavities.

2.1.1.2 Electron Orbit Stability and Bunching

On top of restoring the electron energy, the RF cavities in the storage ring also play an important role in ensuring the stability of the electron orbit. The RF cavities keep the electrons at the correct energy by establishing a stationary wave with an oscillating longitudinal electric field in the direction of the electron beam. The voltage applied to the RF cavity is depicted in figure 2.2a. There are three highlighted spots on the curve representing three different points in time at which the electron could traverse the cavity. The sweet spot is the point marked as *synchronous electron*. The oscillating electric field is parameterized such that in this case, its amplitude is just at the correct level to fully restore the energy ΔE lost by the emission of synchrotron radiation. If the electron enters the cavity at this phase of the electric field consistently, it is considered a synchronous electron. This stable condition can only be met if the electron's energy and phase are just right. If the electron is too fast, i.e. its energy is too high, it will enter the cavity earlier than a synchronous electron. In this case, it will experience a lower electric field which will not fully restore the energy lost by radiation emission. As a result, the electron loses energy and its velocity decreases. This process will continue until the electron has just the right energy and phase synchronous to the RF cavity. In the third depicted case, the electron's energy is too low. Electrons in this condition are slower than a synchronous electron and enter the RF cavity slightly later. As a result, they experience a larger electric field which causes an overall increase of their energy. Again, this process repeats until the electrons become synchronous to the RF cavity. Figure 2.2a also indicates that the cavity can only fulfill its purpose in one half of the oscillation's period which starts at one maximum and ends at the next minimum. If the phase of an electron is too far off, it passes the cavity in the other half of the period and it can not reach the stable condition. In this ideal image, the RF cavity thus manages to capture and lead electrons to the stable condition which end up in 50 % of its oscillation period. Real RF cavities however usually only lead electrons to the stable condition in about 5 % to 10 % of the oscillation period. Electrons with a larger phase shift are inevitably lost.

As a consequence of the phase requirement of RF cavities, there is no continuous stream of electrons in a storage ring. Electrons are always organized in so-called bunches as depicted in figure 2.2b. The time interval in between consecutive bunches is necessarily an integer multiple of the period of the RF cavity's electric field. There are two extremes for this interval. It can be as long as a whole ring orbit period. In this case there's is only a single bunch of electrons in the storage ring. In the other extreme case, the time interval is as low as a single RF period and the storage ring hosts the maximum possible amount of electron bunches. Obviously, in order for this to work, the RF frequency must be chosen to be an integer multiple of the electrons' orbit frequency. The filling pattern of the storage ring, i.e. the *bunch-mode* is a well-controlled machine parameter. The actual setting of this parameter has a big impact on the experiments that can be conducted at a given time.

2.1.2 Synchrotron Light Generation Properties

Due to the electron's relativistic velocity, the synchrotron light is radiated in a cone in the forward direction, i.e. tangentially to the electron's bent trajectory. The spread of this cone is proportional to $1/\gamma$ in which γ is the Lorentz factor defined as $\gamma = 1/\sqrt{1-(v/c)^2}$ Here, v is the electron's velocity and c is the speed of light. Thus, the faster the electron is, the smaller the divergence of the emitted radiation is. Due to this, beamlines and experiments are always placed tangentially to the storage ring as shown in figure 2.1a.

The radiation generated by a charged particle under the influence of a simple bending magnet has a continuous spectrum with a rapid drop below the critical wavelength

$$\lambda_c = \frac{4\pi}{3}\frac{R}{\gamma^3} \tag{2.3}$$

where R is the radius of the charged particle's trajectory. With the Planck constant h, this translates to a critical photon energy of

$$\mathcal{E}_c = \frac{3h}{4\pi}\frac{c\gamma^3}{R} \tag{2.4}$$

which cuts the spectrum of the emitted radiation in two parts both including half of the total radiated power. As depicted in figure 2.3, the intensity of emitted photons continuously rises from low energies until $\mathcal{E}_c$ and then shows a sudden drop above $\mathcal{E}_c$. This drop limits the maximum usable energy of photons emitted by the electrons in the storage ring. Since $\mathcal{E}_c$ depends on the electron energy via its proportionality to γ^3, tuning the electron energy allows changing the high-energy cut-off of emitted synchrotron light photons. Another parameter to tune the high-energy cut-off is the bending radius R. The smaller the radius, the higher the critical energy. As the photon energies of synchrotron light sources are well within the hard X-ray regime, this thesis will use the terms *synchrotron light/radiation* and *X-rays* synonymously.

The y-axis in figure 2.3 is the so-called *brilliance* B which is the leading figure of merit in characterising the performance of synchrotron light sources. The brilliance is a parameter that, in most experiments and regardless of the optical setup and the particular beam conditioning of the beamline, is in some way proportional to the number of X-ray photons than can be effectively used for a particular experiment. The brilliance of a photon beam

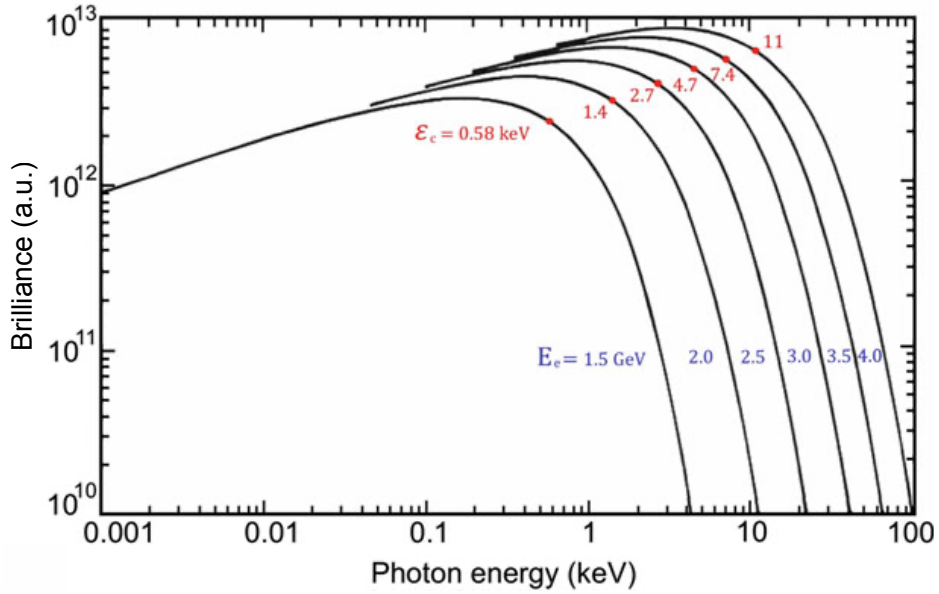


Figure 2.3: Synchrotron light spectrum radiated from a relativistic electron under the influence of a bending magnet's magnetic field. The plot shows a set of curves for different electron energies E_e at a fixed storage ring radius. Above the critical energy $\mathcal{E}_c$, the brilliance drops rapidly. For higher electron energies, the drop shifts to higher emission energies. [12].

is given by

$$B = \frac{\Phi}{4\pi^2 \Sigma_x \Sigma_{\theta x} \Sigma_y \Sigma_{\theta y} \Delta E}, \qquad [B] = \frac{photons}{s \cdot mm^2 \cdot mrad^2 \cdot 0.1\% BW} \tag{2.5}$$

in which Φ is the photon flux, i.e. photon rate per area, and $\Sigma_{x,y}$ and $\Sigma_{\theta x,y}$ are a measure for the electron beam cross section and angular divergence that are usually combined into the beam emittances ϵ_x and ϵ_y. ΔE denotes the photon energy range of interest which is usually taken as 0.1 % of the working energy. As indicated by the brilliance's units, it measures the amount of photons emitted per second, solid angle, unit source size and photon energy bandwidth. Its maximization can be achieved by increasing the photon rate in a given energy band while minimizing electron beam emittance that translates into the photon source size and divergence. The following sections provide insight into how this is achieved from a technical point of view.

2.1.3 Third-Generation Synchrotron Light Sources

In the 1990s, linear sections with so-called insertion devices, i.e. undulators and wigglers, were introduced in storage rings of synchrotron light sources. Figure 2.4 shows a sketch of a insertion device and its working principle. The basic idea is to pass the electron beam through a spatially oscillating magnetic field which is produced by a consecutive set of dipole magnets with alternating polarity. The wavelength of the periodic magnetic field which is perpendicular to the motion of the electron is given by the pitch λ_u of two dipole magnets with identical polarity.

The main property to classify the performance of insertion devices is given by the

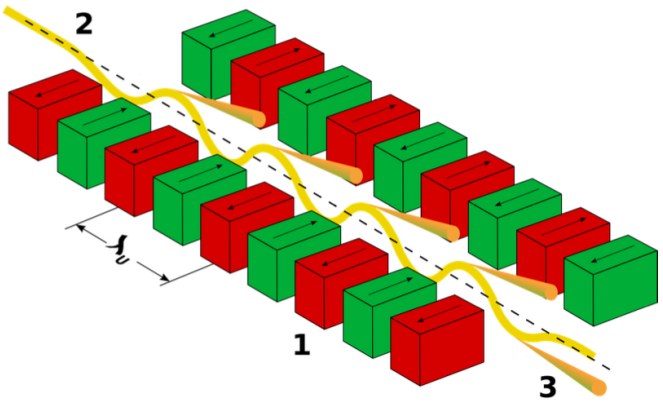


Figure 2.4: Basic structure of an insertion device as implemented in third-generation synchrotron light sources. [18].

undulator parameter K which is defined as

$$K = \frac{eB\lambda_u}{2\pi m_e c} \tag{2.6}$$

in which e is the elementary charge, B is the amplitude of the oscillating magnetic field, m_e is the electron mass and c is the speed of light. For weak magnetic fields, $K < 1$ and the device is considered an undulator. In this case, the electrons travel across the insertion device immersed in their own radiated field and the photon beams generated at individual magnetic poles show constructive interference. As a result, the spectrum is a sequence of high brilliance resonances at frequencies which are characteristic for the chosen undulator parameters like λ_u or K. In the forward direction, the wavelength resonance condition is given by:

$$\lambda_R = \frac{\lambda_u}{2n\gamma^2}\left(1 + \frac{K^2}{2}\right) \tag{2.7}$$

With a strong magnetic field such that $K > 1$, the insertion device is considered a wiggler. In this case, the peaks broaden and overlap forming a continuous spectrum [18].

In actual applications, undulators are most often preferred due to their high brilliance gain. Compared to the conventional storage ring bending magnets, the brilliance of undulators can reach values three or four orders of magnitude higher [19].

2.1.4 Fourth-Generation Synchrotron Light Sources

The main performance boost in fourth generation facilities comes from the significant increase of X-ray brilliance achieved by reducing the emittance of the electron beam in the new storage rings. In order to understand technological advances made to minimize the emittance, one has to start by clarifying the meaning of the word *lattice* which is often used by the synchrotron community in this context: A storage ring lattice the particular arrangement of consecutive bending and focussing magnets that are used to keep the electron beam circulating in the storage ring while minimizing its cross-section. In the most common lattices, there are two types of magnets used to execute these tasks. Dipole magnets take care of forcing the electron beam on the path given by the storage ring. And quadrupole magnets are used to focus the beam, reducing its size. The following section has been compiled from the sources [21, 23, 22, 20].

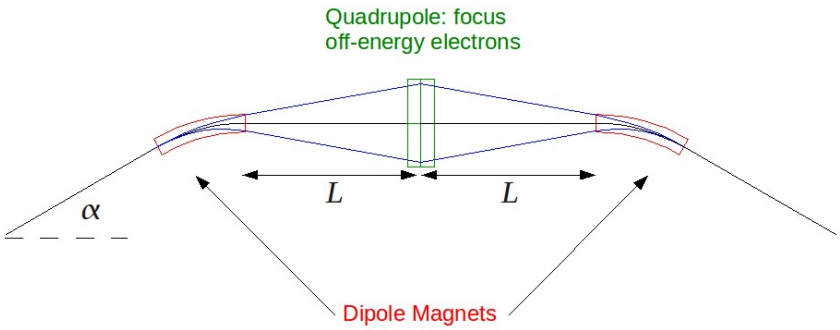


Figure 2.5: Schematic drawing of a Chasman-Green lattice also known as double bend achromat (DBA) lattice [20].

2.1.4.1 Double Bend Achromat Lattices

For third-generation synchrotron light sources, the most commonly used lattice is the Chasman-Green lattice, also known as double bend achromat (DBA) lattice. It is depicted in figure 2.5. With the simplest DBA lattice, each sector of the storage ring consists of two bending magnets with a focussing quadrupole centered between them. When an electron bunch enters the lattice from the left hand side it passes through the first bending magnet. Due to slight momentum mismatches of electrons in the bunch, the bending angle of every electron in the bunch that passes the bending magnet is slightly different. As a result, the electron beam expands horizontally and with it, the beam's horizontal size increases. With no countermeasures, this beam expansion would add up at every trajectory bend, resulting in a loss of electrons and an unstable orbit. In order to counteract this, a quadrupole magnet is used as a focussing lens as shown in figure 2.5. A second bending magnet acts exactly the same as the first one, again applying a slightly different bending angle to electrons in the bunch with a slightly different momentum. However, due to the quadrupole's re-focussing of the beam on the second bending magnet, the resulting electron beam's horizontal size is reduced. There are many different variations of this simple design, always consisting of two bending magnets but with a different combination of quadrupole magnets focussing and defocussing the electron beam. Due to its simplicity and effectivity at the same time, the DBA has been widely used in many different machines like the ESRF, ELETTRA or SPring-8. However, the minimum achievable emittance with a DBA lattice is limited and in order to further reduce it, more and more quadrupole magnets have to be added which is the source of other problems. The most obvious one is an increased size and cost. Another one is the increased chromaticity which acts analogous to chromatic aberrations with optical lenses. The array of quadrupole focussing magnets has slightly different focal points for different electron beam energies. In order to perform chromaticity corrections, complex sextupole magnets have to be used which introduce even more optical aberrations and further increase the cost, size and complexity of the storage ring lattice.

2.1.4.2 Multi Bend Achromat Lattices

But there is another way to further decrease the emittance ϵ which becomes obvious when taking a look at the lattice emittance formula [24]

$$\epsilon = \frac{CE^2}{N_d^3} \tag{2.8}$$

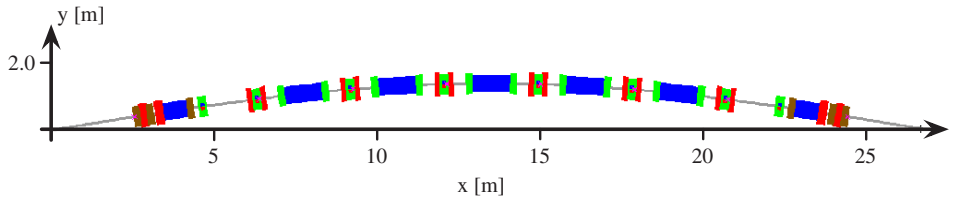


Figure 2.6: Schematic drawing of MAX IV's 7-bend multi bend achromat lattice. The shown colored building blocks are dipole bending magnets (blue), focusing quadrupole magnets (red), sextupoles (green) and octupoles (brown) for chromaticity correction. [24].

in which E is the beam energy, N_d is the number of dipole/bending magnets in each sector of the lattice and C is a lattice constant which is defined by the optical lattice functions, e.g. quadrupole magnet(s). Instead of minimizing C and keeping $N_d = 2$ one could also increase the number of bends N_d to reach lower emittance. With more bending magnets, one can choose lower bending angles with weaker dipole magnetic fields per magnet which reduces the equilibrium emittance. This is the approach that multi bend achromat lattices (MBA) take. In 2015, MAX IV in Lund, Sweden was the first synchrotron facility to implement functional MBAs. This made them the first fourth-generation synchrotron at 3 GeV electron beam energy. A schematic drawing of MAX IV's lattice is shown in figure 2.6. The ESRF then found a way to adjust MBAs to high beam energies with the hybrid achromat lattice approach. The result is the Extremely Brilliant Source (ESRF-EBS) which is the world's first high-energy fourth-generation synchrotron running at a beam energy of 6 GeV.

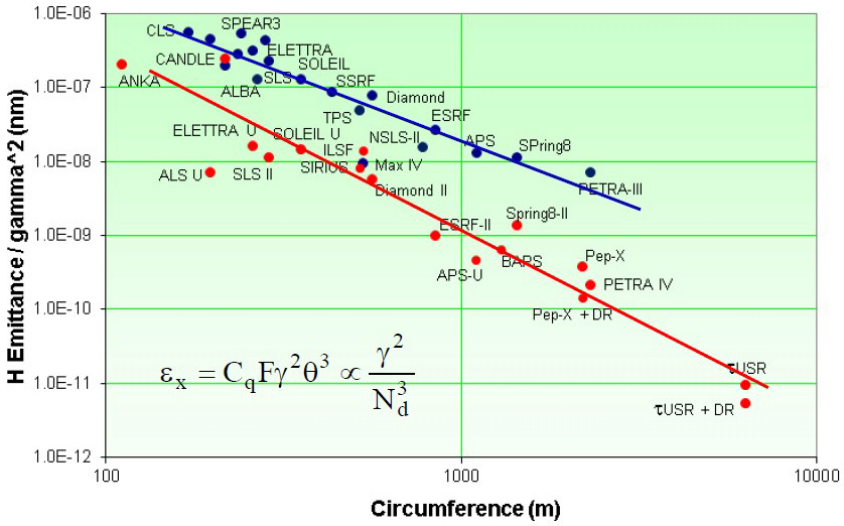


Figure 2.7: World-wide comparison of synchrotron light source emittances from 2019 [25]. The y-axis shows the natural emittance which is the actual emittance divided by the square of the electron gamma factor, i.e. the electron energy. The x-axis depicts the synchrotron's circumference. The blue color shows operational machines, while red shows planned light sources as well as sources under construction at that time.

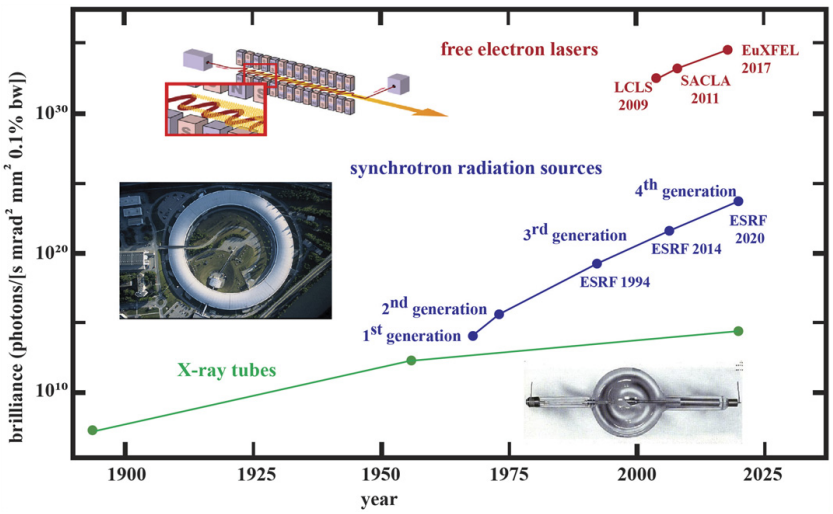


Figure 2.8: Improvement of synchrotron light source peak brilliance throughout the different generations (from 2021) [26].

2.1.4.3 Performance Comparison of Synchrotron Light Facilities

In order to summarize this section, figures 2.7[1] and 2.8 show plots of the emittances and brilliances of different synchrotron light source generations. In this world-wide comparison, one can clearly see the step in emittance between third- and fourth-generation synchrotron radiation sources. For the ESRF, the emittance has been reduced by almost two orders of magnitude. Figure 2.8 depicts the progress made throughout the generations of synchrotron light sources in terms of brilliance. It also provides a comparison to free electron lasers which offer much higher peak brilliance.

2.2 Applications of X-rays in Science

Since their discovery in 1895, X-rays have become a valuable tool utilized in medical, scientific and industrial applications. The following summary introduces a few examples of experimental techniques widely used in the synchrotron science community and has been compiled from the references [12] and [27]. It is by no means an exhaustive list.

- **X-ray Imaging:** Used in many scientific areas, especially medical applications. The most well-known method is X-ray computer tomography (CT) in which a sample is irradiated with X-rays from different angles. Depending on the material's attenuation coefficient and thickness, the X-rays are attenuated while passing through the sample. Detectors measure the attenuation to reconstruct an image of the sample's contents. Combining CT with the high intensity and brilliance of synchrotron light sources enables rapid 3D image acquisition at unprecedented spatial resolutions [28].

- **X-ray Spectroscopy:** Spectroscopic methods seek to study the chemical composition of material compounds as well as their electronic states. There is a wide field of different techniques based on x-ray absorption and emission methods. X-ray fluorescence spectroscopy, for instance, is based on the photoelectric effect where

[1]This figure is from 2019 and denotes the ESRF-EBS (ESRF-II in the plot) as under construction and in commissioning which is no longer true today. The facility is fully functional and open to users since August 2020.

electrons within the sampled material are excited via incident photons to reach energies beyond their binding energy. Via evaluation of the ejected electron's binding energy, researchers can determine the discrete, characteristic binding energies of materials in the probed sample. In this way, a compound's constituents can be identified [29].

- **X-Ray Diffraction:** Based on Bragg's law, diffraction takes place when a periodic structure with a periodicity p is hit by an incident wave with a wavelength λ where p and λ have the same order of magnitude. Bragg X-ray diffraction is the particular case when atomic structures are illuminated with X-rays and it is the main experimental technique foreseen for XIDer. Since X-rays exhibit a typical wavelength in the range of 0.01 nm to 1 nm, they fulfill this condition for the distance of atoms in atomic lattices and crystals. For this reason, X-rays are well-suited to study the physical properties of crystalline structures via x-ray diffraction experiments. Methods like x-ray powder diffraction (XRPD) also known as Debye-Scherrer method expand the field of x-ray diffraction to polycrystalline structures [30, 31].

- **Elastic X-ray Scattering:** One of the most well-known elastic x-ray scattering techniques apart from Bragg diffraction is small angle x-ray scattering (SAXS). In contrast to x-ray diffraction that is sensitive to structures as the atomic level, SAXS is suitable for the study of non-homogeneous distributions of atom aggregates and molecules. With its capability of resolving structures down to nm scales, it allows studying nanoparticles in terms of their individual size, shape and surface structure. On top, SAXS also allows studying the structure and shape of macromolecules such as viruses or proteins rendering it very valuable for biological and chemical applications. A detailed summary of this method can be found in [32] and [33].

2.3 The ESRF – the World's First 4th Generation Synchrotron at High Energies

As a joint research facility, the European Synchrotron Radiation Facility (ESRF) operates on of the world's largest electron storage rings dedicated to research with synchrotron radiation. It is funded by 21 countries with France, Germany, Italy as the main contributors among them and shares a site with the Institut Laue-Langevin (ILL) in Grenoble, France. Figure 2.9 shows an image of this site and the facility's distinctly visible storage ring. With a circumference of about 844 m, the ESRF hosts and stores the 6 GeV electron beam which generates X-ray beams with energies of up to 100 keV.

Electron synchrotrons like the ESRF advertise themselves as user facilities. The ESRF staff is in charge of the operation and improvement of the facility, including the accelerator complex, the beamlines and their experimental stations. Actual research with the synchrotron radiation itself is mainly conducted by external researchers who apply for time slots at the beamlines distributed around the storage ring.

2.3.1 The Extremely Brilliant Source Storage Ring

In 2015, the ESRF started the Extremely Brilliant Source (EBS) upgrade program which aimed to upgrade the storage ring in use. The intention was to increase the brilliance of the X-ray beams by a factor of two orders of magnitudes by reducing the electron

Figure 2.9: Image of the European Synchrotron Radiation Facility (ESRF) in Grenoble, France. [34]

beam emittance. As explained in section 2.1, the ring had to be rebuilt with a hybrid multi-bend achromat (HMBA) lattice to achieve this goal. With the start in user operation in August 2020, the ESRF proved to be able to achieve the expected emittance reduction as shown in the comparison of synchrotron sources plotted in figure 2.7. With this, the ESRF-EBS became the world's first fourth generation high-energy storage ring synchrotron light source.

Alongside the storage accelerator upgrade, the ESRF has started a detector development plan (DDP) to develop and build a new generation of x-ray detectors to fully exploit the properties of the EBS source and similar facilities. The requirements such a detector has to meet are discussed in section 5.1.

2.3.2 Beamlines

Figure 2.10 shows a schematic top view of the ESRF storage ring with close to 45 bealmines currently in operation. Every beamline is tailored to a specific research area or experimental technique such as those presented in section 2.2. For example, ID31 is dedicated to hard x-ray diffraction while BM29 offers a platform for SAXS. The wide variety of available options attracts scientists from research areas like condensed matter physics, medicine, structural biology, chemistry, environmental & cultural heritage studies, many others to the ESRF. As shown, most of the beamlines are for fully public use, while others are partially reserved for collaborating research groups. Some beamlines, dedicated to testing beamline and accelerator instrumentation, are where the ESRF studies and characterises new technologies and detector systems for future beamline implementations. Among these is BM05 where past and future beamline tests of the XIDer detector have been and will be conducted. Examples of these characterisation measurements can be found in section 8.3.2.

2.3.3 Accelerator and Booster

Besides the beamlines, figure 2.10 also illustrates the facility's accelerator complex schematically. An electron gun (not depicted) generates the elctrons by heating a tungsten filament to high enough temparatures so that the energy of electrons inside the filament exceeds their work function. As a result, the filament emits electrons. The ESRF employs a triode electron gun as explained in [36] which focusses and accelerates the freed electrons to energies up to 100 keV. After the triode gun, electrons enter the depicted linear accelerator

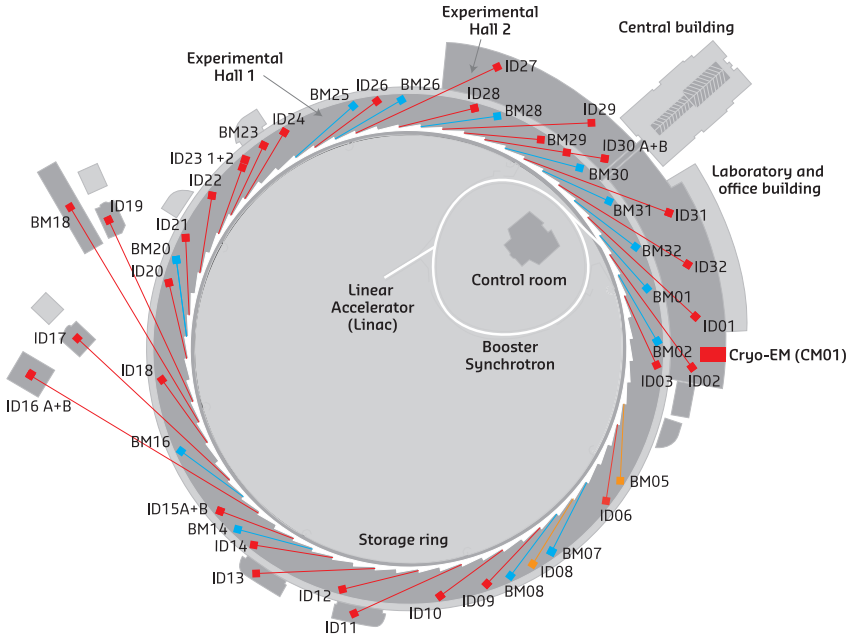


Figure 2.10: Schematic top view of the currently available beamlines at the ESRF. The beamline colour indicates its type as public (red), collaborating research group (blue) or instrumentation test (yellow) beamlines [35].

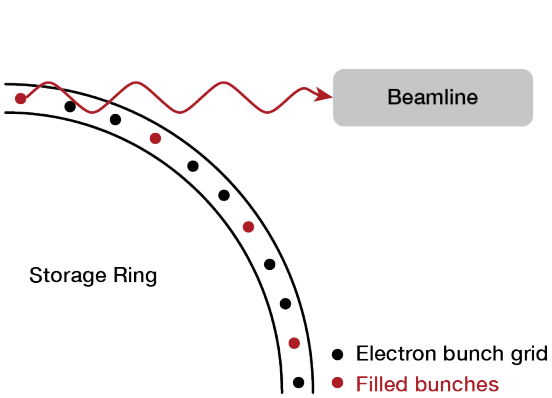
(LINAC) which uses sections of electromagnetic cavities operated by RF fields to increase the electron energy up to 200 MeV. With this energy, the electrons are guided to the booster synchrotron via a transfer line. With a circumference of about 300 m, this booster accelerates the electrons up to their final energy of 6 GeV. Upon reaching this energy, another transfer line guides the electrons into the storage ring.

2.3.4 Filling Patterns

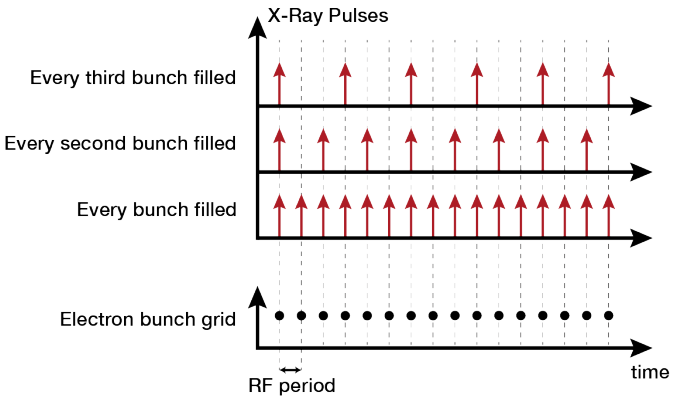
As explained in section 2.1, the stable operation of a synchrotron requires the electrons to travel in the ring grouped in bunches. The bunches are a result of the operation mode of the RF acceleration cavities stability and can be understood as a grid of "buckets" that can be filled with electrons. Particular configuration of filled and empty buckets is known as the filling pattern of the ring. The minimum granularity of this pattern is given by the period of the RF cavities.

As depicted in figure 2.11, an important consequence of the electron filling pattern is that the generated synchrotron light that reaches the beamlines is pulsed with a time structure given by the filling pattern. And the choice of the actual pulse pattern determines the kind of experiments that can be conducted at a given time. As a result, synchrotrons usually offer time periods with different patterns throughout the year which allows for a wider coverage of a variety of experiments.

The filling patterns most frequently used at the ESRF, which at the same time are the most challenging from a detector point of view, are shown in figure 2.12. The corresponding numbers have been taken from [25] and [37]. As illustrated, the orbit period of the ESRF storage ring is about 2.8 µs. With an RF frequency of roughly 352 MHz, there are 992 slots in the electron bunch grid which, if they are all filled, generate X-ray pulses with a repetition period of roughly 2.8 ns. The 7/8 + 1 mode exploits this high repetition rate to generate a quasi-continuous illumination for 7/8 of the storage ring orbit. An additional,



(a) Electron bunches in a storage ring. The black dots show the free, unoccupied bunches while the red dots indicate bunches filled with electrons.



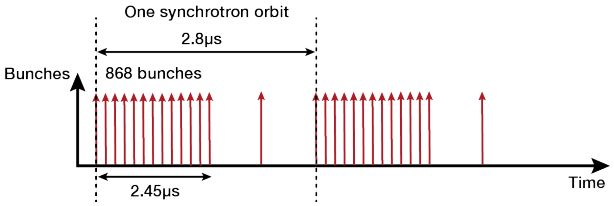
(b) X-ray pulses as seen by the experiment at the beamline depending on different bunch filling patterns. The top most pattern corresponds to the case depicted in figure 2.11a

Figure 2.11: Schematic demonstration of pulsed illumination which is a result of the bunching of electrons in the storage ring.

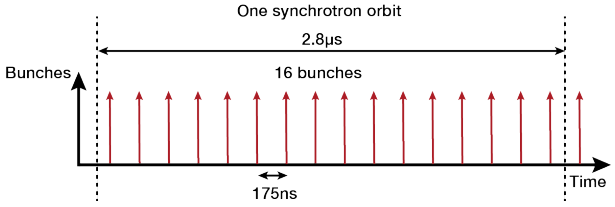
single, isolated pulse provides a distinct time structure for synchronization purposes.

In contrast to this, in the 16-bunch mode only 16 equally spaced electron bunches along the storage ring orbit are populated with electrons. The result is a repetition of X-ray pulses at a frequency of roughly 5.7 MHz, i.e. a spacing of about 175 ns making it the pulsed mode with the highest repetition frequency the ESRF has to offer. It is envisaged to be used for time-resolved measurements and, in order to be fully exploited, the detector needs to be able to resolve every single pulse in time, which means that it has to be able to record and process full images in 175 ns.

In between these two extremes, there are other intermediate filling modes with different foci, depending on the needs of the experiments at the beamlines. However, these two can be considered the benchmark for any detector that is to be used at or designed for optimum operation at the ESRF.



(a) 7/8 + 1 bunch mode: For 7/8 of a storage ring period, the ring is filled with electron bunches with 2.8 ns spacing, the shortest possible at the ESRF.



(b) 16-bunch mode: The storage ring is filled with 16 electron bunches. As a result, there are 16 x-ray pulses per storage ring period.

Figure 2.12: Most extreme bunch filling modes at the ESRF.

3 High-Z Semiconductor Sensors

For the requirements defined by the XIDer project, high-Z compound semiconductors are the most attractive choice as an X-ray photon detecting sensor material. This chapter gives a brief introduction to the properties of sensors based on high-Z compound semiconductor materials and uses the references [38], [39], [40], [41] and [42] in addition to those provided in the text.

3.1 Photon Detection & Signal Generation

For the detection of photons, their fundamental interaction mechanisms with matter are exploited. The three dominant mechanisms are the Compton effect, the photoelectric effect or photoelectric absorption, as well as the electron-positron pair production. Out of these, the photoelectric effect is the process with the highest cross-section in XIDer's aimed for energy range from 30 keV to 100 keV.

The photoelectric effect[1] denotes a process in which a photon is absorbed by an atomic electron to excite it from the semiconductor's valence to the conductance band. The cross-section σ_{pe} of this effect depends strongly on the nuclear charge Z of the absorbing material, such that

$$\sigma_{pe} \propto Z^n \tag{3.1}$$

where n depends on the photon energy and varies between 4 and 5. Subsequently, materials with higher atomic numbers are more efficient at absorbing and detecting photons via the photoelectric effect.

The electron that has been excited to the conductance band leaves behind a vacancy or *hole* in the valence band. Both the excited electron and the hole are so-called free charge carriers, which can move freely in the semiconductor. With the application of an electric field to the semiconductor, the electron-hole pair can be seperated. Their movement in the material induces a signal on the electrodes through which the electric field has been applied.

The number of electrons excited to the conduction band is proportional to the energy of the incident photon. Consequently, also the signal induced exhibits this same proportionality. As a result, by reading out the signal on one or both of the electrodes, the number of photons absorbed by the sensor can be reconstructed.

3.2 Sensor Material Choice

When a sensor is irradiated with a beam of many photons, for each photon there is a probability to be absorbed per distance travelled through the material. Thus, the beam is attenuated more and more, the further it travels through the material. This process is described by the Lambert-Beer law, which predicts the remaining beam intensity I after a given material depth x

$$I(x) = I_0 e^{-\mu x} \tag{3.2}$$

[1] In this context, only the *internal* photoelectric effect is dicussed.

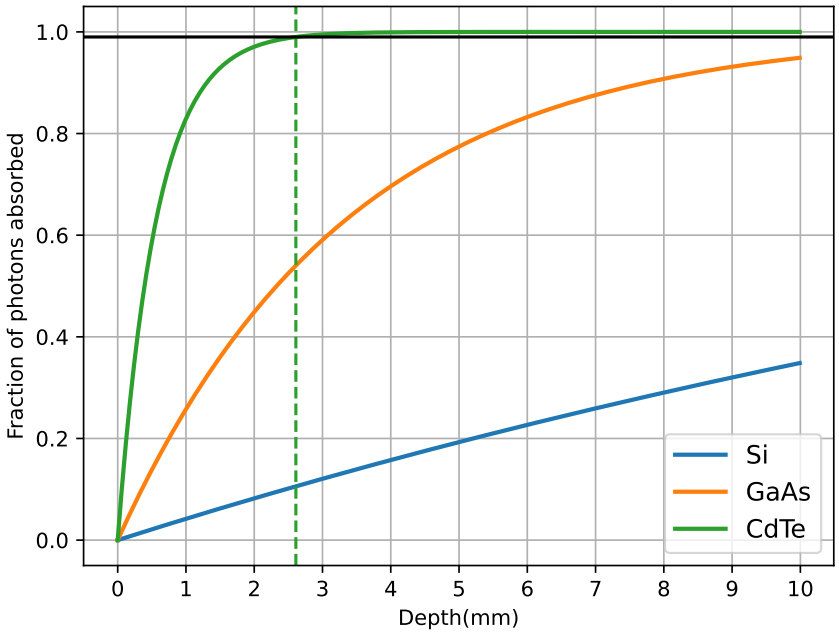


Figure 3.1: Absorption plot at an incident photon energy of 100 keV for different semiconductors. The dashed line shows the thickness of a CdTe sensor at which 99 % of the incident photons are absorbed on average. The underlying data for this plot has been taken from [43].

where I_0 is the initial intensity and μ is the attenuation coefficient which, because it considers effects like the photoelectric absorption, depends on both the material and the photon energy. The attenuation coefficient can be interpreted as the inverse of an attenuation length $\lambda = 1/\mu$. Then, λ denotes the average distance after which the beam's intensity has dropped to $1/e$ of the initial value. Subsequently, the smaller the value of λ, the higher the material's so-called *stopping power*.

For the choice of a detector's sensor material, its stopping power has a decisive impact. In case of XIDer, the X-ray energy range of 30 keV to 100 keV rules out one of the most common semiconductor sensor materials which is silicon. This is evident from figure 3.1. Here, the average absorption of an incident beam is plotted vs. the thickness of the material for a photon energy of 100 keV. Even after 10 mm of silicon, only roughly 35 % of the incident photons have been absorbed on average. In addition, a thick detector is undesirable, because of its reduced spatial resolution. The longer the travel time of the generated charge carrier cloud in the material, the larger its perpendicular spread due to diffusion.

Thanks to their high atomic numbers, both cadmium telluride (CdTe) and gallium arsenide (GaAs) are popular choices for X-ray detectors. However, as is evident from the plot, CdTe offers the highest stopping power in the XIDer's aimed for photon energy range which is why it has been chosen as the material of interest. In addition to the standard CdTe compound, there is another variation with cadmium zinc telluride (CdZnTe or CZT) which introduces a zinc component to the compound. With the right composition, CZT exhibits favourable properties to CdTe that are further discussed in the following sections. While the improved properties would make CZT the obvious choice for XIDer, its low availability make it difficult to obtain in large quantities.

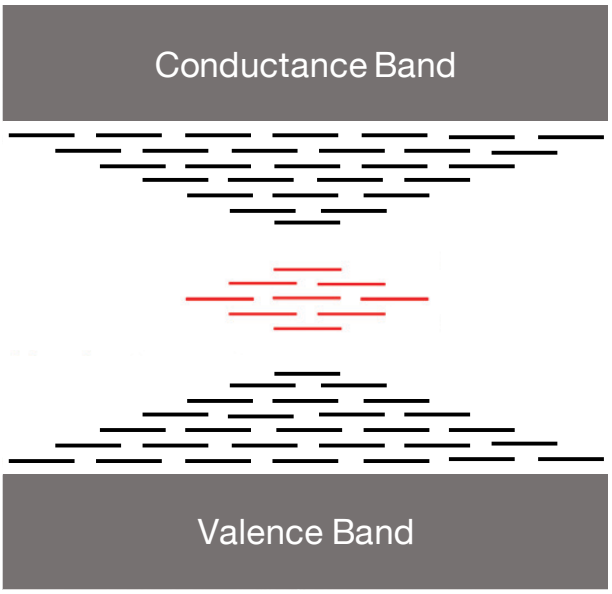


Figure 3.2: Schematic illustration of the different deep (red) and shallow (black) trap energy levels in a compound semiconductor. The schematic has been taken from [46] and modified.

Another advantage of CdTe and CZT is the large band gap energy E_g. While published measurements provide contradicting results, they vary in a range of 1.39 eV to 1.54 eV [44] for CdTe at room temperature.[2] For comparison, the bandgaps of silicon and germanium are 1.12 eV [38] and 0.67 eV [41], respectively. Subsequently, especially in the case of germanium, sensors have to be actively cooled to reduce noise contributions originating from thermal excitation across the bandgap.

3.3 Properties of High-Z Semiconductor Sensors

Independent of the actual material choice, all of the available high-Z compound semiconductors exhibit similar properties. On the one hand, their high absorption efficiency for X-rays and their high bandgap energy makes them desirable for room-temperature X-ray detectors. On the other hand, however, the compound nature of available materials imposes challenges in the production of homogeneous crystal lattices. Impurities emerging from the crystal growth, such as vacancies in the lattice, act as trap centres that can capture and release mobile charge carriers. These impurities give rise to complicated trapping and detrapping sensor dynamics [45].

In semiconductor physics, traps are associated with additional energy levels between the semiconductor's valence and conductance bands. Figure 3.2 provides an illustration of the abundance of trap energy states in a compound semiconductor. In CdTe, a vast amount of different trap energies has been measured with contradicting results. A detailed summary and discussion of the measured trap energies of CdTe can be found in [47]. This reflects the complicated nature of high-Z compound semiconductors and illustrates that there is no clear consensus on their behaviour in the science community. As a theoretical construct to describe the statistics of trapping and detrapping, the Shockley-Read-Hall (SRH) theory is applied. For more information the reader is referred to [45], [48] and [49].

[2] The addition of zinc usually leads to a slightly higher bandgap energy for CZT. The actual value, however, depends on the composition.

The following subsections focus on the effects of the trapping and detrapping dynamics.

3.3.1 Afterglow

As soon as a mobile charge carrier occupies one of these additional energy states, it can no longer contribute to the signal generation until it is released again which can occur on various timescales. Due to this effect, measured signals suffer from less steep rising edges and lower peak amplitudes. At the same time, trapped charge carriers which are released with a delay give rise to a long signal tail, the so-called *afterglow* or *aftersignal*.

The trapping process in a given material is often associated with the mobility-lifetime product of its charge carriers $\mu\tau$. This product gives a measure for the mean distance a charge carrier can travel through the material before it occupies a trap state. In general, $\mu\tau$ differs for holes (h) and electrons (e), such that $\mu_h\tau_h < \mu_e\tau_e$. In CdTe, for example, depending on the crystal purity, typical electron and hole mobility-lifetime products can be in the range of $1 \times 10^{-4}\,\mathrm{cm^2\,V^{-1}}$ to $2 \times 10^{-3}\,\mathrm{cm^2\,V^{-1}}$ and $1 \times 10^{-5}\,\mathrm{cm^2\,V^{-1}}$ to $1 \times 10^{-4}\,\mathrm{cm^2\,V^{-1}}$[50], respectively. In CZT, the disparity can be even larger with $8 \times 10^{-4}\,\mathrm{cm^2\,V^{-1}}$ to $9 \times 10^{-3}\,\mathrm{cm^2\,V^{-1}}$ and $3 \times 10^{-6}\,\mathrm{cm^2\,V^{-1}}$ to $6 \times 10^{-5}\,\mathrm{cm^2\,V^{-1}}$[50], respectively. Due to the largely reduced mobility-lifetime product of holes, XIDer, as per usual for detectors with CdTe/CZT sensors, has chosen to only read out the electron signal.

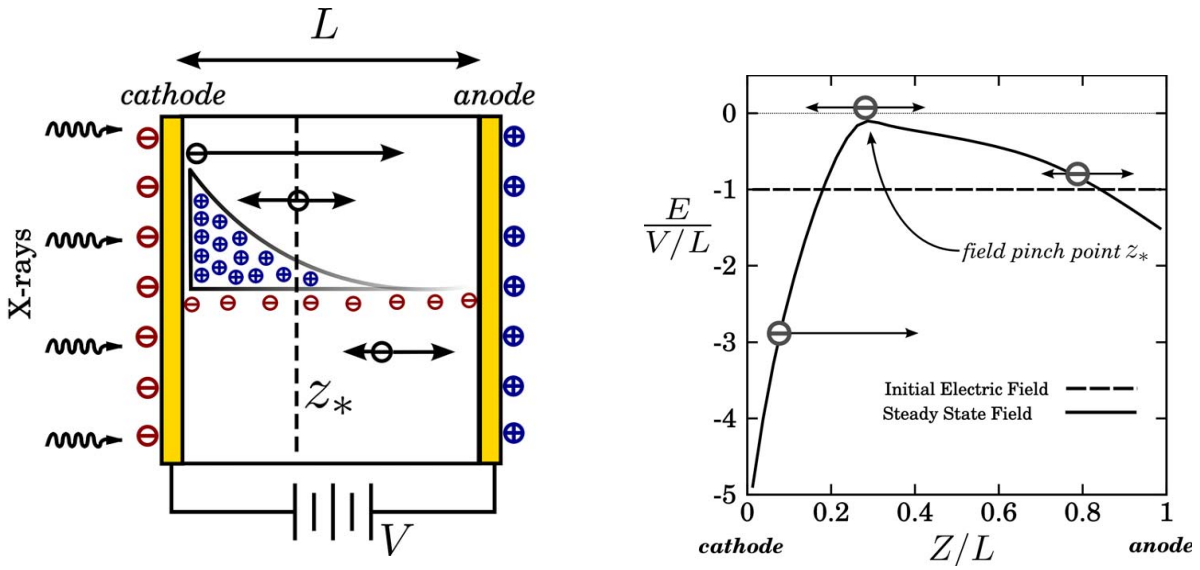
In contrast, the detrapping process is described with time constants $\tau_{d,i}$, each concerned with an individual trap energy state. The size of each $\tau_{d,i}$ depends on the difference of the trap energy and the conductance (electrons) or valence band (holes). The larger the energy difference, the longer the corresponding time constant. Subsequently, on average, charge carriers trapped in deep trap states take longer to be released than those trapped in shallow states. Typical time constants for CdTe are in the order of ns to hrs [51].

A direct consequence of the trapping and detrapping dependencies is that the signal read out by the sensor not only depends on the current illumination, but also on the illumination history. After a large signal, a lot of traps are filled that slowly release their stored charge. Any measurement during this release will be affected by charge stored in previous measurements. For XIDer, measurements with subsequent images spaced by several hundreds of ns are planned. In such a situation, the actual course of the afterglow dynamics is impossible to predict due to the number of overlapping signals. At the same time, waiting several tens of minutes after each measurement for the sensor to stabilize is not practically feasible. Subsequently, a proposal to measure the leakage in between measurements with dark frames has been made (see section 6.1.5) which, if implemented, will be unique to the XIDer detector.

As a side note: Prototype measurements with CdTe sensors presented in section 8 are performed with an initial stabilisation phase after biassing the sensor with the high voltage. In this stabilisation period, the sensor is given enough time to reach an equlibrium state in terms of trapping and detrapping dynamics.

3.3.2 Polarisation

The term *polarisation* is concerned with the unintended formation of local space charge clouds in the sensor. In Cd(Zn)Te, there are two kinds of polarisation, namely *dark* or *low-flux polarisation* and *high-flux polarisation*. Both phenomenons are bound to the low hole mobility-lifetime product, which is the cause of large local positive charge clouds that disrupt the electric field configuration. The result of these local electric field changes



(a) Sketch of the charge carrier concentrations in the sensor after a long ($\propto$ ms) high-flux irradiation [53].

(b) Pinch-off of the electric field underneath the cathode due to the formation of the large positive charge cloud [53].

Figure 3.3: High-flux polarisation of Cd(Zn)Te sensors.

is a reduced signal charge collection efficiency which in turn results in reduced signal amplitudes [45].

Dark polarisation mainly occurs in so-called *Schottky* contact configurations that introduce a diode structure at the sensor electrodes. Depending on the applied field, one of the diodes is biassed in reverse-mode, which greatly reduces the sensor's leakage current. However, it has been observed that applying a voltage to a blocking diode structure in CdTe can cause a deterioration of the electric field around the diode interface. This effect is caused by the formation of a charge cloud with a large concentration of detrapped holes in the vicinity of the blocking diode and is directly correlated to the contact interface design [52]. Since dark polarisation causes Schottky CdTe sensors to behave unreliably at room temperatue, XIDer mainly focusses on ohmic contact configurations that do not implement diode structures.

High-flux polarisation occurs at high incident photon fluxes, or more precisely, when the photoelectric absorption causes the formation of large charge clouds in the sensor. In order to understand this effect, figure 3.3a shows an illustration. In the usual configuration, the sensor is illuminated from the cathode-side. Upon absorbing incident photons, electron-hole pairs are generated. In this process, localized clouds of free charge carriers form. The mean distance of these charge clouds to the cathode depends on the incident photon energy which dictates the mean travel distance of a photon through the material, before it is absorbed.

Due to the electric field applied through the sensor electrodes, electrons drift to the anode and holes drift to the cathode. As a result of the low hole mobility-lifetime product, holes are much more susceptible to being trapped, i.e. held in place, than electrons. Subsequently, the electrons moving to the anode leave behind a large concentration of holes underneath the cathode. This hole cloud locally disrupts the electric field and can eventually cause a pinch-off, i.e. a collapse, as depicted in figure 3.3b [53].

Recently, with modifications to the crystal growth process, promising high flux variations of CdZnTe have been manufactured. These variations trade the electron mobility-lifetime

product for an increased hole mobility-lifetime product to decrease the charge cloud formation via trapped holes. In measurements presented in [54], two materials with hole mobility-lifetime products of $5 \times 10^{-6}\,\mathrm{cm^2\,V^{-1}}$ and $2 \times 10^{-5}\,\mathrm{cm^2\,V^{-1}}$ are compared. The increase by an order of magnitude leads to a higher measured flux counting rate by at least two orders of magnitude with $1 \times 10^{8}\,\mathrm{ph\,mm^{-2}\,s^{-1}}$. An even more promising variation called HFCdZnTe[3] manufactured by Redlen Technology [55] has been characterised to reach hole mobility-lifetime products of $3 \times 10^{-4}\,\mathrm{cm\,V^{-2}}$ [56].

[3] where HF stands for high flux

4 Introduction to Electronic Circuits

In order to design and implement sensor readout ASICs, a fundamental understanding of electronic circuits is necessary. This chapter gives a brief overview of the most important underlying concepts. It includes an introduction to system theory as a tool for the prediction of the behaviour of electronic circuits and an explanation of the working principle of MOSFETs combined with their small-signal description. In addition, chapter B in the appendix provides examples on how to apply system theory to actual circuits.

4.1 Introduction to System Theory

System theory is concerned with the mathematical description of dynamic systems. As such, it addresses the question of how characteristic parameters of a system change depending on provided input stimuli. In this regard, the term *system* describes a functional unit of compartments interacting with each other as well as their surroundings.

Due to its abstract nature, system theory is used in many different fields such as biology, physics or electronics. In the context of this thesis, it has been applied exclusively to the description of electronic ciruits. As the first step in the design process of analog circuitry, system theoretical calculations usually form the fundament. Thanks to the insights and predictions these calculations provide, they prove to be an essential toolkit for sophisticated designs with demanding constraints. For this reason, this section aims to introduce the necessary basics to understand the discussions provided in chapter 6. In order to compile the provided introduction, the references [57], [58] and [59] have been used.

4.1.1 Linear Time Invariant (LTI) Systems

Figure 4.1 shows a simplified illustration of how a system is treated in system theory. It is understood as a transformation that maps an input function $s(t)$ on an output function $g(t)$:

$$g(t) = T\{s(t)\}. \tag{4.1}$$

In analog electronics, these input and output functions are described by *signals*, time-dependent representations of the amplitude of physical quantities like, for instance, voltages, currents or field strengths. Due to this, signals are assumed to be real-valued and smooth time-domain functions. Simply put, this means that signals do not have abrupt or instantaneous changes or jumps. There are a few exceptions to the smoothness criterium

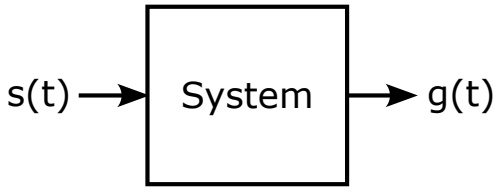


Figure 4.1: System theoretical understanding of a system with an input function $s(t)$ and an output function $g(t)$.

like the rectangular pulse function. However, these exceptions are solely employed in theoretical calculations. In real-world electronic circuits, even rectangular pulses are expected to be smooth due to their finite rise time. In addition to these criteria, another property of signals is that they tend to zero for $t \to -\infty$. For simplicity, functions will be associated with such signals from this point on.

In the wide range of systems described via 4.1, electronic circuits usually belong to a subset called *linear time-invariant*, henceforth denoted as LTI systems. These exhibit a specific set of properties. As the name implies, LTI systems are linear which means that a linear combination of input signals $s_i(t)$ results in a linear combination of output signals $g_i(t)$ such that

$$T\left\{\sum_i a_i s_i(t)\right\} = \sum_i a_i T\{s_i(t)\} = \sum_i a_i g_i(t) \tag{4.2}$$

with a_i being arbitrary constants.

The second important property of LTI systems is their time-invariance. For an input signal which has been shifted in time by an arbitrary amount t_0, the equation

$$T\{s(t-t_0)\} = g(t-t_0) \tag{4.3}$$

holds. This means that the actual shape of a circuit's output signal does not change with a time shift in the input signal. The output signal is simply shifted in time by the same amount.

4.1.2 The Laplace Transform

In the time domain, a system theoretical analysis of electronic circuits can be complicated and extensive. Even in passive circuits with capacitors, inductors and resistors, employing Kirchhoff's laws can lead to a set of differential equations. In more complex systems with more compartments as well as more complicated components like transistors the differential equations easily expand to unmanageable extents.

Instead of finding a solution in the time domain, it turns out that treating the system in the frequency domain is a much easier task. This is due to the properties of transformations which are employed to transfer equations from one domain to the other. The most widely known transformation of this kind is the Fourier transform. It provides a frequency domain representation $F(j\omega)$ to the time domain representation $f(t)$ of a given signal. The Fourier transform of $f(t)$ is defined via

$$\mathcal{F}(f(t)) = F(j\omega) = \int_{-\infty}^{\infty} f(t) e^{-j\omega t} dt \tag{4.4}$$

and divides the signal into its spectral constituents. While in general, $F(j\omega)$ itself is a complex function, the variable $\omega = 2\pi f$ is real-valued.

In order to guarantee that the integral in equation 4.4 is finite and exists, the weak Dirichlet condition

$$\int_{-\infty}^{\infty} |f(t)| dt < \infty \tag{4.5}$$

has to be met. In simple terms, this means that the amplitude of the signal's time domain representation has to approach 0 for $t \to \pm\infty$. However, unstable systems tend to oscillate with a fixed or even increasing amplitude after stimulating them with an input signal. As a result, they do not meet this condition and a finite frequency domain representation

$F(j\omega)$ can not be obtained with equation 4.4. With the Laplace transform, though, this problem is fixed by the introduction of an additional factor $e^{-\sigma t}$ in which $\sigma \in \mathbb{R}$ and $\sigma \geq 0$. The modified signal

$$\tilde{f}(t) = f(t)e^{-\sigma t} \tag{4.6}$$

then fulfills the Dirichlet condition

$$\int_{-\infty}^{\infty} |\tilde{f}(t)|dt = \int_{-\infty}^{\infty} |f(t)|e^{-\sigma t}dt < \infty \tag{4.7}$$

as long as σ is chosen big enough such that the growth of $f(t)$ does not exceed the decay of $e^{-\sigma t}$.

The Laplace transform is obtained by applying the Fourier transform on $\tilde{f}(t)$ instead of $f(t)$:

$$\mathcal{F}(\tilde{f}(t)) = \int_{-\infty}^{\infty} f(t)e^{-(\sigma+j\omega)t}dt = F(\sigma + j\omega).$$

Instead of the real-valued angular frequency ω, $F(\sigma + j\omega)$ acts on the variable $\sigma + j\omega$ which will henceforth be denoted as s. Subsituting $s = \sigma + j\omega$, the two-sided Laplace transform of a signal's time domain representation $f(t)$ is defined as

$$\mathcal{L}_2(f(t)) = F(s) = \int_{-\infty}^{\infty} f(t)e^{-st}dt. \tag{4.8}$$

As before, at the beginning of this chapter, actual real-world signals are expected to be zero for $t < 0$. Subsequently, circuit analysis usually uses the one-sided Laplace transform:

$$\mathcal{L}_1(f(t)) = F(s) = \int_{0}^{\infty} f(t)e^{-st}dt. \tag{4.9}$$

After solving the system of equations for the circuit at hand in the s-domain, the inverse Laplace transform can be used to transfer signals back to the time domain. It is defined as

$$\mathcal{L}^{-1}(F(s)) = f(t) = \frac{1}{2\pi j}\int_{\sigma-j\cdot\infty}^{\sigma+j\cdot\infty} F(s)e^{st}ds. \tag{4.10}$$

As a side note: The Laplace transform can be understood as a Fourier transform with an additional weighting factor $e^{-\sigma t}$. If the integral converges even for $\sigma = 0$, which is the case for signals of stable LTI systems, the Fourier and Laplace transforms are linked via the substitution $s = j\omega$. Due to this, the variable s can be interpreted as a complex frequency. As a consequence, the terms *s-domain* and *frequency domain* will be used synonymously henceforth.

The main advantage of analysing a circuit in the frequency domain compared to the time domain is that the system of equations is easier to solve. Among other simplifications that happen during the transformation, this is mainly due to how time related differential operators act in the frequency domain. After the application of Kirchhoff's laws to a circuit, the general shape of the system of equations describing the circuit signals in the time domain is given by

$$\sum_{k=0}^{m} b_k \frac{\partial^k x(t)}{\partial t^k} = \sum_{i=0}^{n} a_i \frac{\partial^i y(t)}{\partial t^i}. \tag{4.11}$$

Here, $x(t)$ and $y(t)$ are the circuit's input and output signals. The coefficients a_i and b_k

contain information about the parameters of components present in the circuit as well as how they are arranged. Applying the Laplace transform to the derivative of an arbitrary signal $f(t)$ yields:

$$\mathcal{L}\left(\frac{\partial^i f(t)}{\partial t}\right) = s^i F(s) \tag{4.12}$$

As a result, the system of equations transforms to the general shape of

$$\sum_{k=0}^{m} b_k s^k X(s) = \sum_{i=0}^{n} a_i s^i Y(s) \tag{4.13}$$

with polynomials instead of differential operators. While $x(t)$ and $y(t)$ are transformed into their s-domain counterparts $X(s)$ and $Y(s)$, the coefficients a_i and b_k are unaffected.

As an aside: Another important property of the Laplace transform is its action on convolutions. The convolution theorem says

$$\mathcal{L}(c(t) * d(t)) = \mathcal{L}(c(t)) \cdot \mathcal{L}(d(t)) \tag{4.14}$$

for the arbitrary signals $c(t)$ and $d(t)$.

4.1.3 Transfer Function

Every LTI system can be described both in the time and frequency domains. The corresponding functions are the impulse response $h(t)$ and its Laplace transform, the transfer function $H(s)$. For brevity, explanations regarding their deviation are skipped at this point. A more detailed description can be found in chapter A.1 in the appendix.

For a system with the input $X(s)$ and the output $Y(s)$, the transfer function is given via

$$H(s) = \frac{Y(s)}{X(s)}. \tag{4.15}$$

In the case of several chained LTI systems with the impulse responses $h_1(t)$, $h_2(t)$, ..., the output response y(t) to an arbitrary input signal $x(t)$ is given as $y(t) = x(t) * h_1(t) * h_2(t) * \ldots$. Here, the operator $*$ denotes a convolution. Due to the convolution theorem, this simplifies to $Y(s) = X(s) \cdot H_1(s) \cdot H_2(s) \cdot \ldots$ in the s-domain. Subsequently, the transfer function $H_{tot}(s)$ of a chain of n circuits can be calculated via:

$$H_{tot}(s) = \prod_{i=0}^{n} H_i(s). \tag{4.16}$$

4.1.3.1 Poles & Zeroes

When $H(s)$ has been obtained, an inverse Laplace transform allows the determination of the impulse response and with it the circuit's time domain behaviour. However, instead of transforming $H(s)$ back to the time domain, experienced analog designers analyse the transfer function in the s-domain. This is due to the fact that transfer functions of different systems contain reoccuring constituents. With the knowledge of how these are transformed, one can predict the circuit's behaviour without performing the actual transformation. Due

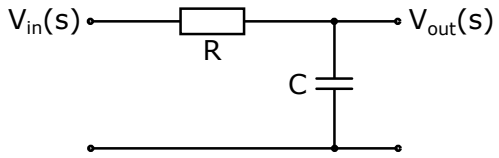


Figure 4.2: Schematics of an RC circuit.

to the polynomial structure of $X(s)$ and $Y(s)$, $H(s)$ can be rewritten such that

$$H(s) = H_0 \frac{\prod_{i=0}^{n}(s - Z_i)}{\prod_{k=0}^{m}(s - P_k)}, \qquad H_0 \in \mathbb{R}; \{Z_i\}, \{P_k\} \in \mathbb{C}. \tag{4.17}$$

In this context, Z_i are called zeroes of $H(s)$ because the transfer function equals zero, if $s = Z_i$. P_k, on the other hand, are called poles, because $H(s)$ approaches infinity for $s \to P_k$. The positions of both zeroes and poles give insight into the frequency dependant response of the analysed circuit. For example, $H_a(s)$ is assumed to be the transfer function of a simple circuit that has a single pole at $s = a$

$$H_a(s) = \frac{a}{s - a}$$

In this case, the inverse Laplace transform yields the impulse response

$$h_a(t) = \mathcal{L}^{-1}(H_a(s)) = ae^{at}. \tag{4.18}$$

This leads to the conclusion, that the circuit can only be stable, if the real part of a is smaller than 0. This is a general rule which is also true for more complicated circuits. A circuit can only be stable, if the real parts of poles are smaller than 0. And in the given example, only if $a < 0$, $h_a(t)$ shows an exponential decay. A very prominent example for such a circuit is the RC low-pass filter as depicted in figure 4.2. Deriving $H_{RC}(s) = {}^{V_{out}(s)}/_{V_{in}(s)}$ can easily be performed by using Kirchhoff's laws as well as the s-domain impedance representations for resistors $Z_R = R$ and capacitors $Z_C = {}^{1}/_{sC}$. The circuit can be treated as a voltage divider such that

$$H_{RC}(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{Z_C}{Z_R + Z_C} = \frac{{}^{1}/_{sC}}{R + {}^{1}/_{sC}} = \frac{{}^{1}/_{RC}}{s + {}^{1}/_{RC}} \tag{4.19}$$

Subsequently, for the RC low-pass filter, the pole is located at $s_P = -1/RC$ and its time domain impulse response is given as

$$h_{RC}(t) = \frac{1}{RC} \cdot e^{-\frac{t}{RC}} \tag{4.20}$$

Since resistances and capacitances are always real-valued and positive, the pole s_P of an RC low-pass filter is always a negative real value. Thus, on its own, this circuit always exhibits stable operation. As a more general note: It turns out that the existence of poles and zeroes in systems allows an immediate prediction of constituents of the time domain impulse response. As a matter of fact, the existence of a pole at $s_P = \sigma + j\omega_P$ always implies the existence of at least one exponential function of the shape $e^{s_P t}$ in the time domain impulse response.

In more complicated circuits, poles can reveal even more information about the system's frequency and time dependent properties. The transfer function of an RLC circuit as

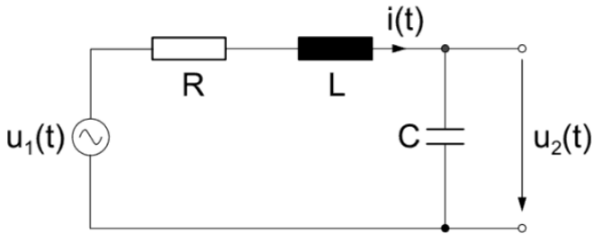


Figure 4.3: Schematics of an RLC circuit with an ac input signal [57].

depicted in figure 4.3 for example is given by

$$H_{RLC}(s) = \frac{U_2(t)}{U_1(t)} = \frac{{}^{1}/_{LC}}{s^2 + ({}^{R}/_{L})s + {}^{1}/_{LC}} \tag{4.21}$$

with its poles at

$$s_{P1,2} = -\frac{R}{2L} \pm \sqrt{\frac{R^2}{4L^2} - \frac{1}{LC}}. \tag{4.22}$$

For further reference, the consituents of $s_{P1,2}$ are denoted as $a = -\frac{R}{2L}$ and $b = \sqrt{\frac{R^2}{4L^2} - \frac{1}{LC}}$. An inverse Laplace transform of $H_{RLC}(s)$ yields

$$h_{RLC}(t) = \mathcal{L}^{-1}(H_{RLC}(s)) = \frac{1}{bL} e^{at} \left(\frac{e^{bt} - e^{-bt}}{2} \right) \tag{4.23}$$

Here, the values of a and b determine the actual shape of $h_{RLC}(t)$. Especially for b, this is due to the fact that the argument of its square root can either be positive or negative. As a result, b itself and thus the poles can either be real or imaginary numbers. In the case that b is real, i.e. $\frac{1}{LC} < \frac{R^2}{4L^2}$, the impulse response $h_{RLC}(t)$ simplifies to

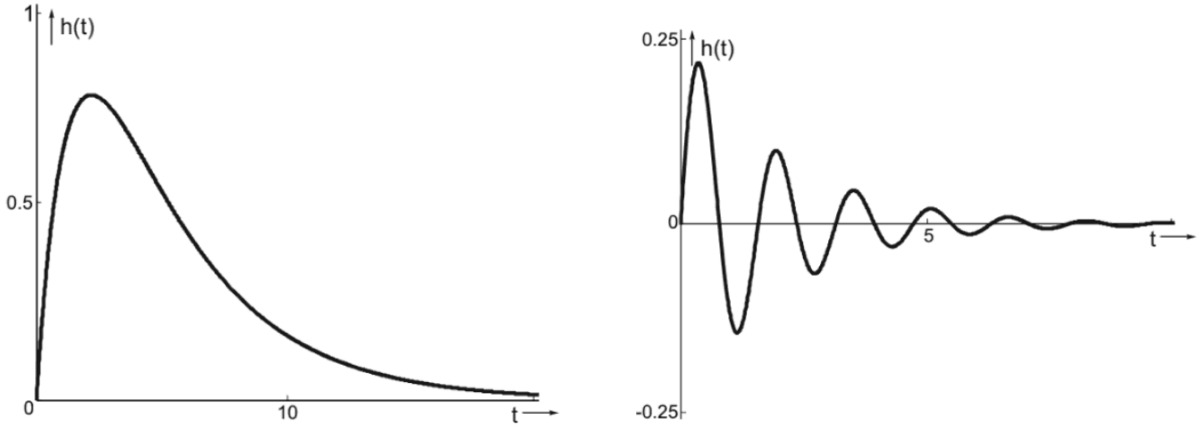
$$h_{RLC,r}(t) = \frac{1}{bL} e^{at} sinh(bt) \tag{4.24}$$

As shown in figure 4.4a for a negative a, $h_{RLC,r}(t)$ shows a quick rise followed by an exponential decay. However, if b is imaginary, i.e. $\frac{1}{LC} > \frac{R^2}{4L^2}$, the impulse response features a sine wave

$$h_{RLC,i}(t) = \frac{1}{\beta L} e^{at} sin(\beta t), \qquad b = j\beta. \tag{4.25}$$

as depicted in figure 4.4b. As a result, the circuit is subject to an oscillation with the angular frequency β enveloped by the exponential function e^{at}. As for the RC low-pass, whether the circuit is stable is dictated by the size of the poles' real part a. If $a < 0$ which is the depicted case, the oscillation is damped and its amplitude disappears over time. Since R and L can only be real-valued and positive, a can only have a real, negative value in this case. Thus, e^{at} can only act as an exponential decay ensuring the circuit's stability. The following list is supposed to summarize the most important properties of poles and their implications for a system's time domain behaviour:

- In general, poles of transfer functions are complex numbers.
- The existence of a pole s_P in the transfer function dictates the existence of at least one exponential function $e^{s_P t}$ in the impulse response.



(a) Real b: No oscillation

(b) Imaginary b: $u_2(t)$ reacts with an oscillation to a δ distribution at the input

Figure 4.4: Impulse responses of a stable RLC system, i.e. $a > 0$ [57]

- If the imaginary part of s_P is unequal to 0, the circuit performs an oscillation in the time domain.

- The polarity of s_P's real part determines whether the corresponding circuit is stable. Only if it is negative, the amplitude of the respective output quantity decays over time.

In addition, zeroes can be used to get rid of undesired poles in a circuit. This is evident from the general shape of a transfer function illustrated in equation 4.17. If a zero has the same value as a pole $Z_i = P_k$, the term $(s - Z_i)$ cancels out $(s - P_k)$. Designers can exploit this by introducing a zero into a circuit to improve its performance, e.g. by getting rid of a pole that causes an instability. This method is called *zero-pole-cancellation*. More details on this can, for instance, be found in [41].

Due to the reoccurence of similar terms in transfer functions, designers started compiling and employing tables listing transformations of common functions. Such a table is attached in chapter A.2 in the appendix.

4.1.3.2 Gain, Phase & Bode Plots

Since the value of a system's transfer function $H(s)$ at a given s is a complex quantity

$$H(s) = Re[H(s)] + jIm[H(s)], \tag{4.26}$$

it can also be described via its absolute value and phase in the complex plane:

$$H(s) = |H(s)|e^{j\phi(s)}. \tag{4.27}$$

$|H(s)|$ describes the gain between the input and output signals depending the variable s. Its value is calculated via

$$|H(s)| = \sqrt{(Re[H(s)])^2 + (Im[H(s)])^2} = \sqrt{H(s)H^*(s)}. \tag{4.28}$$

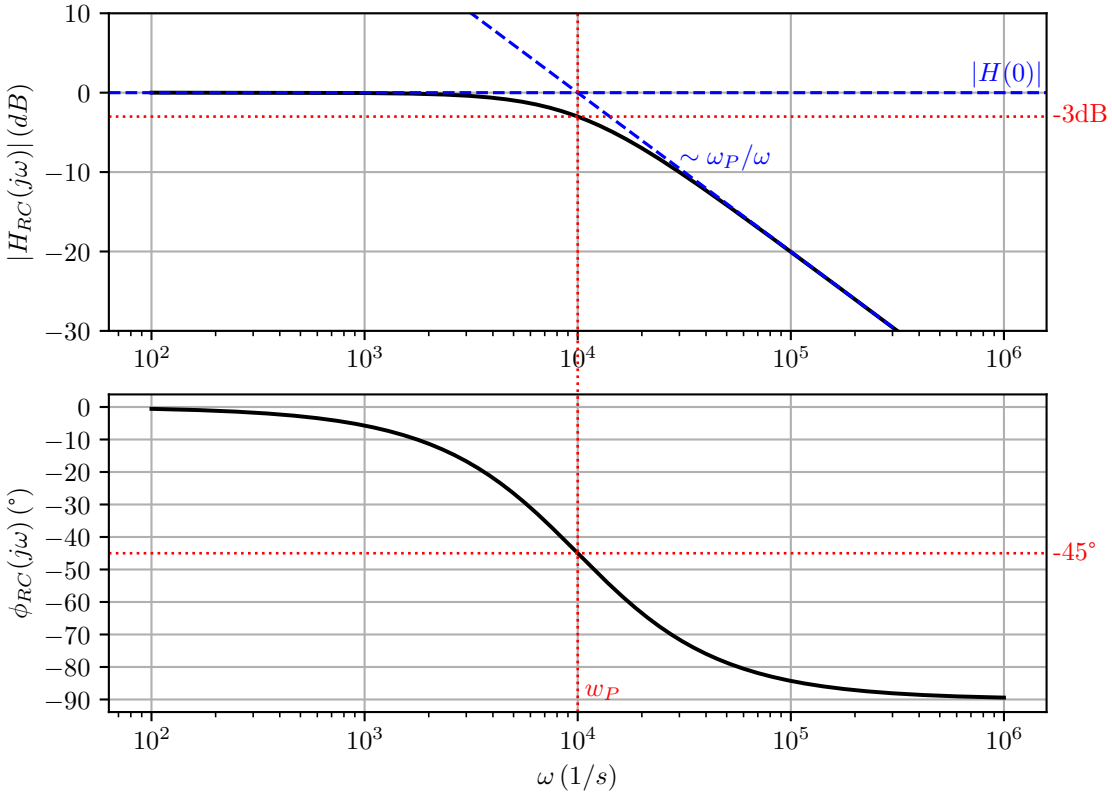


Figure 4.5: Bode plot for an RC low-pass with a pole at $\omega_P = 1 \times 10^4\,\mathrm{s}^{-1}$.

The phase $\phi(s)$ can be determined with

$$\phi(s) = arctan\left(\frac{Im[H(s)]}{Re[H(s)]}\right). \tag{4.29}$$

The meaning of $\phi(s)$ is more obvious when considering the transfer function's definition in equation 4.27. With $X(s)$ and $Y(s)$ as the input and output signals respectively, $H(s)$ can also be written as

$$H(s) = \frac{Y(s)}{X(s)} = \frac{|Y(s)|}{|X(s)|} \cdot e^{j(\phi_Y(s) - \phi_X(s))}. \tag{4.30}$$

Here, $X(s)$ and $Y(s)$ have been split into absolute values and phases $\phi_Y(s)$ and $\phi_X(s)$ just like $H(s)$ in equation 4.27. As can be seen $\phi(s) = \phi_Y(s) - \phi_X(s)$ which means that it contains the phase difference of the output signal to the input signal at a given value of s.

With the substitution $s = j\omega$, the gain $|H(j\omega)|$ and phase $\phi(j\omega)$ can be analysed and plotted vs. the frequency of an input signal. In this approach, the circuit is stimulated with a sine wave with the constant angular frequency ω. The analyzed output quantity oscillates at the same frequency, but with an amplitude and a phase shift given by $|H(j\omega)|$ and $\phi(j\omega)$. A corresponding graph visualizing this for a wide range of frequencies is called *Bode plot*.

Figure 4.5 illustrates such a Bode plot at the example of an RC low-pass filter with frequency axes in logarithmic scale. As derived in equation 4.19, this circuit's transfer

function is $H_{RC}(s) = \frac{1/RC}{s+1/RC}$. The substitution leads to

$$H_{RC}(j\omega) = \frac{1/RC}{j\omega + 1/RC} \tag{4.31}$$

and its gain and phase are:

$$|H_{RC}(j\omega)| = \frac{1}{RC}\sqrt{\frac{1}{1+\omega^2(RC)^2}} \tag{4.32}$$

$$\phi_{RC}(j\omega) = arctan(-\omega RC) \tag{4.33}$$

For $\omega = 0$ there is no phase shift and the gain is equal to 1. As soon as the frequency approaches the circuit's pole $\omega_P = \frac{1}{RC}$, these values start changing. Here, the gain starts to drop. At exactly $\omega = \omega_P$, the gain is at $|H_{RC}(j\omega)| = \frac{1}{\sqrt{2}}$. This is the famous 3 dB- or cut-off frequency. Its name stems from the fact that Bode plots tend to use the decibel unit for the gain's y-axis which is defined via $y(\omega) = 20log|H(j\omega)|[dB]$. Hence, if $H(j\omega_P) = \frac{1}{\sqrt{2}}$, then $y(\omega_P) = -3dB$. Consequently, at the frequency ω_P the gain has reduced to -3 dB which means that the output signal is damped in relation to the input. For frequencies bigger than the cut-off frequency, the gain keeps dropping with a $1/\omega$ dependency. Since both axes in a Bode plot use a logarithmic scale, this dependency is depicted by a line in the gain plot.

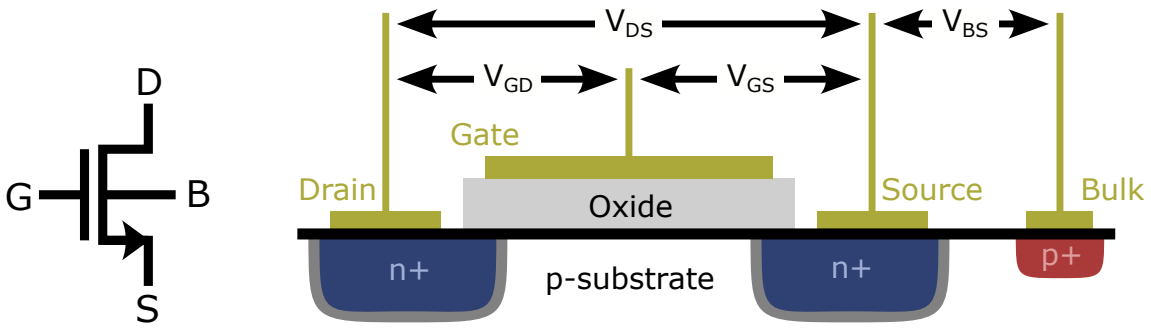
Due to the fact that above the cut-off frequency the gain starts to drop, ω_P can be interpreted the *bandwidth* of the RC low-pass. And since the gain of many circuits actually acts similar to that of the RC low-pass, the 3 dB- or cut-off frequency has become a broadly used quantity to characterize a circuit's frequency response. In more complicated circuits however, there can be multiple poles and the cut-off frequency is not necessarily at a pole frequency. But every pole causes a bend as the one shown in figure 4.5, each decreasing the slope of the depicted line by 20 dB per frequency decade. As a side note: The depicted RC low-pass employs unity gain for low frequencies. For amplifying circuits, the gain at low frequencies is usually much higher than unity before it starts dropping just like for the RC low-pass. In this case, an alternative way to define the circuit's bandwidth is the frequency at which its gain has dropped to unity gain. Fittingly, this is the so-called *unity-gain bandwidth*.

As shown in the phase plot, a pole in the transfer function also causes a phase shift between the output and input signal. While for low frequencies this shift is not yet present, it reaches a value of $-45°$ at $\omega = \omega_P$. Subsequently, the sine wave at the circuit's output is delayed by 1/8 of its period in relation to the input. If $\omega \to \infty$, the phase shift approaches $-90°$. As a side note: zeroes create bends that *increase* the gain's slope by 20 dB per frequency decade. They also cause phase shifts that behave in the same way as for poles but with opposite polarity such that for $\omega \to \infty$: $\phi(j\omega) \to +90°$.

4.2 The MOSFET

The metal-oxide semiconductor field effect transistor (MOSFET) has become the foundation for the implementation of digital and analog circuits in CMOS technology[1]. This section is supposed to give an introduction to its operation principle with a focus on

[1] CMOS stands for complementary metal-oxide semiconductor



(a) Schematic symbol

(b) Cross-section with the most important voltages

Figure 4.6: Sketches of an n-MOSFET

analog features and behaviour. It starts with an overview of the topology, continues with a presentation of its basic physical properties and mathematical description and ends with insights into its noise behaviour. All of the provided descriptions and explanations are based on the references [38], [60] and [61]. Basic knowledge about semiconductor physics, the process of doping and pn junctions is required. For an introduction to these topics, the reader is referred either to the references [38] or [40] for a more fundamental discussion.

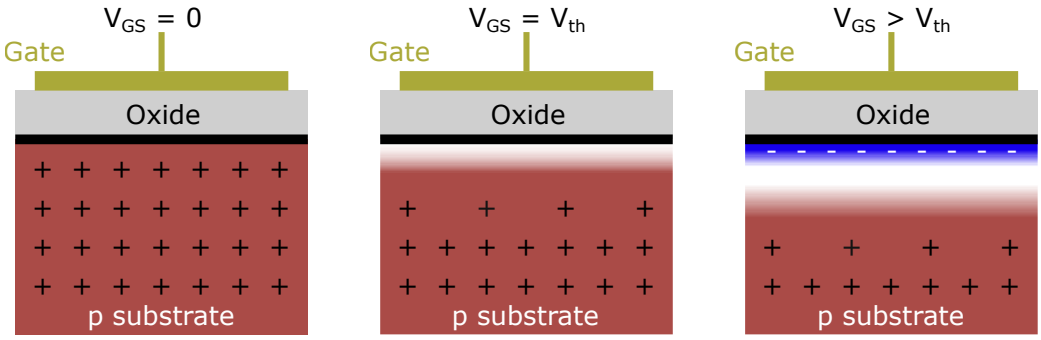
4.2.1 Topology & Large Signal Properties

Among many slightly different variations, CMOS technologies provide two basic, complementary MOSFET types. Both n-type and p-type MOS transistors follow the same operation principle but with different polarities in their control voltages and currents. For clarity, the following explanations focus on the n-MOS.

Figure 4.6a shows the schematic symbol of an n-MOS transistor. The voltages and currents applied to its four terminals, the gate (G), source (S), drain (D) and bulk (B), dictate its behaviour. As far as source and drain terminals go, the MOSFET is symmetric which means that they are interchangeable. In actual operation, the source terminal is defined as the node with the lowest voltage and acts as a voltage reference for the other terminals. Since the bulk has a rather special function and is best shorted to the source terminal for basic operation, it will be treated as such throughout this section, if not mentioned otherwise.

In the most simple view – and this is how the transistor is used in digital electronics – the MOSFET acts as a switch. If the gate terminal is at a logic "high", source and drain are shorted. And they are isolated, if the gate terminal is held at a logic "low". In an analog view however, this simplified description is far from sufficient.

A more detailed illustration is provided in figure 4.6b. It shows a simplified cross section of the physical structure of an n-MOS transistor. A slightly p-doped substrate forms the foundation. The substrate is biased via a strongly p-doped contact with a metal contact on top which is the aforementioned bulk terminal. In this substrate, there are two n+-doped, i.e. strongly n-doped, regions with a metal contact each. These are the source and drain terminals. And in between source and drain, there is a thin oxide layer usually made of SiO_2 covered by a poly-silicon sheet which implements the gate terminal. The drawing also defines the voltages necessary for the operation of an n-MOS transistor in reference to the source potential. The corresponding notation is chosen such that the voltage of terminal X in reference to the source voltage is given by $V_{XS} = V_X - V_S$.



(a) (b) (c)

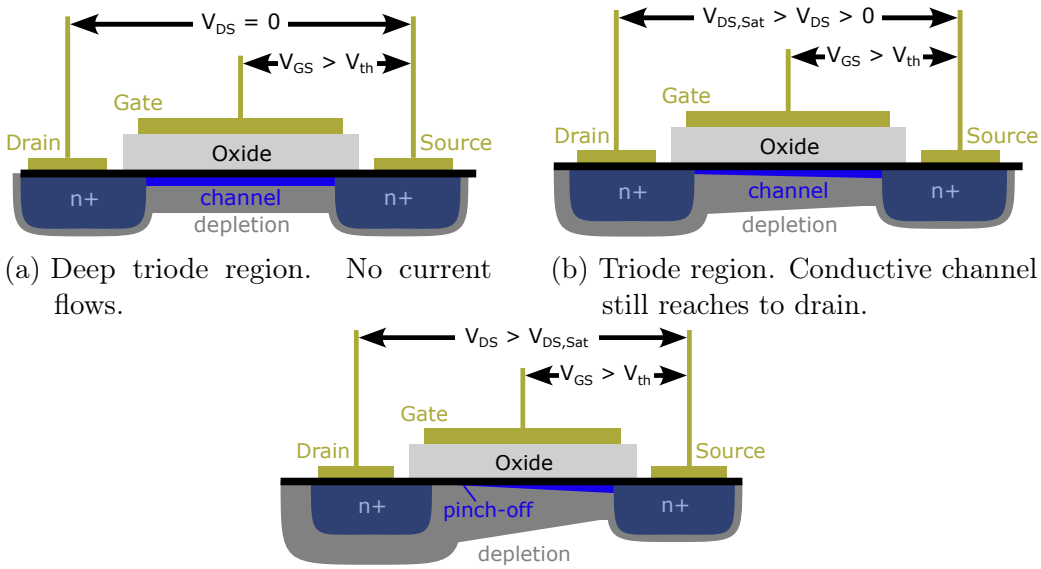
Figure 4.7: Illustration of the effect of the gate-source voltage V_{GS} on the mobile charge carrier densities at the substrate's surface underneath the gate of an n-MOS transistor. a) No gate voltage applied: p-substrate is unchanged. b) $V_{GS} = V_{th}$: Electron and hole densities at substrate surface are equal. The conductive channel is starting to form. c) $V_{GS} > V_{th}$: Electron density is bigger than hole density at substrate surface. The transistor is in the inversion region and a conductive channel has been formed.

The n+ regions of the source and drain form two diodes with the p-substrate. The dark grey halos around the n+ implantations illustrate the respective depletion regions formed in the substrate. From a drain-to-source perspective, these diodes are placed in series but in opposite direction. If there are no voltages applied, as in the depicted case, there is no current flowing between the source and drain contacts except the diode leakage current. This can be changed with the gate-source voltage V_{GS}: the unit of gate, insulator and bulk can be seen as a capacitor. Increasing the gate voltage in relation to the bulk (which is shorted to the source) causes a repelling force on holes in the p-substrate. Subsequently, holes at the surface are pushed deeper into the substrate. If the gate voltage is increased even further, electrons are attracted from the bulk to the surface. And at some point, the electron density equals the hole density at the substrate's surface right underneath the gate. The corresponding gate source voltage for this state which is depicted in figure 4.7b is the so-called *threshold voltage* V_{th}. Increasing V_{GS} from this point on drives the transistor into *inversion* and a *conductive channel* of electrons is formed. In this state, the minority charge carriers, i.e. electrons in p-doped silicon, now form the actual majority at the substrate surface. Correspondingly, the region of gate-source voltages for which $V_{GS} > V_{th}$ is denoted as *inversion region*. This state is illustrated in figure 4.7c.

As soon as the conductive channel of electrons is intact, a current can flow between source and drain. In order to achieve an actual flow, a voltage drain-source voltage $V_{DS} > 0$ has to be applied. As before, the source potential is held at the same voltage. An increase in V_{DS} is actually achieved by only increasing V_D. For a fixed $V_{GS} > V_{th}$, figure 4.8 displays different states and tipping points in the transistor's characteristic behaviour depending on the value of V_{DS}. The first depicted state in which $V_{DS} = 0$ has already been discussed. Here, the conductive channel has been formed, but there is no current flow. By increasing V_{DS} from this point on, the flowing drain-source current I_D follows:

$$I_{D,tr} = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right). \tag{4.34}$$

μ_n is the electron mobility, C_{ox} is the gate capacitance per area and W and L are the



(a) Deep triode region. No current flows.

(b) Triode region. Conductive channel still reaches to drain.

(c) Saturation region with pinched-off conductive channel.

Figure 4.8: N-MOS transistor cross-sections in different operating regions.

width and length of the transistor. In this voltage region, the so-called *triode region*, I_D is highly dependant on both V_{GS} and V_{DS}. The corresponding state is depicted in figure 4.8b. While the actual dependency of I_D on V_{DS} is parabolic, the MOSFET is often considered a linear device with $I_D \propto V_{DS}$ at low V_{DS}. This is due to the fact that for low enough voltages $V_{DS} < 2(V_{GS} - V_{th})$, in the so-called *deep triode region*, equation 4.34 can be simplified to

$$I_{D,tr} \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) V_{DS}. \tag{4.35}$$

As a result of this linear relation, one can attribute a resistance to the transistor's drain-source channel:

$$R_{on} = \frac{1}{\mu_n C_{ox} {}^{W}/_{L} (V_{GS} - V_{th})}. \tag{4.36}$$

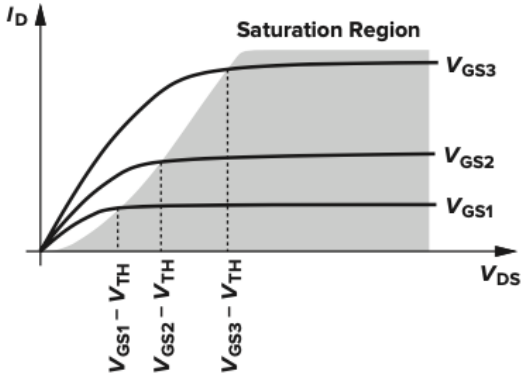
Subsequently, the MOSFET acts like a controllable resistor which explains aforementioned use as a switch.

When increasing the drain-source voltage V_{DS}, the potential difference between the gate and drain V_{GD} decreases. Since this is the voltage that forms the conductive channel at the drain contact, the inversion at the drain is getting weaker. As soon as V_{GD} is too small to generate the inversion at the drain, the conductive channel is *pinched-off*. This state is depicted in figure 4.8c. The pinch-off value of

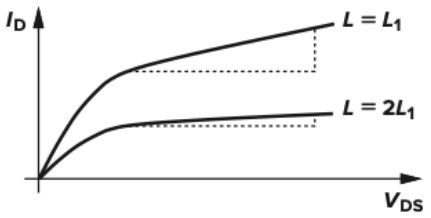
$$V_{DS,Sat} = V_{GS} - V_{th} \tag{4.37}$$

marks an important point in the MOSFET's IV-characterstic. For $V_{DS} \geq V_{DS,Sat}$, the transistor enters the *saturation region*. In the first order approximation, the drain current I_D of transistors in saturation no longer depends on the drain-source voltage. The corresponding equation describing I_D for this condition is given by

$$I_{D,Sat} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2. \tag{4.38}$$



(a) Without channel length modulation and at different values of $V_{GS} > V_{th}$.



(b) With channel length modulation at different transistors lengths L.

Figure 4.9: N-MOS transistor IV-characteristic [60].

From this equation, one can derive a relation between a transistor's saturation voltage and its drain current:

$$V_{DS,Sat} = \sqrt{\frac{2I_{D,Sat}L}{\mu_n C_{ox} W}} \tag{4.39}$$

Beyond the behaviour described by the first-order approximation, second-order effects often play an important role in the performance of a circuit. One of these effects is the *channel-length modulation*. By increasing V_{DS} even further above $V_{DS,Sat}$, the point at which the channel is pinched off moves closer to the source terminal. As a result, the length of the channel decreases and with it the effective transistor length L. In order to describe this effect, an additional factor has to be added:

$$I_{D,Sat,cl} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \tag{4.40}$$

in which λ is the *channel length modulation coefficient*. So, in reality, I_D still shows a slight V_{DS} dependency. This effect is often referred to as the *Early effect*.

Figure 4.9a shows a set of curves of the typical IV-characteristic of the MOSFET neglecting the Early effect. The x-axis shows the applied drain-source voltage V_{DS} with the resulting current I_D on the y-axis. The different curves are the result of different gate-source voltages V_{GS}. At low V_{DS}, the deep triode region is visible via the linear rise of I_D. Moving closer to the saturation voltage, the parabolic nature becomes evident. And as soon as V_{DS} reaches the saturation voltage, I_D saturates as indicated by equation 4.38. In the graph, this is illustrated by the grey region.

With a higher gate-source voltage, the transition from the triode to the saturation region shifts to higher V_{DS}. This is obvious from equation 4.37 because the saturation voltage $V_{DS,Sat}$ depends on V_{GS}. And since I_D is proportional to V_{GS}^2, it shows the same proportionality to $V_{DS,Sat}$ in the plot.

Figure 4.9b shows the effect of the channel length modulation. Instead of saturating at a fixed value, I_D shows a linear rise with V_{DS} in the transistor's saturation region, matching with equation 4.40. As indicated in the graph, the slope is proportional to $1/L$ of the transistor. This is due to the fact that the relative change of the transistor's effective channel length has a larger relative effect for short transistors compared to long ones.

Among many others, there are a two more second-order of the MOSFET worth men-

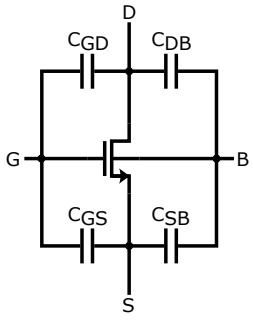


Figure 4.10: Parasitic capacitances of an n-MOS in inversion mode.

tioning before moving on: Firstly, up to this point, the transistor has been considered off or not conductive in the *subthreshold region*, i.e. $V_{GS} < V_{th}$. In reality, this is not the case. With ever-decreasing supply voltages and low power demands, the importance of this region for analog design keeps increasing. Since it has not yet been relevant in the analog design of XIDer's readout ASIC, though, this section does not discuss the subthreshold region. The interested reader is referred to [62].

Secondly, in the discussions above, the bulk contact has been shorted to the MOSFET's source contact. This is due to the *body* or *back-gate effect* which influences the threshold voltage V_{th}. By decreasing the bulk voltage such that $V_{BS} < 0$, holes move to the bulk contact, leaving more negative charge underneath the gate oxide. As a result, the gate contact has to accumulate more positive charge to match the negative charge at the substrate surface. Subsequently, the effective threshold voltage is increased. In large designs however, many transistors share the same substrate, i.e. the bulk contact is shorted. As a result, it is not possible to simply adjust the bulk voltage for each individual transistor. In order to achieve this, special precautions such as the placement of extra wells (see below) have to be made. Due to this complication, the manipulation of threshold voltages via the body effect can be rather tedious in the real world.

As a side note: Due to the fact that the individual transistors of a standard design share the same bulk voltage, most of them are subject to the body effect unintentionally. This is because of the different source bias voltage of each MOSFET in the circuit. Most of the time however, it turns out that the body effect can be neglected or that it is actually less complicated to put up with its influence than trying to eliminate it. Due to this, the body effect is neglected for the rest of this section and the bulk contact is assumed to be shorted to the source contact.

Parasitic Capacitances

Due to its physical implementation, the MOSFET contains parasitic capacitances which gain importance when operating it at high frequencies. Some of them are illustrated in figure 4.10. While there are parasitic capacitances between every two of the four terminals, their values greatly depend on the MOSFET's operating region. The drain-bulk as well as source-bulk capacitances C_{DB} and C_{SB} for example are given by the depletion layer capacitances of the corresponding diodes between the source/drain contact and the substrate. Their sizes depend on the voltages V_{DB} and V_{SB}.

The most important capacitances for operation, however, are the those associated with the gate. These are the gate-source and the gate-drain capacitances C_{GS} and C_{GD}. Both C_{GS} and C_{GD} split up into two parts: A constant contribution C_{ov} which is associated with the overlap area of the gate and the n+-regions in the p-substrate. It is given by

$C_{ov} = WL_{ov}C_{ox}$, where W is the transistor width, L_{ov} is the length of their overlap area and C_{ox} is the capacitance per unit area of the gate-insulator-substrate interface. The second contribution comes from the gate's capacitance to the conductive channel which depends on the operating region of the transistor. Since in deep triode mode, the channel has not yet been pinched off, the total values of C_{GS} and C_{GD} are equal and given by

$$C_{GS,tr} = C_{GD,tr} = \frac{1}{2}WLC_{ox} + C_{ov}. \tag{4.41}$$

In saturation, C_{GD}'s channel contribution vanishes due to the pinch-off. The corresponding total parasitic capacitances can be calculated via

$$C_{GS,sat} = \frac{2}{3}WLC_{ox} + C_{ov}, \tag{4.42}$$

$$C_{GD,sat} = C_{ov}. \tag{4.43}$$

4.2.2 Small Signal Model

In the previous section, the MOSFET's so-called large signal-signal model has been derived. The equations 4.34 and 4.40 describe its IV-characteristic for large perturbations in the bias conditions such as wide V_{GS}- or V_{DS}-sweeps. While large-signal analysis is a useful tool to analyze a circuit in terms of dc characteristics and bias conditions, it has its short-comings in detailed ac-analysis. This is due to the fact that the quadratic nature of the derived IV-characteristics proves to cause complicated and hard-to-solve equations. Actual circuits however, are usually designed to operate at a specified *operation point* with only slight deviations. For this reason, the *small signal model* aims to linearize the circuit at this operation point by only allowing small perturbations that do not substantially change the bias conditions. In this way, it acts as an approximation of the large-signal model in a small area around a specified set of large-signal parameters. For the MOSFET, these large-signal parameters are set by the operation region it is operated in, i.e. the gate-source and gate-drain voltages V_{GS} and V_{DS}. The two most common ones are the already discussed triode and saturation regions.

In deep triode mode, the transistor's defining property is its ability to act like a switch with a linear characteristic between I_D and V_{DS}. Equation 4.35 shows this linear proportionality which is equal to that of a resistor. Thus, in the triode region, the small signal model substitutes the transistor with the resistance r_{on} derived in equation 4.36:

$$r_{on} = \left(\frac{\partial I_D}{\partial V_{DS}}\bigg|_{OP=tr} \right)^{-1} = \frac{1}{\mu_n C_{ox} {}^{W}\!/\!_{L} (V_{GS} - V_{th})} \tag{4.44}$$

where $OP{=}tr$ denotes that the transistor is in deep triode mode. The actual value of r_{on} can be controlled via W, L and V_{GS}. In circuit diagrams, the transistor is replaced with the corresponding small signal equivalent as depicted in figure 4.11.

In saturation region, the transistor acts like a current source controlled via the gate-source voltage V_{GS}. As a result, the small signal model introduces the *transconductance*

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\bigg|_{OP=sat} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})(1 + \lambda V_{DS}) = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \tag{4.45}$$

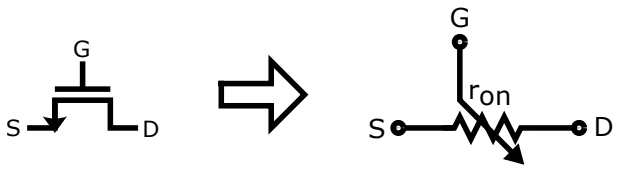


Figure 4.11: Small signal model replacement of the n-MOSFET in deep triode region ($V_{DS} << V_{DS,Sat}$) as illustrated in [60].

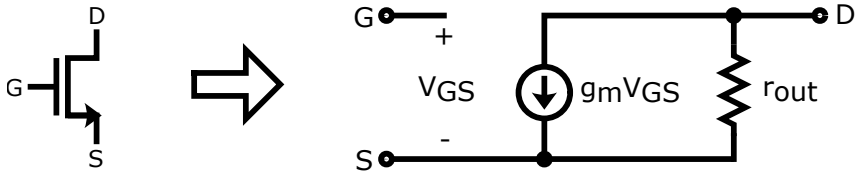


Figure 4.12: Small signal model replacement of the n-MOSFET in saturation region ($V_{DS} > V_{DS,Sat}$).

which can be derived from equation 4.40. Due to the aforementioned channel-length modulation, even in saturation, there is a linear relation of I_D and V_{DS}. Subsequently, I_D slightly varies with the applied drain-source voltage V_{DS}. The small signal model handles this by introducing a resistor r_{out} in parallel to the voltage controlled current source between the drain and the source. This is depicted in figure 4.12. Just like r_{on} in the triode region, its value is defined as

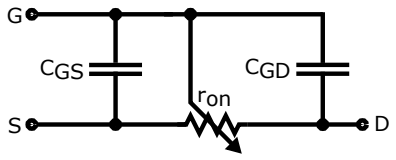
$$r_{out} = \left(\frac{\partial I_D}{\partial V_{DS}}\bigg|_{OP=sat} \right)^{-1} = \frac{1}{\lambda I_{D,sat}} \approx \frac{1}{\lambda I_D} \approx \frac{L}{I_D} \tag{4.46}$$

where $I_{D,sat}$ is the drain current at $V_{DS} = V_{DS,Sat}$. Throughout this work, r_{out} will also be denoted as the drain-source resistance r_{DS}.

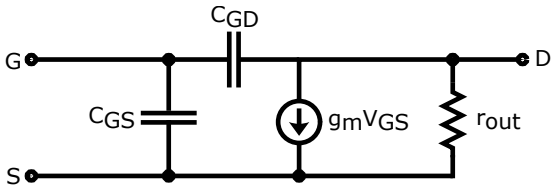
Figure 4.13 shows the presented MOSFET small signal models with the most relevant parasitic capacitors in deep triode and saturation region. Throughout this work, these models are used for analog circuit analysis and system theoretical calculations.

4.2.3 P-Type and Deep N-Well N-Type MOSFETs

The name-giving feature of CMOS-technologies is the availability of two complementary transistor types. Besides the already discussed n-type MOSFET, designers have access

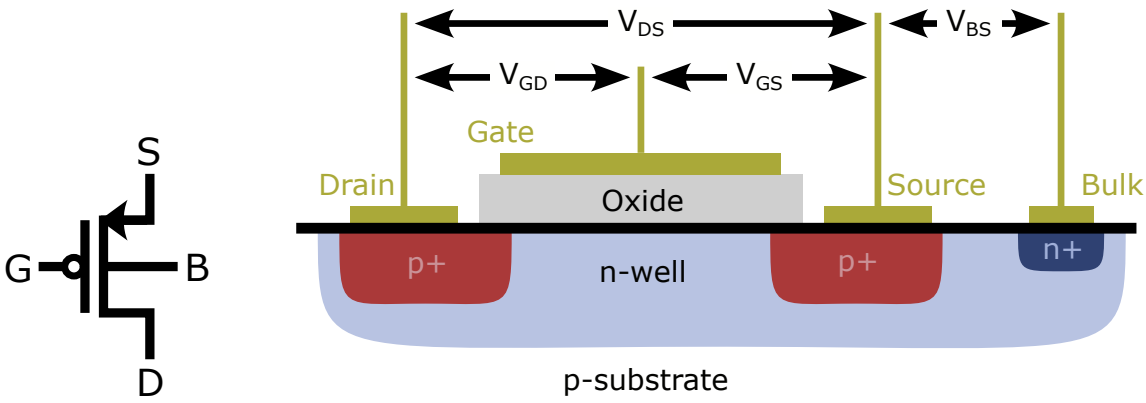


(a) n-MOSFET as a voltage controlled resistor r_{on} in deep triode region



(b) n-MOSFET in saturation region as a voltage controlled current source with the channel-length modulation resistance r_{out} in parallel.

Figure 4.13: Small signal model equivalents for n-type MOSFETs in inversion ($V_{GS} > V_{th}$) including the most important parasitic capacitances C_{GS} and C_{GD}.



(a) Schematic symbol

(b) Cross-section with the most important voltages

Figure 4.14: Sketches of a p-MOSFET

to the p-type MOSFET which is illustrated in figure 4.14. As hinted at by the arrow[2] in the corresponding circuit diagram symbol, the p-MOSFET acts just like the n-MOSFET but with voltages and currents of opposite polarity. The cross-section of the on-silicon implementation shows that the p-MOSFET is embedded in an n-doped substrate, in contrast to the p-doped substrate of the n-MOSFET. Its drain and source are realized via p+-doped regions and the bulk bias contact is n+-doped. Again, the p+-doped source and drain regions form two back-to-back diodes with the n-substrate which prevent a current flow between source and drain. But, instead of increasing V_{GS} to cause the formation of a conductive channel underneath the gate, it actually has to be decreased for the p-MOSFET. The same goes for the drain-source voltage V_{DS} where $V_{DS,Sat} < 0$. In analogy to the n-MOSFET, the source terminal acts as a voltage reference for all the other terminals. In this case however, the source is the terminal with the highest voltage. As a result, the derived equations in the previous section as well as the small signal model can also be applied to the p-MOSFET.

As a result from inverting the doping polarities, holes are now the minority carriers in the substrate. And due to this, the conductive channel is formed by holes instead of electrons. Since holes usually suffer from lower charge carrier mobility $\mu_p < \mu_n$ in silicon, p-MOSFETs are known to be inferior to n-MOSFETs in terms of current drive and transconductance. Subsequently, amplifiers for example exhibit lower gain or lower bandwidth when their input transistor is a p- instead of an n-MOSFET with equal W/L ratios. However, as section 4.3 shows, p-MOSFETs usually have better noise performance. In the end, the actual choice of the MOSFET type depends on the application and the design constraints. Often, there are far more parameters to take into account.

In the actual implementation, the n-substrate of p-MOSFETs is placed as a so called *n-well* in the p-doped silicon. This is achieved by local n-doping. The interface of this n-doped region with the surrounding p-substrate forms a pn-junction, i.e. a diode. While the p-substrate is usually pinned to the ground potential for large designs, the n-well of p-MOSFETs is shorted to the supply voltage. Due to this, the interface diode is biassed in reverse-mode and there is no current flowing between the p-substrate and the n-well. Subsequently, p-MOSFETs are intrinsically shielded from noise and cross-talk of surrounding circuits which could propagate through the p-substrate.

[2]The arrow in the schematics symbols of both the n- and the p-MOSFET (figures 4.6a and 4.14a) indicates the conventional current flow direction of the drain-source current.

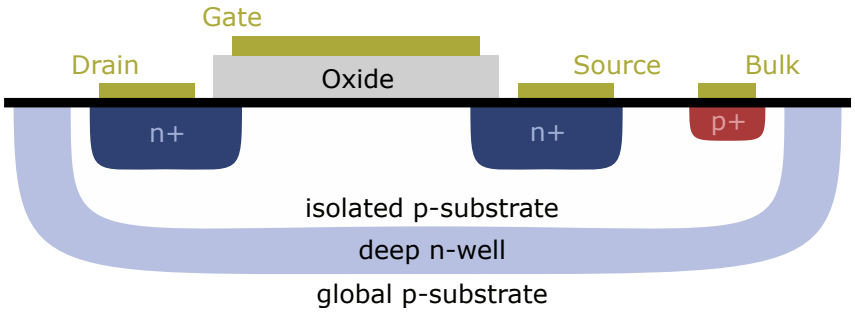


Figure 4.15: Cross section sketch of an n-MOSFET surrounded and shielded by a deep n-well.

Deep n-wells are used to apply this shielding behaviour to n-MOSFETs. A cross-section of their on-silicon implementation is shown in figure 4.15. Instead of embedding the transistor in the global p-substrate, the deep n-well acts like a trench between the MOSFET and its surroundings. With this n-doped region below as well as around the transistor, a local p-substrate is formed. This is due to the p-n-p structure of the deep n-well which causes the formation of two back-to-back diodes. When biassing the n-well to the supply and the p-substrates to the ground potential, both these diodes are in reverse mode. As a result, the local p-substrate is shielded from its surroundings.

In mixed-signal ASICs which host both analog and digital circuitry, deep n-wells find excessive use. Without any shielding, the analog circuits are embedded into the same global p-substrate as the noisy digital circuits which keep switching their outputs in between the ground and supply voltage. Depending on the time constant as well as the rate, these switching processes can couple into noise sensitive nodes of analog circuits. This phenomenon is called *cross-talk*. In order to prevent this, analog circuits are embedded into deep n-wells to shield them from said cross-talk.

Due to their isolating nature, both the shallow n-well of the p-MOSFETs as well as the deep n-well allow tuning the bulk voltages for devices embedded in them. As a result, n-wells do not only shield components from noise, but they also allow compensating or exploiting the body effect.

4.3 Noise in Analog Circuits

Components in circuits generate noisy voltages and currents. In system theory, noise signals are described via their *power spectral density* (PSD) which is a measure for the average power a signal carries at a given frequency. As such it is usually given in V^2/Hz or A^2/Hz.

When analysing a circuit's noise performance, designers are interested in how the power spectral density of the device components transfer to the circuit's output. This can be achieved with the system's transfer function. The propagation of an input signal with the spectral density $s_{in}(f)$ through a linear time-invariant system with the transfer function $H(f)$ is given as

$$s_{out}(f) = s_{in}(f)|H(f)|^2. \tag{4.47}$$

Here, $s_{out}(f)$ is the spectral density of the output signal.

In general, noise from different components is uncorrelated. Subsequently, the power spectral density $s_1(f)$, $s_2(f)$, ..., $s_N(f)$ of the noise generated by different components

can be added up such that

$$s_{out}(f) = |H(f)|^2 \sum_{k=1}^{N} s_k(f). \tag{4.48}$$

Power Spectral Densities of MOSFETs

There are two equivalent ways to describe the noise generated by a transistor. It can either be understood as a current noise in the transistor's drain-source channel or as a corresponding voltage noise at the transistor's gate. Besides these two views, the MOSFET transistor inherits two sources of noise with different frequency dependence. The first one is *thermal noise* which stems from the random movement of charge carriers in the transistor's channel. Its channel current PSD is described via

$$\frac{\langle i_{n,therm}^2 \rangle}{df} = \frac{8}{3} k_B T g_m, \tag{4.49}$$

while the equivalent PSD of the gate votage is given via

$$\frac{\langle v_{n,therm}^2 \rangle}{df} = \frac{8}{3} \frac{k_B T}{g_m}, \tag{4.50}$$

where k_B is the Boltzmann constant and T is the temperature.

The second noise source is the so-called *flicker noise* and is related to defects in the silicon lattice which introduce trap states for charge carriers. The trapping and releasing mechanism from these trap states is a statistical process which can best be modeled by a gate voltage referred PSD of

$$\frac{\langle v_{n,therm}^2 \rangle}{df} = \frac{K}{C_{ox} W L} \frac{1}{f}. \tag{4.51}$$

Here, K is a technology-dependent constant. Due to its $1/f$-dependence, it only plays a role at low frequencies. It can be minimized by increasing the transistor width and length. In the noise calculations provided in this work, flicker noise is usually neglected due to its small contribution.

5 XIDer - The X-Ray Integrating Detector

The XIDer project is an R&D collaboration between the European Synchrotron Radiation Facility (ESRF) and Heidelberg University for a multi-purpose detector for time-resolved X-ray diffraction experiments. It is a part of the ESRF's detector development plan (DDP) which has been initiated alongside the EBS upgrade program. In this context, XIDer's goal is to evaluate the feasibility of a detector that fulfills the demanding requirements imposed by the properties of fourth generation storage ring-based synchrotron light sources.

In 2018, the collaboration has been initiated as a 4-year project and has later been prolonged until the end of 2023. While the sensor research and design is performed by the *Detector & Electronics Group* of the ESRF, the corresponding readout ASIC is designed by the research group *Schaltungstechnik und Simulation* at Heidelberg University. The project's inital focus has been put on potential future experiments conducted at the ESRF. However, feedback of the synchrotron light community hints at the fact that XIDer's novel concepts are also applicable to other machines.

This chapter gives a short overview of the XIDer's target specifications and the design concepts to reach said specifications. Additionally, it provides an overview over existing X-ray photon detection systems and compares them to XIDer's requirements.

5.1 Requirements

With time-resolved X-ray diffraction experiments at storage ring based fourth-generation synchrotron light sources in mind, the following list of requirements has been defined at the beginning of the XIDer collaboration:

- **Energy range:** The XIDer detector is aimed to cover a photon energy range of 30 keV to 100 keV. Subsequently, high-Z compound semiconductor sensors like CdTe or CZT have to be employed (see chapter 3).

- **Pixel pitch:** A pixel size of 100 µm to 200 µm has been chosen. The detector shouls also provide the option to read out the matrix with 2x2 pixel clusters.

- **Dynamic flux range:** In diffraction and scattering experiments, the intensity recorded by 2D detectors usually varies over several orders of magnitude within the same image. In the most intense areas, usually close to the projection of the incident beam to the sample, the detectors may be exposed to photon fluxes of the order of $1 \times 10^{11}\,\mathrm{ph\,s^{-1}\,mm^{-2}}$ and above. And at the same time, in other regions, where the intensity of the scattered signal is greatly reduced, detectors must be able to provide single photon sensitivity.

- **Time resolution:** In order to resolve each of the bunches in the ESRF's 16-bunch mode[1], a time resolution of 175 ns is required. During this short time, the analog sensor signal has to be read out, analog values have to be digitized, processed and stored and the front-end has to be prepared for the next incoming X-ray pulse. Just

[1] see section 2.3

like the wide dynamic flux range, this is one of the most challenging requirements for the XIDer detector.

- **Frame readout rates:** There is a great interest in the X-ray diffraction community to record time dependent, irreversible processes and structural changes on a few microsecond or even sub-microsecond scale [63]. In order to achieve this with a continuous frame readout, XIDer needs to be able to provide a frame readout rate of 100 kHz and above.

- **Flexibility in terms of data acquisition and readout:** The multi-purpose nature of XIDer requires adaptability to different exposure times, data readout rates, data acquisition patterns, triggering as well as spatial and time resolution to name but a few measurement parameters. Subsequently, flexible but accessible and easy-to-use ways to adapt the detector to the conditions and requirements of the different experiments are mandatory.

- **Data handling**: With a detector area of just a few $10\,\mathrm{cm}^2$, a pixel size in the order of 100 µm and 16 bit of data per pixel, the expected data rates rise to the order of $\mathrm{TB\,s}^{-1}$. Thus, the detector needs to be equipped with sophisticated ways to deal with very high raw data rates, either via on-chip pre-processing or fast output data serializers.

For further reading on the background of these requirements, references like [10], [12] and [64] are recommended.

5.2 Concept

As illustrated in figure 5.1, XIDer uses a 2D hybrid pixelated approach. The top-side of the sensor is biassed to a negative high voltage with a single cathode contact shared by all of the pixels. On the sensor's bottom-side there is a pixelated anode grid structure. With a bump-bond connection, each of these anodes is connected to an input pixel pad on the readout ASIC. Subsequently, the ASIC only reads out electrons and neglects the hole-contributions to the signal. In order to enable a parallel readout of the whole pixel matrix, this concept choice imposes a modularized approach on the ASIC featuring a readout channel counterpart for each sensor pixel. Each channel is concerned with the charge signal readout of its corresponding pixel followed by the digitization and storage of the processed input. For this purpose it employs novel concepts like the pipelined continuous conversion approach, the digital integration and the telegram protocol. Besides the signal processing, the ASIC channel is also concerned with biassing the anode of its corresponding pixel. An in-depth description is provided in chapter 6.

5.3 Photon Counting Scheme

XIDer is meant to count single photons with a fixed, pre-defined energy. There are several approaches on how to achieve this. This section provides a brief overview of existing schemes with advantages and disadvantages as well as state-of-the-art references. In the end, it provides a brief introduction to XIDer's chosen approach.

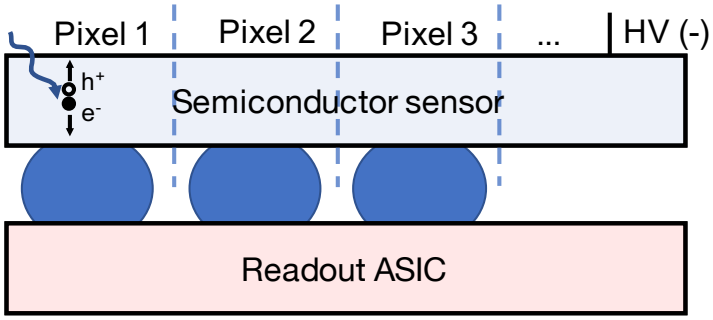


Figure 5.1: Sketch of the 2D hybrid pixelated detector approach chosen for the concept of XIDer.

5.3.1 Conventional Approaches

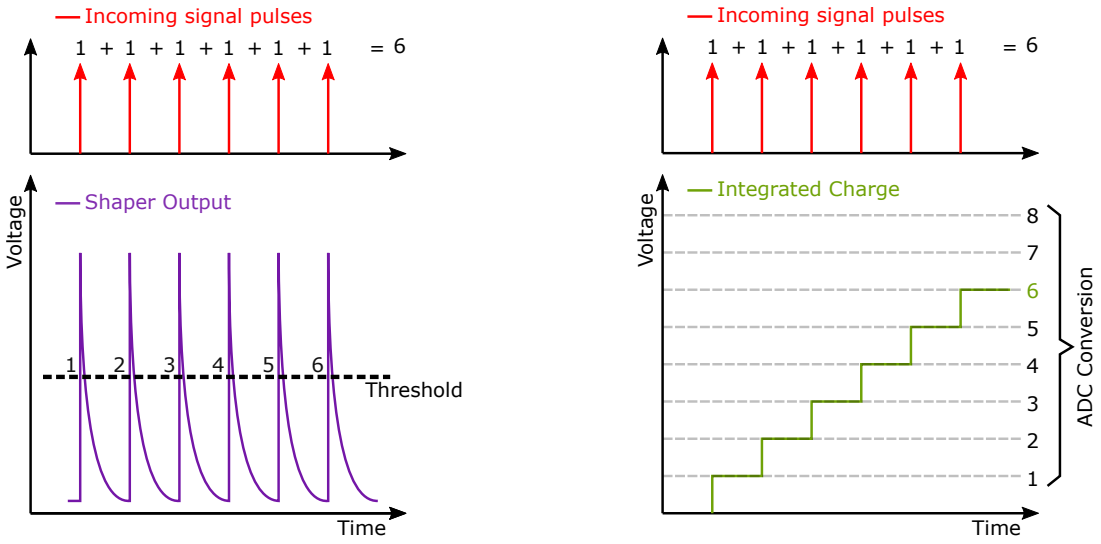
For counting X-ray photons with pixelated hybrid detectors, there are two major readout schemes, namely the *photon-counting*[2] and the *charge integrating* approaches. Both approaches only work with monochromatic irradiation, i.e. photons with a fixed energy. The following elaborations are based on [65] and [66]. Additional references are provided where necessary.

The photon-counting approach uses a preamplifier and signal shapers to transform the charge signals generated by incident photons in the sensor pixel into short voltage pulses. As depicted in figure 5.2a, the result of this shaping is a train of pulses where each pulse is interpreted as a single photon. In order to detect each individual pulse, a threshold voltage is applied. As soon as the signal crosses the threshold, a counter is incremented which counts the total amount of photons. Since the signal amplitude depends on the photon energy, the threshold can be tuned to only detect photons above a given energy.

The advantage of the photon-counting approach is its single photon sensitivity. And thanks to the intrinsic discrimination, it also exhibits good noise performance and sensor leakage suppression. However, the maximum photon count rate that can be achieved with this approach is intrinsically limited by the bandwidth of the readout electronics. As long as the shaper output voltage is above the threshold, the detector is blind to additional incident photons. At higher incident photon rates, additional voltage pulses keep adding up above the threshold, while the detector only counts a single photon from the initial threshold crossing. This effect is known *pile-up* and limits the upper photon count rate capability. Available state-of-the-art detectors with the photon counting approach like the DECTRIS EIGER2 XE CdTe 16M report a maximum count rate of $1.7 \times 10^9\,\mathrm{ph\,s^{-1}\,mm^{-2}}$ [67]. As a reminder: XIDer's requirement is to reach $1 \times 10^{11}\,\mathrm{ph\,s^{-1}\,mm^{-2}}$ which is two orders of magnitude higher. Subsequently, the XIDer collaboration has decided against using a photon-counting approach.

In contrast, the conventional charge integrating approach uses readout electronics which integrate incident charge on a feedback capacitor. Incoming charge is thus transformed to a DC output voltage level. This is depicted in figure 5.2b. At the end of an integration window, the voltage level is digitized by an analog-to-digital converter (ADC) and the integrator is reset. In order to extract the amount of photons that were absorbed by the pixel, the ADC needs to know the output voltage generated by a single photon. This is usually achieved via calibration with well-defined input signals.

[2]Unfortunately, the name that literature uses for this approach leads to confusion with other approaches which also count photons. For clarity, this work denotes the actual method with *photon-counting*, while the process of counting photons does not use a hyphen.



(a) Principle of the photon-counting approach. After propagating through the shaper circuits, the charge signal of incident photons is transformed to narrow voltage pulses. A comparator applies a threshold voltage to detect the pulses.

(b) Principle of the charge integrating approach. An integrator converts the sensor charge generated via absorption of photons into a DC voltage level. This analog voltage is then digitized by an ADC at the end of the integration window.

Figure 5.2: Working principle sketches of the two most commonly used approaches to count photons in the pixels of hybrid pixelated X-ray detectors.

The great advantage of the charge integrating compared to the photon-counting approach is that it has no intrinsical photon count rate limitation. Even if N photons hit the sensor pixel at the exact same instant of time, a charge integrating detector can correctly reconstruct the number N. However, there is an upper limit to the maximum total amount of charge that these circuits can integrate, i.e. to the dynamic photon count range. As soon as the output voltage of the integrator reaches the supply voltage level, no additional charge can be integrated for the rest of the integration window.

By adjusting the gain of the charge-to-voltage conversion, designers can trade measurement resolution for a larger dynamic range. Implemented detectors usually allow switching between different gain settings depending on the expected photon fluxes. State-of-the-art iterations implement an automated in-pixel gain switching which dynamically changes the gain in on-going measurements depending on the already integrated charge amount. This approach is widely used in X-ray detectors at free electron lasers like the European XFEL [68]. Examples are AGIPD [69], JUNGFRAU [70] and ePix10k [71].

However, it turns out that even with the automated gain switching, the conventional charge integration scheme does not provide the necessary flexibility in terms of dynamic photon counting range needed for XIDer. This is due to the fact that, compared to systems like AGPID, XIDer will be operated at storage ring based facilities like the ESRF. Here, the detector has to cover a wide range of different experimental conditions and integration time windows.

Another disadvantage of the conventional charge integrating approach is that it also integrates sensor leakage. Combining this property with high-Z sensors and possible large integration windows poses several complications for its application in the XIDer detector.

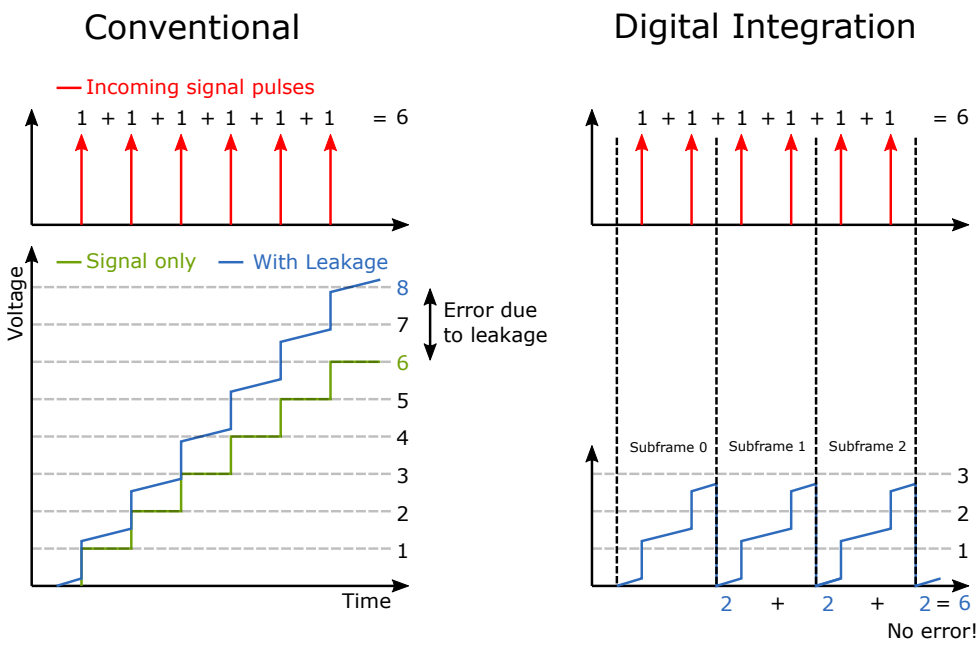


Figure 5.3: Illustration of the digital integration concept [73].

5.3.2 XIDer's Approach

For the reasons stated above, XIDer's readout ASIC uses neither a photon-counting nor a convential charge integrating approach. Instead it uses a pipelined implementation of an approach similar to that of the MM-PAD detector [72]. The basic structure is still a charge integrating procedure. But instead of converting the integrated charge to a digital value at the end of the integration window, the conversion is performed while the integration is still on-going. By subtracting charge packages of well-defined size from the already integrated charge, the output voltage of the charge integrator is decreased before it hits the supply voltage level. By remembering the amount of charge packages used, one can thus reconstruct the total incident charge. Subsequently, if the conversion is performed quickly enough to keep up with the incident photon flux, the amount of photons that can be counted per integration window is no longer limited. For future reference, this approach is called *continuous conversion*. Section 6.1.1 provides a detailed explanation.

While the continuous conversion vastly increases the upper limit of the dynamic photon count range per integration window, it does not fix the problem of integrated sensor leakage. For this reason, XIDer is operated with the digital integration scheme which is explained in the following section.

5.4 Operation: Digital Integration & Subframes

Developed at the ESRF, the digital integration works as depicted in figure 5.3. Instead of using a conventional readout scheme in which the charge signal of a frame is integrated in a single long exposure interval, the digital integration splits the frame into *subframes*. In each subframe, the integrated charge is converted to an equivalent digital number. In the simplest case, this digital number corresponds to the amount of counted photons, but other operation modes with half or quarter photons are discussed. At the end of the total exposure time, the sum of all of these digital values forms the resulting amount of counted photons for the total frame.

In addition to splitting up the frame, a discriminator is applied to the final charge value measured in each subframe. This discriminator discards excess charge beyond the chosen counting granularity. For example, if the detector is calibrated to count single photons and the integrated charge in one subframe corresponds to 2.6 photons, then, the final count for this subframe is 2 photons. As indicated in the illustration, with the correct choice of subframe length, this readout scheme allows a suppression of sensor leakage. Additionally, it prevents the accumulation of noise charge. More details on the digital integration can be found in [10].

With the choice of the digital integration as the readout scheme, there are two major consequences for the actual implementation of the readout ASIC. First of all, the subframe plays a fundamental role which is why it is referenced throughout this work in both the ASIC design as well as measurement chapters. It is mostly denoted as *(sub)frame* to indicate the validity of statements for both subframes and individual frames.

Additionally, the detector has to be designed to run through repeating cycles, i.e. (sub)frames, of charge integration, signal processing, digitization, adding photon counts, data storage and readout. For this reason, the ASIC features an on-chip sequencer as well as the custom-designed telegram interface which allow the definition of (sub)frame cycles that are repeatedly executed by the ASIC channels.

6 Readout ASIC Design

This thesis aims to give an overview of the research work that went into the design of the readout ASIC for the XIDer detector. Over the course of the last five years, this ASIC has gone through several iterations integrating more and more novel concepts to handle the challenges imposed by the very demanding set of requirements. Starting from simple prototypes with simplified test structures, the chip has matured into a pixelated scalable matrix of readout channels. Currently, it is on its way to become a large scale chip for the readout of high-Z compound semiconductor sensors with thousands of pixels. The design's functionality and ability to achieve the required performance has not only been tested in lab characterisation measurements but also in many on-site beamline measurements at the ESRF. Alongside performance tests of the detector concepts, the beamline measurements also include characterisation measurements of the time- and signal-dependant behaviour of high-Z sensor materials like CdTe and CZT.

This chapter provides detailed insights into the chosen design with choices and tradeoffs that have been made to tailor this ASIC to the requirements listed in 5.1. In the first part, a broad overview is provided which contains the concepts of analog signal processing and digital data management implemented in the ASIC's channels. In addition, it features a top-level description of the chip's global digital control and floorplan. This is followed by a detailed discussion of the design's parts starting with the analog domain for signal processing and moving on to digital circuitry for chip configuration, operation, data handling and data readout. Besides detailed explanations about the integrated circuitry, system theoretical calculations and simulations are provided to motivate, justify and reinforce design choices. In the end, a design verification section focusses on verifying the performance of the analog signal processing circuitry with respect to the project requirements followed by a list of manufactured prototypes.

For the design execution, implementation and simulation, *Cadence* [74] tools like *Virtuoso* [75], *Innovus* [76] and *Xcelium* [77] have been used. System theoretical calculations have been carried out by hand supported by the use of *Wolfram Mathematica* [78]. The ASIC has been implemented in the TSMC 65 nm process technology [79].

6.1 Overview

As noted above, the requirements placed on XIDer's readout ASIC demand solutions both in the analog and the digital domain. On the one hand, the analog output signals provided by the sensor pixels have to be received and processed by an analog front-end. This front-end has to convert the pixel's output charge into a signal that can be digitized for further processing, storage or readout. On the other hand, the required flexibility in terms of different readout and operation modes asks for the implementation of many different features in a very limited area. In order to control and adapt the analog front-end to different bunch mode conditions and measurement procedures, store data on-chip in different ways or send out data in different patterns at high speed, a versatile digital block is essential. As a result, the ASIC has to be designed in a mixed-signal fashion.

The compartments that make up XIDer's readout ASIC are shown in figure 6.1. As

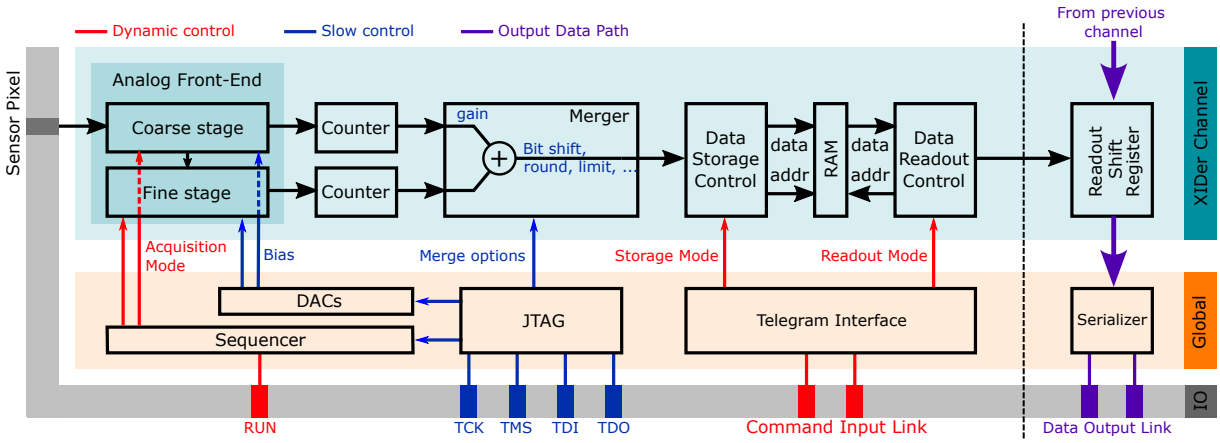


Figure 6.1: Schematic overview of the circuit blocks on XIDer's readout ASIC and their interaction with each other.

depicted, the chip is divided into several domains. There are the readout channels which are instances of the same circuit module with the same functionality designed for the parallel readout of all the sensor pixels. In each channel, the employed front-end is split up into a coarse and a fine stage which use a charge integrating concept with a *continuous conversion* add-on that largely increases their dynamic range. In combination with counters, this add-on allows a dynamic conversion of the incident charge to a digital value while the charge integration is still ongoing. Ultimately, the merger combines the photons counted by both stages into a final result.

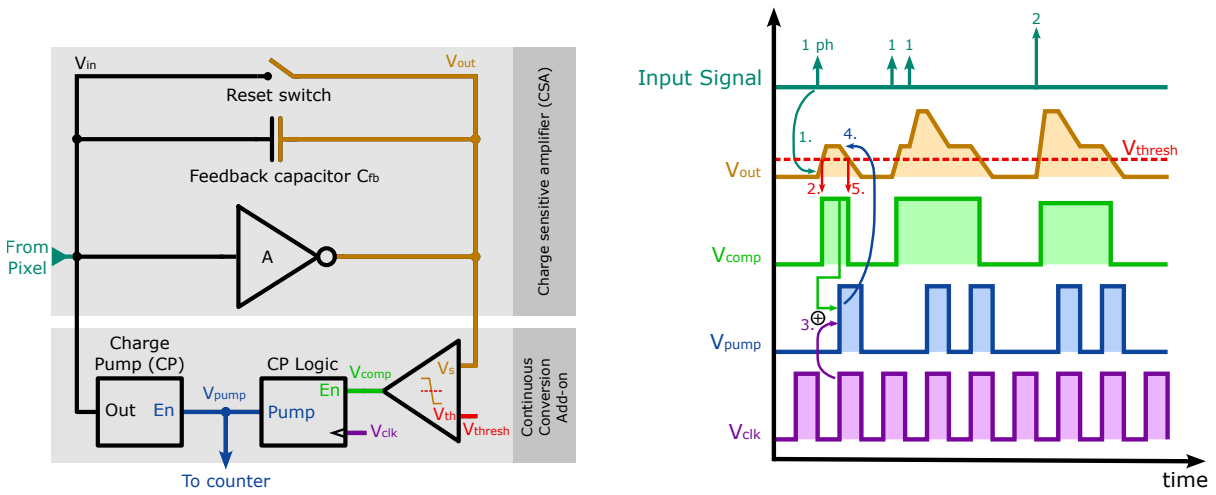
In addition, each channel features a RAM module for on-chip data storage. Read and write accesses are issued by the global telegram interface which is based on the custom-designed telegram protocol. At the end of each channel, there is a shift register which is loaded with output data as soon as a readout command is issued in the data readout control unit. The actual size of the detector has not yet been decided on but the final ASIC version will at least have a few ten-thousand channels.

On the global level, there is the ASIC's global control block. It is instantiated once per chip and contains all the necessary circuitry to operate the matrix of channels like a JTAG interface for slow-control, a sequencer and the telegram interface for dynamic control and a serializer for data readout. The following subsections give a general overview of the concepts and compartments used in the ASIC channels and the digital control block. This overview is followed by a more detailed discussion of the design of single components and modules in sections 6.2 and 6.3.

6.1.1 The Analog Front-End Concept

The task of the analog front-end is to count the amount of monochromatic photons that hit a sensor pixel. An important point to reiterate here is that the energy of photons incident to the sensor pixel is well-known. Synchrotron beamlines employ monochromators to tune the X-ray energy to the desired value. For the proposed front-end architecture presented in the following, this is a necessary requirement.

In order to count photons at high rates and with low dead times, XIDer's design uses a pipelined, two-stage approach. Before discussing the full structure, this section starts by explaining the operation principle of a single stage.



(a) Circuit diagram with all the necessary components.

(b) Timing diagram of the most important signals involved in the operation.

Figure 6.2: Explanatory illustrations of a single stage in the analog front-end of XIDer's readout channel.

The Front-End Stage & Continuous Conversion

Each stage employs the continuous conversion approach which is an add-on to the well-known charge integrating front-end structure (see section 5.2). In this approach, a stage keeps converting incoming charge to digital values while the charge integration is still on-going. This results in a much larger dynamic range compared to standard charge integrating implementations. Figure 6.2a shows a schematic overview of all the needed compartments. The core component is the charge sensitive amplifier (CSA) which consists of an amplifier negatively fed back by a capacitor C_{fb} and a reset switch. In the initital state, there is no charge on the feedback capacitor and the CSA's input and output voltages V_{in} and V_{out} are equal. When charge enters the stage, the CSA integrates it on C_{fb}. It does this by generating a potential difference between its input and output nodes. However, due to the negative feedback, the amplifier keeps V_{in} constant and only changes V_{out}. As a result, monitoring the CSA's output voltage is sufficient to measure the charge that is stored on C_{fb}. The size of an output voltage step ΔV_{out} that is generated by the incident charge Q_{in} can be calculated via:

$$\Delta V_{out} = \frac{Q_{in}}{C_{fb}}. \tag{6.1}$$

With the knowledge of how much charge a photon of given energy γ_E generates in the sensor, this allows calculating the voltage step that corresponds to a single photon ΔV_{γ_E}. And as a result, the amount of photons that contributed to an output voltage step can be determined. In order to do so, one needs the average energy ϵ_{eh} that is necessary to generate an electron-hole-pair in the pixel, the elemental charge q_e and the photon energy E_γ. Taking into account that XIDer only reads out one electrode of the sensor, the read out charge from a pixel that has just absorbed a single photon is given by

$$Q_{\gamma_E} = q_e \cdot \frac{E_\gamma}{\epsilon_{eh}}. \tag{6.2}$$

Inserting this into equation 6.1 yields

$$\Delta V_{\gamma_E} = \frac{E_\gamma q_e}{\epsilon_{eh} C_{fb}}. \tag{6.3}$$

And with this, the amount of photons N_{γ_E} corresponding to the CSA's output voltage ΔV_{out} is given as:

$$N_{\gamma_E} = \frac{\Delta V_{out}}{\Delta V_{\gamma_E}} = \frac{\Delta V_{out} \epsilon_{eh} C_{fb}}{E_\gamma q_e} \tag{6.4}$$

In a conventional charge integration front-end, this is how the actual amount of photons is counted. An ADC converts the final voltage value at the end of an integration cycle, i.e. a (sub)frame. After the conversion, the CSA is reset by discharging the feedback capacitor with the reset switch.

However, this approach has a limitation ruling it out for high continuous photon rate applications that require single photon sensitivity like XIDer: the CSA's output voltage is limited by the dynamic voltage range of its amplifier. If the amount of stored charge on the feedback capacitor is too high, the output voltage V_{out} will hit the upper limit of this dynamic range, i.e. the CSA *saturates*. As a result, there is a maximum amount of photons that can be counted per (sub)frame. While this limit can be increased by choosing a larger feedback capacitor, the circuit's gain and hence its resolution is reduced in the process. In the end, a tradeoff has to be made between the desired upper limit of photons per (sub)frame and the photon counting granularity. Since the main challenge of the XIDer project is achieving an ambitious maximum photon counting rate of $1 \times 10^9\,\mathrm{ph\,s^{-1}\,pix^{-1}}$ at a wide range of (sub)frame lengths while maintaining single photon sensitivity, a classical charge-integrating approach has been deemed unfeasible for its readout ASIC.

This is where the continuous conversion comes into play which is implemented via the addition of the depicted comparator, the charge pump and its enable logic. Their operation principle is demonstrated in figure 6.2b on the basis of a timing diagram of the involved signals. The respective nodes are marked with the same colors in figure 6.2a. At the top, there is the input signal which shows the time structure of X-ray pulses incident to the sensor pixel. As depicted by the pulse height, a pulse can contain a different number of photons which is also indicated by the number written above the pulses. In the provided example, there are only two uniquely different cases: a single as well as two photons per pulse. In reality, this number can be much bigger as discussed in section 6.5.

Below the input signal, the timing diagram shows the circuit's reaction to incoming pulses in a step-by-step fashion. It starts with the initial integration as soon as a photon causes a charge generation in the sensor pixel. As depicted in the **first** step, the CSA's output voltage V_{out} rises. However, instead of an instant voltage step, it takes some time to reach the final output voltage which is due to the finite output resistance of the amplifier stage.

The comparator is supposed to act as a monitor for the CSA's output voltage by comparing it to a fixed threshold voltage V_{thresh}. As long as V_{out} is below V_{thresh}, the comparator output is at ground level. However, if $V_{out} > V_{thresh}$, the comparator drives its output to the supply voltage level. The effect of this behaviour is visible at the **second** depicted step. Here, V_{out} crosses V_{thresh} while the CSA is still in the process of integrating the incident charge. As a result, the comparator's output V_{comp} is activated which triggers the **third** step.

The activated comparator output is supposed to indicate, that a "big enough" charge has entered the front-end, with the actual size of "big enough" being of particular interest

for the calibration of this circuit. It enables the second feedback path in parallel to the feedback capacitor, denoted as "Continuous conversion add-on" in the circuit schematics. The purpose of this path is to stop the CSA from saturating. In order to achieve this goal, it includes a charge pump which is able to inject a charge of opposite polarity to the incident signal charge into the input of the CSA. As soon as the comparator indicates that V_{out} has risen above V_{thresh}, this charge pump is enabled, effectively discharging the CSA's feedback capacitor. And as a result, V_{out} decreases, keeping the CSA from saturating. In the plot, this is depicted by the steps **three** and **four**.

As illustrated, the discharge process performed by the charge pump is executed in a pulsed fashion. There are two reasons for this approach:

- The pulsed structure allows the injection of well-defined charge packages
- Digital counters sensitive to the pulses' rising edges can easily keep track of the amount of injected charge packages

This enables the ASIC channel to precisely reconstruct and remember the amount of injected charge by the charge pump. The time structure for these pulses is provided by the periodic clock signal V_{clk}[1] which is gated with the comparator output in the CP logic block as discussed in section 6.2.3. An important point to note here is that the structure of V_{clk} needs to be precisely tunable and exhibit low jitter for the generation of well-defined, low-noise charge packages.

As depicted by step **five**, the injection of said charge packages eventually drives V_{out} back below V_{thresh}. As a result, the comparator output returns to ground level and the continuous conversion add-on is deactivated. Finally, the total charge integrated by the front-end can be reconstructed by the final digital counter value N_{CP} and the charge package size Q_{CP} via

$$Q_{in,meas} = N_{CP} Q_{CP}. \tag{6.5}$$

Besides the choice of the comparator threshold, the actual size of Q_{CP} is another critical question for the calibration of the analog front-end. The most intuitive choice is a value that is equal to an integer multiple n of the charge generated by a photon in the pixel such that $Q_{CP} = n \cdot Q_{\gamma_E}$ where Q_{γ_E} can be derived from equation 6.2. This is due to the fact that in this case, the amount of incident photons to the pixel can easily be determined via

$$N_{\gamma_E} = n N_{CP}. \tag{6.6}$$

In the illustrated example, the charge pump package size is calibrated such that $Q_{CP} = Q_{\gamma_E}$, i.e. $n = 1$ and the input signal sequence contains five photons in total. Subsequently, the charge pump has to inject five charge packages. Via the five pulses in the time structure of V_{pump}, a connected counter can thus reconstruct the incident photon number as $N_{\gamma_E} = 5$.

With the operation principle explained above, the continuous conversion keeps the CSA from saturating and theoretically extends the circuit's maximum photon counting limit to infinity. In reality, the only limiting factor is the depth of the digital counter. However, the maximum photon count per (sub)frame must not be confused with the maximum photon counting *rate*, this circuit can achieve. This is discussed in the following paragraph.

[1] In the actual implementation, this signal is generated by the on-chip sequencer.

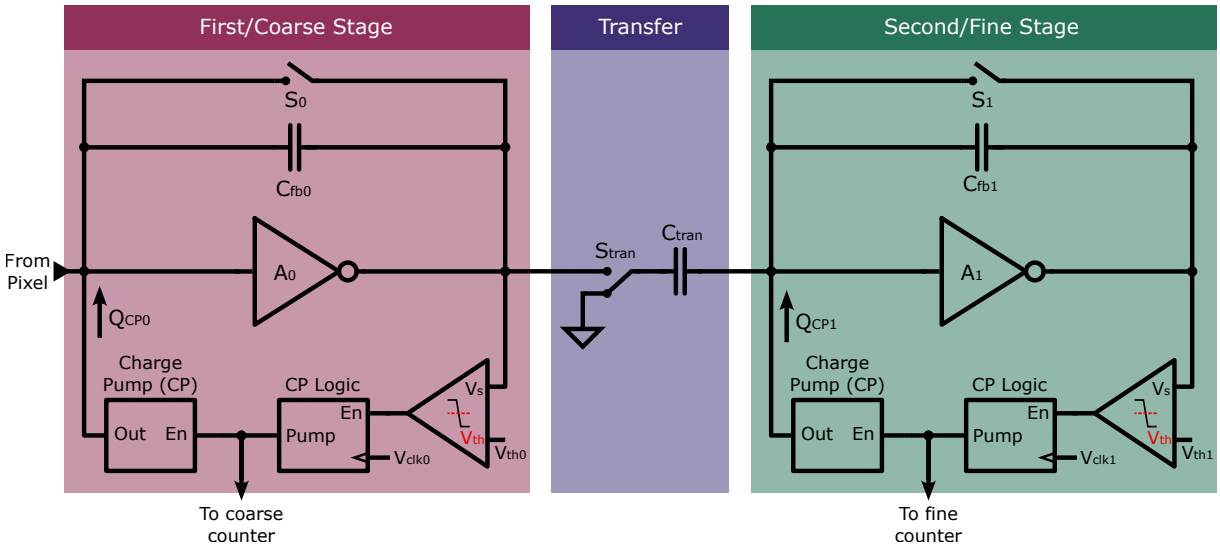


Figure 6.3: Simplified circuit diagram of XIDer's pipelined front-end approach.

The Pipelined Approach

As a reminder, the aim of this detector is to achieve photon count rates of up to 1×10^9 ph pix^{-1} s^{-1} while maintaining single photon resolution. With the continuous conversion concept presented above, reaching single photon sensitivity is a matter of electronics noise, the correct choice of the feedback capacitor size as well as the comparator threshold and the charge package size Q_{CP}. Section 6.4 discusses the necessary parameters and dimensions and showcases that single photon sensitivity can be obtained rather easily.

In order to reach the necessary photon rates, there are two possible ways. One of them is increasing the charge pump package size Q_{CP}. However, the requirement of single photon sensitivity constrains the package size to the equivalent charge generated by a single photon or less. The other is the pump frequency f_p that drives V_{clk} and is thus responsible for the frequency with which the charge pump packages are applied. In the most general case, where $Q_{CP} = n \cdot Q_{\gamma_E}$, the photon count rate is given by

$$R_\gamma = n f_p. \tag{6.7}$$

With the single photon sensitivity requirement, $n = 1$ and this simplifies to

$$R_{\gamma,n=1} = f_p. \tag{6.8}$$

Thus, in order to reach $R_{\gamma,n=1} = O(10^9 \frac{ph}{s})$, the pump frequency has to be in the order of GHz which imposes an unnecessarily strict timing constraint on the CSA. It means that the CSA needs to have a bandwidth of at least 1 GHz because it has to keep its output voltage on track with the charge stored on C_{fb}. If it is too slow in doing so, V_{out} might not have settled to the correct value when the decision whether to pump at the next clock cycle of V_{clk} is made. As as result, the charge pump could potentially apply too many or too few charge packages. For realistic designs, this bandwidth has to be even higher to provide a safety margin for all the different process corners.

In order to relax this constraint to manageable sizes, a pipelined design as depicted in figure 6.3 has been proposed at the beginning of the XIDer project. The idea is to have two stages: a *coarse stage* with a large charge pump package $Q_{CP0} = nQ_{\gamma_E}$ to keep up

with high photon rates and a *fine stage* with a small charge pump package $Q_{CP1} = Q_{\gamma_E}$ to maintain single photon sensitivity. As an important note: the comparator threshold V_{th0} of the coarse stage has to be scaled with the factor n to the correct amount of photons as well. Otherwise, the charge pump will inject its charge package even though $Q_{in} < nQ_{\gamma_E}$.

A simplified illustration of the operation principle is shown in figure 6.4. While the acquisition of the first (sub)frame is on-going, only the coarse stage is active. Depending on the choice of the coarse stage's charge package size Q_{CP0}, there will be a residual charge left on C_{fb0} at the end of the (sub)frame. This is due to the fact that with the higher comparator threshold, the coarse stage is blind to charges smaller than Q_{CP0}. In order to convert this residual, it has to be transferred to the fine stage. This is executed with the help of the transfer capacitor C_{tran} and requires a particular switching sequence of S_1, S_2 and S_{tran} which is explained in detail in section 6.2.4. The idea is to connect C_{tran} at the very end of the (sub)frame and to let the amplifier of the coarse stage charge this capacitor to the final voltage. As soon as it is fully charged, the coarse stage is reset via the reset switch, causing an injection of the residual charge through C_{tran} into the second stage. The completion of this process renders the coarse stage ready for the next (sub)frame, while the fine stage starts with the conversion of the residual in parallel. As a result, the coarse and fine stages work in a pipelined fashion in which the fine stage converts (sub)frame m, while the coarse stage is already processing (sub)frame $m + 1$. The entirety of the transfer process is denoted as T in the diagram. An additional remark to make here is, as explained in section 6.2.4, the transfer process actually injects the charge from the coarse to the fine stage with a gain of $A_C = C_{tran}/C_{fb0}$. This extra charge gain significantly relaxes the fine stage constraints in terms of noise and thus power consumption.

Figure 6.5 shows the typical reaction of the front-end to incident charge on the basis of the important signals involved. The graph is split in two halves. In the left-hand half, there is a circuit diagram of the pipelined analog front-end. The top half of this diagram shows the coarse stage and the transfer capacitor with its respective switch S_{tran}. Below the dividing line, the front-end's fine stage is depicted. The right-hand side of the graph shows the actual timing diagram with the dividing line allocating the signals to their corresponding stage. Subsequently, coarse stage signals are above the dividing line, fine stage signals can be found below. For clarity, the involved signals are colored in the same scheme in both the circuit and the timing diagram. The actual structure of this graph is similar to that for the single stage in figure 6.2. While the status of V_{comp} is indicated by the color underneath the V_{out}-curve of the respective stage, the V_{clk} signal has been omitted completely and can only be seen in the periodic pulse patterns of V_{pump0} and V_{pump1}.

In the depicted case, the chosen charge package size for the coarse stage and fine stages

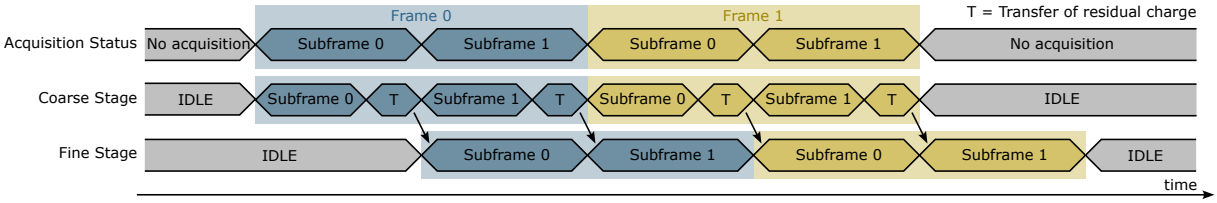


Figure 6.4: Simplified timing diagram of the pipelined (sub)frame acquisition in the analog front-end of XIDer's readout ASIC. Following the principle of the digital integration, frames are divided into (sub)frames. The actual time window of the transfer is not to scale.

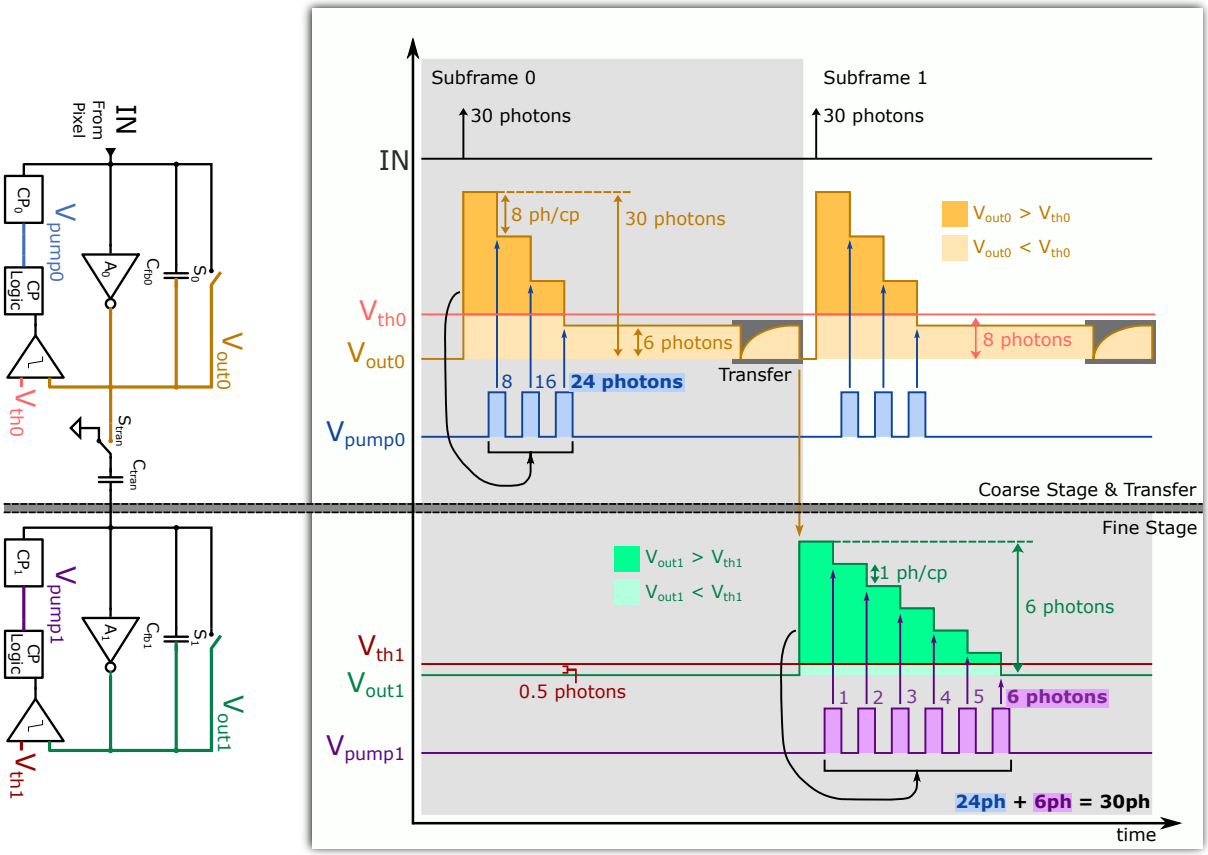


Figure 6.5: Timing diagram of the most important signals in the continuous conversion approach with two stages.

are $n_0 = 8$ photons per pump (indicated as 8 ph/cp) and $n_1 = 1$ photon per pump (1 ph/cp) respectively where the corresponding comparator threshold voltages have been chosen accordingly. While these values turn out to be a good compromise for this detector, the ASIC is designed to allow a wide variation and configurability for different use cases, ranging from single photons to several tens of photons per pump. An actual discussion about the parameters and their choice can be found in section 6.4.

In the shown example, the pixel detects 30 photons in a short X-ray pulse of arbitrary energy right at the beginning of each (sub)frame. The generated charge corresponding to this event is integrated on C_{fb0} by the coarse stage CSA. Since V_{th0} is at a voltage corresponding to the charge of 8 photons, V_{out0} rises above V_{th0} in the integration process and the comparator enables the charge pump logic. As a result, the charge pump injects its well-defined packages with a charge corresponding to 8 photons per package into the coarse stage input. After pumping three times, V_{out0} drops below V_{th0}. Consequently, the charge pump logic is deactivated and the charge package injection stops. At this point, the counter connected to V_{pump0} has counted 3 charge packages. This value has to be multiplied with $n_0 = 8$ to obtain the actual amount of counted photons which is 24 as illustrated. As a result, with an incident amount of 30 photons, there is a *residual charge* corresponding to 6 photons left on C_{fb0}.

In order to convert the residual charge, it has to be transferred into the fine stage which applies smaller charge packages and also employs a smaller comparator threshold V_{th1}. This is indicated by the *Transfer* shaded in dark grey which starts with closing S_{tran}. The transfer capacitor C_{tran} being charged to V_{out0} and as soon as the charging

is done, the coarse stage is reset to inject the residual charge into the fine stage. With single photon sensitivity ($n_1 = 1$), the fine stage has to pump an additional 6 times to drive its output V_{out1} below the threshold. The bright grey background indicates that the coarse stage conversion, the transfer and the fine stage conversion are associated with the same (sub)frame 0. By adding the charge package counts of both stages N_{CP0} and N_{CP1} multiplied with their respective charge package factors n_0 and n_1 the reconstructed photon number is

$$N_{tot} = n_0 N_{CP0} + n_1 N_{CP1}. \tag{6.9}$$

The result in the depicted example is $N_{tot} = 8\,\mathrm{ph\,cp^{-1}} \cdot 3\,\mathrm{cp} + 1\,\mathrm{ph\,cp^{-1}} \cdot 6\,\mathrm{cp} = 24\,\mathrm{ph} + 6\,\mathrm{ph} = 30\,\mathrm{ph}$.

In this example, the total charge is injected at the beginning of the (sub)frame which is the ideal case for the presented principle of operation. One might be wondering if this is a realistic case and how common it actually is. In reality, the ASIC is supposed to run synchronous to the synchrotron it is operated at. This is achievd by feeding the ASIC with a root clock which is derived from the synchrotron's RF clock. As explained in section 2.1, this RF clock dictates the basic granularity of the synchrotron's bunch structure. Each period of the RF clock holds an open bunch slot which can be filled with electrons deliberately when operating the synchrotron. The synchronisation of the ASIC to this RF clock allows aligning the (sub)frame to the bunch structure. And beyond that, the actual position of the X-ray pulses generated by the electron bunches in a (sub)frame can be finely tuned. As a result, the condition that an X-ray pulse hits the pixel right at the beginning of the (sub)frame can be forced while operating the detector. Whether there is only a single or several X-ray pulses per (sub)frame depends on the chosen synchrotron bunch structure and the (sub)frame length. In the ESRF's 7/8+1 mode for example, there can be thousands of pulses per (sub)frame. In contrast, for the 16-bunch mode, it is more likely that experiments require (sub)frames short enough to only contain a single pulse. Both the global sequencer as well as the telegram protocol play a great role in this (sub)frame-to-pulse alignment and the configuration of the (sub)frame length.

Intrinsic Error Correcting Property

The presented front-end design exhibits a robust operating principle which is rather unsusceptible to counting errors and noise. The reason for this is the combination of the discriminating nature of the single front-end stages, their pipelined arrangement as well as the fact that incident X-rays have a well-known energy. In the case that the coarse stage applies a wrong amount of coarse packages, the information about the resulting error is stored in the size of the residual charge. For example, if the coarse stage has applied too few charge packages, the fine stage can easily correct for this by applying more fine packages. In this way, the coarse stage's error is corrected for. Only if too many coarse package have been applied, the fine stage can not correct the resulting error. Due to this, the comparator threshold of the coarse stage is usually placed at voltages corresponding to a few photons above a single coarse charge package size. This ensures that influences like electronics noise in the coarse stage do not cause the application of too many coarse charge packages.

In the theoretical case of a perfect calibration, this leads to situation in which noise influences can only cause counting errors in the order of the fine charge package size, i.e. single photons in the above example. And thanks to the discriminating nature as well as the knowledge of the input signal size, noise contributions have to add up to the size of the configured fine comparator threshold to cause a counting error.

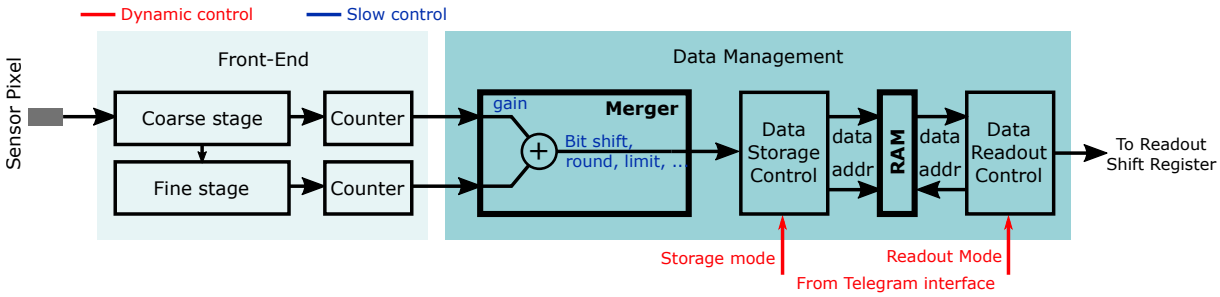


Figure 6.6: Schematic drawing of data flow in a channel of XIDer's readout ASIC from the front-end to the in-channel RAM cell. Merger, RAM, data storage and readout control cells are highlighted to underline their importance in the data pre-processing und storage.

6.1.2 Digital Data Management, Storage & Readout

XIDer is envisaged to be used in many different experiments with different requirements. For instance, some need better resolution with higher amounts of information per pixel, while others focus on higher frame rates. In general, there are two philosophies to provide enough flexibility for the wide variety of requirements: Either the detector sends out all the raw data for processing off-chip or the ASIC itself provides data pre-processing and storage capabilities. While the first approach admittedly provides the highest possible flexibility, it also causes very large data rates. As an example, a XIDer detector with a 100 µm pixel pitch and a size of a few 10 cm^2 will have a pixel number in the order of 100 k pixels. With a 16-bit resolution per pixel and a minium (sub)frame length of 175 ns, expected output data rates reach unmanageable sizes in the order of TB s^{-1}.

In order to avoid this, the XIDer project chose implementing on-chip digital data pre-processing and storage. A schematic of the basic structure is shown in figure 6.6. While the coarse and fine stages process the analog signal and perform the continuous conversion, digital counters count the amount of charge packages used in this process. The final result of the counters is then combined in the so-called *merger*. Configured via JTAG, the merger allows pre-processing the final (sub)frame photon count result with several options like, for instance, a configurable gain between the coarse and fine stage, rounding or dynamic range limit options. More details on the merger are provided in section 6.2.6.

In the end, the data storage control saves the merger output in the channel's RAM module where, depending on the chip iteration, a total of 192 or 256 16-bit words can be stored per ASIC channel. For the choice of the desired operation, the telegram interface receives commands for the data storage control unit on a (sub)frame-level. These commands can, for instance, issue writing the result of the (sub)frame to a given address, or adding it to a value stored at a given address or to discard it altogether. In this way, the on-chip storage control not only allows keeping individual frames for subsequent readout but also accumulating several (sub)frames on-chip, effectively implementing the digital integration scheme described in section 5.4. And with the option to discard (sub)frames, measurements can be pre-filtered on-chip. In this context, the set of pre-defined commands that can be performed by the storage control unit can be understood as a tool set to build a user-defined measurement cycle. Further details on the functions that can be implemented with the telegram protocol can be found in section 6.3.3.2. As demonstrated there and tested in section 7.3.1, the flexibility achieved by this tool set, for instance, allows generating photon count histograms in the RAM storage cells of the individual ASIC channels.

Behind the RAM cell, there is another data readout control unit which takes data from the RAM and sends it to the data output shift register. Just like the data storage control, the readout control unit is also controlled by the telegram protocol. Thanks to this (sub)frame-wise control, users can define, whether they want to continuously read out data from the ASIC for every (sub)frame or, whether data should be stored in the ASIC's RAM cells and read out after recording several images at a high frame-rate. This can be especially useful, when (sub)frame lengths are too short to read out the whole matrix.[2] In such a case, the telegram interface allows defining matrix readout frames with increased length.

For the 4x4 prototype channel matrices of the first ASIC iterations up to T5, there is a single serializer at the end of the chain of the channels' data output shift registers. Operating it at the system frequency suffices to achieve high enough data rates for these prototypes. For instance, at a typical (sub)frame length of 1 µs, streaming out every frame of the 4x4 matrix at 16 bit per channel, requires a bit rate of 320 Mbit s^{-1}.[3] In comparison, at a frequency of 440 MHz, the serializer provides a data rate of 440 Mbit s^{-1}. For larger designs, this will no longer be sufficient which is why the most recent chip iteration, T6, which contains a 16x16 channel matrix incorporates a 14 Gbit s^{-1} serializer IP designed by the STFC [80]. The strategy for the off-chip data transfer of even larger matrices is not yet decided on. Options like the implementation of a few serializers with large data rates opposed to a larger number of serializers with smaller data rates are currently being compared and discussed.

6.1.3 The Global Digital Control

The global digital control block contains modules which are supposed to be instantiated once per readout ASIC. Its structure is depicted in figure 6.7. For slow control, there is a custom-made JTAG interface which is further explained in section 6.3.2. As required by the standard IEEE 1149.1, this interface features four CMOS signals including a clock (TCK), data in- and outputs (TDI and TDO) and a control signal (TMS). The contents of the JTAG registers define the active slow-control configuration of the ASIC. For example, the JTAG registers hold the configuration bits for the current and voltage DACs (see section 6.3.1) which are necessary to bias the front-end in a well-defined operating point.

In addition, there is a global on-chip sequencer which generates dynamic digital control signals for the front-end's reset, injection and transfer switches. When an external RUN signal is provided, the sequencer repeatedly runs through a signal cycle which is pre-defined in slow control JTAG registers. Its function is further explained in section 6.3.3.1.

The previously mentioned global telegram interface is fed externally with 8b/10b encoded input commands which are organized in the custom-designed telegram protocol. The interface includes an 8b/10b decoder and a finite state machine accompanied by the necessary logic to decode the input commands and send the corresponding control bits to the storage and readout control logic units in each channel. A detailed explanation of the structure and contents of the telegram protocol can be found in section 6.3.3.2.

In addition to the mentioned global blocks, the ASIC also contains a serializer that that has already been explained in the previous section. Last but not least, on-chip frequency dividers generate the global clock tree. On the ASIC, there are three different clock

[2] When a readout is issued at the start of a (sub)frame, the whole matrix is read out in series. If the (sub)frame is too short for the whole matrix to be read out, the data stream is cut off.

[3] This includes the fact that the data link is 8b/10b encoded.

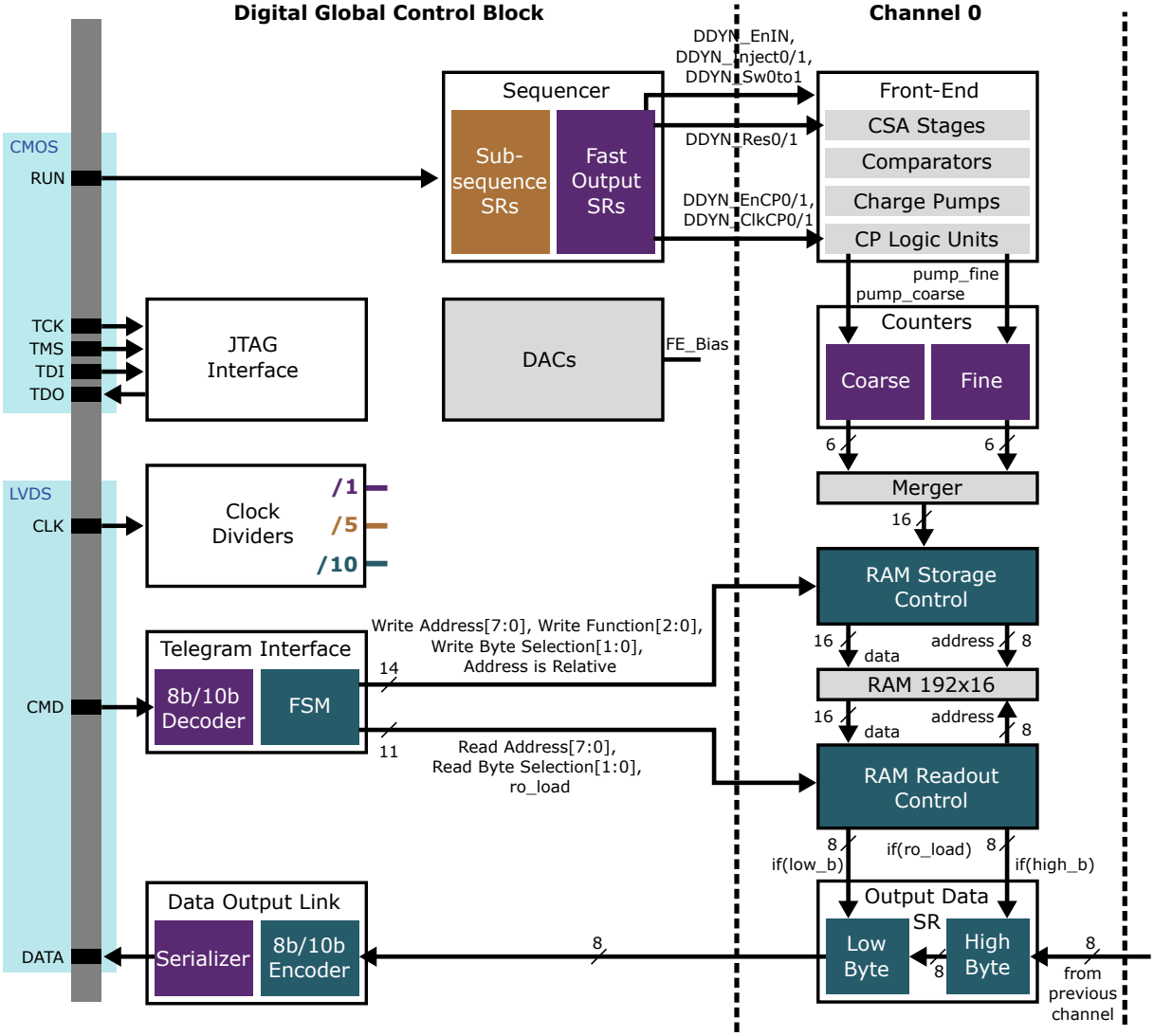


Figure 6.7: Overview of the circuit modules in the global digital control block and their interactions with a single channel. In order to illustrate the in-channel data flow, the image indicates a RAM implementation with a dual-port interface. The actual RAM module, however, uses a single-port interface. The chip features three clock domains which are indicated by the colored outputs of the clock dividers. On top of the indicated connections, the sequencer, DACs, merger and front-end are slow-controlled via the JTAG interface. In addition, the DACs generate the necessary front-end bias voltages and currents. For simplicity, both the JTAG interface and the front-end bias connections are not depicted.

domains (four with the JTAG domain). The color coding in the diagram illustrates which component operates in which of the available domains.

Clock Tree

The digital domain on XIDer's readout ASIC is synchronized to a system clock $f_{clk,system}$ which is provided externally through an LVDS input pad. Not all of the clocked blocks require the same high system frequency, though. Subsequently, one can save power by splitting the chip into several domains provided with different, reduced clock frequencies. At the same time, this relaxes timing constraints to avoid setup and hold time violations. For XIDer, the following list of frequency domains has been defined:

- **High frequency root clock $f_{clk,system}$:** Apart from acting as the root of the ASIC's clock tree, this clock has three main purposes. The dynamic control signals for the front-end require a fine granularity in time. Thus, the clock root drives the signals generated by the global on-chip sequencer. It also drives the data output link's serializer to achieve the highest possible data rates. At the same time, it is used to sample the telegram input link bit by bit.
- **Slow Sequencer Clock $f_{clk,system}/5$:** Besides the clock root, the sequencer is also provided with a slower version. It drives the sequencer tracks' parallel shift register which holds the sub-sequences. Since sub-sequences consist of 5 bits, this clock's frequency has to be a fifth of the root clock. For more details, see section 6.3.3.1.
- **I/O Word clock $f_{clk,system}/10$**: This clock is synchronous to the 8b/10b encoded words on the telegram command input and data output link. As such it allows keeping track the (sub)frame length and identifying the telegram instruction payload words (see section 6.3.3.2).
- **JTAG TCK:** Independent of the rest of the ASIC in terms of timing, the slow control clock is decoupled from and not synchronous to the system root clock.

In the current state of the project, there are no clear constraints for the clock tree. Subsequently, the frequency domains presented above are a preliminary proposal that has been chosen for the latest prototypes. Depending on additional functionality added in the future as well as more characterisation insight, it might be changed for future chip iterations. Project-related implications for the choice of $f_{clk,system}$ are discussed in the following sub-section.

System Frequency Choice & Storage Ring Synchronisation

A well-defined and controlled alignment of the synchrotron orbit with (sub)frames of the XIDer detector is mandatory for the execution of comparable experiments. In order to achieve this goal, the XIDer detector has to be synchronised to the orbit frequency of the ESRF's storage ring. The easiest approach for this synchronisation is to derive the system clock frequency $f_{clk,system}$ from the synchrotron's orbit frequency f_{orbit}. There are two technical constraints for this derivation:

As explained in section 6.3.3.2, the structure of the telegram protocol constrains the (sub)frame length to a multiple of 10 system clock periods. Thus, in order to fit an integer number of (sub)frames into a synchrotron orbit, the system clock has to fulfill the condition

$$f_{clk,system} \stackrel{!}{=} 10 \cdot m \cdot f_{orbit} \tag{6.10}$$

where m is an integer larger than 0. The other constraint is imposed by the measurement set-up. Instead of f_{orbit}, the set-up is provided with f_{RF} which is the repetition rate of the electron buckets in the storage ring, see section 2.3.4. For this reason, XIDer actually derives its system clock frequency from f_{RF} instead of f_{orbit}, where[4]

$$f_{RF} = 992 f_{orbit} \approx 352\,\text{MHz}. \tag{6.11}$$

Subsequently, the choice of $f_{clk,system}$ is constrained via

$$f_{clk,system} = k f_{RF} = k \cdot 992 f_{orbit} \stackrel{!}{=} 10 \cdot m \cdot f_{orbit}, \tag{6.12}$$

where k is not necessarily an integer and has to be chosen such that

$$k = m \cdot \frac{10}{992}. \tag{6.13}$$

While in principle, any integer value for m could be chosen, a large number is desirable to be able to choose (sub)frame lengths with a high granularity which helps aligning (sub)frames with X-ray pulses. At the same time, the multiplication factor k has to be easy to implement with an electronic circuit, preferrably an on-FPGA PLL. Resulting from these requirements, two possible options have been identified for the application of the XIDer detector at the ESRF:

$$f_{clk,system} \overset{k=\frac{5}{4}}{\approx} 440\,\text{MHz}, \tag{6.14}$$

$$\overset{k=\frac{5}{2}}{\approx} 880\,\text{MHz}. \tag{6.15}$$

where $m_{440\,\text{MHz}} = 124$ and $m_{880\,\text{MHz}} = 248$, respectively.

Subsequently, there is a choice to make between 440 MHz and 880 MHz. In comparison to $f_{clk,system} \approx 880\,\text{MHz}$, employing $f_{clk,system} \approx 440\,\text{MHz}$ is easier to implement, reduces power consumption and relaxes timing constraints, but it also results in the previously mentioned reduced accuracy for the alignment of (sub)frames to X-ray pulses. While the final choice is not yet made, the most recently synthesized design has been optimised for a system frequency of 880 MHz. However, the actual ASIC has not yet been operated with frequencies beyond 440 MHz due to a measurement set-up limitation as explained in section 8.3.2.3.

6.1.4 Layout & Floorplan

In terms of layout, the usual readout electronics of pixel sensors replicate their pixelated structure. Figure 6.8 shows a schematic drawing of this approach with the typical arrangement. Each channel of the ASIC is placed right underneath the corresponding pixel, it is meant to read out. In the depicted example, a channel is subdivided into an analog, digital and data storage part. The size of each compartment is arbitrary.

XIDer's readout ASIC uses a different approach. With a very large scale integration in mind, a 4x4 pixel matrix submodule as depicted in figure 6.9a has been proposed and implemented. Instead of having a 1-to-1 translation of the sensor's pixel map onto the ASIC, the proposed matrix has contiguous areas of analog and digital circuitry. In the most recent iteration, 16 pixels are combined in a 4x4 matrix submodule where all of

[4] see the ESRF parameter webapage: [25]

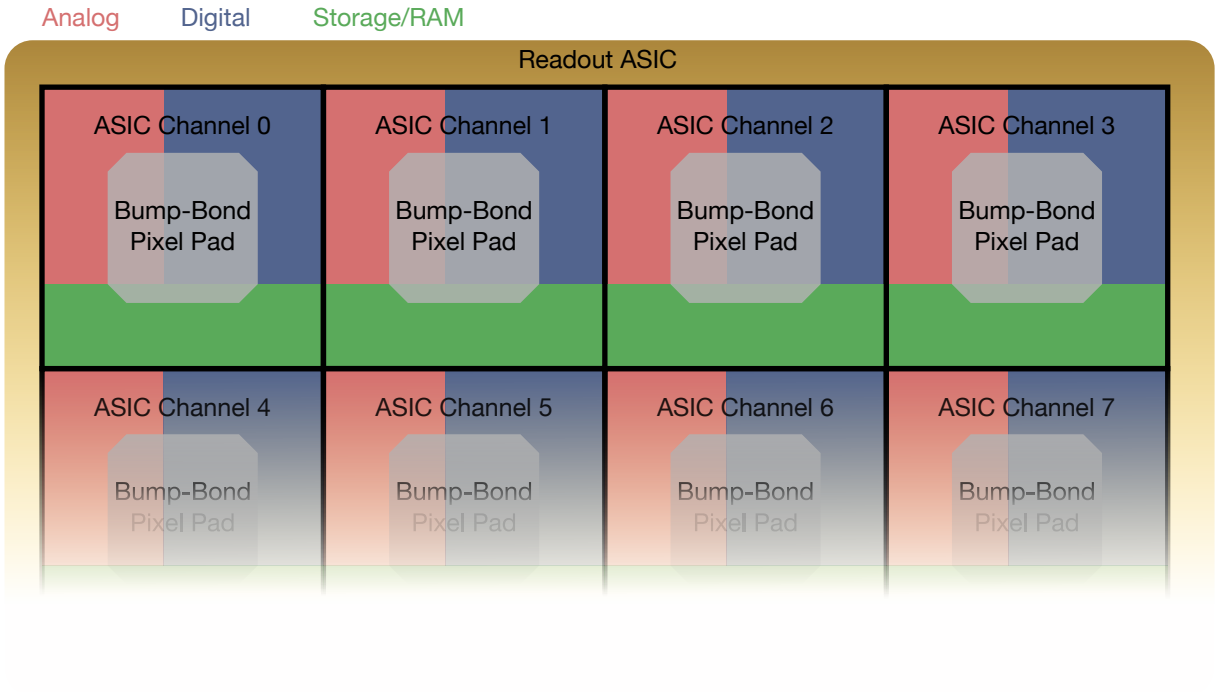
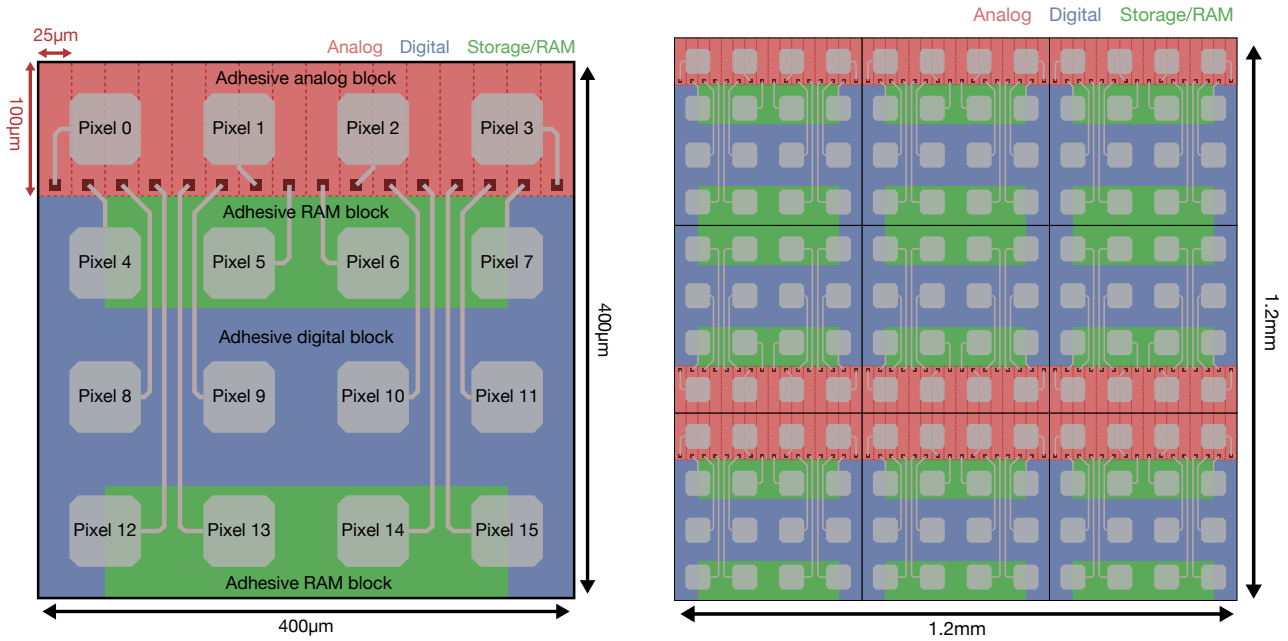


Figure 6.8: Typical 1-to-1 mapping of sensor pixels to readout ASIC channels illustrated with the example of the first two rows of a 4x4 pixel matrix.

the 16 analog front-ends are clustered into a single analog block. The rest of the 4x4 submodule is taken up by a large digital cluster as well as two smaller RAM storage clusters. There are several advantages for this kind of approach: First of all, areas of analog and digital circuits are not as scattered as in the 1-to-1 mapping. As a result, it is much easier to shield the sensitive analog parts from digital crosstalk. In addition, the contiguous approach results in less space consumption on the silicon die. This is due to the fact that, in order to isolate analog circuits in mixed mode designs, they are placed in deep n-wells as explained in 4.2.3. Deep n-wells usually follow special design rules that require additional free space in their surroundings. With the contiguous approach, the whole analog circuitry of a 4x4 matrix can be embedded into a single, large, deep n-well. The resuling single, large interface to the surrounding contiguous blocks only needs to fulfill the spacing requirement once for all of the 16 channels. Another advantage of this approach is that with a digital-on-top workflow, the automated component placing as well as routing works better the larger and more contiguous the areas it can work on are. Choosing one large digital block over several islands relaxes the constraints on the automated synthesis process.

In order to separate the most critical and sensitive areas of the analog domain from active digital areas, less active and less sensitive semi-custom design blocks have been placed as a shield in between. These modules are the custom-designed in-channel RAM storage cells which are further explained in section 6.2.7. As can be seen in the presented matrix module, the RAM cells are split into two contiguous blocks and there are small gaps in which the digital part actually reaches all the way to the analog area. This is due to the un-optimized RAM layout which will be fixed in future iterations to also fill the gaps.

Besides the aforementioned advantages, this contiguous approach also has its disadvantages: Firstly, due to the clustering of all the 16 analog parts in one area, channel input pads are not directly above the corresponding channel as it would be the case for a



(a) The 4x4 channel matrix basic module. The grey structures illustrate the RDL layer on top of the ASIC in which the pixel bump bond pads and their routing to the inputs of their respective channels (dark red) is carried out.

(b) A larger, 12x12 channel matrix built from the basic module. Modules are stacked in the x- and flipped in the y-direction.

Figure 6.9: Schematic illustration of the readout ASIC's 4x4 channel matrix basic module and how to use it as a building block for larger matrices.

1-to-1 mapping. Thus, the input signals need extra routing to their respective channel. Not only does this introduce parasitic capacitances which causes additional readout noise as explained in sections 6.2.1.5 and 6.5.6 but the wires can also act as antennas picking up more crosstalk from their surroundings like the input wires or pads of neighbouring channels. Also, due to the different rerouting wire length, the input capacitances vary from channel to channel which negatively impacts their matching. Subsequently, channels might behave differently in terms of noise performance and bandwidth.

Even with this contiguous layout approach, the area constraint for an ASIC channel is still dictated by the chosen sensor pixel size. Subsequently, for XIDer's readout ASIC, all the functionality has to fit into the $100 \times 100\,\mu m^2$ pixel area. In order to achieve this, the TSMC 65 nm technology has been chosen to allow for compact digital logic. With the low power option it has a core and IO voltage of 1.2 V and the chosen metallization option offers nine core metal layers with an additional aluminum redistribution layer on top. This redistribution layer is used to implement the channel input pads as well as their routing to the actual channel inputs. Output electrodes of the sensor pixels are then bump-bonded onto these input pads as described in section 8.2. Right underneath the redistribution layer lies the top-most metal layer which is reserved solely for the power distribution across the chip and is thus chosen to be as thick as possible.

Figure 6.9b shows the assembly of an example 12x12 matrix with the basic module. In order to further exploit the advantages of isolating the analog areas in large contiguous blocks, basic modules are flipped along the analog edge. For characterisation, this matrix

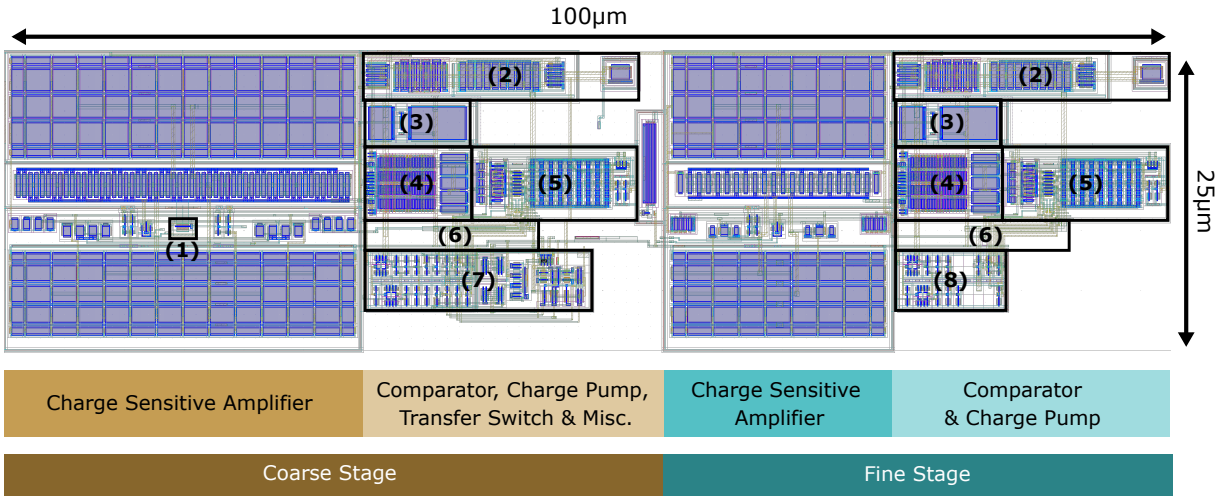


Figure 6.10: Front-end layout up to metal 3.

module has been instantiated on the most recent ASIC prototypes T5 and T6.[5]

6.1.4.1 Channel Layout

On T5 and T6, the most recent version of the analog front-end's layout is optimised for the 4x4 pixel matrix module presented above. The low metal layers as well as the doped substrate areas are depicted in figure 6.10. In total, the design is implemented in a 100 µm × 25 µm area. It intentionally features empty areas to leave space for additional necessary functionality that might be added in the future. An example for such additional circuitry is an analog implementation of the leakage/long afterglow compensation presented in the following subsection 6.1.5.

The layout is split into two halves with the coarse stage on the left hand side and the fine stage on the right hand side. In between these lies the transfer capacitor switch which is connected to the transfer capacitor in the upper metal layers. Both stages are layouted in similar fashion with the CSA to the left and the charge pump, comparator and additional auxiliar modules to the right side. Each stage has its own V_{ref} buffer to generate the dump node for the charge pump as well as a the reference potential for the transfer switch as explained in sections 6.2.3 and 6.2.4. Additionally, there is a pool of standard logic gate cells for both stages which implement the inversion of switch control signals[6].

Since the analog front-end will be surrounded by digital circuits, the layout puts a special focus on shielding analog signals from noise pickup. Due to this, the whole design is embedded in a deep n-well (see section 4.2.3) which is biased by a guard-ring. The guard-ring is structured such that it surrounds the whole analog design as well as single circuit modules. Highlighted in the left part of the figure, is the front-end's input. From the contact on metal 1, this node is wired up to the redistribution layer (RDL) on top of the chip. Since the input is the front-end's most sensitive node, it is shielded on its way to the RDL by a metallized tunnel-like structure that is biased to a fixed potential. In addition, the highlighted sensitive outputs of both stages are mostly isolated from the rest

[5] See section 6.6

[6] Most of the switches in the front-end are charge injection compensated which is why they also need an inverted version of their control signal

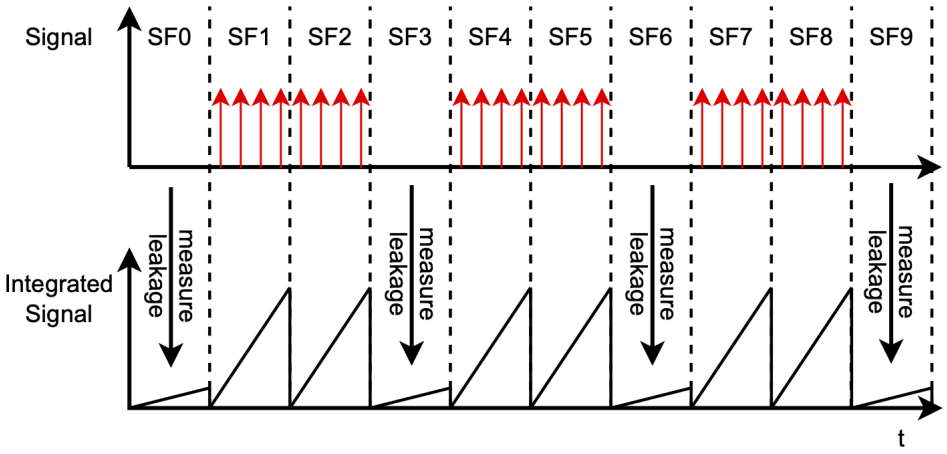


Figure 6.11: Proposed concept for the compensation of long afterglow components. With dark (sub)frames in between measurements, the afterglow is supposed to be tracked [73].

of the circuitry to minimize noise from capacitive coupling. For this reason, there is a small metal 3 sheet on a fixed potential that shields the outputs from digital signals routed above (not visible). In order to achieve the best possible matching, a common-centroid layout surrounded by inactive dummy structures is employed for differential transistors throughout the design. The large current sources at the top and bottom of the charge sensitive amplifiers illustrate this visibly.

6.1.5 Leakage Compensation Concept

As described in chapters 3 and 5, XIDer employs high-Z compound sensor materials. Due to the trapping and detrapping dynamics of these materials, they can exhibit afterglow with time constants much larger than the (sub)frame lengths of measurements performed with XIDer. For this reason, the amplitude and shape of measured signals always depends on the current state of the sensor which is governed by the measurement history. And due to the complicated nature of these dynamics, predictions of the sensor afterglow behaviour prove to be difficult. This section proposes a planned leakage compensation concept that has not yet been tested.

In addtion to the intrinsic leakage and long afterglow suppression by the digital integration (see section 5.4), XIDer's readout concept also allows to track afterglow with long time constants as presented in [73]. Figure 6.11 illustrates the concept of this method. The idea is to track the afterglow with dark (sub)frames in between measurement (sub)frames where the sensor is not illuminated. The gained information in these dark (sub)frames can then be used to correct measurements shortly before or after the afterglow measurement.

There are several ideas on how to implement this correction which can either operate in the analog or digital domain. For example, in the analog domain, the measured afterglow amplitude could be stored as a voltage V_{ag} on a capacitor. V_{ag} could then be used to control a current source which injects an afterglow compensating current into the front-end input. Such a solution is not yet implemented on the readout ASIC. In contrast, a digital correction could be performed with the help of the already telegram protocol. Measured amplitudes in the leakage (sub)frames could be subtracted from the counts of (sub)frames shortly before or after in the pixel RAM storage. The advantages and disadvantages of

these implementations are currently being discussed and studied.

An important point to menation in this context is that in order for the afterglow tracking to work, the beamline has to provide time windows in which the detector is not illuminated. To provide an example, in the 7/8+1 mode of the ESRF[7], such dark (sub)frames could be recorded in the gaps between the quasi-continuous illumination.

6.2 Channel Components

In this section, the individual circuit compartments included in a single channel of XIDer's readout ASIC are discussed in detail. All of the presented components follow the design philosophy of constant power consumption. The reason for this is as follows: A single readout ASIC is supposed to read out sensor pixel matrices with at least a few hundred thousand if not a million of pixels. At such large scales, not only the channel's average power consumption is of concern, but also the dynamics of it, i.e. whether the instantaneuous power consumption changes over time, follows patterns and so on. This is due to the fact that supply lines, no matter how wide the designer chooses them to be, exhibit a finite resistance. Together with additional parasitic capacitances on the line, the whole power net acts like an RC lowpass. Subsequently, if a circuit has a sudden and steep increase or decrease in the current it draws from the supply net, the local supply voltage might vary for a brief moment. If this occurs for a single circuit, this variation is negligible or not even noticeable. However, pixel matrix readout ASICs consist of a large array of equal circuits, each behaving in the same way. Thus, in most cases, it is not too uncommon, that all of these start executing the same operation at the same time. Then, the small, negligible supply voltage drops generated by each circuit can add up to significant scales. As a result, the performance of all the electronics affected by such a local drop changes. In turn, parts of the pixel matrix can end up acting differently than the rest or stop working altogether.

The analog part of XIDer's readout ASIC is designed with this problem in mind. As such, it employs circuits with constant power consumption wherever possible. Of course, this comes with the tradeoff of slightly higher average power consumption, but it circumvents the problem of power spikes affecting local supply voltages which are very hard to predict.

6.2.1 Charge Sensitive Amplifier

A charge sensitive amplifier (CSA) is a circuit that converts an input charge Q_{in} to an output voltage V_{out}. The circuit diagram in figure 6.12 shows the CSA's basic structure as it is implemented in the front-end stages of XIDer's readout ASIC. It is split into three components: the inverting amplifier with its voltage amplification $-A_v$, the feedback capacitor C_f and a reset switch S. While single-ended implementations are an option, XIDer employs a differential amplifier.

6.2.1.1 Charge Integration

The parallel combination of C_f and S form a feedback path for the differential amplifier. When S is closed, the in- and output nodes are shorted. As a result, $V_{in} = V_{out}$. With an infinite amplifier gain $-A_v$ the negatively fed back amplifier ensures that $V_{in} = V_{out} = V_{ref}$. After opening S, an ideal CSA with an infinitely large gain integrates incoming charge

[7] see setion 2.3.4

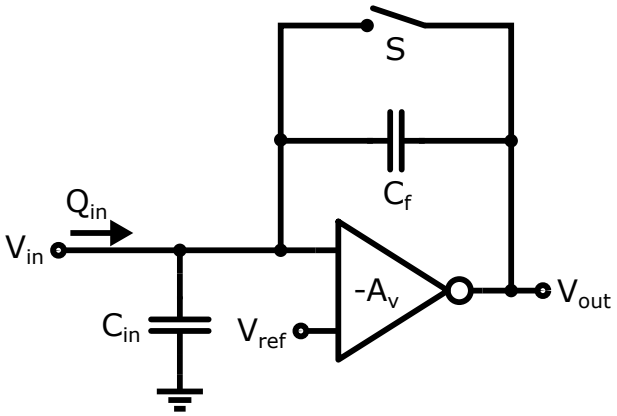


Figure 6.12: Circuit diagram of the CSA structure employed in the analog front-end of XIDer's readout ASIC.

Q_{in} on C_f with a proportional increase in the output voltage $\Delta V_{out} = Q_{in}/C_f$, while V_{in} is held at the level of V_{ref}. In reality, however, the gain $-A_v$ is finite which causes V_{in} to be slightly dependent on the input charge Q_{in}. The deviation from V_{ref} can be determined via

$$\Delta V_{in} = V_{in} - V_{ref} = \frac{Q_{in}}{C_{in} + (1 + A_v)C_f}, \tag{6.16}$$

where C_{in} is the CSA's input capacitance. In a sensor readout chip, C_{in} is the sum of the sensor capacitance C_{det} and the parasitic amplifier input capacitance $C_{in,amp}$ which is formed by stray capacitance on the input wire as well as parasitic contributions of the amplifier's input transistor (see section 4.2).
As a result of the moving V_{in}, the CSA output voltage actually exhibits a step with the size of

$$\Delta V_{out} = -\frac{Q_{in}}{C_f} \frac{1}{1 + \frac{1}{A_v} + \frac{C_{in}}{A_v C_f}} \tag{6.17}$$

as a reaction to incoming charge. Thus, the actual charge-to-voltage gain of the amplifier is reduced significantly, if C_{in} and $A_v C_f$ have equal size and if A_v is small. Both of these conditions can be fixed by designing an amplifier with $|A_v| \gg 1$ [41] [42]. Other requirements specific to XIDer are a high enough bandwidth to keep up with the charge pump frequency, low noise for a good signal-to-noise ratio as well as low power consumption to reduce the heat dissipation.

The following paragraphs dwell into the system-theoretical details and calculations to derive which parameters play an important role. At the end of these detailed discussions, there will be a summary of the CSA's most important properties and their tradeoffs.

6.2.1.2 Requiremenets & Amplifier Topology Choice

As the core element of the CSA and thus of the analog front-end as a whole, the design of the amplifier has a very large impact on the detector's overall performance. As a result, besides a thorough study of different architectures, an in-depth optimisation process is necessary. Before diving into the actual design, the following list gives a brief overview of the most important design constraints for the CSA in XIDer's readout ASIC:

- **Amplifier open-loop voltage gain:** Needed to fix the CSA input voltage at the virtual ground and should at least be a few 100.
- **Bandwidth:** The amplifier has to keep up with a maximum charge pump frequency of 200 MHz for the coarse and 100 MHz for the fine stage in the CSA's closed-loop configuration.

- **Dynamic output voltage range:** Needed for a comparison of the CSA output voltage with a comparator threshold level. It depends on the size of C_f and should at least cover the equivalent voltage range of a single charge pump package $\Delta V_{out,dyn} \overset{!}{>} Q_{CP}/C_f$.[8] As it turns out, a range of 400 mV suffices in most cases.

- **Output voltage noise:** While a clear limit has not yet been defined over the coarse of XIDer's R&D phase, noise should be minimized as far as possible. As further explained in section 6.5.6, the CSA's output voltage noise is mainly responsible for the detector's dark count rate. As a result from detector simulations performed in [8], a dark count rate of $1\,\mathrm{ph\,h^{-1}\,pix^{-1}}$ has been deemed acceptable. With typical measurement conditions foreseen for the XIDer detector, this corresponds to an input referred noise[9] level in the order of $375\,\mathrm{e^-}$.

- **Power:** As with the noise, there is no defined power limit. But, in order to minimize heat dissipation, the power consumption should be kept as low as possible. In order to achieve this, the amplifier is optimised to fulfill the requirements listed above at the lowest achievable power consumption.

For the choice of the amplifier topology, there are several arguments: First, as mentioned before, the amplifier is required to draw a constant current from the supply net to avoid sudden supply voltage variations. Second, in the desired operation of the front-end, a well-defined common potential V_{ref} which everything else is compared to is helpful. This potential is supposed to be the virtual ground for incoming signals, such that the CSA's output voltage is at V_{ref} when no charge has been integrated, yet. Such a topology eases the setting and calibration of the comparator threshold level to match a voltage that corresponds to a certain input charge. Third, a differential structure helps with the suppression of environmental noise due to its common-mode noise rejection as mentioned at the beginning of section. This is further explained in the appendix in section B.3.2. Last, in order to allow a comparison of the CSA output with the threshold voltage via a comparator, the amplifier output voltage has to be single-ended.

In order to fulfill all of these needs, the amplifier topology as drawn in figure 6.13 has been chosen. It features a differential input pair implemented by the p-MOSFETs M_1 and M_2. The choice of p-MOSFETs over n-MOSFETs is deliberate and has been made for two reasons. Since the detector is supposed to only read out the sensor's anode, the incoming charge is negative. Due to the fact that the proposed CSA topology needs a negatively fed back amplifier, the negative input charge leads to a positive output voltage. As a result, the CSA's baseline V_{ref} which is associated with an empty feedback capacitor, has to be at a low voltage level to allow for a large charge integration range before the supply voltage level is reached. And since in the negative feedback scheme $V_{in} = V_{ref}$, the gate voltages of both input transistors have to be at a low voltage level. Subsequently, p-MOSFETs are the preferred option for the differntial input pair. The actual choice of V_{ref} is discussed below. Additionally, as will be demonstrated later in this section, the input transistors of a differential amplifier are the main contributors to the generated electronic noise. And p-MOSFETs are known to exhibit less flicker noise than their n-MOSFET counterparts [42].

[8] For a more conservative approach with a larger safety margin, 1.5 or two charge packages should be chosen.

[9] This refers the CSA's output voltage noise to an equivalent input charge by dividing the voltage noise by the feedback capacitor. Further explanations follow in section 6.2.1.5.

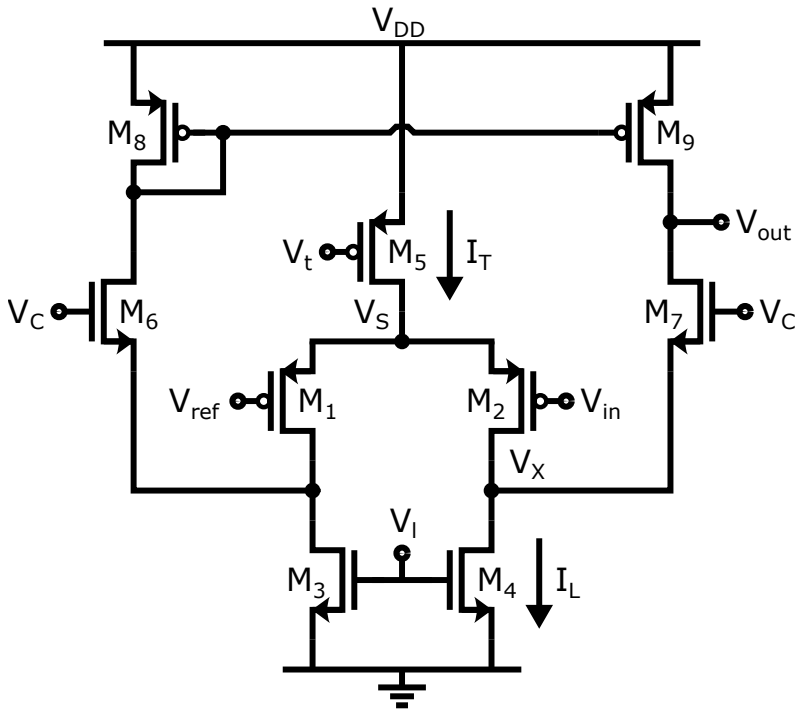


Figure 6.13: Circuit diagram of the differential amplifier implementation in the analog front-end of XIDer's readout ASIC

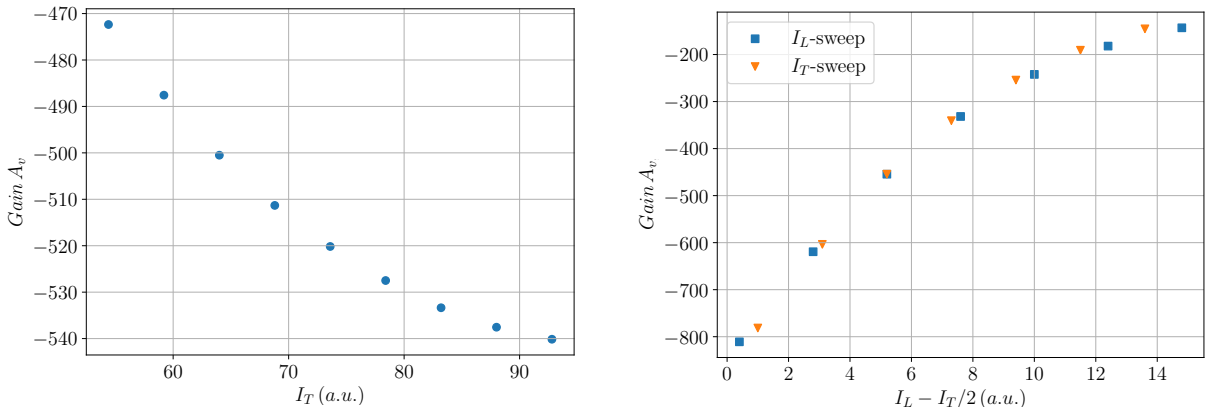
A well-defined power consumption is ensured by the current sources M_3, M_4 and M_5 which bias the circuit in the desired region of operation. The corresponding bias voltages V_t and V_l are generated via current mirrors which, in turn, are fed with DAC-controlled bias currents. For further reference, M_5 and $M_{3/4}$ are denoted as *tail* and *legs* current sources respectively.

In order to improve the amplifier's dc gain, M_6 and M_7 implement so-called folded cascodes. Their operation principle is similar to the cascodes presented in section B.2. The folded structure, however, allows for a higher output voltage swing [60]. And in addition to the tail and legs current sources, the amplifier is loaded with an active current mirror. As discussed in section B.3.2, this results in a single ended-output voltage, while using the other, unused output node to boost the amplifier's differential-to-single-ended gain.

The following explanations focus on the most important steps in the analysis and optimisation process of this design. As usual, the first step is a large signal analysis which focusses on biassing all the involved compartments in the desired operation region. The aim of this step is to set limits for the device parameters and biasses in which the circuit exhibits basic functionality. It acts as a foundation for subsequent optimisation steps. After that, a small-signal analysis is provided which explains how to achieve the desired performance and which parameters play an important role. The final part of this section summarizes the results of this rather technical and detailed analysis in simpler terms. In addition, there will be a table listing the figures of merit for the most recently implemented CSA.

6.2.1.3 Biassing & DC Characteristics of the Amplifier

Since all of the involved transistors work as differential pairs, current sources, current mirrors or cascodes, they have to be operated in saturation region. A sub-threshold operation is also possible. However, sub-threshold circuits usually exhibit lower bandwidths



(a) Dependence on I_T

(b) Dependence on the difference $I_L - I_T/2$

Figure 6.14: Full-blown analog simulation of the open-loop DC gain $A_{v,tot}$ of the front-end amplifier depending on the bias currents I_T and I_L.

which makes them less attractive for XIDer's front-end amplifier.

For all the presented considerations, the assumption $V_{in} = V_{ref}$ is made which holds true as long as the CSA's negative feedback is in action and the amplifier's open-loop gain is large enough. On top, the design is assumed to be fully symmetric. As a result, the device parameters of transistors on the opposite sides of the differential amplifier structure are assumed to be equal. Additionally, for all the involved transistors, only first-order effects are taken into account.

The bias currents I_T and I_L are the first and most important choice to make. Not only do their values dictate circuit's bandwidth, gain and noise, but they also determine its power consumption with

$$P_{avg} = 2V_{DD}I_L, \tag{6.18}$$

where $V_{DD} = 1.2\,\mathrm{V}$ in the chosen technology. This stems from the fact that the current-source transistors M_3 and M_4 force a current with the size I_L through both symmetrical sides of the amplifier. As a result, the total drawn current by this design is $2I_L$.

The design process and optimisation of an analog circuit is always a tradeoff of many different quantities with opposite dependencies. For the amplifier, the first introduced quantity is the *open-loop DC gain* $A_v = v_{out}/v_{in}$. As demonstrated in equation 6.17, a large A_v improves the the CSA's charge-to-voltage gain. This is due to the fact that the size of A_v dictates how well the amplifier manages to establish V_{ref} as the virtual ground as a no-charge reference level. The determination of A_v involves the application of MOSFET small-signal models. For the sake of clarity and brevity, the actual calculation has been moved to section C in the appendix. As presented there, A_v can be approximated via

$$A_v \approx -g_{m1}(r_{ds8} \parallel g_{m6}r_{ds6}(r_{ds1} \parallel r_{ds3})) \propto -\frac{\sqrt{I_T}}{I_L - I_T/2}. \tag{6.19}$$

A very intuitive understanding of this equation can be found with the following observation: In general, the gain of an amplifier is given by the product of its effective transconductance G_m and its output resistance r_{out}. Here, G_m is given as the ratio of the circuit's output current and its input voltage i_{out}/v_{in}. In the chosen architecture, the transconductance of the differential input pair g_{m1} dictates G_m. Each transistor of the differential input pair, in turn, conducts the current $I_T/2$ which leads to $G_m \propto \sqrt{I_T}$, the numerator of A_v. And r_{out} is dominated by the biassing of the folded cascodes. In fact, the size of the current flowing

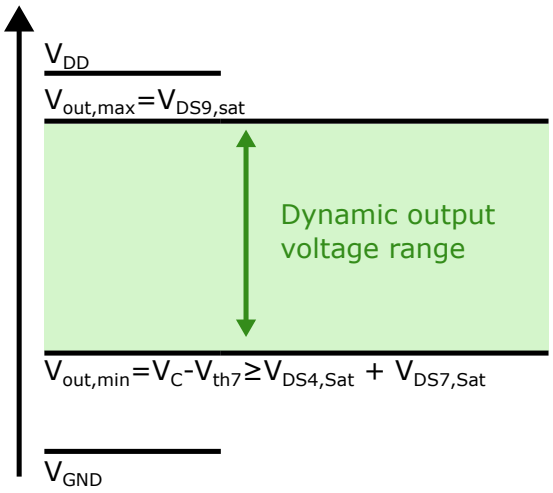


Figure 6.15: Dynamic output voltage range of the amplifier in the analog front-end of XIDer's readout ASIC.

through the active current mirror load M_8 and M_9 has a major impact on r_{out}. This is due to the fact that the drain-source resistances of M_8 and M_9 contribute a substantial part of r_{out}. And since for a transistor in saturation $r_{ds} \propto L/I_D$, the choice of $I_{D8/9}$, is crucial for the size r_{out}. The chosen architecture allows choosing this current via

$$I_{D8/9} = I_L - \frac{I_T}{2} \tag{6.20}$$

which is the denominator of A_v's approximated current dependence. Subsequently, a large dc gain can be achieved by tuning the two bias currents such that the difference $I_L - I_T/2$ is small. Figure 6.14b shows a plot of the amplifier's dc gain $A_{v,tot}$ vs. the difference $I_L - I_T/2$. As demonstrated, the smaller the difference of the two currents, the higher the absolute value of the gain. This is due to the aforementioned fact that with a decreasing difference, the current flowing through the folded cascode is decreasing and the current in the differential input pair is increasing. Subsequently, the amplifier's output resistance and overall transconductance increase which results in a higher gain. The two different curves are obtained by either sweeping I_T and keeping I_L constant or vice versa. Figure 6.14a shows the simulated gain in dependence of I_T for a fixed current difference $I_L - I_T/2$. As predicted by equation 6.19, a higher gain is achieved by a higher I_T.

Another important DC quantity is the amplifier's dynamic output voltage range. This discussion splits up into two branches: The actual dynamic range the amplifier can achieve and the range of possible virtual ground voltages V_{ref} in the closed-loop operation. In order to keep all of the involved transistors in saturation, the upper and lower boundaries of the former one are ultimately given by:

$$V_C - V_{th7} \leq \boldsymbol{V_{out}} \leq V_{DD} - |V_{DS9,Sat}|, \tag{6.21}$$

where $|V_{DS9,Sat}| = \sqrt{2(I_l - I_t/2)/(\mu_p C_{ox}) \cdot L_9/W_9}$ in which μ_p is the hole mobility and C_{ox} is the gate capacitance per area. While the upper boundary can be tuned to be high via L_9 and W_9 in correspondence to the bias currents, the lower boundary is tunable via the cascode voltage V_C. The lower limit of V_C itself is driven by the saturation condition of M_4 and M_7. As such, it can be found as

$$V_{DS4,Sat} + V_{DS7,Sat} + V_{th7} \leq \boldsymbol{V_C}. \tag{6.22}$$

Just as for $|V_{DS,Sat9}|$, $V_{DS4,Sat}$ and $V_{DS7,Sat}$ can be chosen small by choosing a small

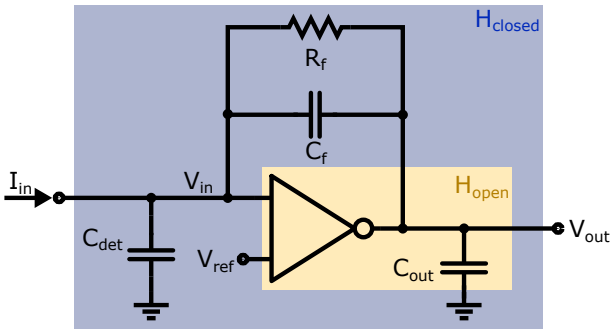


Figure 6.16: Charge sensitive amplifier with a differential amplifier and a feedback capacitor C_f. The reset switch is represented by its resistance R_f which opens a second feedback path parallel to C_f.

$L_{4/7}/W_{4/7}$. As a result of this equation, if the designer or the user manages to tune V_C exactly to its minimum value the largest achievable dynamic output voltage range is given as

$$V_{DS4,Sat} + V_{DS7,Sat} \leq \boldsymbol{V_{out}} \leq V_{DD} - |V_{DS9,Sat}|. \tag{6.23}$$

Figure 6.15 illustrates this with respect to the available supply and ground voltage levels. In a realistic design however, transistors exhibit manufacturing uncertainties which can lead to mismatch between the symmetric sides of the amplifier. Additionally, transistor parameters such as their lengths, widths or threshold voltages can vary. As a result, it is advisable to always choose V_C with an actual safety margin on top of $V_{DS4,Sat} + V_{DS7,Sat} + V_{th7}$. A typical value would be 100 mV to 200 mV.

6.2.1.4 CSA AC Characterstics

This subsection is concerned with the closed-loop transfer function of the CSA to describe how the circuit's output voltage reacts to a dynamically changing input current.

$$H_{closed}(s) = \frac{v_{out}(s)}{i_{in}(s)} \tag{6.24}$$

As usual, the evaluation of this circuit's AC characteristics proves to be much more complex and involved. For a full picture, all the transistors in figure 6.13 have to be replaced with their small-signal model including the most important parasitic capacitances (see figure 4.10 in section 4.2.1). Since the resulting set of equations is quite extensive, this section concentrates on presenting an approximated transfer function and its properties. A detailed derivation of the approximation can be found in the appendix in section C.2. The derivation is based on the circuit schematic drawing in figure 6.16. Since for XIDer, the pixel capacitance C_{det} dominates the front-end's input capacitance, the schematic only includes C_{det} at the circuit's input.

The approximated closed-loop transfer function of the CSA is given as:

$$H_{closed}(s) \approx \frac{H_{closed}(0)}{(1 + \frac{s}{s_{p,fb}})(1 + \frac{s}{s_{p,amp+}})(1 + \frac{s}{s_{p,amp-}})} \tag{6.25}$$

with a single real pole at

$$s_{p,fb} = \frac{1}{R_f C_f} \tag{6.26}$$

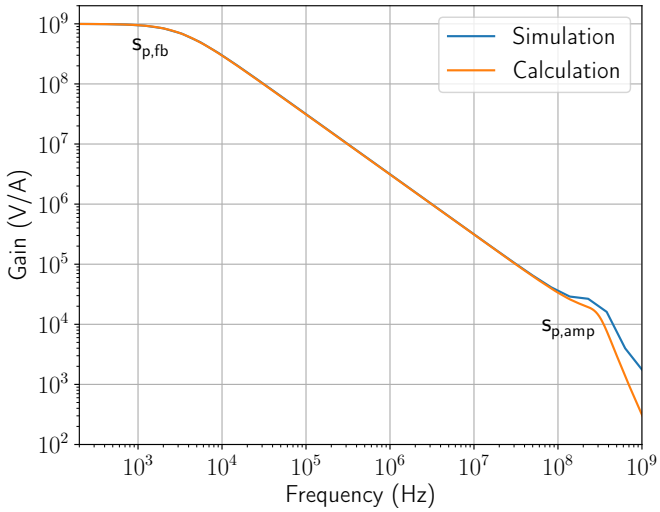


Figure 6.17: Comparison of the approximated closed-loop transfer function H_{closed} with a gain-vs-frequency plot extracted from an analog simulation.

and a complex conjugate pole pair at

$$s_{p,amp+/-} = \left(\frac{1}{2}(s_{p,mirr} + s_{p,out}) \pm \sqrt{s_{p,mirr} s_{p,out} \frac{C_f}{C_{det}} A_v} \right). \tag{6.27}$$

where

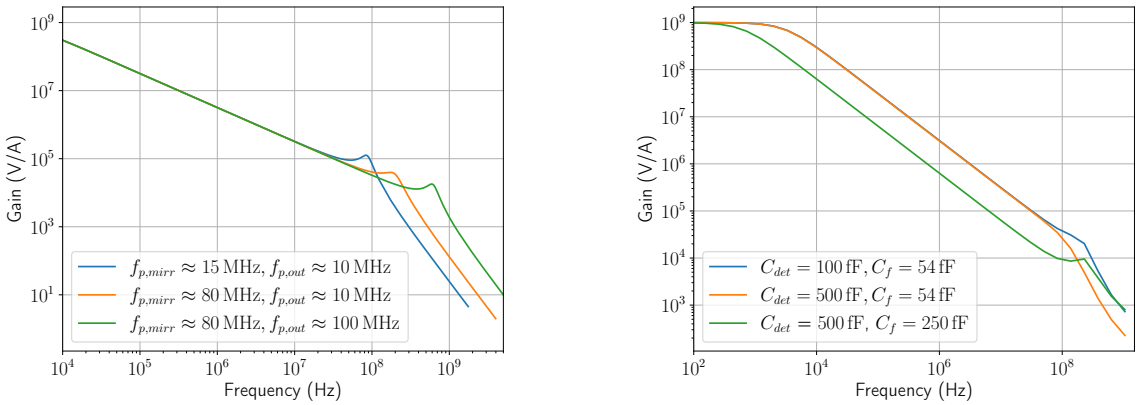
$$s_{p,mirr} \approx \frac{g_{m8}}{2C_{mirr}}, \tag{6.28}$$

$$s_{p,out} \approx \frac{1}{r_{out} C_{out}} \approx \frac{1}{r_{ds8} \parallel (g_{m6} r_{ds6} (r_{ds1} \parallel r_{ds3})) C_{out}} \tag{6.29}$$

are poles of the amplifier's open-loop transfer function. In this context, C_{mirr} is the sum of the parasitic gate-source and gate-drain capacitance of the transistors M_8 and M_9 in figure 6.12. C_{out} denotes the CSA's output capacitance. The closed-loop transfer function's dc value is given as $H_{closed}(0) = \frac{A_v R_f}{1-A_v} \approx R_f$.

In the integrating state, the reset switch is open and R_f is very large. As a result, $s_{p,fb} \to 0$ which means that the circuit exhibits a pole at $s \approx 0$. With $s_{p,fb} \to 0$, the circuit's DC gain rises to infinity which is the expected behaviour of an integrating system. In theory, with an open reset switch, an incoming DC current will inevitably cause an infinite output voltage signal because the charge can only be stored on the capacitor. In reality, this will only work until the output voltage hits its upper limit of the dynamic output voltage range.

The plot in figure 6.17 shows a comparison of the approximated transfer function $H_{closed}(s)$ with an analog simulation. Transconductances, resistances and capacitors that have to be substituted in $H_{closed}(s)$ have been extracted from the analog simulation. As can be seen, calculated approximation and simulation lie in good agreement up until the complex conjugate pole pair. Even the position of $s_{p,amp+/-}$ is predicted quite well by $H_{closed}(s)$. The approximation, however, is missing a zero s_z at high frequencies. Its position is close to $s_{p,amp+/-}$ and causes the gain to drop less rapidly beyond $s_{p,amp+/-}$ than predicted by $H_{closed}(s)$. s_z finds its origin in parasitics which have been neglected



(a) Calculated closed-loop transfer function of the CSA in XIDer's analog front-end for different values of $s_{p,mirr}$ and $s_{p,out}$.

(b) Simulated closed-loop transfer function for different values of C_{det} and C_f. As demonstrated by the peak's size at the high-frequency pole, the ratio C_f/C_{det} plays a great role in the circuit's stability.

Figure 6.18: Closed-loop transfer function of the CSA for varying device parameters.

throughout the calculated approximation for clarity. Subsequently, with an even more elaborate analysis which will not be presented here, one could find an even better fitting approximation.

The complex conjugate pole pair plays a defining role in the CSA's speed and stability. Figure 6.18a shows its position in the transfer function depending on $s_{p,out}$ and $s_{p,mirr}$ of the open-loop system. In a Bode plot, a complex conjugate pole pair appears as a single pole. If its imaginary part is much larger than its real part, the Bode plot exhibits a spike around the pole frequency. This spike can be interpreted as a resonance and has to be treated carefully.

If the gain of this resonance rises to high values, the circuit might suffer from stability issues. For a deeper discussion of complex conjugate pole pairs, the reader is referred to Appendix D in [61]. As can be seen in the plot, both $s_{p,out}$ and $s_{p,mirr}$ contribute equally to $s_{p,amp+/-}$. In order to achieve a high CSA speed, the same conclusions as for the open-loop case can be made: $s_{p,out}$ and $s_{p,mirr}$ need to be chosen high. Subsequently, C_{out} and C_{mirr} as well as r_{out} need to be small, while g_{m8} has to be large.

Another important point is that the ratio of feedback and input capcitors C_f and C_{det} solely appear in the square root of $s_{p,amp+/-}$. Subsequently, they have a dominant effect on the size of its imaginary part. With a larger C_{det} compared to C_f, the imaginary part and with it the extent of the gain's peaking at $s_{p,amp+/-}$ is decreased. This is shown in figure 6.18b where the gain has been simulated for different values of C_{det} and C_f. As a result, the circuit's stability is increased with increasing C_{det}. While a stable circuit is desirable, a slight peaking provides the circuit with extra speed. The gain-vs-frequency plot alone does not help in finding an optimum here. The tradeoff between circuit stability and desired speed is far from straightforward and needs to be analysed with the help of transient simulations that show the circuit's response to sudden changes in the input current. As a side note: In this plot, the frequency range is chosen such that the low frequency pole $s_{p,fb} = 1/(R_f C_f)$ is visible. As can be seen, it moves with the size of C_f.

6.2.1.5 CSA Noise Performance

Before moving on to a summary of the derivations above, there is one last remaining design property which is the output voltage noise generated by the amplifier. It is usually expressed in an *equivalent noise charge* (ENC). The ENC's idea is to relate the output voltage noise of the circuit $\langle v_{n,out} \rangle$ to an equivalent input charge. In this view, the generated voltage noise $v_{n,out}$ can be compared to input signals and the circuit's *signal-to-noise ratio* can be determined. Since the gain of the of input charge to output voltage is given by the feedback capacitor C_f, the ENC can be calculated via

$$ENC = C_f v_{n,out}. \tag{6.30}$$

Subsequently, the determination of $v_{n,out}$ allows finding the ENC.

Each transistor in the amplifier generates a noise current. Neglecting all the other noise sources but thermal, the spectral density of this noise current is described via equation 4.49:

$$\frac{d\langle i_n^2 \rangle}{df} = \frac{8}{3} k_B T g_{m,k}, \tag{6.31}$$

where k is the number of the corresponding transistor. With the circuit's output resistance r_{out}, this noise current is converted to an output noise voltage with the spectral density

$$\frac{d\langle v_{n,out,open}^2 \rangle}{df} = \frac{d\langle i_n^2 \rangle}{df} r_{out}^2. \tag{6.32}$$

This output noise voltage can then be referred back to an input noise voltage at the gate of the CSA's input transistor via

$$\frac{d\langle v_{n,in}^2 \rangle}{df} = \frac{d\langle v_{n,out,open}^2 \rangle}{df} \frac{1}{|A_{v,tot}|^2}, \tag{6.33}$$

where $A_{v,tot}$ is the open-loop gain of the amplifier.

$d\langle v_{n,in}^2 \rangle / df$ now generates a noise current at the CSA's input node $d\langle i_{n,in}^2 \rangle / df$. This current flows through the input impedance Z_{in} which is dominated by the detector capacitance C_{det} such that

$$\frac{d\langle i_{n,in}^2 \rangle}{df} = \frac{d\langle v_{n,in}^2 \rangle}{df} |(sC_{det})^2|. \tag{6.34}$$

And with the closed-loop transfer function, this noise current now leads to a total closed-loop output noise voltage spectral density of

$$\frac{d\langle v_{n,out,closed}^2 \rangle}{df} = \frac{d\langle i_{n,in}^2 \rangle}{df} |H_{closed}(j\omega)|^2. \tag{6.35}$$

In the end, an integration over all frequencies yields the final result:

$$\langle v_{n,out}^2 \rangle = \int_0^\infty \frac{d\langle v_{n,out,closed}^2 \rangle}{df} df = \int_0^\infty \frac{d\langle i_{n,in}^2 \rangle}{df} |H_{closed}(j\omega)|^2 df. \tag{6.36}$$

In most cases, the spectral density to be integrated is dominated by thermal noise which usually has a white spectrum. With the inclusion of the transfer function $|H_{closed}(j\omega)|$ as a factor in the equation above, this means that circuits with a large bandwidth integrate

Transistor	% of noise in coarse stage	% of noise in fine stage	Function
M_1	17.1	19.3	Input
M_2	21.2	20.5	Input
M_3	20.6	19.0	Legs current source
M_4	16.2	20.7	Legs current source
M_5	1.2	1.4	Tail current source
M_6	1.8	1.0	Cascode
M_7	2.5	1.4	Cascode
M_8	5.6	4.5	Current mirror load
M_9	5.2	3.7	Current mirror load

Table 6.1: Simulated contributions of transistors in XIDer's front-end amplifier to the total output voltage noise $v^2_{n,out}$ (eq. 6.36). The presented numbers are taken from the most recent design iterations of both the coarse and fine stages. Contributions only include thermal noise.

more of this white noise. As a result, high-bandwidth circuits suffer from worse noise performance. This conclusion plays an important role in optimising the amplifier for XIDer's requirements and will be used throughout this section.

For the sake of brevity, this section does not provide a complete execution of the procedure presented above. Instead, the dependencies of the input referred spectral noise density $d\langle v^2_{n,in}\rangle/df$ are motivated and used for conclusions on how to minimize the CSA's noise. Since the noise contribution of each individual transistor is uncorrelated with the others, one can add up all of their individual squared spectral densities. With equation 6.31, 6.32 and 6.33, a single transistor contributes with

$$\frac{d\langle v^2_{n,in,i}\rangle}{df} = k_B T \frac{g_{mi}}{g^2_{m1}}. \tag{6.37}$$

Adding up all of the contributions leads to

$$\frac{d\langle v^2_{n,in}\rangle}{df} \propto \left(\frac{2}{g_{m1}} + \frac{2g_{m3}}{g^2_{m1}} + \frac{g_{m5}}{g^2_{m1}} + \frac{2g_{m6}}{g^2_{m1}} + \frac{2g_{m8}}{g^2_{m1}}\right). \tag{6.38}$$

As can be seen in this equation, the noise is dominated by the transconductance g_{m1} of the differential input pair. The larger g_{m1}, the lower the noise. Also, the transconductances of every other transistor should be minimized against that of the differential input pair such that their contributions can be neglected. However, one has to be careful to not deteriorate the circuit's performance with regard to other design constraints like the bandwidth or the gain. As a sanity check, in the most recent coarse stage iteration, the calculated spectral density of the squared input referred noise is given as $\approx 300\,\mathrm{aV^2\,Hz^{-1}}$. A comparison to the simulated value of $\approx 170\,\mathrm{aV^2\,Hz^{-1}}$ shows good agreement in the same order of magnitude with a deviation by a factor of ≈ 1.8.

With an analog noise simulation, it is possible to verify whether the differential input pair actually dominates the circuit's noise contribution as desired. Designers can extract a list of contributions of each individual transistor to the design's total noise. Table 6.1 shows a such a contribution list for the finally optimised design of the coarse and fine

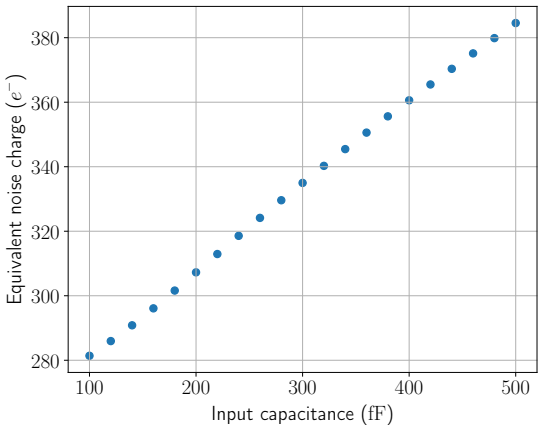


Figure 6.19: Equivalent noise charge (ENC) in units of electrons for XIDer's coarse stage vs. its input capacitance C_{det}. The ENC refers the CSA's output voltage noise $v_{n,out}$ to an equivalent input charge by multiplying $v_{n,out}$ with the charge-to-voltage gain factor C_f.

stages. Here M_1 and M_2 are the differential input pair. While they both contribute significantly with about 20 % of the total noise each, the contribution of the leg current source transistors, i.e. M_3 and M_4, can not be neglected. This is due to a tradeoff that had to be made with the dynamic output voltage range. In order to reduce the saturation voltage of M_3 and M_4 such that the output voltage can reach low enough values, their widths had to be increased. In turn, their transconductance is increased which causes them to contribute more thermal noise. The other listed transistors exhibit negligible contributions.

In addition to the motivation above, there is another important dependence of the ENC on the input capacitor of the CSA. As stated in [41], ENC $\propto C_{det}$ which means that the size of the detector capacitance plays an important role in the CSA's noise performance. For XIDer's design, figure 6.19 shows a simulation of the total integrated noise vs. different detector capacitor sizes. The plot demonstrates the expected linear proportionality. As mentioned at the beginning of this section, the design constraints ask for an ENC of roughly 375 e^- or less with a connected sensor pixel. Subsequently, even for a very high input capacitor of 500 fF, the simulated coarse stage of the CSA meets this requirement.

6.2.1.6 Summary of the CSA Performance Optimisation

The discussions provide a wide overview on the complicated nature of the CSA optimisation process. The main difficulty lies in the interweavement and the conflicting dependence of the dc gain, bandwidth and noise on the different device parameters. Even with all the equations and dependencies in mind, finding an actual optimum that achieves the desired performance constraints is far from trivial. Elaborate analog ac and transient simulations are necessary. The following list briefly summarizes the most important dependencies and tradeoffs that have to be made for this CSA architecture:

- **DC Gain:** For XIDer, the DC gain has a smaller priority compared to bandwidth and noise. Still, a high DC gain is needed for a well-defined virtual ground to achieve the highest possible charge-to-voltage gain. A value of a few 100 is desirable. Increasing the gain is achieved by a large g_{m1} of the differential input pair as well as a large output resistance r_{out}. In terms of transistor device parameters, a large g_{m1} is reached with a large W_1/L_1 and a large r_{out} can be obtained with long current source transistors. In terms of biassing currents, a high gain is achieved by a high tail current I_T as well as a small difference of I_L and $I_T/2$.

- **Bandwidth:** This is by far the most important quantity for XIDer's readout ASIC and should have the highest priority in its optimization process. The CSA needs a large bandwidth to keep up with high pump frequencies of the charge pump in order to reach a high dynamic photon counting rate. As a design goal, the first and second stage should be able to keep up with pump rates of 200 MHz and 100 MHz, respectively. A high bandwidth needs a large g_{m1} and g_{m8}. In conflict with the gain, it also requires a small output resistance. Biassing-wise, the bandwidth is maximized by maximizing the difference of I_L and $I_T/2$. At the same time, providing the amplifier with a higher overall current[10] also leads to a larger bandwidth. Last but not least, the amplifier's output capacitance should be chosen low. A small input capacitance helps as well but it deteriorates the CSA's stability.

- **Noise:** A good noise performance is necessary to reach a satisfying signal-to-noise ratio. The best way to achieve this is by increasing g_{m1} of the differential input pair, while decreasing the transconductance of every other transistor involved. A small difference of I_L and $I_T/2$ also results in low noise but this is mostly due to the fact that it limits the CSA's bandwidth tremendously. In addition, the noise increases with C_{det}. As a result, the CSA's input capacitance should be as small as possible. An increased overall current consumption also leads to a decreased spectral density (see equation) due to the increased g_{m1}. But the higher currents result in a larger bandwidth which deteriorates the noise performance. Subsequently, providing the CSA with more power does not necessarily lead to an improved noise performance.

Trading off bandwidth and noise while keeping the circuit's power consumption in mind is the most difficult in this context. While this circuit has to be optimized for high speed, a larger bandwidth intrinsically causes more noise. This is due to the fact that the thermal noise spectrum of transistors is given by a constant value (white noise). Thus, a larger bandwidth results in integrating more noise.

With the correct transistor parameter choices, this tradeoff boils down to the choice of the bias currents. While the choice of I_L dictates the total power available to the circuit via equation 6.18, the difference of I_L and $I_T/2$ trades bandwidth vs. noise performance. Thus, the optimisation strategy is to

1. pin the amplifier's power consumption with I_L to reach the desired bandwidth.

2. Minimize the transistor thermal noise with a wide and short input pair as well as narrow and long current sources and mirrors.

3. Cut into the amplifier's bandwidth by decreasing $I_L - I_T/2$ if the noise acquired in step 2 is too high.

4. Increase the power via I_L to cope with the lost bandwidth in step 3.

This cycle needs to be repeated until the desired performance is met.

As a summary, the circuit's power consumption is ultimately dictated by the required bandwidth and noise performance. In order to improve either while keeping the other constant, the amplifier needs more power. At the same time, one can trade bandwidth vs. noise, while keeping the power consumption fixed.

[10]This means increasing both I_L and I_T at the same time

	Open-loop gain Absolute	Bandwidth f_{bw} MHz	ENC e^-	Dynamic output range V	Power µW
Simulated	450	230	385	0.3 to 1	90
Constraint	$\gg 1$	> 200	$\lesssim 375$	0.4 to 0.8	–

Table 6.2: Simulated performance parameters of the CSA in the coarse stage of the analog front-end at $C_f = 50\,\text{fF}$, $C_{out} = 15\,\text{fF}$ and $C_{det} = 500\,\text{fF}$. The bandwidth is given as the absolute value of $s_{fb,amp}$ in the closed-loop state.

	Open-loop gain Absolute	Bandwidth MHz	ENC e^-	Dynamic output range V	Power µW
Simulated	500	120	370	0.3 to 0.8	30
Constraint	$\gg 1$	> 100	< 1000[12]	0.4 to 0.8	–

Table 6.3: Simulated performance parameters of the CSA in the fine stage of the analog front-end at $C_f = 50\,\text{fF}$, $C_{out} = 15\,\text{fF}$ and $C_{det} = 400\,\text{fF}$. The bandwidth is given as the absolute value of $s_{fb,amp}$ in the closed-loop state.

6.2.1.7 Performance of the Most Recent CSA (T6)

Table 6.2 lists all the parameters discussed above for the first stage in XIDer's front-end channel. All the provided values were extracted from a full-blown analog simulation. The table also presents a comparison with performance constraints as defined by the project specifications. For the definition of the amplifier's bandwidth, the position of $s_{fb,amp+/-}$ in Hz has been chosen:

$$f_{bw} = \frac{|s_{fb,amp}|}{2\pi}. \tag{6.39}$$

This is due to the fact that it has proven to be a reliable measure in transient simulations where the circuit has been stimulated with a step input current. As it turns out, $1/f_{bw}$ roughly provides the time it takes the CSA to drive its output voltage through 90 % of the transition $\Delta V_{out} = Q_{in}/C_f$.[11]

As stated in section 6.1.1, XIDer's front-end features two stages. While the first/coarse stage is supposed to provide a large dynamic photon counting range and run at higher pump frequencies, the second/fine stage's timing constraints are relaxed. In addition, the charge gain from the coarse to the fine stage also relaxes the fine stage's noise constraint significantly. Subsequently, it can be designed with a focus on reduced power consumption. The corresponding performance parameters are listed in table 6.3. Here, the chosen input capacitor $C_{det} = 400\,\text{fF}$ represents the transfer capacitance C_{trans} in between the stages which is permanently connected to the input of the fine stage.

As presented in the provided tables, both stages meet the specified design parameters in simulation. Section 6.5 demonstrates their performance in simulations with the fully

[11] This includes the settling time, if the circuit is in an unstable condition, e.g. if C_{det} is small compared to C_f.

[12] Due to the gain in the coarse-to-fine transfer, the constraint on the fine stage's noise contribution is relaxed. The value of 1000 is a rather loose requirement which ensures that the fine stage noise remains negligible to that of the amplified coarse stage contribution for a charge transfer gain of 8.

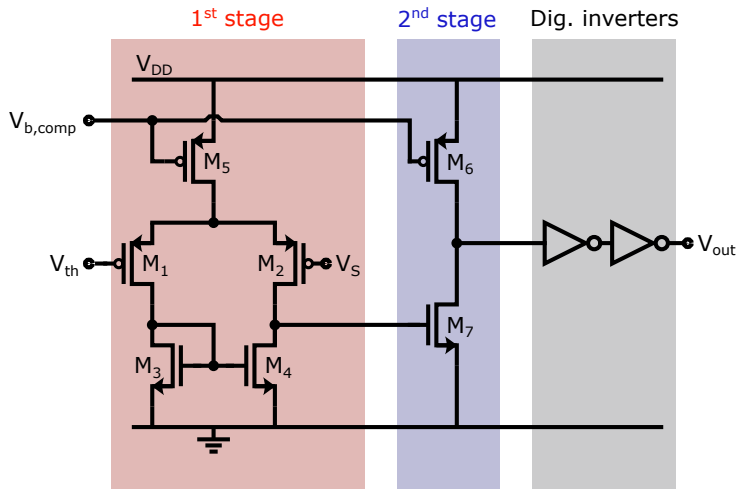


Figure 6.20: Circuit diagram of the comparator's basic structure used in the front-end of XIDer's readout ASIC. V_S is the input voltage that is compared to the threshold voltage V_{th}. The bias voltage $V_{b,comp}$ controls the current flowing through both stages of the comparator. Both V_{th} and $V_{b,comp}$ are provided by an on-chip DAC as described in section 6.3.1.

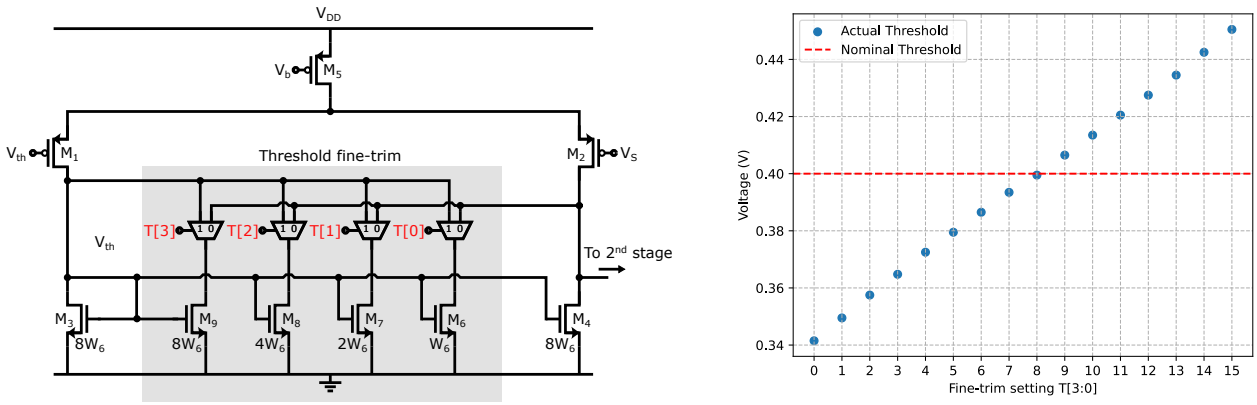
assembled front-end design.

6.2.2 Comparator

A circuit diagram of the basic comparator structure is shown in figure 6.20. It features a two-stage amplifier in which the first stage is implemented as a differential amplifier with active current mirror loading. The second stage in form of a common-source amplifier provides extra gain. At the output of the comparator, there are two digital inverters that produce fast rail-to-rail rising and falling edges.

An important part of the comparator design is to ensure the matching of the differential transistors M_1 and M_2 as well as M_3 and M_4. Differences in their properties introduce asymmetries to the circuit which lead to a deviation of the circuit's effective threshold voltage from the nominal bias V_{th}. While systematic sources of mismatch can be minimized by a careful layout design, random mismatches can rise from manufacturing uncertainties. The easiest way to reduce the impact of these random fluctuations is by choosing transistors with large feature sizes. However, large components consume extra space on the silicon die and exhibit large parasitic capacitances which negatively impact the circuit's bandwidth and thus speed. This is not only true for the circuit itself, but also for the CSA which has its output connected to the input of the comparator. Subsequently, there is a tradeoff to make between parasitic capacitances, i.e. speed of the comparator and the CSA, available space and size of the statistical variation of the comparator threshold voltage.

Even with all of the precautions, the random manufacturing uncertainties can never be fully eliminated. In order to cope with this, fine-trim circuits are introduced to counter their effects for each channel individually. T6, the most recent ASIC iteration, uses a fine-trim add-on in the first stage of the comparator as shown in figure 6.21a. It introduces a deliberate, tunable asymmetry in the active current mirror load of the comparator's differential stage where the four control bits T[3:0] dictate the mirror ratio. This is implemented via an array of multiplexers which control the connection of the transistors M_6 to M_9. Each of the control bits distributes its corresponding transistor to either side



(a) Circuit diagram of the first stage of XIDer's comparator with an included threshold fine-trim capability.

(b) Simulated fine-trim sweep. The red line symbolizes the nominal threshold voltage of $V_{th} = 400\,\mathrm{mV}$.

Figure 6.21: Comparator fine-trim add-on in the T6 ASIC.

of the differential design. In this way, the LSB T[0] is responsible for the LSB transistor M_6, while the MSB T[3] controls the MSB transistor M_9. All of the transistors have the same length as M_3 and M_4 but their widths are dimensioned in multiples of the smallest, i.e. M_6. A desired binary encoding of the fine-trim bits T[3:0] then dictates that the width of M_6 to M_9 has to increase in a binary fashion such that $W_9 = 8W_6$. Each channel is provided with its individual set of control bits, such that statistical threshold voltage variations can be mitigated on a channel-to-channel basis.

The resulting simulated trim of the effective threshold voltage is plotted in figure 6.21b. In this simulation, the nominal value V_{th} was fixed at a constant value. As demonstrated, the trimming addition shows a linear behaviour throughout the setting range. In the implemented design, the step per trim bit has the size of $\approx 7\,\mathrm{mV}$ with a total trimming range of $\approx 110\,\mathrm{mV}$ around the nominal threshold value. While Monte Carlo simulations including the manufacturing uncertainties hint at the fact that this provided tuning range and granularity are sufficient, future measurements with T6 are expected to provide more insight.

Power Consumption & Timing

At a power consumption of $30\,\mu\mathrm{W}$, the comparator achieves a simulated switching delay of less than 2 ns if $|V_S - V_{th}| > 50\,\mathrm{mV}$. This delay measures the time difference between the moment at which the input signal crosses the threshold and the corresponding rising or falling edge in comparator's output voltage. The simulated rise and fall times are in the order of roughly 300 ps. With this speed, the comparator meets the requirement to indicate a threshold crossing of the CSA's output voltage in much shorter time than the minimum charge pump period of 5 ns. The corresponding simulation includes a parasitic output capacitance of roughly 15 fF which is a worst-case estimation from a parasitic capacitor extraction of the final analog layout design as presented in section 6.1.4. Also, the simulations have been performed with the slowest available process corner.

A common approach to save power is to use a pulsed comparator operation where the circuit is only activated when it is needed. In XIDer's front-end, however, the active time of the comparator is highly dependent on the input charge and the time it takes the charge pump to perform the continuous conversion. In addition, at the beginning of each (sub)frame, every channel would have to turn on its comparator which leads to sudden

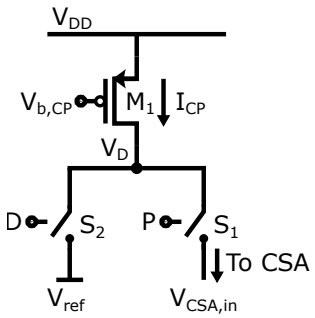


Figure 6.22: Circuit diagram of the charge pump's basic structure.

voltage drops on the supply voltage due to sudden increased current consumption. For these reasons, a permanent operation has been chosen.

6.2.3 Charge Pump & CP Logic

The basic charge pump architecture in the front-end of XIDer's readout ASIC is implemented by the circuit depicted in figure 6.22. It uses a simple current source transistor M_1 which is biassed via an on-chip DAC with the voltage $V_{b,CP}$ to provide the current I_{CP}. With the switch S_1, this current source can be connected to the input of the stage. Doing so for a well-defined time interval T_{CP} injects a charge package with the size

$$Q_{CP} = I_{CP} T_{CP} \tag{6.40}$$

into the CSA input node. The second switch S_2 is needed to dump the current into a fixed reference potential V_{ref} as long as the charge pump is inactive.[13] There are two main reasons for this:

S_2 allows the charge pump to follow the design philosophy in which the ASIC should have a constant power consumption. When I_{CP} is not needed to generate a charge package, S_2 ensures that the charge pump still draws the same amount of current. Subsequently, current spikes and sudden local voltage drops on the supply voltage are prevented. At the same time, the current source transistor is held in the same operating state throughout the charge pump operation. Instead of being turned on only when a charge package should be generated, M_1 keeps conducting the same current even if the charge pump is inactive. Due to this, parasitic transient effects from turning M_1 off and on which could cause errors and uncertainties in the charge package size are eliminated.

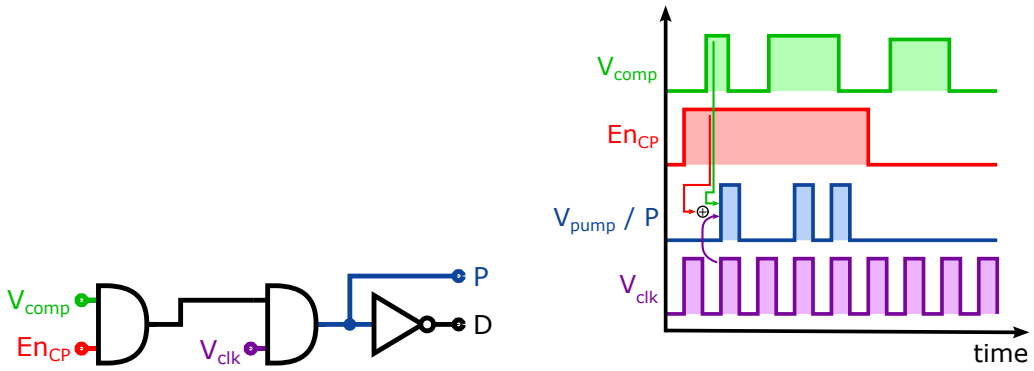
Resulting from this architecture, the charge pump has two possible states:

- **PUMP:** I_{CP} flows into the CSA input. S_1 is closed and S_2 is open.
- **DUMP:** I_{CP} is dumped into the reference potential. S_1 is open and S_2 is closed.

There is no operation mode in which both S_1 and S_2 are both open or closed. Consequently, in the simplest implementation, the corresponding control signals P and D for S_1 and S_2 are inverted versions of the same signal.

The P and D control signals are generated by the charge pump logic block. A simplified version of the charge pump logic as well as the corresponding sequence of input and output signals is illustrated in the figures 6.23a and 6.23b. In reference to figure 6.2, P is also denoted as V_{pump} in the displayed sequence. A logic AND combination of the sequencer

[13] V_{ref} is the same reference potential used by the CSA.



(a) Simplified schematics (b) Sequence of involved signals

Figure 6.23: Charge pump logic

track En_{CP}[14] with the comparator output V_{comp} dictates, whether the charge pump can enter its PUMP state. While V_{comp} displays, whether the charge integrated by the CSA exceeds the defined threshold value, the idea of En_{CP} is to give the user control over the enable of the charge pump in a dynamic fashion. With it, one can define time intervals in the front-end's integration window, in which the charge pump can be turned off, if desired.

If En_{CP} and V_{comp} are enabled, the V_{clk} sequencer track represents the clocked time reference for the charge packages. Depending on whether $V_{clk} = 1.2\,\mathrm{V}$ or $0\,\mathrm{V}$, the charge pump is in its PUMP or DUMP state, respectively. In this way, the charge package definition of equation 6.40 is then given as

$$Q_{CP} = I_{CP} T_{clk} \tag{6.41}$$

in which T_{clk} is the time interval in which V_{clk} is active. For a duty cycle of 50 %, T_{clk} is given by half a period of V_{clk}. The actual implementation of the logic block includes a few extra safety measures to ensure clean switching with well-defined timings.

In theory, the inherent strength of this charge pump architecture is its insensitivity to its output voltage. In reality, however, this strength is deteriorated by two parasitic effects:

- **Early Effect:** The finite output resistance of M_1 causes I_{CP} to depend on either V_{ref} or $V_{CSA,in}$, depending on the state the charge pump is in.
- **Charge Injection:** Parasitic capacitances at the drain contact of M_1 cause an injection of additional charge between the PUMP and DUMP states depending on the difference of V_{ref} and $V_{CSA,in}$.

In order to mitigate these effects, the node V_D has to be cascoded. Instead of introducing more transistors and an additional cascode bias voltage to the circuit, XIDer's charge pump hides the cascode in the switches S_1 and S_2. Both these switches are implemented via p-MOSFET transistors which are operated in saturation region. Due to this, they keep V_D constant which both counteracts the early effect of M_1 and hides parasitic capacitances. As a result, this design has a high insensitivity to its output voltage, i.e. the input voltage of the CSA. This is demonstrated in the linearity measurement presented in section 7.2.2.

An importand side note: in an initial intuitive guess, one would assume that both the early effect and the charge injection should not play a role, because the CSA should ensure that $V_{CSA,in} = V_{ref}$ at all times. As discussed in section 6.5.2, however, the CSAs in

[14]Table 6.4 in section 6.3.3.1 lists all of the sequencer signals

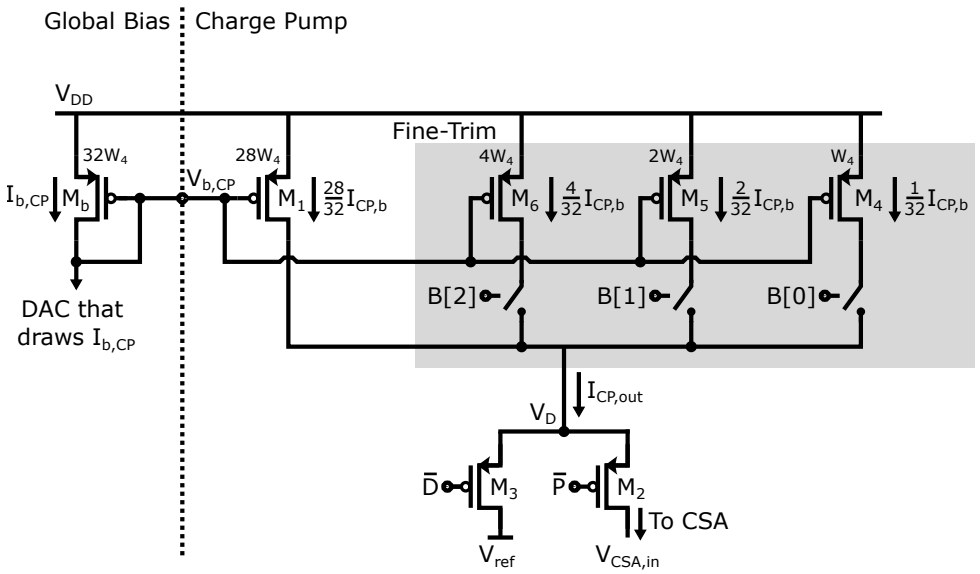


Figure 6.24: Charge pump circuit diagram with fine-trim functionality to fine-tune the charge pump output current channel-wise.

XIDer's front-end are often faced with big enough charges to drive their output voltage to the upper supply voltage. In this case, the CSA feedback loop is broken and the amplifier's input voltage $V_{CSA,in}$ starts moving with additional charge. With enough time, the charge pump can remove sufficient charge from the feedback capacitor to restore the CSA's feedback. But only if the charge package size is independent of the CSA input voltage, the correct amount of input charge can be reconstructed in this process. This remarkable property of XIDer's front-end allows it to handle large bursts of charge, while employing small feedback capacitors for a large charge-to-voltage gain.

Fine-Trim

All of the instantiated channels on XIDer's readout ASIC are provided with the same bias voltages $V_{b,CP0}$ and $V_{b,CP1}$ for the coarse and fine stage charge pumps, respectively. With perfect components, this would result in equal bias currents $I_{CP0/1}$ in every channel of the chip. In reality, however, manufacturing uncertainties can cause these currents to vary slightly. On top, the ASIC-wide distribution of the sequencer track V_{clk} is affected by parasitic resistances and capacitors associated with the corresponding wiring. These parasitics can also cause channel-wise differences in the size and timing of T_{clk}. As a result, charge package sizes are expected to vary from channel to channel even if every channel is provided with the same $V_{b,CP0/1}$ and sequencer track V_{clk}. In order to mitigate these variations, XIDer's charge pump has been equipped with a charge package fine-trim in its latest design iteration (SUS65T6, see 6.6). The most recent circuit diagram including both the cascode switches as well as the fine-trim feature is illustrated in figure 6.24. It also shows the generation of the bias voltage $V_{b,CP}$ via the global bias diode transistor M_b. The bias current $I_{b,CP}$ is generated by a global on-chip DAC.

As demonstrated, the fine-trim is implemented via an array of current source transistors in parallel to M_1. Each of these additional transistors is controlled by one of the bits of B[2:0]. Just as for the comparator threshold fine-trim, the transistors are dimensioned such that they have equal lengths but their widths increase with a power of two for each bit. Subsequently, the LSB transistor M_4 has the smallest width of W_4, while the MSB transistor M_6 is the widest with $W_6 = 4W_4$.

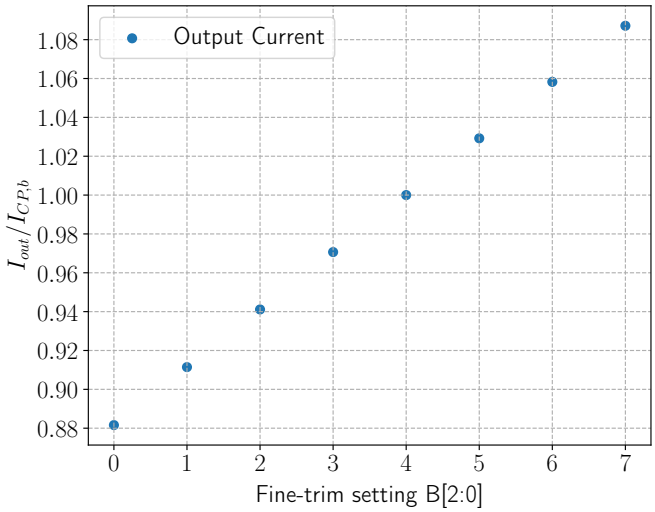


Figure 6.25: Simulated fine-trim sweep of the charge pump's output current I_{out} in relation to the nominal, global bias current $I_{b,CP}$.

Independent of the setting of B[2:0], the base current source M_1 is always conducting the current I_{D1}. Without any uncertainties, the transistors are dimensioned such that

$$I_{D1} = \frac{28}{32} I_{CP}. \tag{6.42}$$

in which I_{CP} is the nominal bias current. Subsequently, the output current for B[2:0] $= 0$ is given by

$$I_{CP,out,0} = I_{D1} = \frac{28}{32} I_{b,CP}. \tag{6.43}$$

A more general formula for the theoretical output current is given by

$$I_{CP,out} = \frac{28}{32} I_{b,CP} + B \cdot \frac{1}{32} I_{b,CP} \tag{6.44}$$

in which B is the decimal representation of the value of B[2:0]. Subsequently, at a setting of B[2:0] $= 4$, the output current matches $I_{b,CP}$.

Figure 6.25 shows a simulation of $I_{CP,out}$'s size for different fine-trim settings in relation to the global, nominal bias current $I_{b,CP}$. With a linear characteristic, the current can be tuned in a range of roughly $0.88 \cdot I_{b,CP}$ to $1.1 \cdot I_{b,CP}$. The simulated step size is given as $\approx 3\,\%$ of $I_{b,CP}$ with a total of eight available steps.

Due to an oversight in the bias voltage distribution across several channels, lab-tested chip iterations can hardly provide insight into the actual channel-to-channel charge package variation in the lab. And since the channel-to-channel variation in terms of T_{clk} is difficult to predict in simulation, it is tough to make an actual, reliable prediction. As a result, the proposed circuit is meant as a first step towards fine-trimmable charge packages. Actual lab measurements with the latest chip iteration SUS65T6 will be necessary to verify the needed tuning range and granularity.

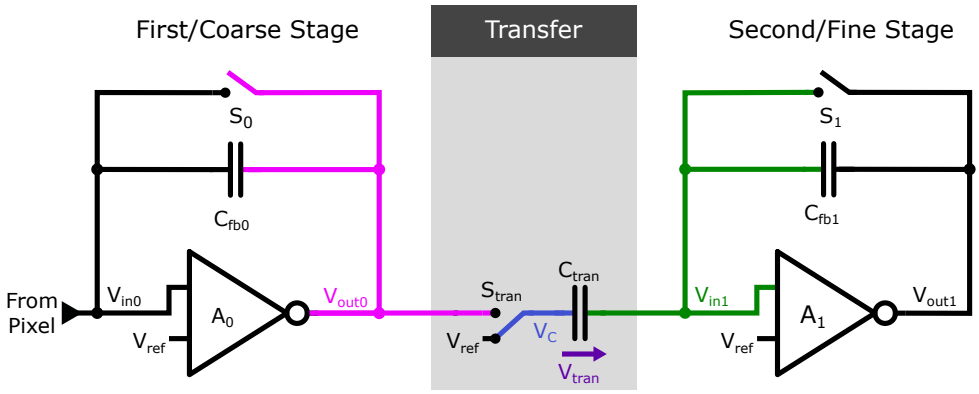


Figure 6.26: Circuit diagram of the most important components involved in the charge transfer from the coarse to the fine stage. The signal color coding matches with that in figure 6.27 where the corresponding signal sequences are presented.

Possible Charge Pump Design Alternatives

There are several different options for the implementation of the charge pump. Instead of using the pulsed operation, one could also leave the charge pump current flow as long as the comparator is active. In this approach, one would have to measure the time the charge pump needs to reduce the integrated charge below the threshold voltage and reconstruct the total integrated charge from this time interval. However, this raises the need for a circuit like a time-to-digital converter that actually measures the time. In addition, the reconstruction of the charge package size is more complicated than with the chosen architecture. Thus, while this approach might look simpler at first sight, its implementation entails a more complicated design.

Furthermore, one could use a switched capacitor circuit for the charge pump. Such a charge pump would also generate well-defined charge packages with a tunable size. But it has the disadvantage that the package size largely depends on the circuit's output voltage. In XIDer's design, the charge pump output node is the input of the corresponding CSA stage. As explained in section 6.5.2, this input node is expected to go through substantial voltage changes in extremal operation modes. In these cases, a switched capacitor charge pump would generate charge packages with varying size. For these reasons, the architecture explained above has been chosen for the charge pump of XIDer's readout ASIC.

6.2.4 Coarse-to-Fine Charge Transfer

At the end of each (sub)frame, the coarse stage is expected to still have a *residual* charge Q_{end} left on its feedback capacitor. This is due to the fact that its charge package and comparator threshold are tuned to handle high photon rates. Subsequently, depending on the settings and calibration, it is usually blind to charges that correspond to only a few photons. In order to still achieve high resolution, the residual charge has to be transferred to the fine stage which exhibits smaller charge packages and comparator thresholds. This is usually the last step performed by the front-end before the charge integration for a new (sub)frame is initiated.

Figure 6.26 shows the important parts of the front-end for the execution of this transfer. While most of the front-end compartments are involved, the transfer capacitor C_{tran} and its control switch S_{tran} form the central components. Throughout the coarse stage's continuous conversion, S_{tran} connects the left side of C_{tran} to a buffered version of the

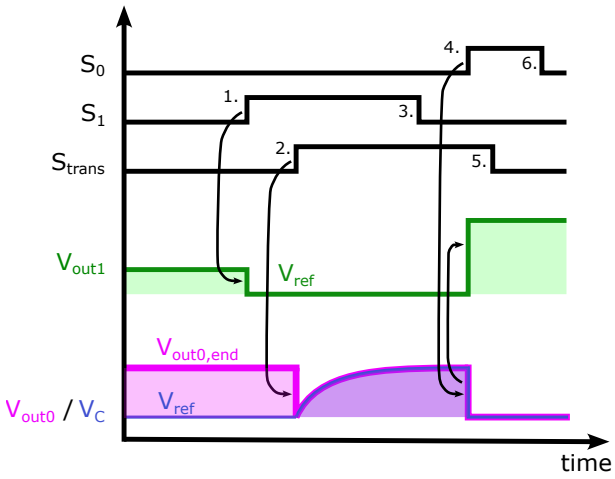


Figure 6.27: Signal sequence for the charge transfer from the coarse to the fine stage.

reference potential V_{ref}. Only after the coarse stage's conversion is complete, the transfer is initiated which can be subdivided into the steps illustrated in figure 6.27:

1. **Fine stage reset:** Resetting the fine stage via closing S_1 causes C_{tran} to be fully discharged due to the defined potential of V_{ref} on both sides.

2. **Charging the transfer capacitor:** While S_1 remains closed, S_{tran} connects the left side of the transfer capacitor to the output of the coarse stage. As a result, the coarse stage begins to charge C_{tran} from $V_{tran} = 0\,\mathrm{V}$ up to $V_{tran} = V_{out0,end}$. In this context, $V_{out0,end}$ is the voltage that corresponds to the residual charge.

3. **Stop the fine stage reset:** As soon as the capacitor is charged, S_1 is opened to stop the reset of the fine stage. Subsequently, the fine stage is ready and sensitive and ready for the charge transfer.

4. **Injection into the fine stage:** By resetting the coarse stage via closing S_0, its output voltage steps back to V_{ref}. Subsequently, the left-hand-side node of C_{tran} experiences a sudden voltage step of $V_{out0,end} - V_{ref}$. This step results in a charge injection through C_{tran} into the fine stage.

5. **Disconnect transfer capacitor:** S_{tran} disconnects the left side of C_{tran} from the coarse stage output and reconnects it to V_{ref}.

6. **Start the next (sub)frame:** After completing the charge transfer, S_0 is opened to stop the reset of the coarse stage priming it for the next (sub)frame.

All of the involved dynamic signals to control S_0, S_1 and S_{tran} are generated by the on-chip sequencer and are globally shared by all the channels. In reference to table 6.4 in section 6.3.3.1, the corresponding signals are called Res0, Res1 and Sw0to1, respectively.

An important feature of this transfer process is that, alongside passing the residual charge Q_{end} from the coarse to the fine stage, it also exhibits an intrinsic charge gain A_C. This means that the charge Q_{tran} that is injected into the fine stage is actually given via

$$Q_{tran} = A_C Q_{end}. \tag{6.45}$$

Instead of the original residual charge $Q_{end} = (V_{out0,end} - V_{ref})C_{fb0}$ on the coarse stage's feedback capacitor, the transfer capacitor holds a charge of $Q_{tran} = (V_{out0,end} - V_{ref})C_{tran}$

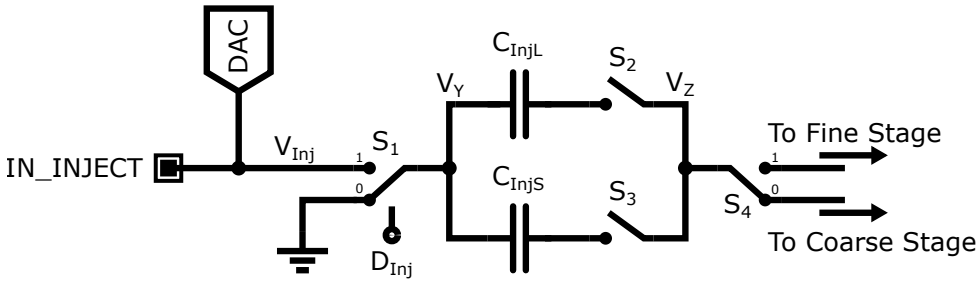


Figure 6.28: Circuit diagram of the on-chip test charge injection circuit. Each channel features two of these circuits to allow for more flexibility.

at the end of step 2. Subsequently, the transfer gain is given via

$$A_C = \frac{Q_{tran}}{Q_{end}} = \frac{C_{tran}}{C_{fb0}}. \tag{6.46}$$

This gain can be exploited to relax several constraints on the fine stage. Most importantly, the increased charge causes larger voltages at the output of the fine stage. As a result, the required resolution of the fine stage comparator is reduced. At the same time, with the right choice of A_C the noise contribution of the fine stage can be neglected to that of the coarse stage. This is due to the fact that its signal-to-noise ratio is increased by the factor A_C compared to the coarse stage. Subsequently, the fine stage can be optimised for less power consumption.

The flip-side of a large A_C, however, is that C_{tran} has to be chosen large. And since C_{tran} adds to the output capacitance of the coarse stage, a large C_{tran} degrades the CSA's bandwidth in step 2. Subsequently, the larger C_{tran}, the longer its charging and hence the whole charge transfer process take to complete. This, in turn, limits the minimum (sub)frame length which this front-end can operate at. However, as described in section 6.5.4 and 7.2.4, this problem is only of concern for the most ambitiuous 16-bunch mode at the ESRF. In this mode, the charge transfer of current ASIC iterations takes up a substantial portion of the (sub)frame length which is why it remains an open question to solve. A possible fix would be to decrease the size of C_{tran}. While this shortens the transfer time, it also decreases the gain A_C and thus tightens the constraints on the fine stage. In order to find a reasonable tradeoff, this topic is currently under investigation.

6.2.5 Test-Signal Injection Circuit

For debugging and calibration purposes, each front-end contains a test charge injection circuit as displayed in figure 6.28. The circuit consists of two capacitors with different sizes to cover a large range of possible input charges. Via slow control, the user can control the switches S_2 and S_3 to choose which one of the capacitors should be used for injection. Besides choosing either 20 fF or 160 fF, one could also use both capacitors to have a total capacitance of 180 fF. At the circuit's output, the switch S_4 allows to choose between injecting the charge into the coarse or fine stage.

The dynamically controlled switch S_1 executes the necessary steps to perform the charge injection. It is controlled via a sequencer track D_{Inj}[15] which is shared globally by all the channels. While the connected front-end stage is in reset to keep V_Z at a defined level, connecting V_Y and V_{Inj} via S_1 charges the chosen injection capacitor C_{Inj}. After releasing

[15] InjB0/1 in table 6.4 in section 6.3.3.1.

the front-end stage from its reset, S_1 can inject the charge into the front-end stage by shorting V_Y to the ground potential. Due to the sudden voltage step of V_Y a charge of the size

$$Q_{Inj} = C_{Inj}(V_{Inj} - V_{gnd}) = C_{Inj}V_{Inj} \tag{6.47}$$

enters the front-end stage through C_{Inj}. The actual size of V_{Inj} can be chosen either via slow-control with an on-chip DAC or with an externally applied input voltage through the I/O-Pad IN_INJECT. In this way, the choice of V_{Inj} as well as the size of the injection capacitor provides direct control over the size of the injected charge.

Due to the fact that injection capacitors can only be charged while the connected front-end stage is being reset, a single charge injection circuit can only inject once for every performed stage reset. In order to provide more flexibility, each front-end is actually equipped with two identical instances of this charge injection circuit. This allows for two injections per (sub)frame instead of only one.

6.2.6 Merger: Digital Data Pre-Processing Unit

Since it operates on digital values, the merger is a semi-custom design and synthesized from Verilog source code. The merger module combines the values of the coarse and fine counters by adding them. There are several tunable options which define the combination procedure. Instead of being dynamically controlled, these options are set via slow control registers. This is due to the fact that they are of a more general and basic nature and are most likely defined once for a set of measurements. The list below provides an overview of the available functions on the most recent ASIC iteration, based on the contents of [73]:

- **Coarse-to-fine charge gain:** Defines a multiplication factor of the coarse stage's counter value before adding it to the fine stage's counter value. This value should match the charge package ratio of the two stages Q_{CP0}/Q_{CP1}.
- **Bit shift:** Shifts the combined result by 0,1 or 2 bits two the right. This setting allows limiting the final result's dynamic range to sacrifice resolution for higher frame rates.
- **Limit:** Sets an upper limit for the combined result which is another way to decrease the dynamic range for higher frame rates.
- **LSB correction:** Adds a small value of 1,2 or 3 on the final combined result which can be used for rounding.
- **Clear on read:** Clears the contents stored at a RAM address after reading its contents[16].

These options are globally shared by all of the channels on the ASIC. With the probability to change the multiplication factor of the coarse stage charge pump count, users can adjust the charge package ratio between the stages while operating the ASIC. An example use-case would be a measurement that requires higher photon count rates. Instead of sticking to the ESRF-like 8 photons per pump in the first stage, 16 photons might be more useful to keep up with the high input current. While adjusting the size of Q_{CP0} in the coarse stage, one can also set the merger's coarse stage multiplication factor to 16 instead of 8. Except for "Clear on read", the other options allow trading the frame and data rate for another quantity of choice.

[16]The read RAM address is provided by the telegram interface on a (sub)frame-level (see section 6.3.3.2)

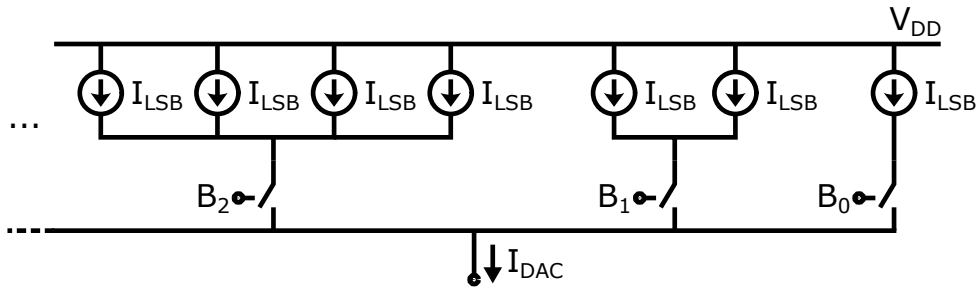


Figure 6.29: Schematic drawing of a current digital-to-analog converter used for the bias generation on XIDer's readout ASIC.

6.2.7 Custom-Made RAM

Depending on the ASIC iteration, the RAM storage in each channel features 192 or 256 addresses for 16-bit words where individual bit cells use standard 6T SRAM bit cells provided by the foundry.[17] For an increased flexibility in the data storage and readout modes (see section 6.3.3.2), the low and high bytes of the 16-bit word at each address can be accessed individually. In order to implement this option, the storage is composed of two parallel RAM matrices with 8-bit words. Both matrices are accessed with the same address but with different write and read enables. In this way, each matrix implements the low and high byte storage, respectively.

Due to only a few read and write accesses per (sub)frame, the timing constraints for these processes are rather lenient. For this reason, the access logic implementation can choose a strong focus on low power consumption instead of speed. Subsequently, it is implemented in a custom-made design which omits any circuitry that usually increases the access speed as for example sense amplifiers. The power saving potential of this approach is currently under investigation.

6.3 Global Components

For the configuration, operation and readout of the individual channels, XIDer's readout ASIC includes several global modules which are instantiated once. The following subsections provide a detailed insight into their design. Except for the bias generation circuits, all of the modules presented here have been designed and synthesized in a semi-custom design flow on the basis of Verilog source code.

6.3.1 Front-End Bias Generation

In order to generate the bias voltages and currents for the operation of the analog front-end, the XIDer readout chip uses digital-to-analog converters (DACs). These are built as depicted in figure 6.29 where an array of parallel unit current sources is used to generate a desired output current I_{DAC}. The unit current sources are grouped in a binary fashion such that the first group consists of single source, the second consists of two sources, the third of four sources and so on. An extra switch in series to each group allows controlling

[17] An explanation of a 6T SRAM cell can e.g. be found in [81].

how many current sources contribute to I_{DAC} such that

$$I_{DAC} = \sum_{k=0}^{N} B_k 2^k I_{LSB} \tag{6.48}$$

where B_k is the digital control value for the k-th switch, N is the number groups, i.e. bits and I_{LSB} is the current generated by a unit current source. Depending on the polarity of the required bias current, i.e. whether the current has to be drawn out of or driven into the circuit, the DACs also feature a (not depicted) NMOS current mirror to switch the polarity of I_{DAC}.

The control bits B_k are configured via the slow control JTAG interface. For all of the manufactured iterations of XIDer, 10-Bit DACs have been used. With a nominal unit source current of $I_{LSB} = 250\,\text{nA}$ and a total of $2^{10} = 1024$ unit steps, the employed DACs can reach a maximum output current of 256 µA. While this granularity proves to be too fine for most of the bias signals, it serves as a good starting point for prototype tests. Investigations on the necessary tuning resolution are currently on-going.

Some front-end circuits require bias voltages rather than currents. For this purpose, the same DAC structure is used in combination with a series resistor R_{DAC} at the output. The current generated in the DAC flows through said resistor to the ground potential. As a result from Kirchhoff's law, a voltage drop V_{DAC} is generated on R_{DAC}:

$$V_{DAC} = R_{DAC} I_{DAC}. \tag{6.49}$$

With $R_{DAC} = 4\,\text{k}\Omega$, the resulting bias voltage has a nominal tuning range of 0 V to 1.024 V with a step size of 1 mV. Subsequently, the voltage DAC values can be converted to mV in a 1-to-1 fashion.

The employed DACs in current designs are used on a global level. Subsequently, all of the front-ends share the same bias currents and voltages. As explained in sections 6.2.2 and 6.2.3, the most recent chip iteration introduced fine-trim circuits for the comparator threshold and charge pump package biasses to finely tune the channel-specific biasses around the global DAC setting.

6.3.2 Slow Control

A standard Joint Test Action Group (JTAG) interface implements the readout ASIC's slow control. With its first definition in the IEEE standard 1149.1 [82], JTAG has been developed as a means of testing integrated circuits and their functionality. Due to its architecture, however, JTAG can also be used as a chip configuration interface which is its purpose in the XIDer project.

With TMS, TCK, TDI and TDO, the standard defines four mandatory I/O pins. While TCK provides a time base for the interface, the combination of TMS and TCK control the JTAG's core unit, the Test Action Port (TAP). The TAP is a state machine which allows multiplexing input and output data to and from pre-defined shift registers. These include a set of mandatory as well as optional user-defined instances. Among these is the instruction register which is the most important mandatory one. It holds the address of the register to be accessed by the TAP controller. If the the register at the provided address is supposed to be written, the desired input data is provided serially via the input data port TDI. Vice versa, data shifted out of the corresponding register is transmitted via the TDO pin.

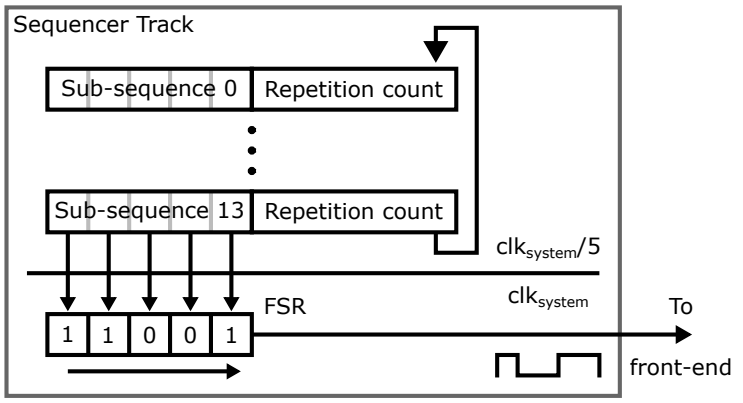


Figure 6.30: Simplified schematics of the sequencer track module. Each sequencer track provides a dynamic digital control signal which consists of a repeating bit pattern. The pattern contents are stored in a parallel shift register and serialized by the fast shift register (FSR). The tracks are globally shared by all of the ASIC channels.

XIDer's readout ASIC uses the optional JTAG registers for its slow control. Their content holds the configuration for every core module like the global sequencer or the bias front-end bias DACs. The actual on-chip interface is synthesized from Verilog source code which is provided from the research group libraries and adapted to this project. In a final detector, several ASICs could be configured in a daisy-chained operation. However, whether JTAG or other protocols like SPI or I^2C will be employed in the full-blown detector system, is not yet decided.

6.3.3 Dynamic Control

Besides the global slow control, the ASIC's channels require dynamic control signals for charge signal processing and data management. The corresponding global modules needed to generate these stimuli are discussed in the following sub-sections.

6.3.3.1 Sequencer

As described, for instance, in sections 6.1.1 and 6.2.4, the operation of the analog front-end requires precisely timed dynamic signals. For the execution as well as the adaptability of processes like the CSA stage reset or the charge transfer between the stages, the control signals need to be tunable with a fine time granularity. This task is handled by the global on-chip sequencer which is a deviation from the flexible sequencer module employed in the DSSC readout ASIC [83].

The sequencer is subdivided into *sequencer track* modules as depicted in figure 6.30 where each of the tracks is responsible for the generation of one control signal. Inside the sequencer track module, there is a loop of 14 parallel shift registers with a width of 5 bits. Each of these shift registers defines a sub-sequence and is associated with a 5-bit repetition count which defines how often a sub-sequence is repeated before the track moves on to the next. Driven by a clock with the frequency $f_{clk,system/5}$ ($= f_{clk,system}/5$, see 6.1.3), the sub-sequences' bit patterns are cycled through the parallel shift register.

In addition to the parallel shift registers, there is a fast 5-bit shift register (FSR). Its contents are serialized with the fast system clock $f_{clk,system}$[18]. At the same time, the

[18]The final design aims at a frequency of 880 MHz, see section 6.1.3.

Track Name	Function
Res0	Coarse stage reset switch (sec. 6.1.1)
Res1	Fine stage reset swtich (sec. 6.1.1)
InjB0	Dyn. switch in first test charge injection instance (sec. 6.2.5)
InjB1	Dyn. switch in second test charge injection instance (sec. 6.2.5)
EnIN	Dynamic front-end input switch (sec. 6.5)
Sw0to1	Transfer capacitor switch (sec. 6.2.4)
EnCP0	Coarse stage charge pump enable (sec. 6.2.3)
EnCP1	Fine stage charge pump enable (sec. 6.2.3)
ClkCoarseCP	Coarse stage charge pump clock (sec. 6.2.3)
ClkFineCP	Fine stage charge pump clock (sec. 6.2.3)
Ch0CoarsePump	Manual coarse charge pump control[19]
Ch0FinePump	Manual fine charge pump control

Table 6.4: Sequencer tracks on the most recent readout ASIC iteration T6 with their corresponding functions.

contents of the FSR are loaded from the parallel shift register with the frequency of $f_{clk,system/5}$. As a result, since a sub-sequence is 5 bits long, the FSR is being loaded with a new sub-sequence, whenever it finishes shifting out the current one. In this way, a sequencer track generates a train of bits which are encoded and pre-configured in the parallel shift register. As long as the sequencer is provided with an active RUN, its tracks keep cycling through the same sub-sequences over and over again. In order to achieve an even finer granularity, the sequencer features an optional DDR mode. For configuration of the generated bit patterns, each of the sequencer tracks has its own JTAG register. With 14 sub-sequences that each have 5 bit of sequence information and a 5 bit repetition count, such a JTAG register contains 140 bits.

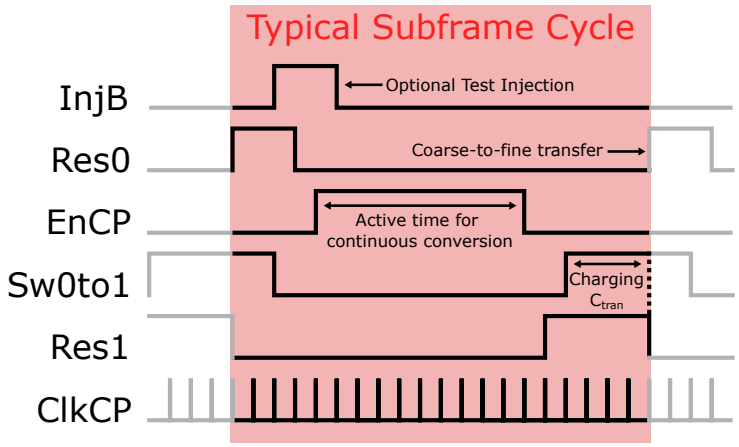


Figure 6.31: Typical signal sequence of the most important sequencer tracks.

[19] Both Ch0CoarsePump and Ch0FinePump can be chosen as a substitute for the charge pump logic output signals in the coarse and fine stages, respectively.

The latest ASIC iteration, SUS65T6 (see section 6.6) employs a total of 12 sequencer tracks which are listed in table 6.4. The tracks are globally shared by all of the channels. A typical sequence of the most important signals is drawn in figure 6.31. For the sake of brevity, ClkFineCP and ClkCoarseCP as well as EnCP0 and EnCP1 are merged into the ClkCP and EnCP, respectively. The same is true for InjB0 and InjB1 which are merged into InjB. Due to their debugging purpose, Ch0CoarsePump and Ch0FinePump are omitted in the drawing.

6.3.3.2 The Telegram Protocol

Besides the global sequencer module, XIDer's readout ASIC features another global dynamic control unit. While the sequencer provides channels with periodic control signals that run through the same sequence for each (sub)frame, the telegram module provides channels with (sub)frame-specific commands. These commands are globally shared by the channels and control the digital data flow into and out of the channels' individual RAM modules. As a result, each channel performs the very same data write and read operations. Just like the pixel-wise merger block which is used for data pre-processing and storage, the telegram module has also been designed for the purpose of output data rate reduction and adaptability to different experiments. Like section 6.2.6, the following explanations are based on the contents of [73].

Basic Telegram Protocol Structure

The telegram module is based on the custom-designed telegram protocol. Said protocol defines a sequence of characters and bits as depicted in figure 6.32 consisting of three seperate parts:

1. **SYNC:** A unique sync word indicates the beginning of a new (sub)frame. Also, it allows synchronizing the ASIC telegram module which receives instructions with the external sender module.

2. **Instruction Payload:** After the sync character, the telegram protocol contains three instruction words. Their contents define the ASIC channels' data flow for the current (sub)frame.

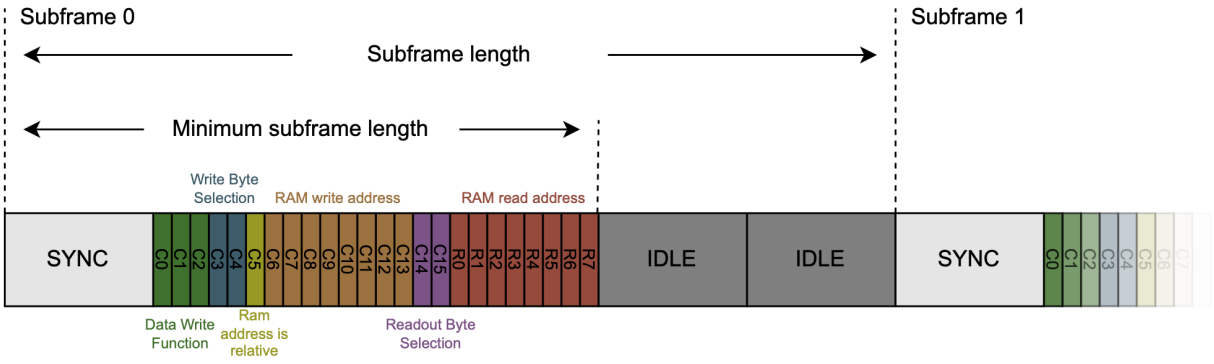


Figure 6.32: Illustration of the telegram protocol structure. It contains (sub)frame-specific data storage and readout instructions which are globally shared by the ASIC channels. The length of a telegram defines the length of the corresponding (sub)frame. [73]

3. **IDLE:** At the end of each (sub)frame, the amount of IDLE words controls the (sub)frame length.

The unit formed by both the sync character and the instruction payload defines the minimum possible (sub)frame length T_{min}. Since the serial telegram link is 8b/10b encoded, this means that T_{min} is given by the time it takes to transmit 4 10-bit words which contain the minimum of 4 8-bit words of information. Every extra IDLE character increases the (sub)frame length by the transmission time of another 10 bits. The combination of the sync character, the instruction payload and the tailing IDLE charcters are henceforth called *telegram*.

The 24 control bits contained in the instruction payload are compiled in the following list:

- **Data Write Control Function:** Define how to proceed with the final photon count value. There are five available options ranging from **discarding** the value, to **storing** it at, **adding** it to or **subtracting** it from the contents of the provided RAM write address. In addition, one can choose to ignore the photon count value and **increment** the content of the given RAM address instead.
- **Write Byte Selection:** Each RAM address consists of two bytes. Choose, whether to perform the data write control function on only the low, the high or both bytes. A fourth option allows to perform the function on neither of the two bytes.
- **RAM Address is Relative:** If this bit is set, the data write control function is performed at the address that equals the final photon count value. Subsequently, the provided RAM Write Address is ignored.
- **RAM Write Address:** Specify the RAM address at which the data write control function is supposed to be executed.
- **Readout Byte Selection:** Similar to Write Byte Selection, choose which of the two bytes should be read from the provided RAM readout address. The available options range from low to high to both bytes. If none of these is chosen, there is no data readout in this (sub)frame.
- **RAM Readout Address:** Choose which RAM address to read data from. If no bytes have been selected in the readout byte selection, this instruction is ignored.

The on-chip telegram interface employs a state machine to decode the input telegram word by word and send the corresponding command bits to the data write and read control units in each channel.

Example Use Cases

Instead of featuring hard-coded measurement and readout modes, the flexibility of the telegram protocol allows users to define their own routines. Taken from [73], figure 6.33 showcases a few examples of possible modes. At the top, there is a simplified display of a train of x-ray pulses. For simplicity, each of the bunches is associated with one (sub)frame. The numbers above specify the amount of photons contained in the corresponding pulses. Below the pulse train, there are five bucket-like structures subdivided in smaller boxes. The bucket-like structures are supposed to illustrate the contents of a channel's RAM after performing custom-defined example measurements. In this context, each bucket

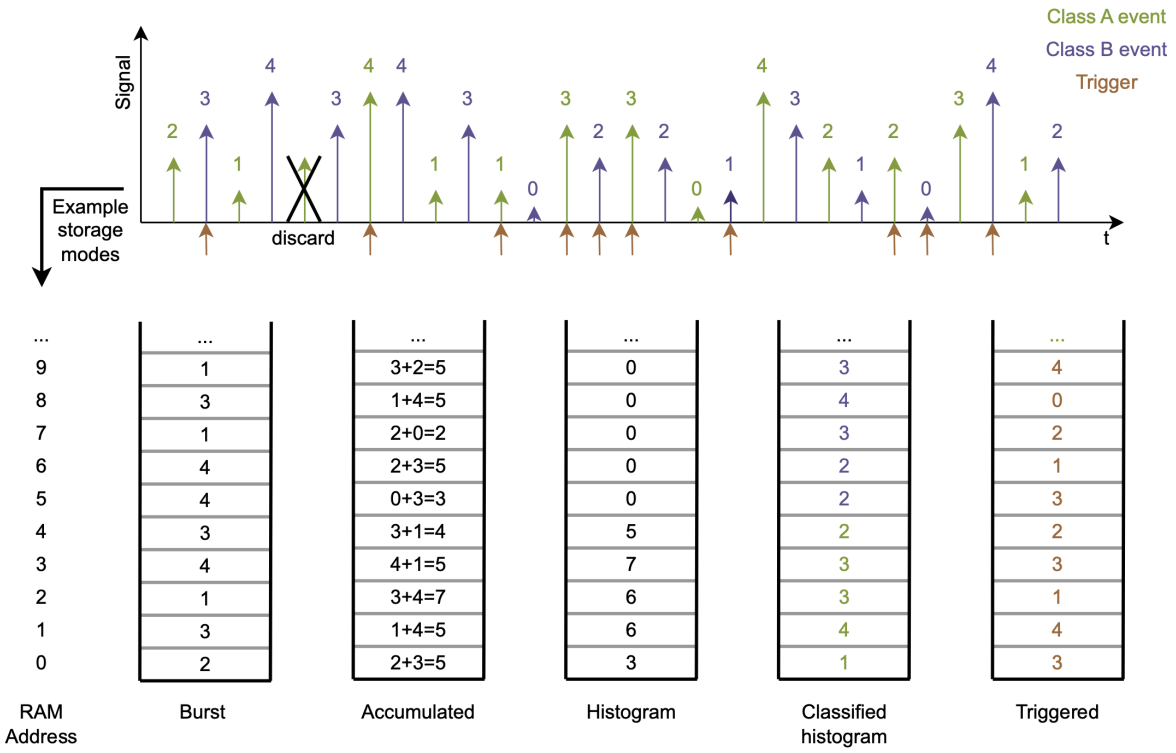


Figure 6.33: Illustration of example storage modes that can be realised with the telegram protocol. [73]

corresponds to a seperate, individual measurement/storage mode with its corresponding name underneath. The boxes illustrate the contents at the different RAM addresses which are listed on the left-hand side.

For every mode, the fifth pulse is chosen to be discarded. In the *burst* mode, the counted photon values of each (sub)frame are stored one by one. This could be an example for measurements with very fast frame rates, where it is impossible to send out a live-feed from the whole pixel matrix due to too high data rates. With a current RAM size of 192 or 256 words[20], the burst mode allows taking 192 or 256 frames in quick succession and reading them out afterwards.

The *accumulated* mode is very similar to the burst mode. But instead of storing each (sub)frame individually, they are digitally added up in the RAM to form a combined frame. This is the implementation of the digital integration scheme as explained in section 5.4. The amount of added (sub)frames per frame can be chosen freely.

In the *histogram* mode, the ASIC channel generates a histogram of the recorded photon amounts per pulse on-chip while the measurement is on-going. Instead of storing each (sub)frame photon count individually, the channel increments the value stored at the corresponding RAM address. After the measurement has been performed, the resulting histogram can be read out from the RAM.

In some measurements, it might be useful to have a classification of events, e.g. where samples are illuminated from different angles or undergo transitions from one state to another. With the telegram, users could e.g. store histograms of different classes of events as illustrated by the *classified histogram* mode. The shown colors green and blue indicate which class the event initially belonged to.

[20]This depends on the ASIC iteration.

The *triggered* mode is another example in which only certain pulses are selected and stored. These could correspond to events of interest, while others are discarded from the beginning. In the figure, pre-selected events which are chosen with a trigger are marked by brown arrows.

In addition to the presented example modes, the telegram protocol also allows a continuous readout stream of recorded (sub)frames. While almost all of the measurements presented in the sections 7 and 8.3 have been controlled via the telegram protocol, section 7.3.1 presents an example measurement for the histogram mode. Beyond the presented examples, there are many other possible modes and combinations.

6.4 Parameter Choices

The choice of the different capacitors, bias voltages and currents allows tuning the front-end performance for different use cases. While on the one hand, this increases the complexity of the design, it also increases the design's adaptability to different challenges, on the other hand. This has become more and more important in the later stages of the R&D phase of XIDer. Alongside the growth and maturing of the project, the interest of other synchrotron light sources sparked the research about how to adapt the design to various environments with different parameters.

To begin with, the following list compiles the parameters needed to adapt the XIDer readout ASIC to a desired light-source:

- **X-ray energy range:** The range of X-ray energies the detector is supposed to detect.
- **Expected average single photon input charge Q_{phot}:** The average charge generated by an individual photon in the sensor material.
- **Expected photon fluxes Φ:** The expected amount of X-ray photons hitting the sensor per time and area.
- **Sensor pixel pitch:** The pixel pitch allows deriving the incident photon rate per pixel from Φ.
- **Detection sensitivity:** The smallest amount of charge, the detector has be able to resolve.

In addition, the adaptable ASIC design parameters are highlighted in figure 6.34 and listed below:

- **Feedback capacitors C_{fb0} and C_{fb1}:** Dictate the charge-to-voltage gain of the individual front-end stages as well as the dynamic output voltage range. Their choice depends on the expected input charges.
- **Transfer capacitor C_{tran}:** Dictates the charge gain between the coarse and the fine stage. Its choice is directly bound to the choice of the feedback capacitors and the desired photon count rates per pixel.
- **Charge pump frequency f_{pump}:** Is limited by the bandwidth of the front-end stages. Its choice depends on the desired photon counting rates, front-end stage power consumption and size of the charge pump packages.

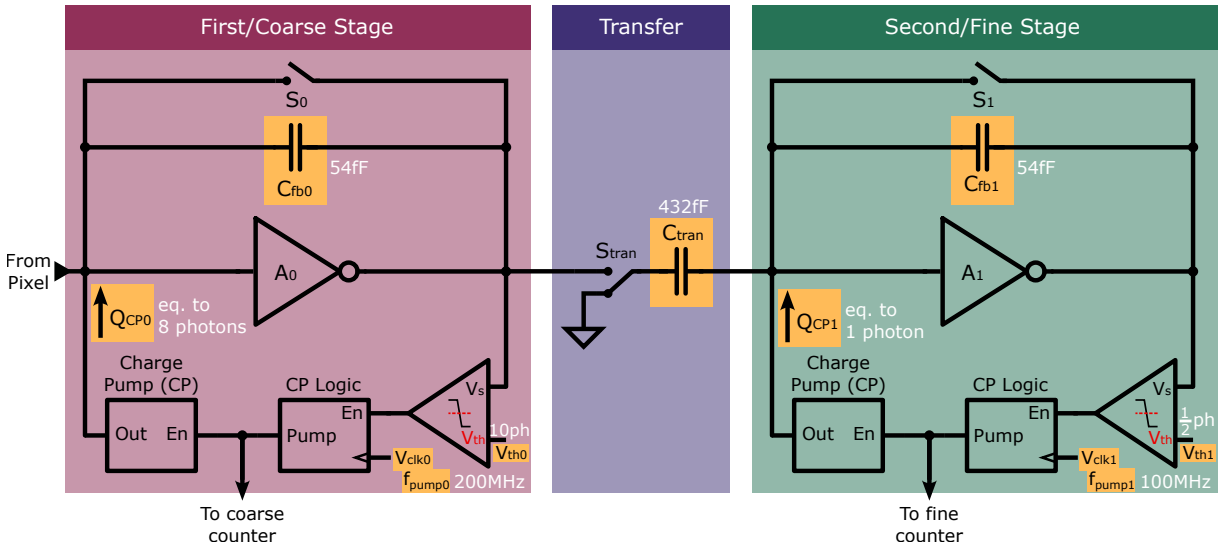


Figure 6.34: Simplified front-end schematics with adaptable design parameters highlighted in yellow. While the non-highlighted compartments play an important role in the front-end's general functionality, the highlighted ones allow tailoring the design to the desired constraints. The parameters chosen for all the ESRF-specific ASICs, i.e. all of the manufactured ones up to this point, are highlighted in white.

- **Charge pump packages Q_{CP0} and Q_{CP1}:** Dictate the upper and lower boundaries of the dynamic photon counting range and sensitivity. Their choice depends on the expected input charges, f_{pump} and the charge gain between the coarse and fine stages. On top, their choice dictates the size of the charge pump bias currents $I_{CP0/1}$.
- **Threshold voltages V_{th0} and V_{th1}:** Depend entirely on the charge pump package sizes and feedback capacitors.

Obviously, the actual choice of these parameters occurs at different stages of design. While capacitors can not be changed after manufacturing, the bias voltages and currents can be chosen via slow control when operating the ASIC. But even for the biasses, one has to choose their global and local trim setting range before actual manufacturing to make sure that the desired values can be reached.

ESRF-Specific ASIC Iterations (SUS65T1-SUS65T6)

The corresponding requirements for XIDer's operation at the ESRF include an X-ray energy range of 30 keV to 100 keV imposing the need to use cadmium telluride or, if acquirable, cadmium zinc telluride as the sensor material. With an average energy-hole-pair production energy of $\epsilon_{CdTe} = 4.43\,\text{eV}$[84] and $\epsilon_{CZT} = 4.64\,\text{eV}$[21][84], individual photons in this energy range generate charges in the range of roughly $6 \times 10^3\,\text{e}^-$ to $23 \times 10^3\,\text{e}^-$, i.e. 1 fC to 3.7 fC when they absorbed by the sensor. And expected photon fluxes of up to $1 \times 10^{11}\,\text{ph}\,\text{mm}^{-2}\,\text{s}^{-1}$ with a pixel pitch of 100 µm yield an expected photon rate of up to $1 \times 10^9\,\text{ph}\,\text{s}^{-1}\,\text{pix}^{-1}$ while maintaining single photon sensitivity.

The design choices for the ESRF-specific front-ends made from these input parameters are highlighted in white in figure 6.34. In order to keep up with the high photon rates, the

[21]This value depends on the actual compound.

coarse stage charge pump frequency is chosen to be $f_{pump0} = 200\,\mathrm{MHz}$ with a package size Q_{CP0} equivalent to the charge of 8 ph. With this, the upper limit for the photon counting rate per pixel is $1.6 \times 10^9\,\mathrm{ph\,s^{-1}\,pix^{-1}}$.

The choice of the fine stage charge package Q_{CP1} follows from the required single photon sensitivity, where Q_{CP1} has to have the size equivalent to the charge generated by a single absorbed photon or less.

The feedback capacitor of the coarse stage C_{fb0} should be chosen as small as possible to guarantee a high charge-to-voltage gain and ease the comparator's task. At the same time, the CSA's dynamic output voltage range should be large enough to cover the equivalent of at least 1.5 charge packages. With a safety margin, the dynamic output voltage range is roughly $V_{out0,dyn} \approx 600\,\mathrm{mV}$ (see table 6.2). Subsequently, the choice of C_{fb0} can be calculated as

$$C_{fb0} = \frac{1.5 \cdot Q_{CP0,100keV}}{V_{out0,dyn}} \approx 75\,\mathrm{fF}. \tag{6.50}$$

Since the initial designs focussed on verifying the operation principle, mostly at low photon energies of 30 keV, the coarse stage has been equipped with a slightly larger gain by choosing $C_{fb0} = 54\,\mathrm{fF}$ to relax the constraints on single front-end modules like the CSAs and the comparators.

The choice of C_{tran} and C_{fb1} has been driven by the principle of simple implementation and verification of the front-end's functionality. Due to the fact that Q_{CP0} corresponds to 8 photons and Q_{CP1} corresponds to a single photon, choosing a charge transfer gain $A_C = C_{tran}/C_{fb0}$ from the coarse to the fine stage (see section 6.2.4) equal to 8, allows implementing the fine stage as a copy of the coarse stage. For this reason, C_{fb1} is chosen equal to C_{fb0} and $C_{tran} = 400\,\mathrm{fF}$. Besides the simplified implementation, the large coarse-to-fine charge gain $A_C = 8$ further relaxes the performance constraints on the fine stage. In reality, of course, there are differences between the coarse and the fine stages. For instance, since it does not have to keep up with high photon rates, the fine stage's charge pump frequency is only $f_{pump1} = 100\,\mathrm{MHz}$. Subsequently, the fine stage CSA's bandwidth can be reduced in relation that of the coarse stage to save power (see also section 6.2.1.7).

In terms of threshold voltages, V_{th0} and V_{th1} follow from the choice of the respective charge packages and feedback capacitors. Their actual value is not as critical as long as they are precise enough to indicate whether a charge package should be subtracted or not. However, one has to make sure that the threshold is high enough such that none of the stages pump their output voltages below their virtual ground level. For the ESRF-specific design, the coarse and fine threshold voltage usually sit at roughly 10 and 1/2 equivalent photons, respectively.

Over the course of the project, these initial choices have proven to fit the requirements for chip characterisation as well as those of the ESRF quite well. Due to this, they have been kept throughout all the ASIC iterations up to the point when this work has been compiled. Every simulation and measurement presented in this work is based on a chip iteration that was implemented with these parameters.

Upcoming XIDyn design

In the wake of a currently forming XIDyn collaboration with the STFC [80], the ASIC's upcoming iteration is meant to fulfill the design constraints of at least two machines. While the first one is still the ESRF, the concepts of XIDer will also be tested at the Diamond Light Source [85] in the UK. For this reason, the list of requirements has been defined in a broader fashion. However, most of the detector constraints are currently being discussed

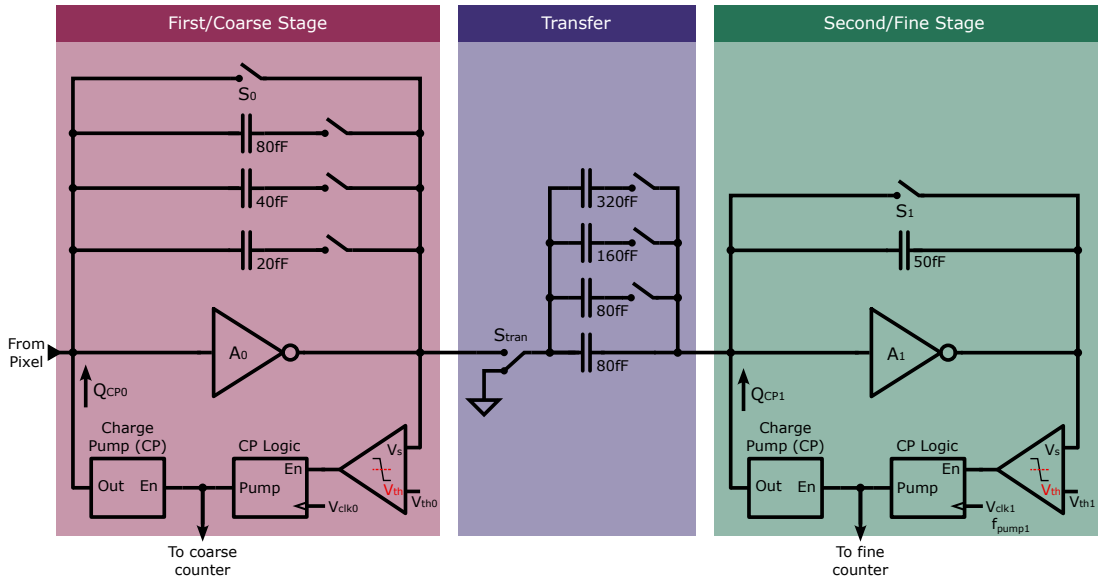


Figure 6.35: Preliminary front-end circuit diagram for future ASIC iterations. The switchable array of coarse stage feedback and transfer capacitors offers more flexibility to use the ASIC at various synchrotron light sources with different X-ray energies and photon fluxes.

which prevents a detailed presentation at this point.

Figure 6.35 shows an initial, modified front-end concept. As illustrated, the design is supposed to feature several different feedback and transfer capacitors. This decision stems from the fact that the big variety in different X-ray energies can no longer be covered by a single set of capacitors. Instead, users are supposed to be provided with a choice which fits their energy range. At the same time, an array of different transfer capacitors allows for a tradeoff between charge transfer gain A_C and transfer time. A smaller transfer capacitor allows for faster transfer and shorter (sub)frames but provides a smaller gain.

6.5 Design Verification

In order to fully verify the functionality of the readout ASIC, a full-blown mixed mode simulation is necessary. This has been performed successfully for several chip iterations throughout this project. However, an isolated analog front-end verification proves to be more instructive and helpful to demonstrate the chip's functionality and performance. For this reason and for the sake of brevity, this section solely focusses on the analog front-end.

Figure 6.36 shows the circuit diagram of the entire analog front-end of XIDer with the ESRF-specific design parameters discussed in section 6.4. Besides the already explained components, it features a few more auxiliary components which improve its functionality in extremal edge cases. One example are the addable input capacitors $C_{add0/1}$. As explained in sections 6.5.2 and 6.5.3, in order to correctly count the amount of absorbed photons by the sensor pixel in pulsed modes with large average photon fluxes, the front-end has to be able to cope with large amounts of instantaneous charge. In this context, the term *instantaneous charge* is used for charges which are injected in a time scale shorter than the period of the charge pump clock. The purpose of $C_{add0/1}$ is to extend the size of instantaneous charges that can be processed, if necessary.

The additional input switch S_{in} adds another feature to dynamically cut-off the front-end

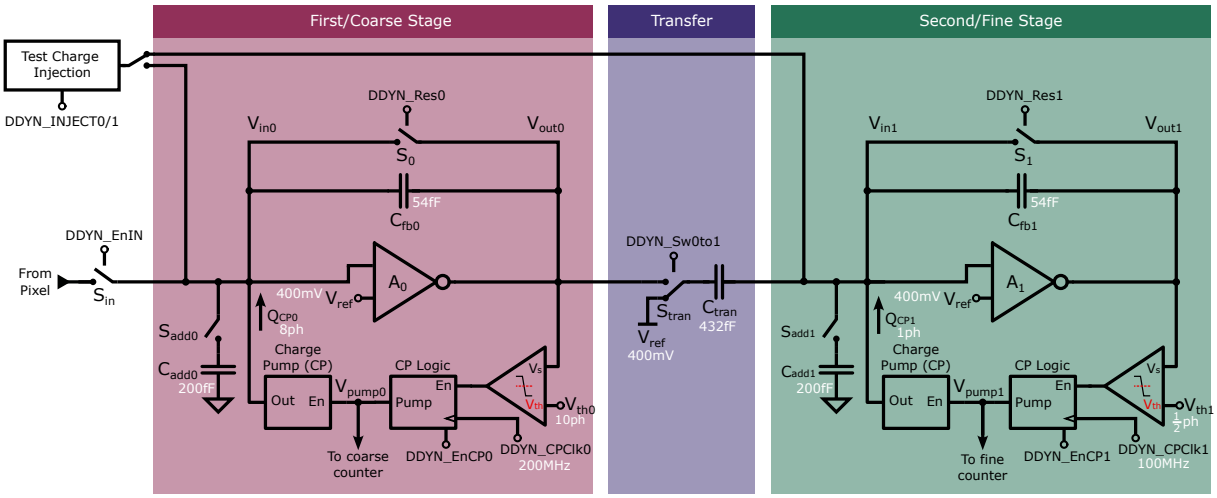


Figure 6.36: Detailed circuit diagram of XIDer's analog front-end as implemented on the most recent iteration SUS65T6.

from its sensor pixel. This can be useful to prevent charge from entering the front-end when the coarse stage is currently charging the transfer capacitor. Also, it allows studying the performance of the isolated front-end without the influence of a connected sensor pixel or input pad.

In the circuit drawing, dynamic signals are denoted with the prefix "DDYN_". In the real-world implementation these are generated by the on-chip sequencer as described in section 6.3.3.1. In the simulations, they are provided by a simplified module written in Verilog-A [86].

Signals without a prefix are static control signals like, for instance, bias voltages or currents. On the actual chip, these are configured via the JTAG slow control interface, while the simulation generates them via ideal voltage and current sources. An additional Verilog-A module counts and adds the charge packages applied by the coarse and fine stages, respectively, and presents the result as its output voltage.

The following sub-sections present a few selected full-blown analog simulations of the fully assembled front-end design. They are used to characterise the front-end's

- general functionality,
- ability to deal with large instantaneous charges,
- counting linearity,
- coarse-to-fine charge transfer time and its importance for achievable photon count rates
- and noise performance.

At the end of this section, a summary provides an overview of the key aspects.

If not mentioned otherwise, the following is true for all the simulations: An ideal current source draws a pulse-shaped current from the input.[22] This pulsed current occurs once at the beginning of a (sub)frame and all of the input charge injected per (sub)frame is contained in the pulse. The front-end itself is calibrated to count 30 keV-photons where

[22] Since the front-end is connected to the sensor pixel anode, the front-end reads the electron-induced signal. Subsequently, following the technical current definition, current is drawn out of the front-end.

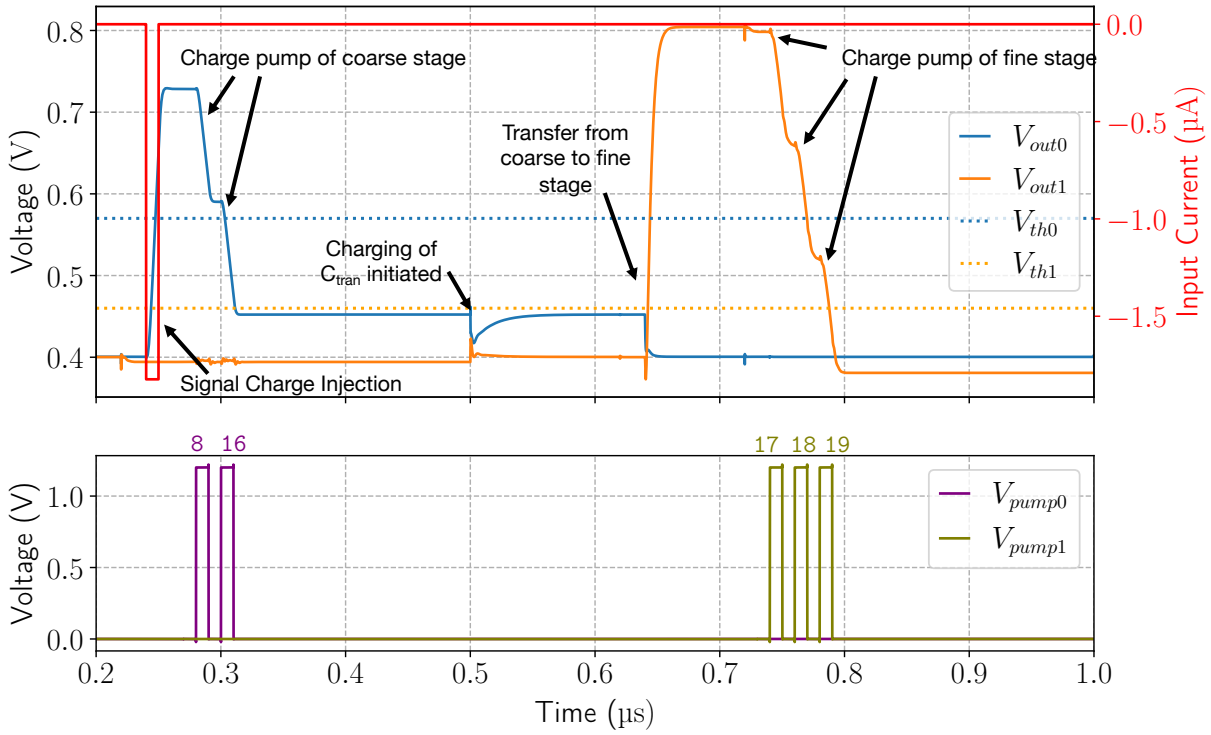


Figure 6.37: Analog simulation of the assembled front-end.

the coarse stage counts 8 photons and the fine stage counts a single photon per charge package. In this context, the sensor is assumed to be a cadmium telluride sensor with an average electron-hole-pair production energy of $\epsilon_{CdTe} = 4.43\,\text{eV}$.

6.5.1 General Front-End Functionality

This simulation demonstrates a full (sub)frame cycle. For illustrative purposes, the pump frequency for both stages is at $f_{pump} = 50\,\text{MHz}$ and the (sub)frame is 400 ns long[23]. As a test case, the charge in the input current pulse corresponds to 19 30 keV-photons. Figure 6.37 shows the results and signal sequences. For clarity, the DDYN control signals are omitted.

As soon as the charge enters the front-end, the output of the coarse stage V_{out0} rises. When it crosses the threshold V_{th0}, the comparator activates the charge pump which starts injecting charge packages into the coarse stage input. V_{pump0} shows the corresponding enable pulses generated by the charge pump logic. As a result, the coarse stage output decreases with each charge pump enable pulse. As soon as V_{out0} falls below the threshold voltage, the charge pump is deactivated and no further charge packages are injected.

At the end of the (sub)frame, the transfer capacitor C_{tran} is charged to the coarse stage's residual voltage. After completing the charging process, the residual charge is transferred to the fine stage with a charge gain of $C_{tran}/C_{fb0} = 8$. There, the same process takes place. The fine stage output voltage rises above the threshold and the charge pump injects charge into the fine stage input until the output drops back below the threshold. As indicated by the numbers above the lower plot, the front-end correctly counts 19 photons.

[23] As a reminder: The actual (sub)frame length is denoted by the individual stages' cycle from reset to reset.

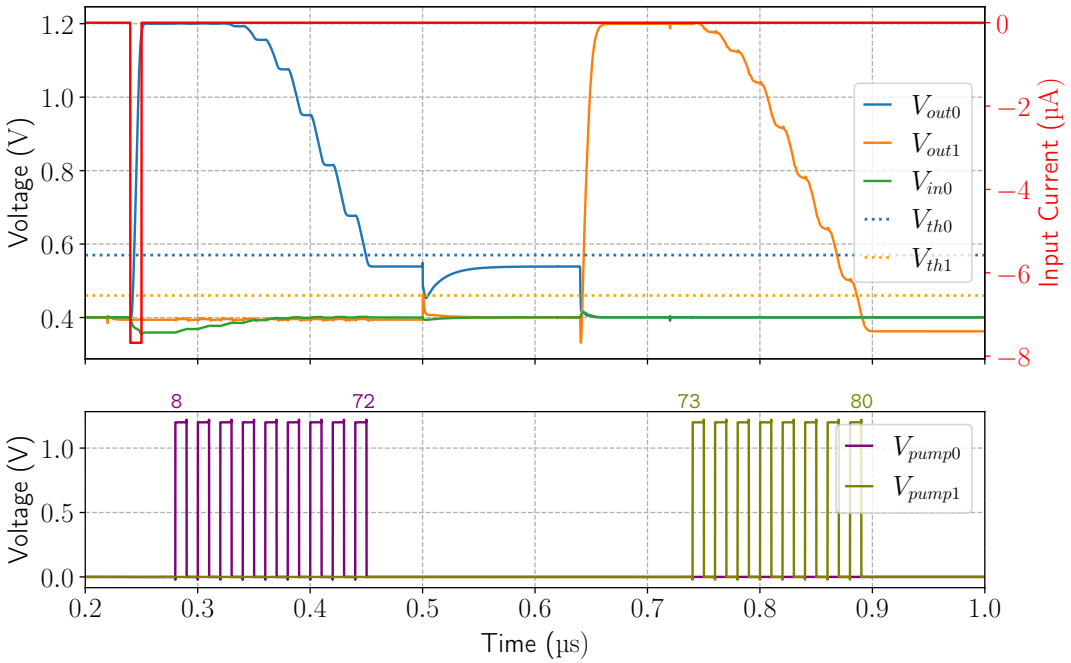


Figure 6.38: Analog simulation demonstrating the front-end's robustness to large input charges which saturate the coarse stage. The injected charge corresponds to 80 photons with an energy of 30 keV. As soon as V_{out0} saturates a the supply voltage of 1.2 V, the coarse stage input voltage V_{in0} starts decreasing. With charge packages injected by the charge pump, V_{in0} keeps recovering until the feedback is restored.

6.5.2 Robustness to Large Instantaneous Input Charges

A remarkable feature of this front-end is that its operation principle is unperturbed by saturation of its CSA stages. The saturation of a CSA occurs, when its input charge is high enough to drive its output voltage to the upper voltage limit. For the coarse stage of XIDer's front-end, this state is reached for an input charge equivalent to roughly 37 30 keV.

As soon as the coarse stage enters saturation, the feedback loop is broken such that V_{out0} is no longer proportional to the input charge. Intuitively, one would assume that the CSA can not store any additional charge beyond this point. In reality, additional charge is stored on the input capacitor C_{in} and the stage's feedback capacitor C_{fb0}. This is achieved by a decreasing input voltage V_{in0} where the deviation from the virtual ground ΔV_{in0} is given via

$$\Delta V_{in0} = \frac{Q_{in}}{C_{fb0} + C_{in}} \approx \frac{Q_{in}}{C_{det}}. \tag{6.51}$$

Here, C_{in} consists of the parasitic input capacitance of the amplifier, stray capacitance on the input wiring as well as the sensor pixel capacitance C_{det}. The final approximation only holds, if C_{det} has the size of at least a few 100 fF. In this case, C_{det} dominates C_{in} and $C_{det} >> C_{fb0}$.

Figure 6.38 shows the result of a simulation with an input charge equivalent to 80 30 keV photons and $C_{det} = 500$ fF. As demonstrated, the coarse stage output voltage V_{out0} rises to the supply voltage of 1.2 V and the input voltage V_{in0} is decreased. With every package, the charge pump removes the charge stored on C_{det} and V_{in0} steadily returns back to the

reference ground voltage. With enough charge packages, the coarse stage CSA's feedback is restored and V_{out0} starts to fall again. Beyond this point, this simulation is equvialent to the previous show-case.

Due to the fact that the charge package size is independent of the charge pump's output voltage, there is no signal loss in this process. This is because the charge pump only operates on charges, not on voltages. As long as the comparator is active, the charge pump can keep injecting its well-defined charge packages into the input. At the same time, the CSA output voltage is only needed to act as a monitor which signals, whether the input charge is above a pre-defined threshold. As long as it manages to act linearly around the threshold voltage, it can fulfill this task. Subsequently, the front-end manages to correctly count the amount of incident photons even though the coarse stage saturated in the process. The same argument works for the fine stage.

The advantage of this approach is that a small feedback capacitor can be used to obtain a large charge-to-voltage gain without substantially limiting the dynamic photon counting range. Thanks to the large signal gain, the constraint on the electronic noise contribution of the CSA's amplifier is relaxed. In addition, the comparator does not have to be as precise which simplifies its design.

However, there is a limit to this effect. If the stage's input voltage drops low enough, diodes between transistor contacts and the substrate will start conducting in forward direction. As a consequence, charge on the input node is lost. This usually happens at around a few hundred negative mV. The following counting linearity simulation gives insight into when this point is reached and how it depends on the size of the pixel capacitance.

As a side note: Due to the different modes and measurements, XIDer is designed for, the size of instantaneous charges the detector has to face can vary largely. On the one hand, in pulsed high-flux modes like the 16-bunch mode[24], for example, the coarse stage is expected to be driven into saturation on a regular basis. A discussion of expected photons per pulse can be found in the following sub-section. On the other hand, in continuous modes like the 7/8+1-bunch mode, the input charge of an individual (sub)frame is not injected at once but distributed over the whole (sub)frame length. Subsequently, in this case, the coarse stage CSA is not expected to be driven into saturation. For this reason, XIDer's analog front-end was designed to be able to both deal with high instantaneous charges and continuous input currents.

6.5.3 Counting Linearity

This simulation's purpose is to demonstrate the front-end counting linearity. It is performed like the two previous simulations where the total input charge is injected in a single pulse at the beginning of the (sub)frame. In addition, the input charge size is swept. As before, the input charge is referred to the equivalent charge that a 30 keV-photon generates in a CdTe sensor. For each swept input value, the amount of photons counted N_{count} by the front-end is extracted. Figure 6.39 shows a plot of the counted photons vs. the incident photon number for different sensor pixel capacitor values C_{det}. As demonstrated, in the simulated range from 0 to 200 photons, the front-end exhibits perfect linearity for every value of C_{det}. For the values of $C_{det} = 0\,\text{fF}$[25], $C_{det} = 200\,\text{fF}$ and $C_{det} = 500\,\text{fF}$, the point

[24] see section 2.3.4 for an explanation of the bunch modes

[25] In this case, the front-end's input capacitance is dominated by the parasitic gate-source and gate-drain capacitance of the coarse stage's input transistor.

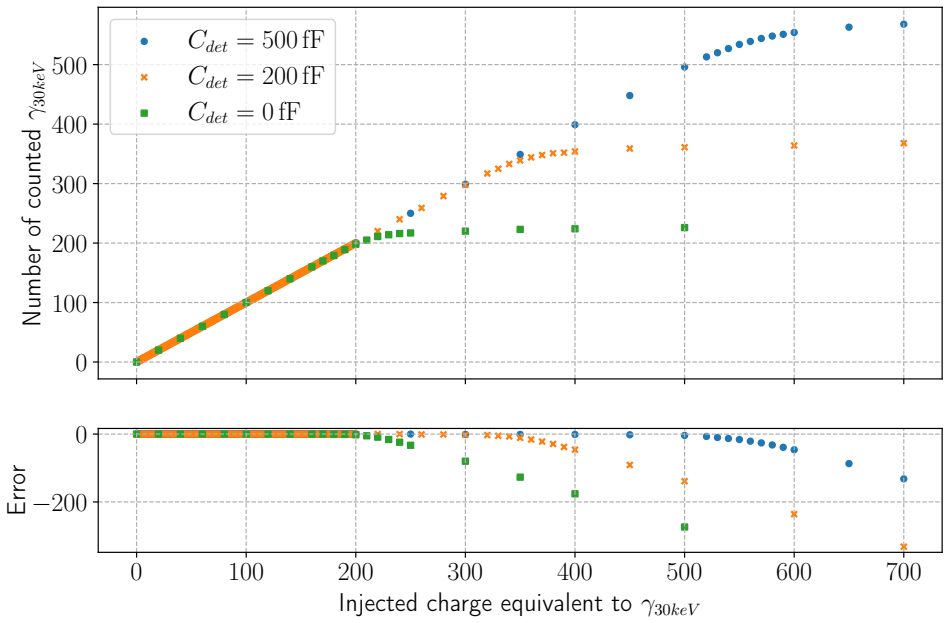


Figure 6.39: Analog simulation of the front-end's counting linearity for different pixel capacitances C_{det}. The injected charge on the x-axis is given in units of the equivalent charge generated by a single 30 keV-photon in a CdTe sensor. The y-axis displays the amount of 30 keV-photons that have been counted by the front-end.

of charge loss due to diodes opening at the front-end input node is reached at charges equivalent to $\approx 200\,\gamma_{30\text{keV}}$, $\approx 350\,\gamma_{30\text{keV}}$ and $\approx 520\,\gamma_{30\text{keV}}$, respectively.

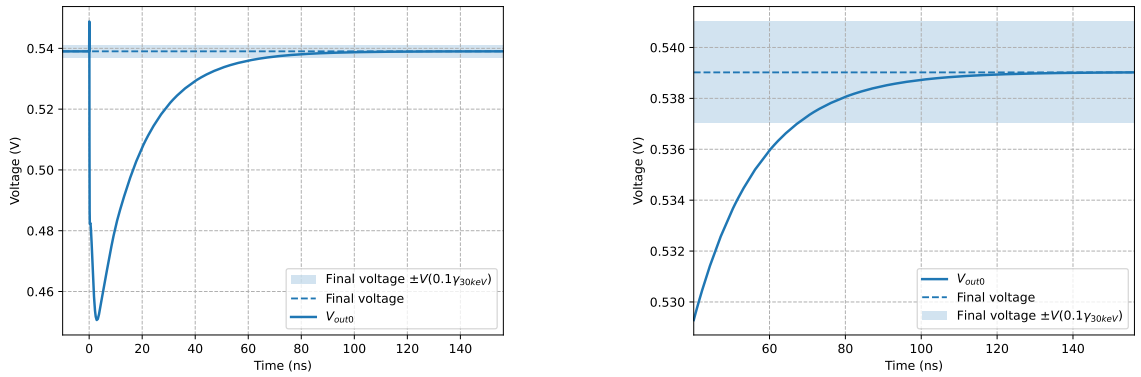
An important point to note is that this simulation assumes no errors or uncertainties of the charge generated by individual photons in the sensor pixel. It also excludes the Poisson-shaped photon statistics as well as the electronic noise of the simulated circuit. In the real world, these effects add up as a random contribution in each counting measurement performed by the ASIC. Subsequently, in an actual measurement, the values displayed in figure 6.39 would only represent the mean count of a distribution which is shaped by all of the noise contributions.

However, since this is a full-blown analog simulation of the front-end design, it includes each component down to the individual transistor level. Subsequently, it does include all of the systematic errors introduced by the non-ideal circuit components.[26]

While there is no clearly defined design constraint to compare these numbers to, one can make an estimation regarding the expected instantaneous input charge: In the most extreme mode, i.e. the 16-bunch mode, bunches are ≈ 175 ns apart. At an incident photon rate of 1×10^9 ph pix^{-1}, this corresponds to an average number of 175 photons per bunch and pixel. Due to the Poissonian nature of photon counting statistics, the actual amount of incident photons can vary. For this reason, a conservative requirement has been defined in which the front-end has to be able to handle the instantaneous charge generated in the sensor by 200 30 keV-photons as a maximum.[27] And according to simulation,

[26] The underlying BSIM device models are part of the technology's design kit which is provided by the foundry.

[27] While the generated charge per photon increases with the energy, the X-ray beam brilliance drops



(a) Total charging process

(b) Zoomed-in view

Figure 6.40: Simulation of the coarse stage's output voltage V_{out0} while the transfer capacitor is being charged. The charging process is initiated at the time $t = 0$. The dashed line shows the voltage $V_{out0,r}$ which C_{tran} has to be charged to. The blue area shows the accepted systematical error around $V_{out0,r}$. In this context, the notation $V(0.1\gamma_{30keV})$ denotes the voltage that corresponds to 10 % of a 30 keV-photon.

XIDer's front-end manages to achieve this even if the pixel capacitance is $C_{det} = 0\,\text{fF}$. As demonstrated in the measurement, larger values of C_{det} extend the range. Due to this, $C_{add0/1}$ have been added to increase the front-end's input capacitance, if needed.
As a result, there are several conclusions to draw from this simulation:

- The design demonstrates a remarkable counting linearity up to 200 30 keV-photons even for a sensor pixel capacitance of 0 fF.
- In this simulation, the upper limit for the linear region is introduced due to the input charge being injected at once. As demonstrated, in this situation, the upper counting limit extends even beyond the required 200 30 keV-photons, if the input capacitance is larger than 0 fF. For instance, at $C_{det} = 500\,\text{fF}$, up to a total count of 500 photons, the simulation records a systematic deviation of a single photon.
- The design can handle the most stressful conditions which it is supposed to face: Just like in the ESRF's 16-bunch mode, all of the charge is injected at once and in a single pulse. Subsequently, the front-end has to deal with large instantaneous charges, far beyond its coarse stage CSA saturation limit. Any other mode with, for instance, a continuous distribution of the same charge over the whole (sub)frame eases the counting process.

As a direct comparison, section 7.2.2 presents a counting linearity characterisation measurement with SUS65T4 to verify the simulation in the lab.

6.5.4 Transfer Time

In addition to the large instantaneous charges, the ESRF's 16-bunch mode is the most challenging mode in terms of timing. And the most limiting factor from the front-end

significantly at higher energies [25]. Subsequently, the instantaneous charge is expected to be lower for higher energies.

perspective in terms of timing is the time it takes to transfer the coarse stage's residual charge to the fine stage. Due to its importance in the transfer process, the following elaborations focus solely on the coarse stage.

In the 16-bunch mode's (sub)frame length of $\approx 175\,\mathrm{ns}$, the signal charge has to be processed and digitised, residual charge has to be transferred to the fine stage and both stages have to be reset. Subsequently, the (sub)frame cycle of the coarse stage splits up into the parts

$$T_{sub} = T_{act} + T_{charge} + T_{res0} \tag{6.52}$$

where T_{act}, T_{charge} and T_{res0} are the time intervals needed for the continuous conversion, charging the transfer capacitor and resetting the coarse stage, respectively.

In the worst case, photon rates in the order of $1 \times 10^9\,\mathrm{ph\,s^{-1}}$ are incident to the sensor pixel. In the 16-bunch mode, this means that 175 photons hit the sensor pixel per (sub)frame on average. Subsequently, T_{act} has to be long enough to allow for the charge pumps to get rid of the equivalent sensor charge of 175 photons. At a pump frequency of 200 MHz and a charge package of 8 photons, the coarse stage needs 105 ns to reduce the charge to an equivalent of 7 photons. This residual can then be transferred to the fine stage. Subsequently, the lower limit for T_{act} is given as $T_{act,min} = 105\,\mathrm{ns}$ which leaves 70 ns for the sum of T_{charge} and T_{res0}. While the coarse stage reset takes about $T_{res0} \approx 20\,\mathrm{ns}$, figure 6.40 shows a simulation that allows determining T_{charge}. At an example residual voltage of $V_{out0,r} = 540\,\mathrm{mV}$, the charging process of C_{tran} is initiated at $t = 0\,\mathrm{s}$. It is assumed to be completed as soon as the voltage on C_{tran} deviates from $V_{out0,r}$ by a voltage that corresponds to 10 % of a 30 keV-photon ($\approx 2\,\mathrm{mV}$ for $C_{fb0} = 54\,\mathrm{fF}$). As demonstrated, for $C_{det} = 500\,\mathrm{fF}$, the simulated charging time is $T_{charge} \approx 67\,\mathrm{ns}$.

Equation 6.27 in section 6.2.1.4 shows that the front-end's input capacitance which is dominated by the pixel sensor capacitance C_{det} plays an important role in the bandwidth of the coarse stage CSA. Subsequently, it is expected that T_{charge} is influenced by C_{det}. Figure 6.41 shows a plot of T_{charge} for different values of C_{det}. Here, T_{charge} has been determined in the same way as in figure 6.40.

As demonstrated, whether the current front-end design can achieve a count rate of $1 \times 10^9\,\mathrm{ph\,s^{-1}}$ in the 16-bunch mode depends on the front-end input capacitance C_{det}. For example, with a conservative estimation of $C_{det} = 500\,\mathrm{fF}$, the transfer time is

$$T_{tran} = T_{charge} + T_{res0} \approx 87\,\mathrm{ns} > 70\,\mathrm{ns}. \tag{6.53}$$

In an optimistic case of $C_{det} = 200\,\mathrm{fF}$, it is roughly 72 ns which would be very close to the target. However, this simulation has been performed with a typical process corner. Slower corners are expected to have longer transfer times.

Thus, in the optimistic setting of $C_{det} = 200\,\mathrm{fF}$, the simulation predicts that the front-end is very close to reaching a sustainable count rate of $1 \times 10^9\,\mathrm{ph\,s^{-1}}$ in the most challenging conditions of the 16-bunch mode. This topic will be revisited in the following simulations.

6.5.5 Photon Count Rates

This simulation is concerned with the maximum photon counting rate $R_{ph,max}$ that the analog front-end can keep up with. As already hinted at in the previous simulation, $R_{ph,max}$ largely depends on the bunch mode, or more precisely, the (sub)frame length, the front-end is operated at.

At long enough (sub)frame lengths, the sustainable rate is dictated by the chosen charge pump frequency and coarse stage charge package size. For a frequency of 200 MHz and

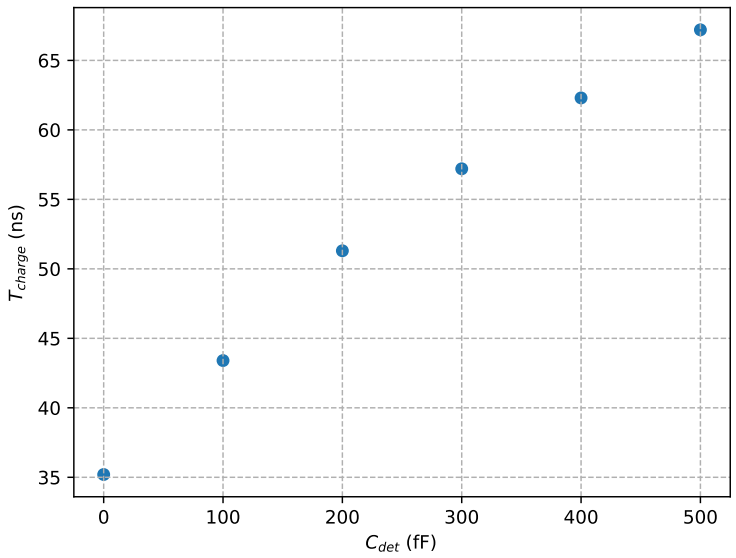


Figure 6.41: Analog simulation of the charge transfer time for different pixel sensor capacitances C_{det}. For the determination of T_{charge}, the point in time at which the CSA coarse stage's output voltage has reached its final within a window of 10 % of a 30 keV-photon has been used.

a package size equivalent to 8 photons, the maximum count rate for long (sub)frames is theoretically given as $R_{ph,max,long} = 1.6 \times 10^9\,\mathrm{ph\,s^{-1}}$.

In order to evaluate $R_{ph,max,long}$ in simulation, the input current source is tuned to generate a DC current. This DC current is supposed to represent the average current flowing through the sensor pixel for an incident 30 keV-photon rate $R_{ph,in}$. The front-end is operated in a mode, in which there is no charge transfer to the fine stage. Subsequently, the coarse stage can perform its continuous conversion throughout the whole (sub)frame length. At the end of a (sub)frame of 2 µs, the amount of counted photons by the coarse stage $N_{ph,count} = N_{ph,coarse}$ is evaluated for different values of $R_{ph,in}$. Dividing $N_{ph,count}$ by the (sub)frame length results in the corresponding photon count rate $R_{ph,count}$ at a given incident photon rate $R_{ph,in}$.

The result of this simulation is shown in figure 6.42. As demonstrated, the simulated counting rate matches the photon input rate closely until it saturates at $\approx 1.6\,\mathrm{Gph\,s^{-1}}$ which fits the expected $R_{ph,max,long}$.

In the case of shorter (sub)frames, the fixed transfer time starts playing a larger role. This is demonstrated in figure 6.43 which shows the simulated photon count rate $R_{ph,max}$ vs. the (sub)frame length T_{sub} at different pixel capacitances. In this simulation, the input photon rate is fixed at $1 \times 10^9\,\mathrm{ph\,s^{-1}}$ and the total charge if injected at the beginning of a (sub)frame. For each data point, the simulated front-end has executed a full integration cycle as depicted in the functionality simulation in section 6.5.1. At the end of this cycle, the coarse and fine stage count values are added.

The x-axis shows the swept (sub)frame length $T_{sub} = T_{act} + T_{tran}$. More precisely, only T_{act} is swept, while T_{tran} remains at a fixed value throughout the sweep for each individual input capacitance value C_{det}. The T_{tran}-value for the corresponding size of C_{det} is extracted from the previous transfer time simulation in section 6.5.4. For example, in the case of $C_{det} = 500\,\mathrm{fF}$, T_{tran} has been fixed to 87 ns. This leaves the front-end stages with an active

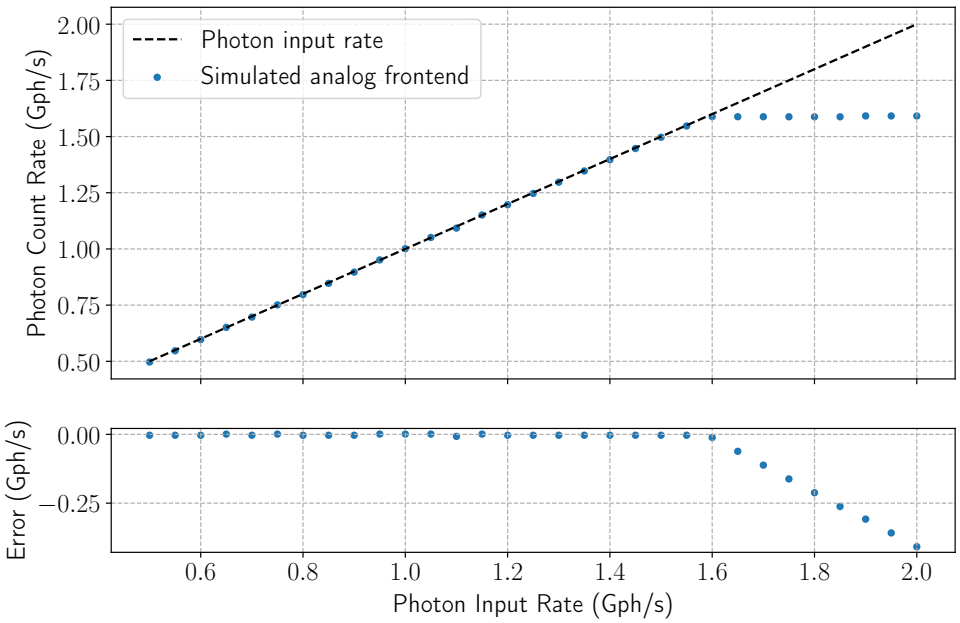


Figure 6.42: Analog simulation of the front-end's photon count rate at a constant and steady rate of input photons. The constant input photon rate is simulated with a DC current source which is scaled to the current generated by an equivalent rate of photons illuminating a CdTe sensor. The chosen photon energy is 30 keV.

time of $T_{act} = T_{sub} - T_{tran}$. In order to extract the photon rate, the amount of counted photons in the (sub)frame has been divided by the (sub)frame length.

The graph demonstrates the behaviour expected from the transfer time simulation. For an input capacitance of 500 fF, the front-end can not keep up with the input photon rate of 1×10^9 ph s^{-1} at a (sub)frame length of 175 ns. Still, it manages to reach a count rate of roughly 0.73×10^9 ph s^{-1}. Only at a (sub)frame length of roughly 280 ns, it manages to match the input photon rate.

With an input capacitance of 200 fF, the simulated front-end reaches a photon count rate of roughly 0.93×10^9 ph s^{-1} at a (sub)frame length of 175 ns which is very close to the aimed for 1×10^9 ph s^{-1}. In this case, the front-end catches up with the input photon rate at a (sub)frame length of roughly 200 ns. The slight deviation of the count rate plateau from the input photon rate stems from a minor miscalibration of the charge pumps' packages.

In both depicted cases, the front-end is capable of recording every second bunch of the 16-bunch mode which corresponds to a (sub)frame length of 350 ns.

6.5.6 Front-End Electronics Noise

In terms of noise generated by the readout electronics, there are two different figures of merit that have to be considered:

1. Baseline noise and dark count rate

2. Counting error induced by readout electronics noise

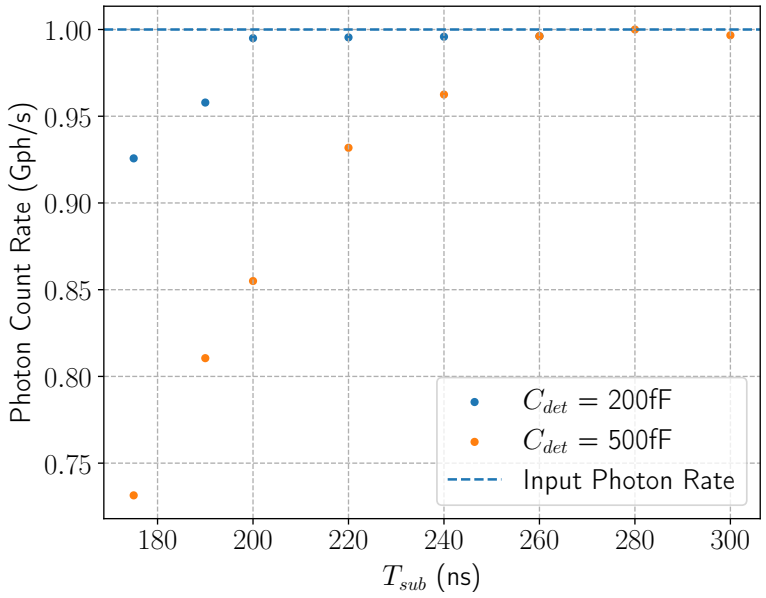


Figure 6.43: Analog simulation of the front-end's count rate vs. the chosen (sub)frame length at a fixed input rate of 1×10^9 ph s^{-1} for different input capacitances C_{det}.

The first one is concerned with the question of how often the front-end erroneously counts a hit when there was no incident photon. This property is governed by the voltage noise of the CSA baselines. This is due to the fact that, in the case no photon is absorbed in the sensor pixel, the front-end can only erroneously count a photon, if the variation of the CSA baselines is high enough for the comparator to trigger.

The second one is concerned with the photon counting error in the case of several or many photons in an individual measurement. Subsequently, it is governed by a combination of the noise contributions of the CSAs, the coarse and fine charge pumps as well as the fine stage comparator.[28] Furthermore, the influence of noisy charge package sizes is expected to be increased, the more often the charge pump applies a charge package where the noise is expected to increase proportional to $\sqrt{N_{c/f}}\sigma_{CP,single,c/f}$ in both stages. Here, N and $\sigma_{CP,single}$ denote the amount of applied charge packages and the noise contribution of each charge package in the coarse (c) and fine (f) stages, respectively.

The following simulation provides insight into the first property. In order to determine a theoretical dark count rate, the baseline noise performance of both CSAs is studied in a transient noise simulation. It starts with resetting the coarse stage CSA. After opening the reset switch, the noisy output voltage value is used to charge the transfer capacitor C_{tran}. Then, the coarse stage's noise stored on C_{tran} is transferred into the fine stage. Here, the fine stage output voltage is sampled. This same simulation is repeated 1000 times. The standard deviation of all of the simulated final voltages in the fine stage is then used as a measure of the front-end's total baseline noise $\sigma_{tot,v}$. This, of course, assumes that the noise is Gaussian-distributed.

[28] As discussed in 6.1.1, if the coarse stage threshold is at a high enough value, erroneous pumping by the coarse stage can be corrected for by the fine stage. Subsequently, noise contributions of the coarse stage comparator can be considered negligible.

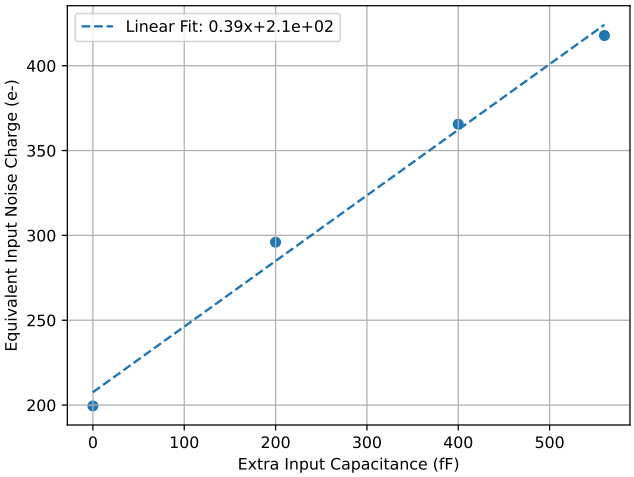


Figure 6.44: Simulated front-end baseline noise including only the coarse and fine stage CSA contributions in relation to the input capacitance.

In this simulation, the front-end's total baseline noise is given by

$$\sigma_{tot,v}^2 = A_C^2 \sigma_{c,v}^2 + \sigma_{f,v}^2 \tag{6.54}$$

where $\sigma_{c,v}$ and $\sigma_{f,v}$ are the output voltage noise contributions of the coarse and fine stages, respectively. With the fine stage feedback capacitance C_{fb1} as well as the charge transfer gain factor A_C, the voltage standard deviation is converted into a front-end input referred equivalent noise charge (ENC):

$$\sigma_{tot,inp,ENC}^2 = \frac{C_{fb1}^2}{A_C^2 q_e^2} \sigma_{tot,v}^2 = \frac{C_{fb1}^2}{q_e^2} \left(\sigma_{c,v}^2 + \frac{1}{A_C^2} \sigma_{f,v}^2 \right) \tag{6.55}$$

where q_e is the elementary charge. Subsequently, the coarse stage CSA dominates the front-end's baseline noise performance for the case that $A_C = 8$.

Figure 6.44 shows a plot of this simulation for several input capacitor values. As depicted, for no extra input capacitance, the total simulated noise is roughly 200 e^-. For the highest simulated value of $C_{in} = 560\,\text{fF}$, this noise rises to approximately 417 e^-. As stated in section 6.2.1.5, the CSA noise is expected to increase linearly with the input capacitance. For this reason, the data has been fitted with a linear function indicated by the dashed line. While the general trend of the data seems to resemble a linear relation, there are not enough data points to make a clear statement.

Reference [8] provides a dedicated dark count rate simulation for XIDer's digital integration scheme where the threshold has been set to half a 20 keV photon. Chosen (sub)frame lengths are in the range of 1 µs to 10 µs. For an ENC of 375 e^-, an expected dark-count rate in the order of $1\,\text{ph}\,\text{h}^{-1}\,\text{pix}^{-1}$ has been determined. In the context of typical experiments the XIDer detector has been designed for, this value has been deemed acceptable. Also, in XIDer's actual energy range of 30 keV to 100 keV, the threshold voltage will be higher which is expected to further decrease the dark count rate.

Since $\sigma_{tot,inp,ENC}$ ranges from 200 e^- to 417 e^- in an input capacitance range of 0 fF to 560 fF, the simulated front-end noise performance is expected to provide sufficiently low dark count rates. Section 7.2.3 provides a measurement to verify these results. As a

reminder, the coarse stage's single, isolated performance is listed in table 6.2 in section 6.2.1. The table lists an input referred noise charge of 385 e^- at an input capacitance of 500 fF.
This simulation allows several conclusions regarding the front-end's baseline noise and dark count rate:

- Against the contribution of the coarse stage CSA, the fine stage noise contribution can be neglected.
- Within the scope of the presented data, the baseline noise shows a linear dependency on the size of the input capacitance.
- Both the simulation presented here and the one discussed in section 6.2.1 result in comparable values for the noise with 400 e^- and 385 e^- at an input capacitance of 500 fF, respectively. In this context, it is important to keep in mind that these values have been determined with completely different procedures. The value presented in table 6.2 stems from an ac simulation of a single stage, while the value presented here results from a transient noise simulation.
- The expected dark count rate resulting from the measured baseline noise is expected to be below 1 $ph\,h^{-1}\,pix^{-1}$ for typical conditions that the XIDer detector has been designed and thus fulfills the requirements. Actual dark count measurements are necessary for verification.

In order to minimize the noise-induced counting error, the charge pumps have to be designed such that the generated charge packages exhibit a negligible variation. On the one hand, this is achieved by choosing long current source transistors[29] to decrease the bias current variation. On the other hand, the ASIC needs a low-jitter input clock to provide a low-jitter time reference for the charge pump clock. Since the influence of the latter highly depends on the measurement set-up, the charge package noise is studied in an actual measurement presented in sections 7.2.2 and 7.2.3.

6.5.7 Summary of Simulated Analog Front-End Performance

The simulations above present the analog front-end's current state. With one exception, they demonstrate that the most recent iteration is capable of meeting the requirements set by the XIDer project, at least in simulation. The most important features are:

- **Counting linearity:** With the correct calibration, the front-end manages to count photons reliably over a wide dynamic range. In the presented simulation, the average count exhibits a systematic error of 1 photon at an input charge equivalent to 500 30 keV photons.
- **Robustness against large instantaneous charges:** Depending on the average photon flux, pulsed bunch modes like the ESRF's 16-bunch mode can cause the generation of large amounts of charge in a short time window[30]. Up to an instantaneous input charge equivalent to 200 30 keV-photons, the front-end shows no counting performance degradation, even for the unrealistic case that the pixel capacitance is $C_{det} = 0$ fF. A higher pixel capacitance increases this upper limit. For $C_{det} = 500$ fF,

[29] M_1 in figure 6.22 of section 6.2.3
[30] In this context, short time windows are time intervals in the order of the charge pump period or shorter.

the range is extended up to 500 30 keV-photons. Both of these values verify that the simulated front-end provides the capability to cope with the instantaneous charge of 200 30 keV-photons and thus meets the requirement.

- **Sustainable photon count rates:** For long enough (sub)frames, i.e. $T_{sub} > 280\,\text{ns}$, the front-end can keep up with an incident photon rate of $1.0 \times 10^9\,\text{ph}\,\text{s}^{-1}$ for input capacitances smaller than 500 fF
- **Short (sub)frame count rate:** For shorter (sub)frames, the count rate is limited by the time it takes to charge the transfer capacitor T_{charge}. In order to operate the front-end in the 16-bunch mode at $1 \times 10^9\,\text{ph}\,\text{s}^{-1}$, T_{charge} has to be smaller than 50 ns. In the current front-end iteration, it is approximately 70 ns for an input capacitance of 500 fF. As a result, the ASIC can only process every second pulse of the 16-bunch mode or the input photon rate has to be moderated to $\approx 0.73 \times 10^9\,\text{ph}\,\text{s}^{-1}$. At an input capacitance of 200 fF, the maximum achievable rate is $\approx 0.93 \times 10^9\,\text{ph}\,\text{s}^{-1}$ which is close to the requirement of $\approx 1 \times 10^9\,\text{ph}\,\text{s}^{-1}$. The actual input capacitance which contains the sensor pixel capacitance as well as parasitics on the front-end's input line is yet to be determined.
- **Baseline noise and dark count rate:** At an input capacitance of $C_{det} = 500\,\text{fF}$, the simulated input referred noise charge of the baseline noise is roughly $400\,\text{e}^-$. At an input capacitance of $C_{det} = 200\,\text{fF}$, the baseline noise is reduced to roughly $295\,\text{e}^-$. For these values, the expected dark count rate lies in the order of $\approx 1\,\text{ph}\,\text{h}^{-1}\,\text{pix}^{-1}$ and below for a photon energy of 20 keV and (sub)frame lengths in the range of 1 µs to 10 µs. At higher photon energies, the dark count rate is expected to be even lower due to the increased comparator threshold voltage. For comparison, a photon with the minimum energy of 30 keV in XIDer's energy range absorbed in a CdTe[31] sensor generates a charge signal of roughly $6800\,\text{e}^-$. Subsequently, the front-end reaches a signal-to-noise ratio of about 20 which is more than enough to resolve single photons. Whether the whole detector can achieve this baseline noise and dark count rate performance, is yet to be determined.

While the underlying device models for simulation are quite sophisticated, these simulations have to be verified in actual measurements. The sections 7 and 8 provide an overview of a few selected measurements to verify the front-end performance.

6.6 Submitted Chip Iterations

Since XIDer's initiation in 2018, there have been six readout chip iterations. Over the course of the project, the focus and research interest developed from initial concept tests over readout circuit and sensor characterisation to preparing and implementing modules for large scale integrations. Figure 6.45 shows images of all the protoypes. While all of the iterations are denoted with their full names *SUS65T** here, the abbreviation *T** is used throughout this work.

SUS65T1

Submitted in November 2018, SUS65T1 was the the first ASIC iteration. Since this was the research group's very first submission in the TSMC 65 nm technology, almost all of the

[31] $\epsilon_{CdTe} = 4.43\,\text{eV}$

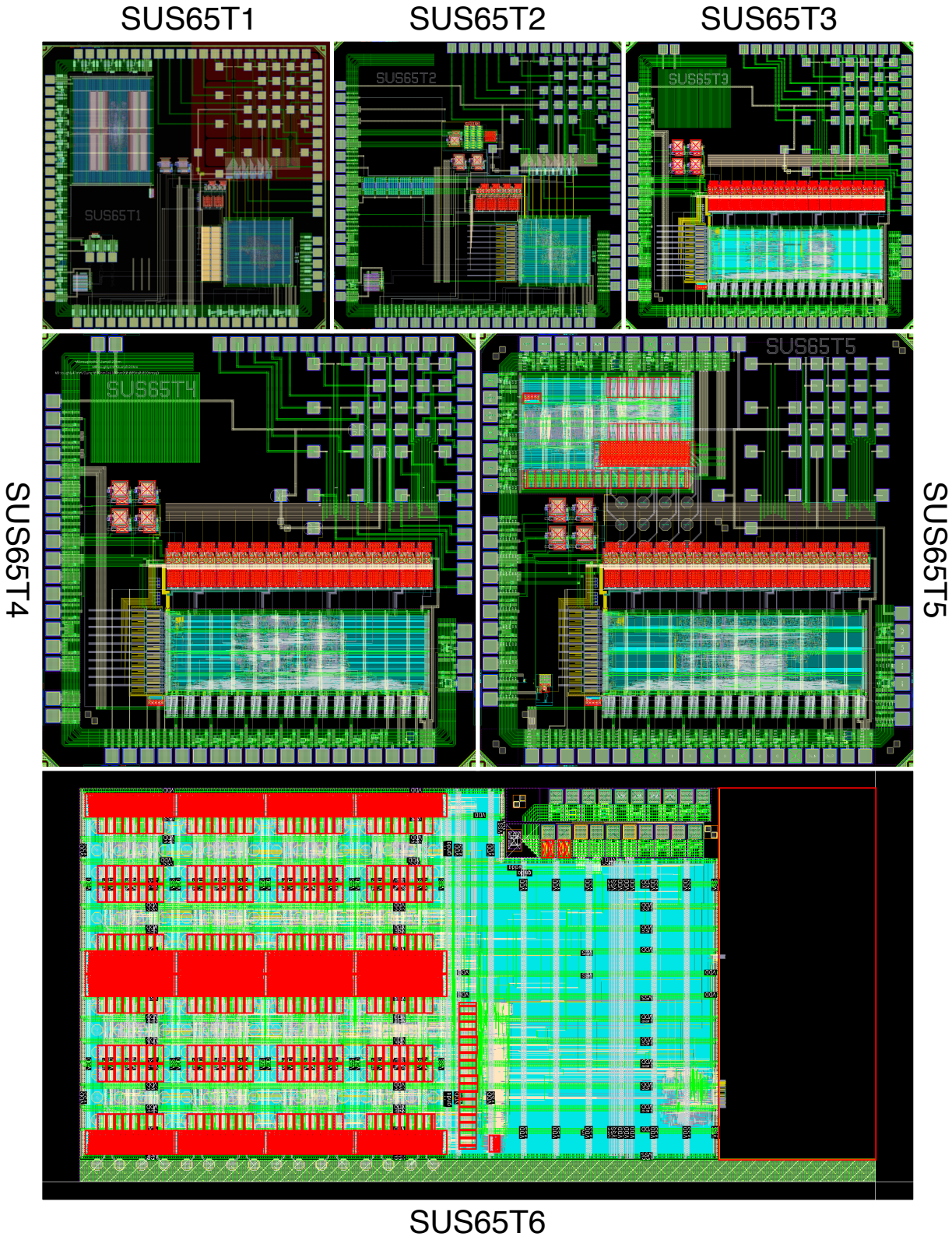


Figure 6.45: Layouts of chip iterations since the foundation of XIDer in 2018. Chip sizes are not to scale. SUS65T1-SUS65T5 all have the same size of $2 \times 2\,\mathrm{mm}^2$. SUS65T6 has a dimension of approximately $4 \times 2\,\mathrm{mm}^2$.

included circuit blocks had to be developed from scratch. The chip features two instance of the core analog front-end design with coarse and fine stages, transfer capacitances, charge pumps, the corresponding logic blocks as well as comparators. Visible in the top right corner of the corresponding figure, there is a pad matrix in preparation for the connection of a bump-bonded sensor both in 100 µm and 200 µm pixel pitch. Multiplexers allow connecting the front-ends to the desired input pixel.

On top, the ASIC includes a semi-custom synthesized digital control block with an early version of the adapted DSSC sequencer[32] for the global dynamic control of the front-ends. The digital block also contains a standard JTAG interface. This interface allows the slow control of said sequencer as well as 20 instances of 10-bit DACs[33] which are concerned with providing bias voltages and currents. In order to count the coarse and fine stage pumps, the control block contains two digital counters per front-end. For data readout, their contents are loaded into a simple output shift register at the end of the sequencer cycle. Along a serial data link, the contents of this shift register are sent out bit by bit. This simple data readout structure suffices for the very first prototype iteration. It is the predecessor to the more sophisticated telegram interface. Also, the design does not yet feature RAM cells.

The outer pad ring features 80 wire-bond pads with custom-designed CMOS and LVDS I/O drivers. 28 of these pads in the top-right corner are reserved for a possible wire-bond connection of a pixel matrix, which is supposed to be bump-bonded to another interposer PCB. The only purpose of this approach is to provide extra flexibility in the sensor connection since CdTe proves to be difficult to handle. However, the wire-bond pixel pads have never been used throughout this project. In addition, there are several other building blocks to the left side of the chip which are not associated with the XIDer project.

SUS65T1 had several purposes to fulfill. Most importantly, since it was the first the group's first TSMC65 design, the ASIC acted as a proof-of-concept for the correct set-up of the design environment and tools. At the same time, it was supposed to demonstrate the functionality of the chosen front-end concept on a basic level. And with a confirmation of functionality, first insights into the ASIC-sensor interconnection as well as sensor characterisation measurements were planned. While the general functionality of all the auxiliary blocks like the pad drivers, the sequencer, the JTAG interface and the DACs was confirmed, it turned out the SUS65T1 has a major problem. One of the bias DACs for charge pumps in the analog front-end is connected with the wrong polarity. Unfortunately, there is no way to fix this problem externally which is why the basic front-end functionality could not be verified.

SUS65T2

Only half a year after SUS65T1, the second iteration SUS65T2 was submitted for manufacturing in May 2019. The general structure remained the same. Alongside the fixed DAC connection, the chip featured additional test structures dedicated to the front-end and sensor characterisation. SUS65T2 allowed confirming the basic front-end functionality and provided insight into its counting linearity performance as well as necessary calibration steps. For more information, the interested reader is referred to [87].

Besides the front-end characterisation, SUS65T2 also gave access to sensor prototype characterisation. It allowed developing and evaluating a bump-bonding process for prototype ASIC-sensor interconnection (see 8.2) and gave the first insights into the performance

[32] See section 6.3.3.1
[33] see section 6.3.1

of ASIC-sensor assemblies. Apart from simple lab tests with LEDs and lasers, SUS65T2 has also been succesfully employed in the project's first on-site beamline tests at the ESRF. Section 8.3.1 presents one of these measurements. Further information can also be found in [7].

SUS65T3

With the insights gained from SUS65T2, XIDer's third readout ASIC iteration has been submitted in May 2020. SUS65T3 poses a significant upgrade in the direction of large scale integration. Instead of multiplexing the pixel pad matrix onto only a few front-ends, this ASIC features a one-to-one direct pixel-to-front-end connection for each pixel pad. Supporting either a 100 µm or 200 µm 4x4 pixel matrix, there are 16 front-ends which allow a parallel readout of all of the pixels at once. Besides, the front-end design has been optimised for better noise performance, decreased power consumption as well as improved charge pump linearity following the guidelines presented in the sections 6.2.1 and 6.2.3. Also, SUS65T3 is the first chip iteration to employ a fine stage which trades performance and speed for even lower power consumption. In addition, every channel now contains a 16-bit RAM storage with 256 words each. The implemented RAM cell is the initial iteration of the full-custom design presented in section 6.2.7.

In the digital domain, there has been a major redesign of the data handling. Instead of the simple shift register readout structure of SUS65T2, the global control block has been expanded with the telegram interface that controls the data flow into and out of the channel-wise RAM cells. Additionally, every channel on SUS65T3 features a local data merger block as described in section 6.2.6.

Unfortunately, just like one of its predecessors, SUS65T3 is subject to a design oversight. The LVDS input pads exhibit an undesired polarity inversion which causes the serial telegram input to be inverted. As a result, the ASIC behaved in unforeseen and unpredictable ways. In principle, this can easily be circumvented externally by inverting the telegram interface input. Due to the link's 8b/10b encoding, however, the inversion remained hidden long enough for a new chip iteration with improved debugging features to be submitted.. This is due to the fact, that the 8b/10b encoding's control words, like the sync and idle characters, are invariant to inversion, while data words are not. Additionally, inverted data words are still valid but they carry the wrong contents. And since the full-blown simulation of the whole chip used simplified simulation models for the LVDS pads that do not include the inversion, it passed by into submission unseen. This oversight has been found only after the submission of the next iteration. As a result, SUS65T3 has barely been used.

SUS65T4

SUS65T4 has been submitted in May 2021. It features no major changes compared to SUS65T3. Its purpose was to further investigate SUS65T3's unexpected behaviour via the addition of improved debugging capabilities in the digital domain. After the discovery of the inverted LVDS input pad, SUS65T4 became the flagship of characterisation measurements and replaced SUS65T2. Selected measurements can be found in the chapters 7 and 8. In addition, further results are published in [51].

SUS65T5

With the fifth readout ASIC iteration submitted in September 2021, the design made another significant step towards large scale integration. While conceptually the same as SUS65T4, the main upgrade of SUS65T5 lies in the improved and minimized front-end layout with additional shielding of important signal wiring. As described in section 6.1.4, this layout is built to fit in a 4x4 channel module that has the same area as the corresponding 100 µm-pitch 4x4 pixel matrix. It is designed in a stackable way, such that one can use it as a basis for large matrices.

Said 4x4 module is placed in the top left corner of the chip right underneath its corresponding bump-bond pads. For direct performance comparison, the old layout version of T4 was placed on the same chip. Both layout versions are completely independent and except for the substrate, they do not share a connection.

SUS65T6

Submitted in October 2022, SUS65T6 is the last chip iteration designed in this work. The design consists of a 256 (16x16) channel matrix assembled from SUS65T5's 4x4 core module. Digital-wise, the chip contains a few bug fixes compared to SUS65T5. Additionally, it uses a new Aurora protocol-based serializer IP that manages to operate the data output link at $14\,\mathrm{Gbit\,s^{-1}}$. In terms of analog design, this is the first ASIC iteration to introduce the comparator and charge pump fine-trim circuits as presented in the sections 6.2.2 and 6.2.3. Also, there have been a few minor layout changes to further prepare the design for large scale integration such as improved shielding to prevent crosstalk between the analog and the digital domain.

The chip submission itself is a collaboration with the STFC [80]. The depicted layout in figure 6.45 is only one half of the whole ASIC. To the top of SUS65T6, there is another (not depicted) implementation of a similar ASIC developed by the STFC. Due to the similarities of the designs and constraints, this shared submission is a first step towards merging both designs into a single collaboration. As with SUS65T5, both SUS65T6 and the STFC's readout ASIC design are independent and only share the substrate.

Due to the effort to design a combined test PCB for both the STFC and the XIDer project, there have been several delays in the design and manufacturing process of the characterisation set-up. Subsequently, SUS65T6 could not be tested before this work has been compiled. A corresponding test PCB with a mounted ASIC has just arrived by the time this work has been compiled. Its characterisation is currently on-going.

7 ASIC Characterisation

Besides the design, optimisation and simulation, ASIC characterisation is another large part of this work. In order to test the performance of manufactured chips, a test set-up had to be designed and assembled. Since the beginning of this project, said test set-up has gone through many different iterations all of which included the design of PCBs, firmware and software. While some of the presented measurements have been performed with earlier[1] iterations, this chapter focusses on introducing only the most recent one. Significant differences will be highlighted when necessary. After the initial set-up presentation, this chapter shows a few selected ASIC characterisation measurements. The selection verifies the following simulated properties of the analog front-end:

- Functionality of the pipelined structure with continuous analog-to-digital conversion.
- Photon counting linearity over a wide dynamic range.
- Robustness against high instantaneous input charges up to 200 equivalent 30 keV-photons.
- Front-end baseline noise equivalent to an input noise charge in the order of $375\,\mathrm{e}^-$.
- Transfer time low enough to record (at least) every second bunch in the 16-bunch mode at a photon rate of $1 \times 10^9\,\mathrm{ph\,pix^{-1}\,s^{-1}}$.

In addition, the readout electronics noise-induced photon counting error is evaluated. And at the end of this section, a measurement that utilizes the histogram readout (see 6.3.3.2) mode verifies the functionality of the digital control block and on-chip data management modules. Measurements with a mounted sensor are presented in chapter 8.

7.1 Measurement Set-Up

The latest test set-up iteration by the time this work has been compiled is depicted in figure 7.1. It features three PCBs:

- **Main Board:** Is supposed to act as the central measurement platform. It has been provided by the research group where it is used as a basis in many different projects. For further reference, it will be called the *PETA board*. The PCB hosts a Xilinx Artix 7 [88] FPGA for the transmission and reception of fast and time-constrained command and data signals. FTDI ICs form a USB-to-FPGA interface for JTAG configuration and data transmission via/to a connected PC. On top, the board features several universal test points which can be connected to FPGA outputs for monitoring.
- **ASIC Carrier:** ASIC-iteration-specific PCB. ASICs are glued onto and wired-bonded to this board. Except for a few test points for iteration-specific analog signal monitors, it is mainly concerned with wiring ASIC signals to the corresponding FPGA in- and outputs.

[1] And in some cases quite different

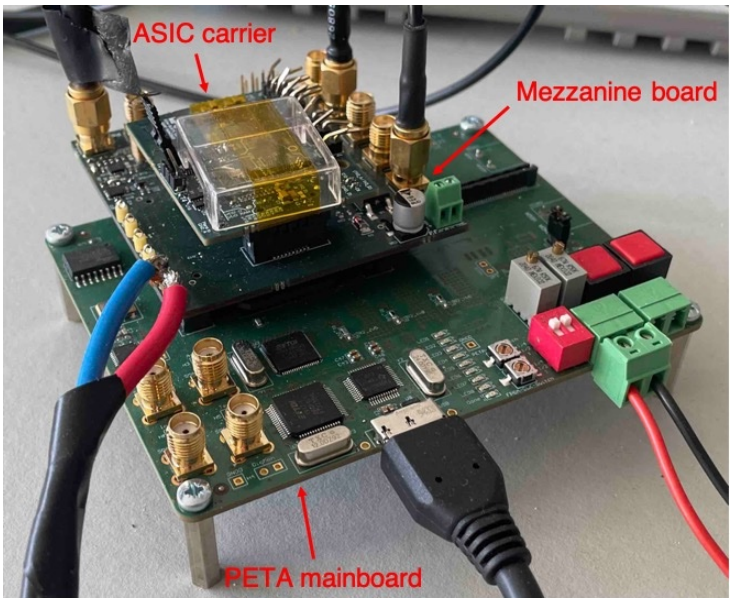


Figure 7.1: Photograph of the measurement set-up.

- **Mezzanine Adapter:** Adapter PCB between the ASIC carrier and the main board which remains unchanged throughout changing ASIC iterations. It implements universal functions specific to the XIDer project. For example, it includes voltage dividers for the ASIC supply voltages as well as SMA connectors for different analog and digital monitors provided by the ASIC. The most important of these monitors are the buffered output voltages of both stages of one of the on-chip front-ends as well as the display of digital signals like the charge pump control signals and sequencer tracks.

All of the universal features of the main and mezzanine boards remain unchanged, while the carrier boards can be adapted to features of new ASIC iterations. This modularized approach saves costs and effort.

Figure 7.2 shows a block diagram of the most important set-up structures. The FPGA on the PETA PCB is the core control unit for measurements. Written in Verilog, the implemented firmware utilizes an on-FPGA PLL which generates the clock tree. At the PLL input, there is a multiplexer to choose from two different input clocks. While one of them is provided externally by e.g. the synchrotron, the other is generated by a 622.08 MHz oscillator on the PETA PCB. In addition, the on-board oscillator's frequency can be divided by either 2 or 4 to provide more flexibility. As described in section 6.1.3, if the chosen input clock is generated by the synchrotron, the ASIC root clock has to be derived from the synchrotron clock with a multiplication factor of 5/4 or 5/2. This is performed by the PLL's FPGA. The clock resulting from this multiplication is then used as the root clock for the FPGA as well as the ASIC.

The color coding in the FPGA block indicates which of the implemented modules operates in which clock domain. One of these modules is a sequencer control unit which controls the point in time at which the RUN signal for the on-chip sequencer is sent. At the same time, it synchronizes the RUN signal to the fast system clock. Another module is the telegram control which is concerned with sending telegram commands to the ASIC. Besides the depicted 8b/10b encoder and the serializer, this module also includes a telegram assembler as well as a sequencer. While the assembler pieces together single telegrams following the protocol explained in section 6.3.3.2, the sequencer allows running

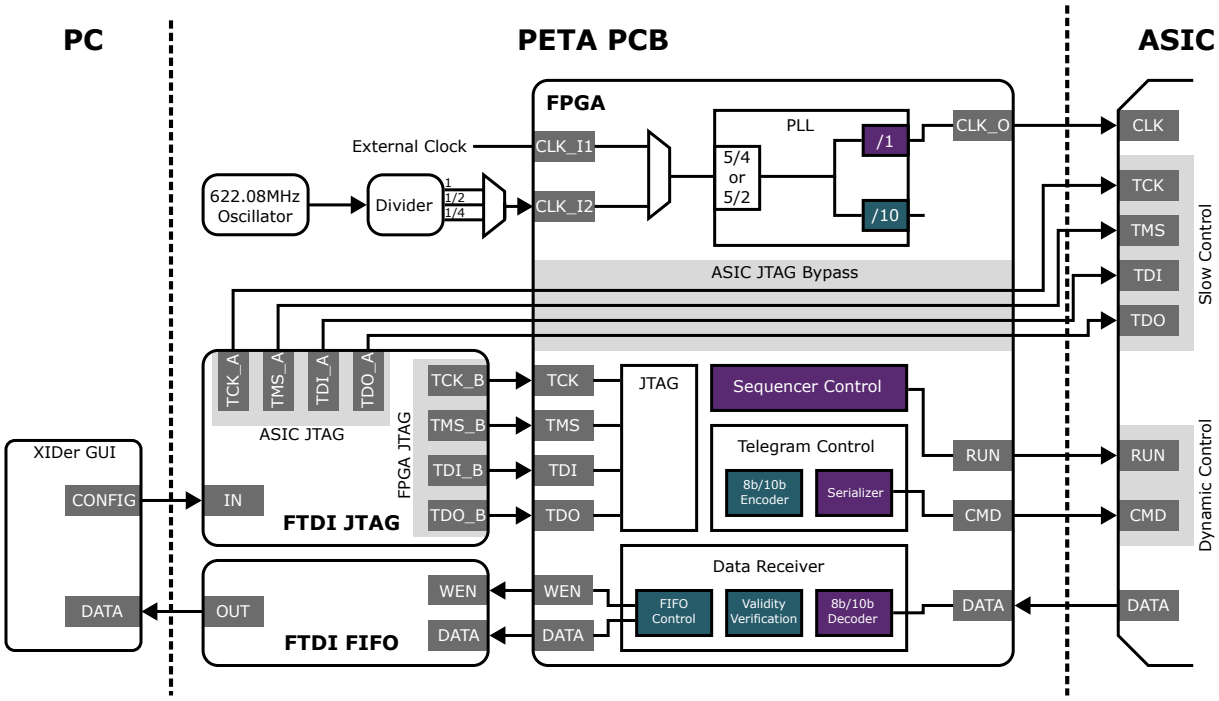


Figure 7.2: Block diagram of the measurement set-up.

through a set of pre-defined telegrams. Drawn at the bottom of the FPGA block, there is the data receiver. After decoding the ASIC's output data, it checks the contents for validity. When the data is deemed valid, it is transmitted to the FTDI FIFO on the PETA board.

The interconnection between the PC and the FPGA is implemented with the depicted FTDI ICs on the PETA PCB. In this way, both the ASIC and the FPGA can be programmed from the PC via JTAG by providing the JTAG FTDI IC with the address of the corresponding device to be programmed. Apart from the firmware bit file, the JTAG communication with the FPGA also contains control bits for the sequencer control, the telegram control as well as the data receiver. In addition to the set-up control, data that is stored in the FTDI FIFO IC by the FPGA can be read out by a Python command in the set-up software on the PC.

7.1.1 Software & GUI

All of the software employed in the set-up control is written in Python3 [89]. Its core element is a graphical user interface (GUI) which employs the model-view-controller (MVC) paradigm wherever possible. The GUI itself is written in PyQt5 [90] and depicted in figure 7.3. As shown, there are four tabs. The currently active one is the *Sequencer Tracks* tab which allows configuring the course of all the ASIC's global sequencer tracks. A display of their signal sequence to the right is rendered from the set configuration to the left.

Three of the tabs are dedicated to modules of the global digital control blocks on the ASIC. While the *Register Configuration* and *Sequencer Tracks* tabs are concerned with the ASIC's JTAG configuration, the *Telegram* tab allows programming the telegram sequence generated by the FPGA. Additionally, the GUI allows controlling which input clock to use and if the ASIC is supposed to be run in triggered or free-running-mode (not depicted). Also, settings can be stored in configuration files. This enables reusing desired configurations via the GUI's load function for future measurements. Apart from the ASIC

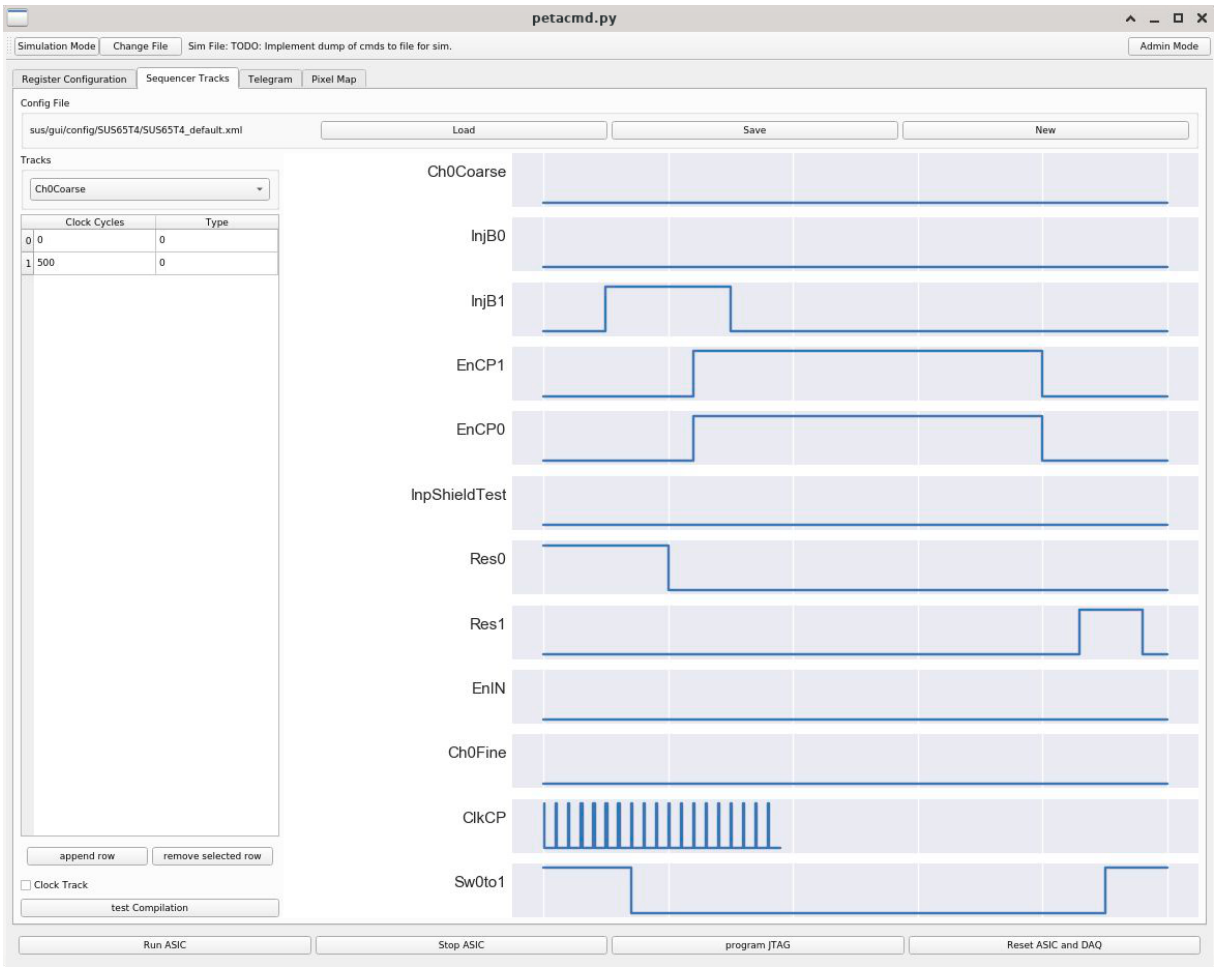


Figure 7.3: Illustration of the set-up control GUI at the example of the sequencer track configuration tab.

and FPGA configuration, the GUI also includes a live-display of the pixel matrix in the tab *Pixel Map*. This feature has been especially useful when aligning the set-up with the X-ray beam in actual beamline measurements. Section 8.3.1 showcases a few images of test measurements with a laser.

All of the displayed GUI buttons are linked to underlying functions which can be accessed with customly written Python scripts. With an implemented command prompt, this allows for quick prototype tests as well as sophisticated, repeatable measurements in a well-defined environment. In addition to the depicted functions, the GUI also includes underlying DAQ functions which store the ASIC output data in structured hdf5 files together with meta data like the time of the measurement or used configurations.

7.2 Selected Analog Measurements

The measurements presented here are supposed to give insight into the behaviour and performance of the analog front-end. They are meant to verify the simulations shown in section 6.5. In order to achieve this, a small set of the most important characterisation measurements has been selected. These include a basic, qualitative functional test as well as quantitative noise, linearity and charge transfer time measurements. The latter are performed to derive a maximum count rate that the analog front-end can achieve

depending on the chosen (sub)frame length. If not mentioned otherwise, the bias DACs are tuned such that the coarse and fine stages consume about 90 µW and 30 µW, respectively. This is achieved by setting the corresponding DACs to the nominal values which are derived from simulation. In reality, the exact biasses are expected to vary from chip to chip as well as from channel to channel due to manufacturing uncertainties. The size of this variation has not yet been measured.

7.2.1 Qualitative Integration Cycle Display

One of the very first questions is, whether the on-silicon front-end acts as expected and predicted by the concepts and simulations. This measurement is supposed to provide an answer in a qualitative way. For this reason, the front-end has not been calibrated thoroughly.

The measurement has been performed with T2, i.e. a chip implemented with the parameters shown in section 6.4 for the ESRF-specific chip iterations. With the help of its monitoring capabilities, the oscilloscope image in the top of figure 7.4 has been recorded. Below the image, the sequencer configuration is depicted which goes through the following steps:

1. Reset the first stage to prepare it for a (sub)frame.
2. Enable the coarse charge pump to execute the continuous conversion in the coarse stage.
3. Inject input charge with the test injection circuit.
4. Charge the transfer capacitor to initiate the residual charge transfer. This is achieved by first resetting the fine stage and then closing the Sw0to1 switch.
5. Reset the coarse stage to inject the charge from the coarse into the fine stage.
6. Enable the fine charge pump to execute the continuous conversion in the fine stage.

The measurement has been taken at a system frequency of 125 MHz, while the charge pump clock has reoccuring clock pulses with a frequency of 12.5 MHz.

The oscilloscope image shows the signal sequence of the coarse stage in pink, the fine stage in green and the output of the fine stage's charge pump logic in blue.[2] The depicted time interval starts with the reset of the coarse stage. At the end of the reset, there is a slight increase in the coarse stage's output voltage which restuls from a charge injection through the reset switch. As soon as the injection is triggered with the falling edge of the INJECT0 track, the output of the coarse stage rises and settles at a value corresponding to the injected charge. Since the charge pump logic is enabled, it starts generating control voltage pulses for the coarse stage charge pump (not depicted). The width and frequency of these pulses is defined by the ClkCP track. As a result, the charge pump injects well-defined packages into the coarse stage input which leads to a periodic decrease in the output voltage of the coarse stage. As soon as the voltage drops below the threshold, the charge pump stops pumping. Subsequently, the output voltage of the coarse stage remains at a residual voltage which is below its threshold voltage.

[2] Unfortunately, the digital monitoring capabilities do not allow a simultaneous display of the charge pump logic outputs of both the coarse and the fine stages.

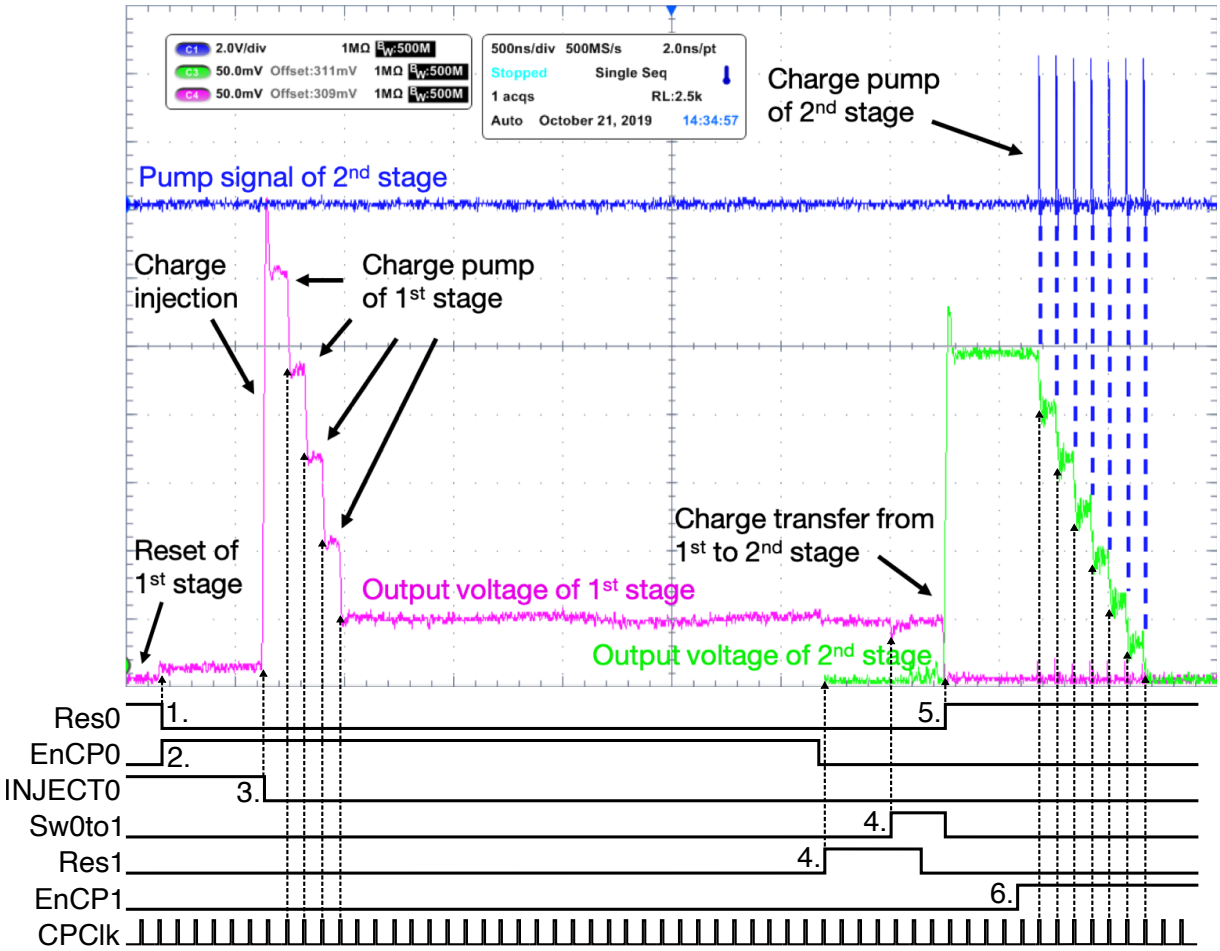


Figure 7.4: Measurement for a qualitative functionality test of the analog front-end of XIDer's readout ASIC. The top part shows an actual oscilloscope image with the buffered output of the coarse stage (purple) and of the fine stage (green) as well as the monitored output of the fine stage charge pump logic (blue). Underneath the oscilloscope image, the corresponding configuration of the global sequencer tracks is drawn for reference. Oscilloscope image taken from [87]. The terms 1^{st} and 2^{nd} *stage* denote the coarse and fine stages, respectively.

At the end of the coarse stage's continuous conversion, the fine stage is reset which is followed by closing the Sw0to1 switch. With this, the charging process of the transfer capacitor is initiated. The following reset of the coarse stage injects the amplified residual charge into the fine stage. As a result, the coarse stage output drops back to the reference voltage and the fine stage output rises. After completing the charge transfer, the fine stage performs its continuous conversion. The charge pump enable pulses in blue align with the periodic decrease of the fine stage's output voltage. As soon as the output voltage has decreased below the fine stage threshold, the fine stage stops pumping and the conversion is completed. This integration cycle shows a close resemblance the simulation in section 6.5.1. As a result, it confirms the basic qualitative functionality of many involved modules, such as

- the I/O pads and monitoring buffers,
- the global digital control including the JTAG interface, the bias DACs, and the sequencer,

- the analog front-end stages with their comparators, charge pump logic units, charge pumps,
- the charge transfer
- and the test charge injection circuit.

As a side note: It may seem like the fine stage output voltage does not correspond to 8 times the coarse stage output voltage. However, opening the Sw0to1-switch results in an additional negative charge injection into the fine stage input. Subsequently, the effective baseline of the fine stage is shifted by this negative input voltage. In an actual measurement, this effect is mitigated with a proper comparator threshold calibration that incorporates the baseline shift. Also, subsequent chip iterations after T2 include optimisations to the transfer switch to reduce the size of the injected charge.

7.2.2 Front-End Linearity

The main task of XIDer's channel is counting the amount of photons that hit a sensor pixel. In order to do this, it needs to convert the charge generated by incident photons of a fixed energy in the pixel sensor to a digital photon count number. In this conversion, the front-end has to provide a linear input-charge-to-photon-count relation. This measurement is supposed to verify this linearity for the most extreme case the ESRF has to offer. In the 16-bunch mode, large amounts of charge are injected into the front-end in a single pulse. For all the other modes, the constraints on the front-end are much more relaxed as instantaneous charges[3] are lower and (sub)frames are usually longer.

The measurement is performed with a single front-end of T4 and uses the integrated test charge injection circuit (see 6.2.5). The injection circuit allows injecting a charge Q_{inj} of known size into the front-end input. After charge injection, the front-end under test converts the input charge to a digital count N_c which is then read out via the ASIC's serial data output link. A sweep through the available DAC range of the injection circuit should result in a linear proportionality of N_c to the set DAC value. The observed front-end has been roughly calibrated via measuring the buffered output voltage of the coarse and fine stages with the help of an oscilloscope. By measuring the size of the voltage steps induced by the charge packages, the package size has been calibrated to generate steps of the expected size.

For every injection DAC value, the measurement has been repeated 10000 times. In every measurement, the front-end is driven through the same cycle. The sequencer starts with a coarse stage reset, enables the coarse stage charge pump for the coarse continuous conversion, transfers the residual charge to the fine stage and enables the fine stage charge pump for the fine continuous conversion. At the end of the fine stage's conversion, the final coarse and fine stage counter values are added and read out via the serial output data link. The injection circuit injects the charge in a very short time interval[4] right after the reset phase of the coarse stage. Subsequently, this measurement directly corresponds to the counting linearity simulation in section 6.5.3.

Figure 7.5 illustrates the result of this measurement. The upper plot shows N_c on the y-axis vs. the input charge Q_{inj} on the x-axis. For clarity, Q_{inj} is given in units of charge

[3] As explained in 6.5, the term *instantaneous charge* refers to charges that are injected in time intervals which are shorter than one period of the charge pump clock.

[4] In this context, *very short* corresponds to time intervals which are smaller than the period of the ClkCP sequencer track

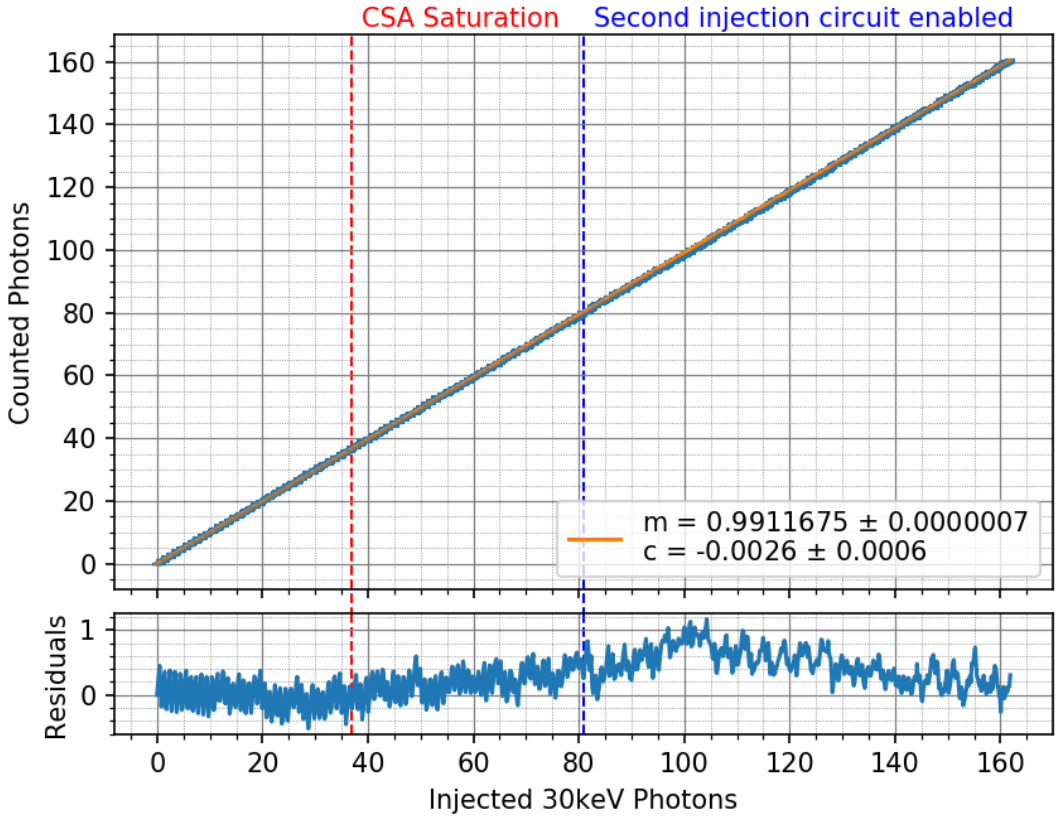


Figure 7.5: Front-end linearity measurement. The x-axis is given in units of 30 keV photons which would generate the equivalent amount of charge in a CdTe sensor. The y-axis of the upper plot shows the average amount of photons counted by the front-end in a set of 10000 measurements per injection setting. Error-bars indicating the standard deviations of the counted values are included. However, they prove to be too small to be visible in the chosen scale. Graph taken from [91] and modified.

equivalent to the charge that is generated by a single 30 keV-photon in a CdTe sensor. The corresponding values have been calculated from the injection voltage DAC settings. A setting that injects a charge equivalent to N_{ph} photons with an energy of E_{ph} is given via

$$DAC\_INJECT_{N,E_{ph}} = N_{ph}\frac{1024 E_{ph} q_e}{\epsilon_{CdTe} C_{inj} I_{max} R_{DAC}}, \tag{7.1}$$

where q_e is the elementary charge and $\epsilon_{CdTe} = 4.43\,\text{eV}$ is the average energy needed to generate an electron-hole pair in CdTe. $I_{max} = 256\,\mu\text{A}$ and $R_{DAC} = 4\,\text{k}\Omega$ are the maximum current, the DAC can drive, and the resistance that is used to convert the DAC current to a voltage. Obviously, this conversion neglects manufacturing uncertainties of the DACs and injection capacitors. For the investigated front-end, however, the coarse stage output voltage has been monitored with an oscilloscope for a few example cases. In these test cases, no significant systematic deviations of the voltage steps induced by the charge injection to the expected values have been observed.

In order to avoid the non-linearity of the p-MOSFET current source in the peripheral injection DACs (see sections 6.3.1 and 6.2.5) at high output currents, this measurement

uses both instances of the charge injection circuit. This is indicated by the dashed blue line in the plot. The first half of the x-axis is covered by an injection voltage sweep of the first circuit instance until about half of the maximum voltage. In the second half, the first instance is kept at this value and the bias voltage of the second injection instance is swept.

The red dashed line indicates the charge amount at which the CSA in the front-end's coarse stage is expected to saturate.[5] The corresponding value can been calculated from the CSA's feedback capacitor C_{fb0}, and the the dynamic output voltage range of the CSA ΔV_{dyn}:

$$Q_{sat} = C_{fb0} \Delta V_{dyn}. \tag{7.2}$$

This yields an equivalent amount of roughly 37 incident 30 keV-photons. This value has been confirmed via a beamline measurement with actual photons. For the sake of brevity, the measurement is not included in this work.

In order to demonstrate the front-end's counting linearity throughout the whole measurement range, a linear function following the equation

$$f(x) = mx + c \tag{7.3}$$

has been fitted to the data, where x is the input charge, m is the slope and c is the y-intercept. And in order to exclude any non-linear effects from the coarse stage CSA saturation, only the data points below an input charge equivalent to 37 30 keV-photons have been used for the linear fit. The lower plot shows the residuals of the data to the linear fit.

As presented in the plot, the average amount of counted photons by the front-end shows a linear behaviour up to the maximum value of the measurement range of roughly 162 incident 30 keV-photons. With the depicted fit values for m and c, the data points exhibit a maximum systematical deviation of roughly 1 photon at a charge equivalent to 100 incident 30 keV-photons. An important point to mention is that this systematical deviation not only inlcudes the influence of the analog front-end but also the injection circuits. Especially at the transition from the first to the second charge injection circuit, non-linearities are expected. Remarkably, figure 7.5 shows the raw data without any correction for mismatches between the two instances. And as depicted, there are no obvious sharp bends at the transition. Arguably, the measured deviation of 1 ADU at roughly 100 equivalent 30 keV photons might be caused be a mismatch of the two injection circuit instances. For a clear statement, however, further studies are necessary.

In addition, figure 7.6 shows an example histogram for the counted photons at 140 injected 30 keV-photons. As depicted, the standard deviation is at a level of 0.13 30 keV-photons. Hinting at the statistical counting error exhibited by the front-end, this will be more thoroughly discussed in the second part of the following noise measurements.
These results allow three main conclusions:

- For this measurement, the by-hand calibration achieved a remarkable precision.
- In a charge range up to roughly 162 30 keV-photons per (sub)frame, the front-end has been demonstrated to act linearly with a maximum deviation of about 1 photon from the linear trend.
- The front-end can handle instantaneous input charges which are significantly beyond the saturation limit of the coarse stage CSA. As stated in section 6.5.2, the requirement for the maximum instantaneous input charge is equivalent 200 30 keV-photons.

[5] See section 6.5.2 for a detailed explanation of the significance of this point.

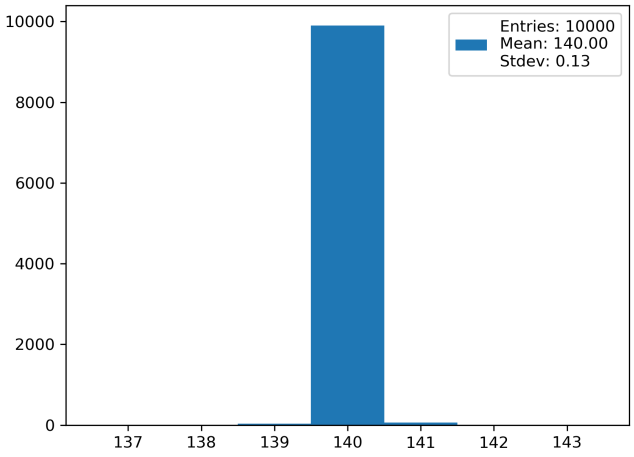


Figure 7.6: Example histogram of the amount of counted photons at an input charge of 140 30 keV-photons.

In reality, however, most of the measurements are expected to operate at significantly lower instantaneous charges.

With these conclusions, the front-end's counting linearity is in agreement with the simulations and performs within the constraints set by the conditions at the ESRF. A larger charge injection range would help to confirm that the counting linearity is maintained up to the requirement of 200 incident 30 keV-photons.

The main contributor to this linearity even beyond the saturation of the coarse stage CSA is the charge pump. The charge packages it generates have to be independent on the input voltage of the CSA. As described in section 6.2.3, this has been achieved by cascoding the charge pump's current-source transistor and providing it with a large length. Said cascode prevents charge injection induced by parasitic capacitances between the PUMP and DUMP states and mitigates the current-source transistor's early effect.

7.2.3 Front-End Electronics Noise

Just like the noise simulation in section 6.5.6, this measurement considers two different noise quantities which are important in different measurement scenarios:

1. Baseline noise and dark count rate

2. Counting error induced by readout electronics noise

Dark counts denote the erroneous detection of photons, when the sensor is not illuminated. This erroneous detection can be triggered by statistical fluctuations, e.g. readout electronics noise. In this context, the *dark count rate* is a measure for how often the detector erroneously counts a fake/dark photon in a given time interval. This quantity is mostly important for measurements in which only a few or even no photons at all have been absorbed by a pixel in a (sub)frame. Examples would be a pixel located in a minimum of a diffraction pattern where the detector's single photon sensitivity is most important. In contrast, the *counting error* considers the statistical fluctuation of counted photons at a fixed amount of incident photons.

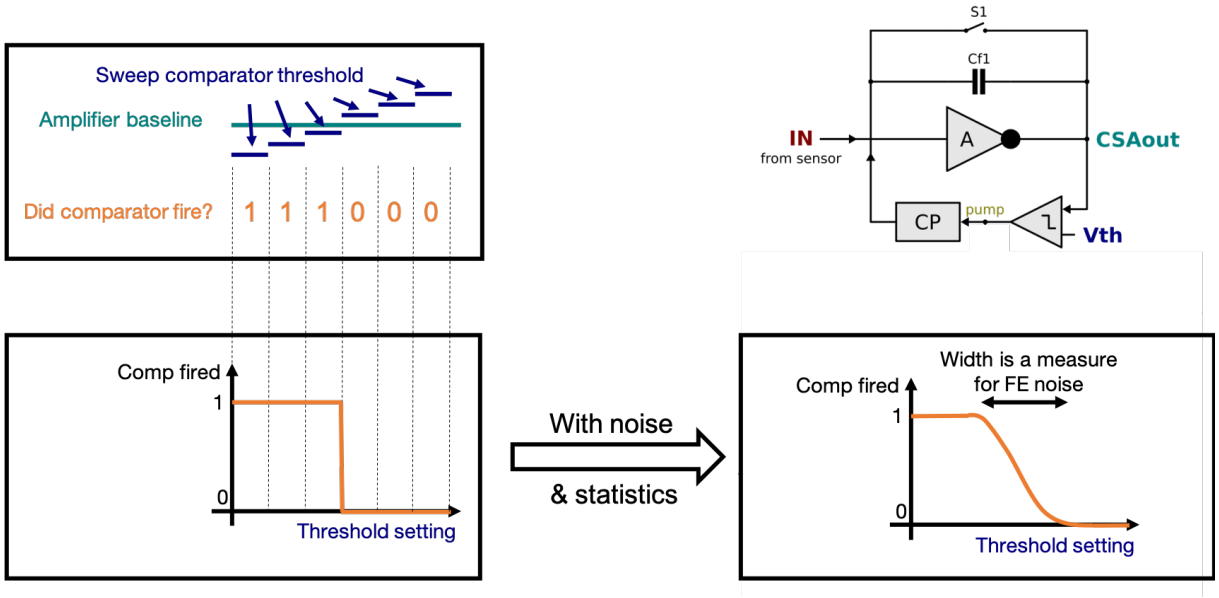


Figure 7.7: Comparator sweep procedure to measure the combined output voltage noise of the coarse and fine stages [92].

Both of these quantities are affected by different noise sources in the detector where a major distinction between sensor- and readout ASIC-related effects can be made. This section exclusively discusses the ASIC-related effects.[6]

Baseline Noise & Dark Count Rate

As discussed in section 6.5.6, the dark count rate induced by electronics noise is mainly caused by the output voltage noise of both CSA stages.[7] This is due to the fact that only if the statistical variation of the CSA output voltages is high enough to trigger the comparators, the charge pump is activated and a charge package is counted. Since this is the most common use case, this measurement assumes a charge package size equivalent to a single photon such that a single charge pump trigger corresponds to one dark photon.

In order to measure the size of the output voltage fluctuation, a comparator threshold sweep is performed. This method is depicted in figure 7.7. In each step of the sweep, the comparator threshold is set to a different voltage, increasing from low to high values. As long as the threshold voltage is below the CSA output voltage, the comparator output is active. Vice versa, the comparator output drops to ground as soon as the threshold is above the CSA output voltage. Measuring the comparator output repeatedly for each threshold voltage thus results in the depicted S-curve. With no noise at all, this S-curve is expected to show a sharp, sudden drop between two threshold voltage settings around the amplifier baseline. In the real world case, however, where both the CSA output voltage as well as the sampling process of the comparator are subject to noise, the sharp drop transitions into a smooth S-like shape. In this context, the curve can be understood as a probability that the comparator will trigger for a given threshold voltage. And the width of the transition from a probability of 1 to a probability of 0 is a measure for the present noise in the circuit.

[6] Since this section is only about noise generated by the readout electronics, the Poissonian nature of photon counting statistics are excluded in this context.

[7] Noise in the triggering process of the comparators also has an effect, but has been found to be negligible against the CSA contributions.

With the assumption of a Gaussian-like noise distribution, such a behaviour can be described by the error function. Subsequently, the function

$$y(x, \mu, \sigma) = \frac{1}{2}\left(1 - erf\left(\frac{x-\mu}{\sigma\sqrt{2}}\right)\right) \tag{7.4}$$

is fitted to the experimental data where y is the comparator trigger probability, x is the threshold voltage, μ is the amplifier baseline and σ is the standard deviation of the measured noise.
The actual measurement cycle to implement the threshold sweep works as follows:

1. No charge is injected into the front-end.
2. Reset the coarse stage, then open its reset switch.
3. Initiate the charge transfer by charging the transfer capacitor with the coarse stage's noisy output voltage.
4. Transfer the noisy coarse stage output voltage to the fine stage.
5. Read out the fine stage comparator output in a time window of a single period of the fine stage's charge pump clock.
6. Repeat the same procedure 10000 times for each fine stage comparator threshold voltage.

This results in measuring both the noise performance of the coarse and the fine stage CSAs as well as the fine stage comparator, such that the total measured noise in the fine stage is given as

$$\sigma^2_{tot,v,f} = A_C^2\sigma^2_{CSA,c} + \sigma^2_{CSA,f} + \sigma^2_{C,f} \tag{7.5}$$

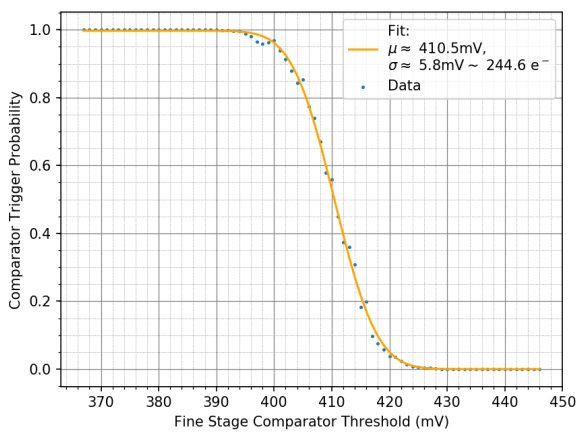
where A_C is the charge transfer gain and $\sigma_{CSA,c/f}$ and $\sigma_{C,f}$ are the noise contributions of the CSA and comparator in the coarse (c) and fine (f) stages, respectively.

The result of such a measurement is depicted in figure 7.8a. It has been performed with a single front-end of a T5 ASIC with no extra input capacitance. Subsequently, the front-end's input capacitance is dominated by that of the coarse stage amplifier. While the blue data points show the average of 10000 measurements for each threshold value, the orange curve shows a fit of the function 7.4 to the data. The extracted amplifier baseline μ and the standard deviation σ have been scaled from DAC values to corresponding voltages where a DAC value corresponds to 1 mV. In addition, the noise is also given in the equivalent input referred noise charge in units of electrons. The corresponding calculation is performed via $\sigma_{tot,v,f}C_{fb1}/(A_C q_e)$ in which $\sigma_{tot,v,f}$ is the measured noise in the fine stage in volts.[8] A_C is the transfer charge gain, C_{fb1} is the fine stage feedback capacitor and q_e is the elementary charge. As demonstrated, the measured noise is at an equivalent input noise charge of $(242.6 \pm 0.3)\,\mathrm{e}^-$ for the combined contributions of the coarse and fine stage CSAs and the fine stage comparator.

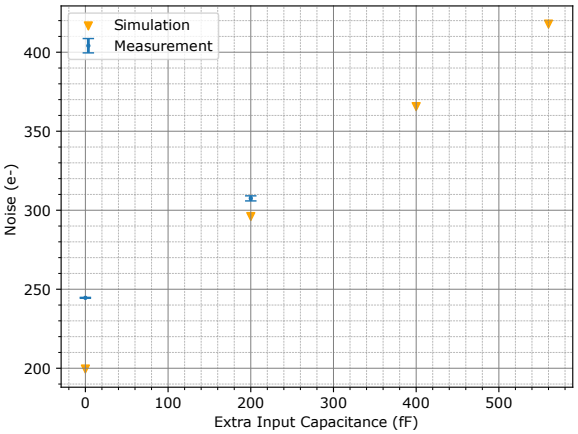
With the optional on-chip input capacitance C_{add0}[9], the noise performance in relation to the input capacitance can be measured. Figure 7.8b shows a plot of the noise extracted

[8] In order to refer this value to the front-end input, it is first transferred to the equivalent fine stage input charge $\sigma_{tot,v,f}C_{fb1}/q_e$. In the end, it has to be converted to the equivlant coarse stage input charge with a division by the coarse-to-fine charge gain factor A_C.

[9] see figure 6.36 in section 6.5



(a) S-curve for no extra input capacitance. Function 7.4 has been fitted to the data. The resulting parameters are: $\mu = (410.471 \pm 0.004)\,\mathrm{mV}$, $\sigma = (244.6 \pm 0.3)\,\mathrm{e^-}$



(b) Measurement with two different values of input capacitors in comparison with the simulated noise in section 6.5.6.

Figure 7.8: Comparator threshold sweep measurement to determine noise performance of the analog front-end including the contributions of the coarse stage CSA, the fine stage CSA and the fine stage comparator. In the right plot, *extra input capacitance* denotes the additional capacitance on top of the parasitic input capacitance of the amplifier as well as stray capacitance on the input line. The measurement for 200 fF has been performed with the on-chip capacitance C_{add0} (see figure 6.36 in section 6.5)

.

from comparator threshold sweeps in the fine stage for no extra input capacitance as well as 200 fF. It also compares these values to the simulation performed in section 6.5.6. As demonstrated, the measured noise lies in the same order of magnitude as the simulated values. Out of the two data points, the one for no extra input capacitance shows the largest deviation with about 45 $\mathrm{e^-}$, i.e. roughly 20 % deviation. The size of the measured values is given as $(242.6 \pm 0.3)\,\mathrm{e^-}$ and $(307.5 \pm 1.6)\,\mathrm{e^-}$.

As referenced in section 6.5.6, for an ENC of 375 $\mathrm{e^-}$, a dark count rate in the order of $1\,\mathrm{ph\,h^{-1}\,pix^{-1}}$ is expected at photon energies of 20 keV and (sub)frame lengths in the range of 1 µs to 10 µs [8]. This dark count rate has been deemed acceptable. Subsequently, for the presented measurement, the isolated front-end fulfills the project requirements. In addition, the dark count rate depends on the value of the fine comparator threshold. Usually, it is tuned to a voltage corresponding to charge of a half of an equivalent incident photon. Subsequently, if the photon energy increases, the fine comparator threshold does as well. As a result, the dark count rate decreases with higher energies. For this reason, the dark count rate is expected to be even lower than $1\,\mathrm{ph\,h^{-1}\,pix^{-1}}$ in XIDer's energy range of 30 keV to 100 keV.

In order to provide another scale for the measured CSA output noise: A single absorbed photon with an energy of 30 keV generates roughly 6800 electron-hole pairs in a CdTe sensor. Subsequently, at the lowest expected input energy, the signal-to-noise ratio of the tested front-end is given as roughly 22 for an input capacitance of 200 fF.

Unfortunately, with only two data points, it is not yet possible to confirm the linear relation between the noise performance and the input capacitance. Further measurements have to be performed. In addition, the same noise measurements also have to be repeated with connected sensor pixels. In the currently available assemblies, T4 is used which

exhibits pads with unnecessarily high input capacitances. Future assemblies with T6 will provide more insight.

Noise-Induced Counting Error

Besides the dark count rate, noise of the readout electronics leads to statistical fluctuations in the amount of counted photons in individual measurements. While the CSAs and the comparator contribute in the way discussed above, the charge pumps' contributions are related to the statistical fluctuations of their charge package sizes. Their influence is expected to scale with the amount of applied charge packages $N_{c/f}$ in the coarse (c) and fine (f) stages. Subsequently, in measurements with no applied charge package, i.e. no counted photon, the charge pumps contribute no noise. In contrast, in measurements with high photon counts, the charge pumps are anticipated to be the dominating source for statistical counting errors. The expected proportionality of their noise contribution is given as $\sigma_{CP,c/f} \propto \sqrt{N_{c/f}}\sigma_{CP,single,c/f}$ where $\sigma_{CP,single,c/f}$ is the fluctuation of a single coarse or fine charge package. As before, the noise is assumed to be Gaussian distributed.

The actual size of the statistical fluctuation in the counting process can be extracted from the counting linearity measurement executed in the previous subsection 7.2.2. For this purpose, the following steps have been performed on the previously presented data plotted in figure 7.5: First of all, the DAC settings which correspond to an injected charge equivalent to the amount of integer 30 keV photons are identified. For each of these settings, a histogram is plotted as depicted in figure 7.6 at the example of 140 counted photons. In the depicted case, almost all of the 10000 measurements performed with the same injection DAC setting are in the centered bin for 140 counts. Only a small fraction is located in the neighbouring bins for 139 and 141 counts. Then, for each of the histograms the standard deviation is extracted to gain a measure for the size of the statistical variation. Arguably, looking at the histogram for the example case, the standard deviation might not be the optimal measure because of the coarse binning. However, it can still provide a tendency for the observed statistical variation. As the last step, the extracted standard deviation for each of the selected DAC settings is plotted vs. the amount of injected equivalent 30 keV photons. This is depicted in figure 7.9.

Up to an amount of 45 injected equivalent 30 keV photons, the measurement shows a standard deviation of 0 photons for almost every setting. With the exception of the measurement for 20 and 28 counted photons, the front-end has reliably counted the same amount of injected photons 10000 times for each setting. It is important to note that this does not mean that there are no variations in the charge pump package sizes. Instead, the variation is low enough to not be visible in the granularity provided by the front-end, i.e. 30 keV photons with the calibration used for this measurement. At injected charges above 45 equivalent 30 keV photons, the standard deviation starts to increase. In these cases, the amount of counted photons fluctuates. And as expected, the size of the fluctuation increases with the amount of counted photons, i.e. with the amount of pumps the front-end has to perform.

The cause for the higher fluctuations at 20 and 28 equivalent injected photons is currently unknown. A possible reason could be that the injected charge has not been mapped correctly onto an integer number of equivalent photons with regard to the front-end calibration.

Because of the fact that this measurement has been performed with the front-end's internal charge injection circuit, it also includes the statistical variation of the injection. Since the variation of the injected charge is currently unknown, this measurement does

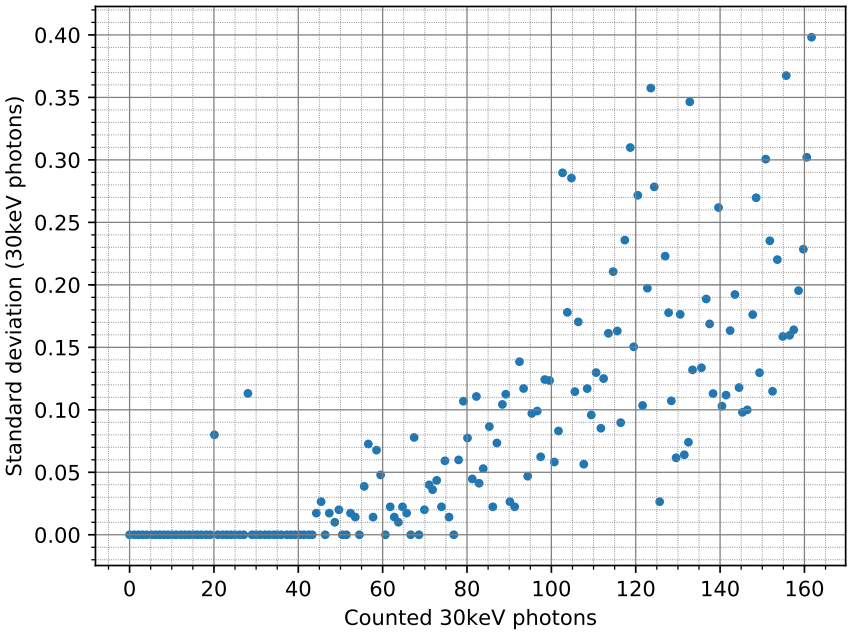


Figure 7.9: Measured standard deviation of counted 30 keVphotons vs. the amount of injected equivalent 30 keV photons

not allow a clear statement, whether the observed photon count fluctuation is caused by the injection circuit or the front-end. In any case, even with the injection circuit included, the maximum measured counting standard deviation lies below 0.4 30 keV photons up to a total number of 162 counted photons. With this, the counting error in an individual measurement introduced by electronics noise can be neglected vs. error sources like the Poissonian nature of photon counting statistics.

The main contributors to this remarkably low statistical counting variation are the well-defined charge pump packages. Their low noise contribution has been achieved by choosing long current source transistors (M_1 in figure 6.22, section 6.2.3).

Obviously, in order to make a clear statement of the actual detector performance, these measurements have to be repeated with an ASIC-sensor assembly and an actual X-ray source. Results of such measurements can be found in [93].

7.2.4 Coarse-To-Fine Charge Transfer Time

As described in section 6.5.4, the limiting factor to operate the front-end at a photon rate of $1 \times 10^9\,\mathrm{ph\,pix^{-1}\,s^{-1}}$ in the 16-bunch mode is the charge transfer time. As stated there, the total charge transfer time is given by $T_{tran} = T_{charge} + T_{res0}$ and has to be lower than or equal to 70 ns. In this context, T_{charge} is the time needed to charge the large transfer capacitor $C_{tran} = 432\,\mathrm{fF}$ and dominates the sum. T_{res0} is the time needed for the coarse stage reset.

The measurement presented here, is supposed to determine T_{charge} as well as show the effect the coarse stage's CSA bandwidth on T_{charge}. It has been performed with a T5 ASIC following the procedure:

1. Reset the coarse stage CSA, then disable the reset.

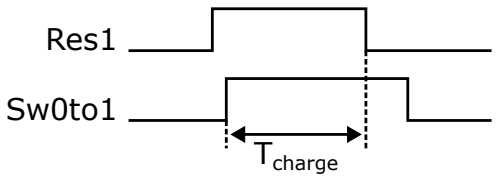


Figure 7.10: Illustration of the charging time T_{charge} for the transfer capacitor C_{tran} by means of the involved sequencer tracks Sw0to1 and Res1.

2. Disable the coarse stage charge pump.
3. Inject a charge into the front-end with the on-chip test charge integration circuit.
4. Transfer the charge to the fine stage.
5. Enable the fine stage charge pump and convert the injected charge into a digital value.
6. Read out the digital value.
7. Repeat the same measurement with the same input charge but different values of T_{charge}, i.e. transfer charge time windows.

Instead of using the typical charge package equivalent to a single 30 keV-photon, the fine stage charge pump package has been roughly calibrated to a charge equivalent to a 15 keV-photon. The reason for this is an increased sensitivity to changes in the transferred charge. The injected charge is equivalent to roughly 16 15 keV-photon.

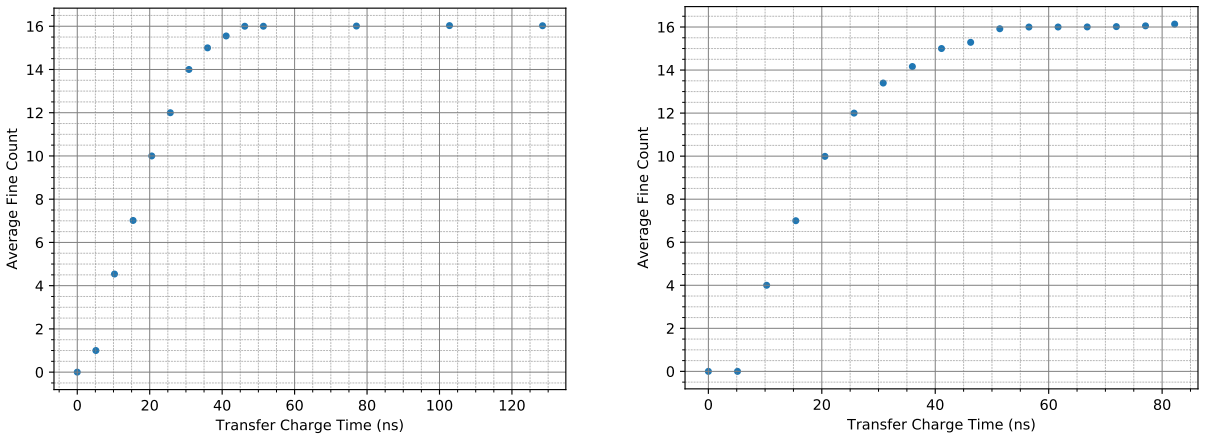
The size of T_{charge} can be manipulated with the sequencer cycle. It is given as the time between the rising edge of Sw0to1 and the falling edge of Res1 as depicted in figure 7.10. By moving the former closer to the latter, T_{charge} is reduced.

Figure 7.11a shows the result of such a measurement for varying sizes of T_{charge} with no additional input capacitance. It illustrates the amount of counted photons in the fine stage after the charge transfer process. Each data point shows the average of 10000 measurements for the same T_{charge} setting. The measurement has been taken at a system frequency of roughly 194 MHz which allows T_{charge} to be tunable with a granularity of roughly 5.2 ns.

The plateau at larger transfer times indicates the state in which T_{charge} has been long enough to fully charge C_{tran}. With a count of 16 photons, this value fits the expectation. At smaller values of T_{charge}, the expected drop of the fine stage count is visible. In these cases, T_{charge} has been too short to fully charge C_{tran}. Said drop is visible at charging times below $T_{charge,min} \approx 47$ ns in the depicted case.

Figure 7.11b shows the same measurement with $C_{add0} = 200$ fF connected to the front-end input node. As expected from the simulations in 6.5.4 as well as equation 6.27 in section 6.2.1.4, the higher input capacitance slows down the charge transfer process. Instead of the previous 47 ns, the fine stage count now starts dropping for T_{charge} less than ≈ 57 ns. Subsequently, the measurement confirms that a higher input capacitance increases the charge transfer time.

Figure 7.12 shows a comparison of these two measurements with the simulations presented in section 6.5.4. For the errors of the measurements, half a step size of the timing granularity has been assumed. Due to the digital counting and time step granularity of the measurement, a 1-to-1 comparison to the simulation has to be taken with caution,



(a) No extra capacitance at the front-end input.

(b) Extra input capacitance of 200 fF at the front-end input via the connection of C_{add0} (see figure 6.36 in section 6.5).

Figure 7.11: Measurement of the transferred charge vs. the transfer capacitor charging time. The y-axis shows the fine stage count which is roughly calibrated to 15 keV-photons. For each measurement, a charge equivalent to 16 15 keV-photons has been injected.

though. Still, both simulation and measurement lie in the same order of magnitude, with with a deviation of roughly 30 % and 10 %.

This measurement shows that the time the front-end needs for the charging process of the transfer capacitor is in the order of ≈ 57 ns with an input capacitance of 200 fF. By adding the necessary coarse stage reset with $T_{res0} \approx 20$ ns on top, the total transfer time is given by at least $T_{tran,meas} \approx 77\,\text{ns} > 70\,\text{ns}$. Judging from equation 6.52, this leaves the coarse stage with an active continuous conversion time of $T_{act,meas} \approx 98$ ns. Due to the planned maximum charge pump frequency 200 MHz, the active time can only be an integer multiple of 5 ns. Subsequently, $T_{act,meas,200\,\text{MHz}} = 95$ ns. Comparing this to the requirements of $T_{act,min} = 105$ ns[10] to achieve a count rate of $1 \times 10^9\,\text{ph}\,\text{s}^{-1}$ in the 16-bunch mode yields the ratio $T_{act,meas,200\,\text{MHz}}/T_{act,min} = 0.9$. As a result, the measured transfer time is expected to enable recording the 16-bunch mode with a reduced photon rate of roughly $(0.90 \pm 0.05) \times 10^9\,\text{ph}\,\text{pix}^{-1}\,\text{s}^{-1}$. Here, an error of one charge pump clock period has been assumed. This allows concluding that the front-end is close to reaching the requirement of $1 \times 10^9\,\text{ph}\,\text{pix}^{-1}\,\text{s}^{-1}$ in the most challenging bunch mode. And it confirms that the front-end is able to record every second bunch at an additional input capacitance of up to 200 fF which is what this measurement was supposed to verify. At the same time, a (sub)frame length above 185 ns would increase the front-end's active time by another 10 ns to reach the goal of 105 ns. Subsequently, expected from this measurement, the front-end can reach a count rate of $1 \times 10^9\,\text{ph}\,\text{pix}^{-1}\,\text{s}^{-1}$ at a (sub)frame length of at least 185 ns. While these conclusions are true for an input capacitance of 200 fF, it does not provide a clear statement for the actual detector where the front-end input capacitance is not yet known. In addition, the actual upper limit for the photon count rate in the 16-bunch mode has to be verified in an actual count rate measurement.

[10] see section 6.5.4

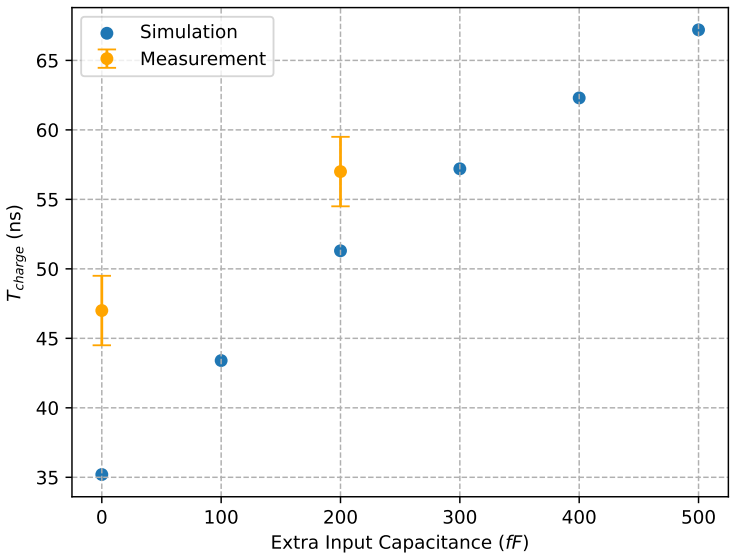


Figure 7.12: Comparison of the measured transfer capacitor charging time with the simulation in section 6.5 for different input capacitor values.

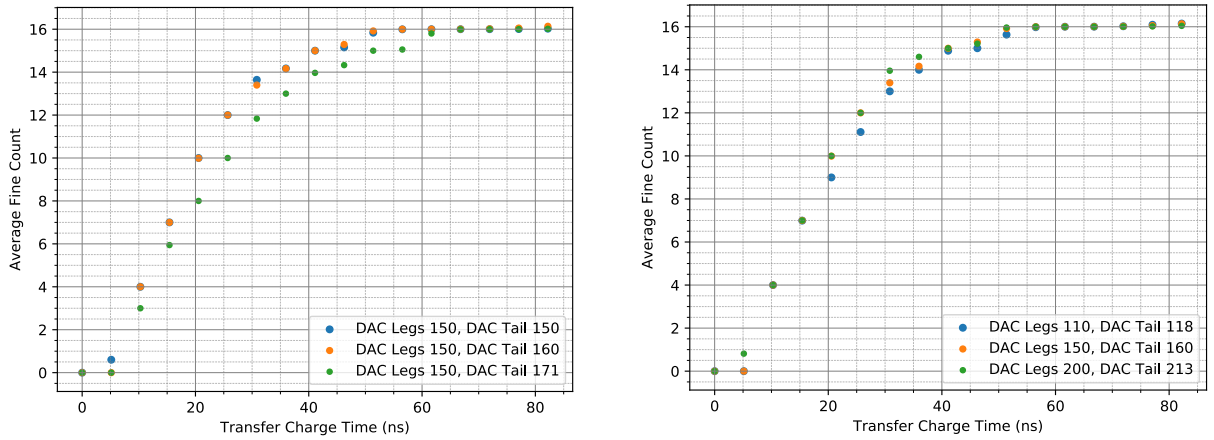
Variation of the Coarse Stage CSA Bandwidth

In the previous measurement, bias voltages and currents for the coarse stage are similar to the values that were used for the transfer time simulation in section 6.5. The bias DACs are tuned to provide the front-end with a total coarse stage current of roughly 75 µA which corresponds to a power consumption of roughly 90 µW. By changing the power consumption as well as the ratio of the legs and tails currents, the bandwidth of the coarse stage CSA can be changed (see section 6.2.1.4). Figure 7.13 shows the influence of the bias current DACs on the charge transfer time with an input capacitance of 200 fF. In figure 7.13a the overall power consumption is held constant and the tail current is swept. An increased tail current in relation to the legs current decreases the bandwidth of the coarse stage CSA. This is visible from the increased $T_{charge,min}$ below which the transferred charge starts to drop. In figure 7.13a, the overall power consumption of the coarse stage CSA is changed while keeping the ratio of the legs and tail current equal. While the bandwidth seems to increase with extra power, the effect is barely visible in the resolution of this measurement.

7.3 Selected Digital Functional Tests

The analog measurements presented in the previous section already verify the basic functionality of all of the digital blocks including

- the global slow control for ASIC configuration.
- the global sequencer for dynamic front-end control.
- the global telegram interface for the dynamic data management and readout.
- the pixel-wise RAM modules.



(a) Tail current variation at a fixed legs current value. The default as given by the setting of 150 and 160 for the legs and tail DAC is the depicted case in figure 7.11b.

(b) Sweep of both the tail and the legs current at the same time, keeping the ratio equal.

Figure 7.13: Influence of the bias DACs on the charge transfer speed.The *legs* DAC controls the CSA's overall power consumption where a value of 150 corresponds to a roughly 90 µW. The choice of the *tails* DAC can introduce an additional bandwidth cut where lower current corresponds to a lower bandwidth (see section 6.2.1.4.)

- the pixel-wise data merger unit for data pre-processing.

In addition, the ASIC's digital power consumption has been measured at the example of T5's 4x4 channel matrix. Its actual size depends on the chosen operation mode. For a typical setting with a (sub)frame length of 1 µs at a system frequency of 440 MHz, a power consumption of $(300 \pm 100)\,\mu\mathrm{W\,pix^{-1}}$ has been evaluated. The large uncertainty stems from the fact, that it is not possible to seperate the power consumption of the ASIC's global blocks from that of the channel matrix. With a higher channel count, the current consumption per channel is expected to decrease.

In order to demonstrate the chip's mentioned flexibility in terms of data taking, the following subsection presents a showcase measurement of the histogram mode explained in section 6.3.3.2.

7.3.1 The Histogram Mode

The readout ASIC's histogram mode is implemented via the custom-made telegram protocol. Instead of storing the amount of counted photons N of a (sub)frame in the pixel's RAM storage, the histogram mode allows incrementing the stored value at the RAM address N. Subsequently, the channel generates a histogram in its RAM module where each address represents a bin. The following measurement to test this mode has been published in [73].

In this test, the channel-wise merger has been used to generate data of a known distribution on-chip. In order to achieve this, the following steps have been performed for each single value written to the RAM storage:

1. Take a number A from the known distribution
2. Record a dark frame and count $N = 0$ photons

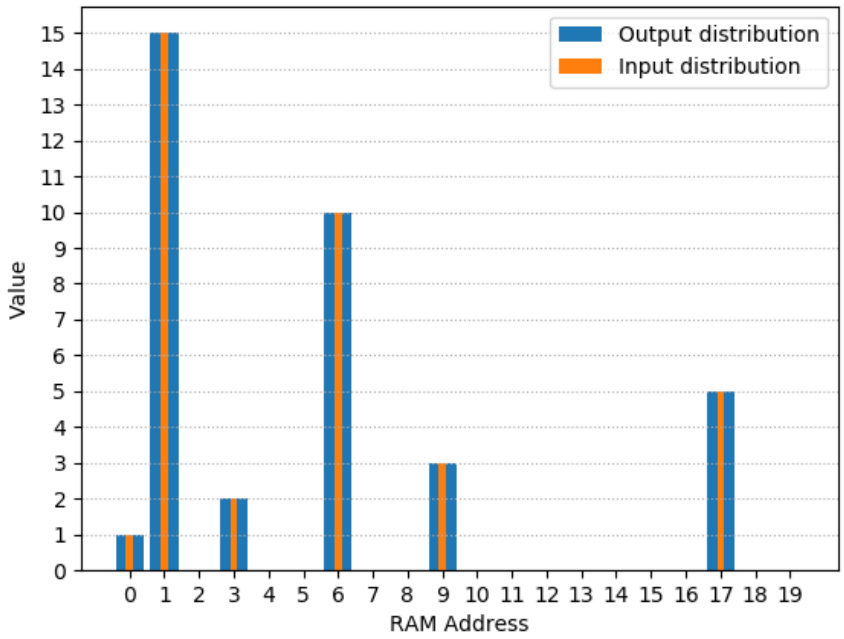


Figure 7.14: Graph of the histogram mode test. The blue bars show the input distribution that have been stored via the on-chip histogram storage mode. The orange bars show the distribution obtained from the subsequent readout of every RAM address. Graph taken from [73].

3. Use the merger to convert the N such that $N = A$

4. Use the telegram command *RAM Address is relative* to increment the stored value at the address $N = A$

After repeating this procedure 36 times, the RAM has been read out. Figure 7.14 compares the distribution of input values (orange) to the read out contents of the RAM (blue). As demonstrated, the distribution of the read out RAM contents perfectly resembles the input distribution. This verifies the histogram mode functionality.

As a next step, it has to be tested with real data. In a planned future measurement, charge from a known distribution is supposed to be injected into one of the front-end channels and recorded with the histogram mode.

7.4 Reflections on ASIC Characterisation Measurements

This chapter presents a selection of performed ASIC characterisation measurements throughout this work. In order to perform these measurements, a full-blown test set-up has been designed. This includes the design of test PCBs, the development of a test software framework as well as FPGA firmware for the set-up control and data readout. The selected measurements are supposed to give insight into the conducted research as well as the performance of XIDer's readout ASIC in a laboratory environment.
The most important conclusions to draw from this chapter are:

- With the initial **functionality** test, all of the custom-designed auxiliary blocks, like the I/O pads, monitoring buffers, global digital slow control, bias DACs and the sequencer have been proven to work on a manufactured ASIC

- The **analog front-end's functionality** test has demonstrated the operability of the continuous conversion in both the coarse and fine stages. Alongside, the charge transfer procedure between the stages works as expected.

- The **test charge injection** works as expected. While manufacturing uncertainties are expected, in the tested cases, the injected charge resembled the expected theoretical values. However, since the injection will be used as a basis for channel calibration, the manufacturing variation needs to be studied in a sophisticated measurement for many channels.

- The front-end exhibits a remarkable **counting linearity** even under extreme conditions. After a by-hand calibration, the front-end under test has reliably reconstructed the amount of equivalent photons in a test charge injection sweep. In a range from 0 to 162 equivalent 30 keV photons, a maximum systematical deviation of 1 photon has been recorded.

- The front-end is capable of handling high amounts of **instantaneous charge**. In the linearity measurement, all of the input charge has been injected at once[11]. Even though the coarse stage CSA is expected to saturate at an input charge equivalent to roughly 37 30 keV photons, the front-end kept reconstructing the amount of photons reliably until the highest measured value of 162 30 keV photons. In the measured range, the front-end lies in agreement with the simulation presented in section 6.5.2. In order to ensure that the front-end can achieve the requirement cases of 200 instantaneous 30 keV photons, another measurement with a slightly extended input charge range has to be executed.

- For the combined noise contributions of both CSA stages an equivalent **input referred noise charge** of $(307.5 \pm 1.6)\,\mathrm{e^-}$ at an input capacitance of 200 fF has been measured. This measurement shows a close resemblance with the simulations where a value of $295\,\mathrm{e^-}$ has been predicted. With this value, the front-end is expected to exhibit a **dark count rate** in the order of $1\,\mathrm{ph\,h^{-1}\,pix^{-1}}$ or less.

- For a fixed amount of incident photons, the front-end's **statistical counting uncertainty** at an input capacitance of 200 fF has been measured. Over the measurement range of 0 to 162 incident 30 keV photons a standard deviation of less than 0.4 photons has been determined. With this, the contribution of electronics readout noise is expected to be negligible vs. other influences like the Poissonian photon counting statistics. The measurement has been performed with the on-chip test signal injection.

- The measurement of the minimum necessary **coarse-to-fine charge transfer time** without substantial charge losses provides a value of roughly 77 ns for an input capacitance of 200 fF. With this, a count rate of $(0.90 \pm 0.05) \times 10^9\,\mathrm{ph\,pix^{-1}\,s^{-1}}$ is expected to be achievable in the ESRF's 16-bunch mode which is off by 10 % to the required $1 \times 10^9\,\mathrm{ph\,pix^{-1}\,s^{-1}}$.

  The simulation provides a transfer time of roughly 72 ns for an input capacitance of 200 fF which is comparable to the measurement. However, the simulation employs a harder constraint on the final voltage on C_{tran}. This is due to the fact that the measurement's granularity is limited by the fine charge package size. As a

[11] In this context, *at once* means in a time window shorter than the charge pump clock period

comparison, the measurement provides a charge resolution of 0.5 30 keV photons, whereas the simulation demands the voltage on C_{tran} to settle within an area of 0.1 30 keV photons of its final value. While in principle the package size used in the measurement could be reduced further to reach a better resolution, a more thorough calibration is needed. In parallel, a higher system frequency would also increase the measurement resolution.

A possible improvement to the transfer time can be achieved by decreasing the size of the transfer capacitor. This is currently being discussed.

All of the stated results have only been verified with single readout ASIC channels. Variations between channels are expected and will be studied in future measurements.

8 ASIC-Sensor Assembly Measurements

In parallel to the ASIC development in Heidelberg, the ESRF has collaborated with Acrorad [94], Redlen Technologies [55], Due2labs [95] and Polymer Assembly Technology [96] for the design and submission of CdTe and CZT sensors as well as the assembly of ASIC-sensor prototypes. From the beginning of the project, the XIDer collaboration chose to perform sensor characterisation measurements with the readout ASIC designed in Heidelberg. In order to achieve this goal, a tight collaboration between the labs at Heidelberg University and the ESRF was and still is necessary. This includes the design of test set-ups, sharing and development of software/firmware, and system operation in beamtimes.

This chapter gives an overview of the ASIC's capabilities in the environment it is meant to be used in. Starting from an overview of the assemblies built throughout the project and the assembly procedure, it showcases a few selected milestone measurements performed with assemblies in Heidelberg and in ESRF beamlines. Besides the assembly characterisation, these measurements also focus on functionality and performance tests of the detector concept. For a more thorough and deep analysis of assembly and sensor characterisation measurements performed within the XIDer project, the reader is referred to [93].

8.1 Assembly Prototypes

Both T2 and T4 ASICs[1] have been used in assemblies with sensor prototypes. Table 8.1 shows a list of all the different available combinations. Besides the CdTe and CZT versions, the list also features GaAs:Cr assemblies. However, these are yet to be tested as they were deemed lower priority due to their less efficient absorption at the high energies required.

The CdTe sensors have been manufactured by Acrorad [94], while the (HF)CZT[2] sensors have been produced by Redlen Technologies [55] and post-processed by Due2labs [95]. In addition, the GaAs:Cr sensors have been acquired from Tomsk State University [97]. While all of the CdTe sensors exhibit a thickness of 1 mm, the CZT sensors are 2 mm thick. With the exception of the first few prototypes, the ASIC-sensor assembly, has been performed by Polymer Assembly Technology [96]. The corresponding procedure is explained in the following section.

8.2 Assembly Procedure

Figure 8.1 shows a to-scale comparison of a T2 ASIC and a CdTe sensor prototype. The CdTe sensor prototype contains several 4x4 pixel matrix structures with different pixel pitches. This is due to the technical fact, that the purchased sensors needed to have a minimum size of 4 mm × 4 mm. So, instead of ordering several different prototypes with an individual matrix each, a single prototype with several different matrices has been

[1] See section 6.6 for a list of submitted ASIC iterations.
[2] HF stands for high flux as explained in section 3.3.2

ASIC	Pixel Pitch [µm]	Sensor Material	Amount
T2	100	CdTe(ohmic)	3
		CdTe(Schottky)	5
		GaAs:Cr	3
	200	CdTe(ohmic)	4
		CdTe(Schottky)	3
T4	100	CdTe(ohmic)	4
		CdTe(Schottky)	4
	200	CdTe(ohmic)	4
		CdTe(Schottky)	4
		GaAs:Cr	4
		CZT	5

Table 8.1: List of produced XIDer prototype ASIC-sensor assemblies.

designed. In order to shield the individual matrices from their surroundings, additional guard ring structures are added. Most of the pixel matrices of interest for ASIC-sensor interconnection are placed in corners of the sensor prototype such that they can be placed on top of the ASIC without blocking any mandatory wire-bond pads.

The geometries of the ASIC prototype and the sensor impose a challenge on the bump-bonding process. As depicted in figure 8.1, when connecting one of the 4x4 matrices to the ASIC, only a small fraction of the sensor actually rests on the ASIC. Subsequently, mechanical support has to be added underneath the sensor overhang. Otherwise, the sensor employs a torque on the 16 bump-bonds which is large enough to break the connection. As an aside, while this is a challenge for the assembly of small-scale prototypes, the final detector will use ASIC and sensor geometries, such that the sensor can actually rest on the ASIC without a mechanical support.

In order to cope with these difficulties, the following assembly procedure has been developed. For reference, figures 8.2a and 8.2b show images of an example assembly built with it. The procedure starts with glueing a carrier structure made from ULTEM for both the ASIC and the sensor onto the PCB. In a pre-defined cut-out area the ASIC is glued onto the ULTEM-carrier. Then, the ASIC is wire-bonded to the PCB and stacks of gold studs are placed on the ASIC sensor and guard ring pads. After covering the CdTe sensor pads in silver-epoxy glue, the sensor is flipped onto the ASIC and glued to the ASIC as well as the ULTEM carrier.

In this configuration, the upwards-pointing back-side of the sensor is connected to a wire via conductive glue. This wire is used to bias the sensor back-side contact to a high voltage in the order of several hundred negative volts in relation to the pixel contacts. While this presented procedure has initially been developed for CdTe sensors, it has also been successfully applied to CZT and GaAs:Cr sensors.

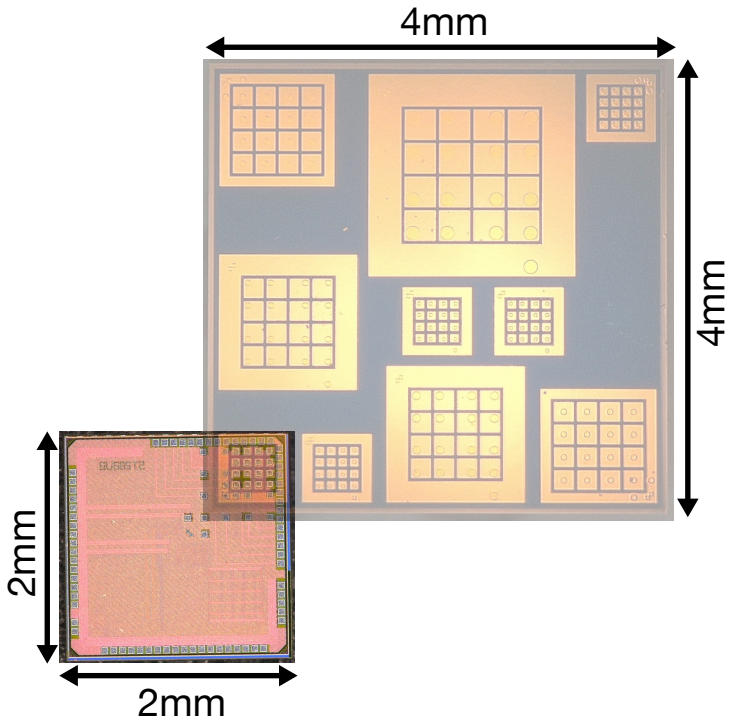


Figure 8.1: Images of a T2 ASIC and a CdTe sensor prototype placed on top of each other. The ASIC's pixel pad matrix is aligned with the 100 µm pixel pitch matrix in one of the cornser of the sensor prototype to illustrate what a bump-bonded assembly would look like. The size relation of the ASIC and sensor are to-scale. Sensor image taken from [7]. Illustration taken from [92] and modified.

8.3 Selected Measurements

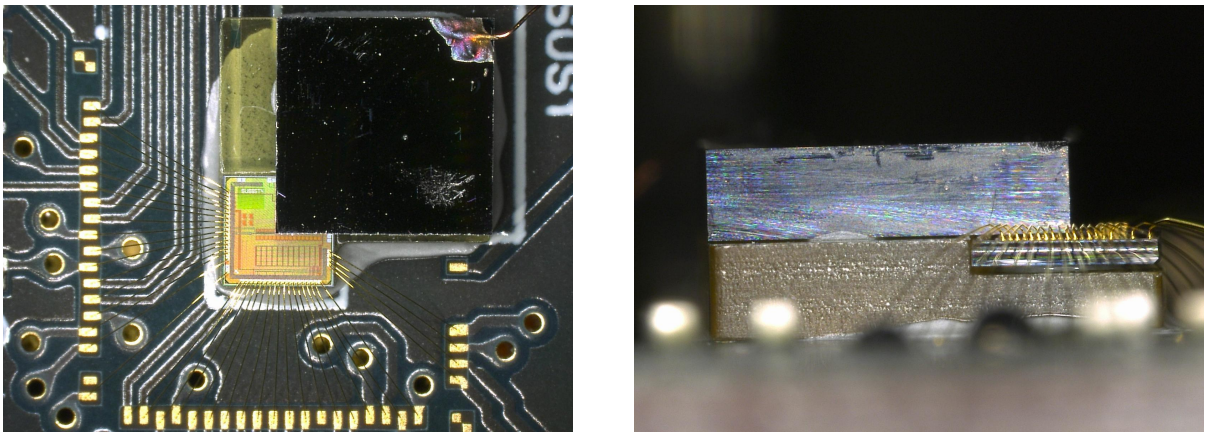
This section presents a few of the milestones in the XIDer project that were achieved with ASIC-sensor assemblies. It includes:

- Functionality test with very first ASIC-sensor (CdTe) assembly
- Dynamic range and linearity measurement with CdTe at the beamline BM05
- Bunch synchronisation with a CdTe sensor at the beamline BM05
- Preliminary afterglow measurements with CdTe sensors at the beamline BM05

While the first measurement is of qualitative nature, the others demonstrate the current prototype assembly performance in comparison to the project's requirements. Since these measurements have been taken at different states of the project, the employed ASIC control and readout environment has gone through ever-improving iterations. However, the overall architecture for employed measurement set-ups is similar to the one explained in section 7.1 for most of the measurements. Significant differences that have a substantial impact are explained where needed.

8.3.1 Assembly Functionality Test

The project's very first assembly formed by a T2-ASIC and an ohmic 200 µm-pixel pitch CdTe sensor has been tested in Heidelberg. In this simple test, the set-up depicted in

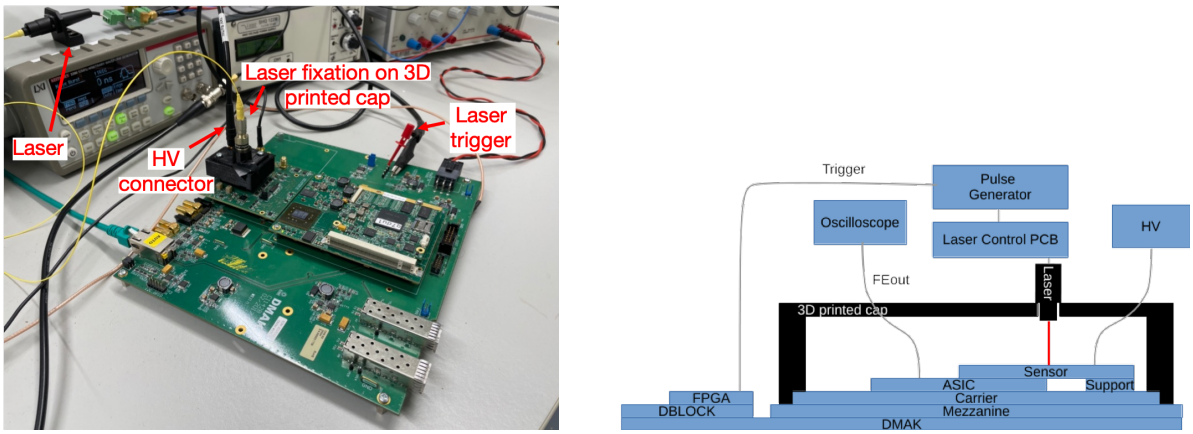


(a) Top view (b) Side view

Figure 8.2: Images of an ASIC-CdTe sensor assembly taken from [91].

figure 8.3 has been used. At the bottom, there is the PCB stack with the topmost ASIC carrier. Mounted to the carrier, there is a 3D-printed cap with a small opening as well as a cut-out slot at the top. This cap surrounds the assembly and covers it from external stray light. The slot at the top acts as a mount for a 642 nm laser which is aligned with the sensor. With a custom control PCB designed by the research group, the laser can be controlled via digital control signals. These are provided from the same FPGA that is used for the ASIC control as well as the data readout. With a remotely controlled HV source, the sensor back-side is biassed at −400 V. All of the involved components, i.e. the FPGA and the HV power supply, are connected to a PC via the FTDI USB interface and a GPIB interface.

The purpose of this measurement is to qualitatively verify that the assembly procedure produces functional ASIC-sensor assemblies. For this purpose, the laser is roughly aligned with a sensor pixel. After the alignment, the whole 4x4 matrix is read out via the readout ASIC.



(a) Actual laboratory image (b) Schematic drawing

Figure 8.3: Measurement set-up for assembly functionality test with a laser. This is one of the initial set-up iterations which uses the ESRF-specific DMAK/DBLOCK instead of the PETA mainboard. Since it fulfills the same purpose as the PETA board, details in their technical differences are skipped throughout this section. Images are taken from [92].

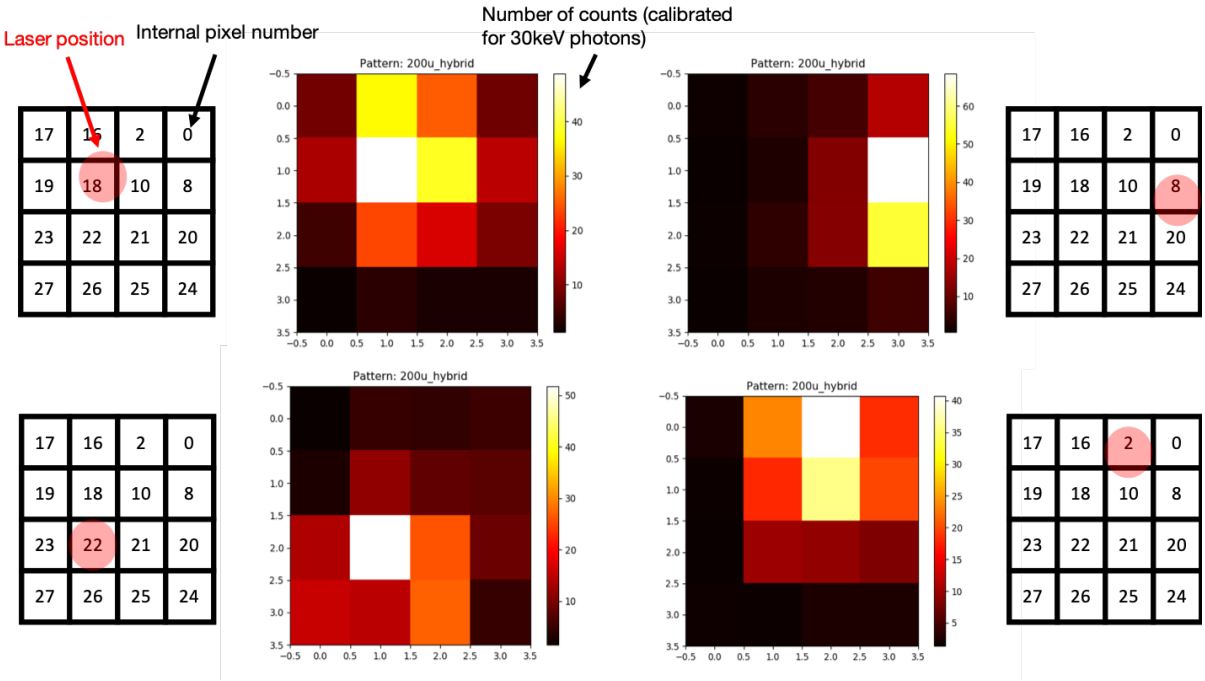


Figure 8.4: Heat maps taken with the T2-CdTe prototype assembly to determine the laser position and verify the success of the bump-bond procedure. Taken from [92].

A few images recorded in this measurement are shown in figure 8.4. They have been taken at a system frequency of 125 MHz with a charge pump clock frequency of 12.5 MHz. With a (sub)frame length of 4 µs, the default sequencer track configuration as depicted in 6.3.3.1 has been used. For each of the 16 pixels, the depicted heat maps indicate the counted photons per (sub)frame in the corresponding ASIC channels. As demonstrated, the readout shows a clear image of the laser's current position. An important point to mention here is that the depicted laser positions next to the read out heatmaps have been estimated by eye and do not represent a precise measurement or alignment. Also, since this measurement does not aim to precisely count photons of a given energy, the ASIC has not been calibrated thoroughly.

This result verifies that the employed assembly exhibits functional pixel-to-channel connections. Additionally, it shows that the ASIC channel manages to read out the charge signal of its corresponding CdTe sensor pixel and convert it into a digital value. More thorough assembly performance measurements with quantitative analyses are discussed in the following subsections.

8.3.2 Beamline Measurements

All of the following measurements have been performed at the ESRF's BM05 beamline. The research presented here has been performed in close collaboration between the ESRF and Heidelberg University. Researchers of the ESRF's Detector & Electronics Group adapted the existing ASIC characterisation set-up to conditions and needs at the beamline. This also includes planning the performed measurements in terms of goals, execution and schedule as well as subsequent data analysis.

At the same time, the author contributed support on a firmware and software level for the set-up control and data readout. This includes contributions to the measurement preparations and the execution at the beamline. The software implemented for beamline

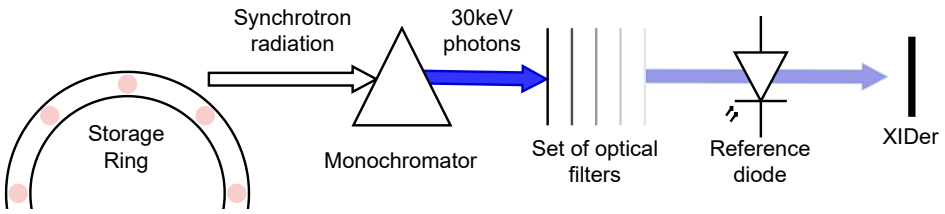


Figure 8.5: Schematic drawing of the measurement set-up at the beamline BM05. Taken from [91] and modified.

measurements is based on an underlying set-up control and data readout framework explained in section 7.1.

8.3.2.1 Beamline Set-Up

A schematic drawing of the beamline measurement set-up is shown in figure 8.5. X-rays radiated from the electron bunches in tangential direction to the synchrotron storage ring propagate through a monochromator. Here, the energy of X-rays incident to the measurement set-up is tuned to the desired value. Behind the monochromator, there is an air-pressured automated filter box which allows placing a set of metal filters into the X-ray beam path. Depending on the X-ray energy the choice of the amount of filters, their thickness as well as the filter material allows controlling the X-ray beam intensity incident to the measurement set-up. For example, for smaller energies in the range of 30 keV, Al filters with a thicknesses in the order of several 100 µm up to milli-meters can be used. For harder X-rays in the range of 60 keV, Molybdenum filters with thicknesses in the order of several 10 µm are employed.

After the filter box, the beam passes through a reference silicon photo-diode with a thickness of 500 µm. Recording its output current provides an indirect measurement of the current beam-flux to provide a reference. Finally, the XIDer assembly is placed behind the diode to measure the incident x-ray photon flux.

An image of this set-up is shown in figure 8.6. After the filter box (not depicted), the beam enters the set-up in the depicted angle from the right. The XIDer assembly prototype is covered by black tape on the readout PCB to the left. The reference diode is placed in the grey aluminum block with the black opening in the bottom mid part of the image.

In addition to the set of filters, the beamline also features two tunable slits to control the cross-sectional beam size. Prior to every measurement, these slits have been used to center the beam on the XIDer assemblies. In order to achieve this, a Basler camera has been used to track the beam position, size and uniformity. Furthermore, a shutter allows blocking the beam completely from the measurement set-up.

To calibrate the used assemblies, an automated calibration procedure has been developed at the ESRF. It is performed with the on-chip test signal injection which in turn is calibrated with the analog output buffers of the coarse and fine stages. A detailed explanation can be found in [93].

All of the presented measurements have been performed with single pixels of the employed assembly prototypes. In order to exclude parasitic edge effects from the measurements, only pixels in the center of the 4x4 matrices have been chosen.

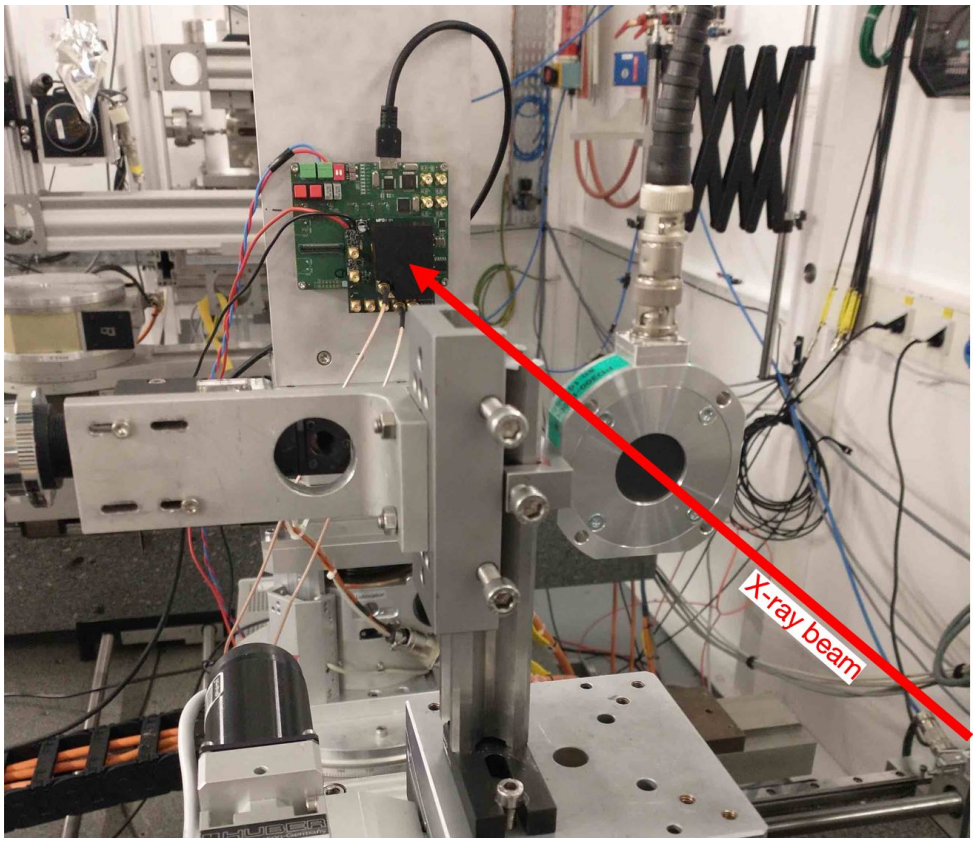


Figure 8.6: Photograph of XIDer's measurement set-up at the ESRF beamline BM05 taken by Morag Williams.

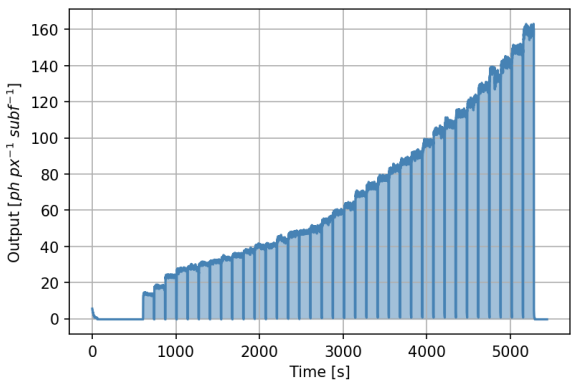
8.3.2.2 Dynamic Counting Rate Range & Linearity

One of the most important requirements of the XIDer detector is a high dynamic counting range up to $1 \times 10^{11}\,\mathrm{ph\,s^{-1}\,mm^2}$ while maintaining single photon sensitivty for pixels with low flux. With a planned pixel pitch of 100 µm, this corresponds to a required photon counting rate of $1 \times 10^{9}\,\mathrm{ph\,s^{-1}}$ for each pixel.

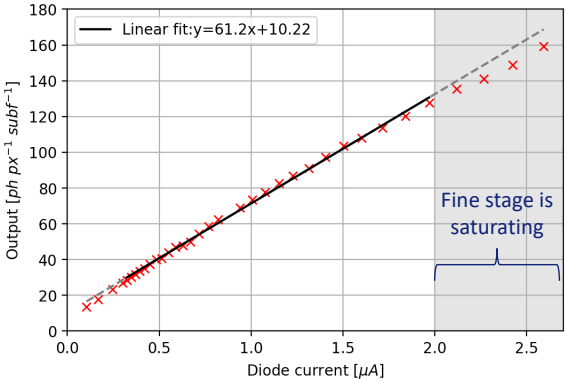
Subsequently, beamline measurements have put a focus on measuring the maximum counting rate that can be achieved with the assembly prototypes. This subsection focusses on a dynamic range measurement performed with a T4-CdTe assembly. The used assembly exhibited a pixel pitch of 100 µm and the measurement has been performed with the ESRF's 7/8+1 bunch filling mode[3], which corresponds to quasi-continuous illumination. Figure 8.7a shows the underlying pattern that these measurements have been performed with. Each depicted data point shows the amount of counted photons by a single pixel of the XIDer assembly with a (sub)frame of 2 µs. In this (sub)frame, the active integration window is 1.65 µs. After biassing the sensor, the assembly is put in a rest-state for 10 min, i.e. 600 s, without X-ray irradiation. This time is necessary for the sensor charge trapping and detrapping dynamics to reach an equlibrium state[4].

After the initial idle-time, the assembly is irradiated with different X-ray fluxes tuned by the filter settings. In the depicted case, the filter settings are swept through from the strongest to the weakest attenuation in steps of 500 µm thickness of Al. For each filter configuration, the XIDer prototype assembly is irradiated for 2 min. In between each

[3] see section 2.3.4
[4] see section 3



(a) Recorded flux pattern.



(b) Extracted photon rates vs. photo-current measured in reference diode.

Figure 8.7: Front-end linearity measurement at the ESRF's beamline BM05.[98]

setting, the main beamline shutter is closed for 5 s to simplify the separation of different filter settings in the data analysis. The chosen X-ray energy is 30 keV which the assembly has been calibrated for.

Plotting the mean of the plateaus for each filter setting vs. the reference diode current leads to the graph shown in figure 8.7b. In the mean calculation, the plateau edges, i.e. the initial as well as the final 10 % of the data points of each plateau, are excluded. In addition, a line has been fitted to the data points to examine the counting linearity.

As demonstrated, the studied pixel shows a linear behaviour up to a point of roughly 130 ph pix^{-1} subfr^{-1}. With a (sub)frame length of 2 µs, this corresponds to a photon count rate of 6.5×10^7 ph s^{-1} pix^{-1}. Above this point, the data points are subject to an artifact which stems from the fact that the detector has not been synchronised to the synchrotron for this measurement. If charge enters the front.end while the charge transfer is ongoing, this charge is not converted by the coarse stage. Instead, it is transferred to the fine stage. For low rates, the fine stage can cope with a little extra charge. At higher rates, however, the additional integrated charge drives the coarse stage output to the upper supply voltage before the charge transfer is finished. Any extra charge entering the front-end beyond this point can not be transferred to the fine stage and is inevitably lost. The plot denotes this area as *Fine stage is saturating*.

In future measurements, the detector is planned to be synchronised to the synchrotron, such that one can carefully align the detector's (sub)frame to the synchrotron bunch structure. This will allow aligning the charge transfer window with the gap in the 7/8+1 mode (see section 2.3.4). Unfortunately, the mentioned input switch in section 6.5 can not be used here. Indeed, it fulfills the purpose of disconnecting the pixel from the front-end and preventing charge from entering the front-end while the charge transfer is in progress. However, the charge that builds up on the pixel capacitance during this time and in this bunch mode has been underestimated in the initial design. For the chosen charge transfer time, the charge build-up drives the voltage on the sensor capacitance to such low values, that the switch starts conducting. For future iterations, different input switch architectures are under development.

8.3.2.3 Bunch Synchronisation

As demonstrated in the previous subsection, in order to create well-defined conditions for experiments, the detector has to be synchronized to the storage ring. More precisely, the

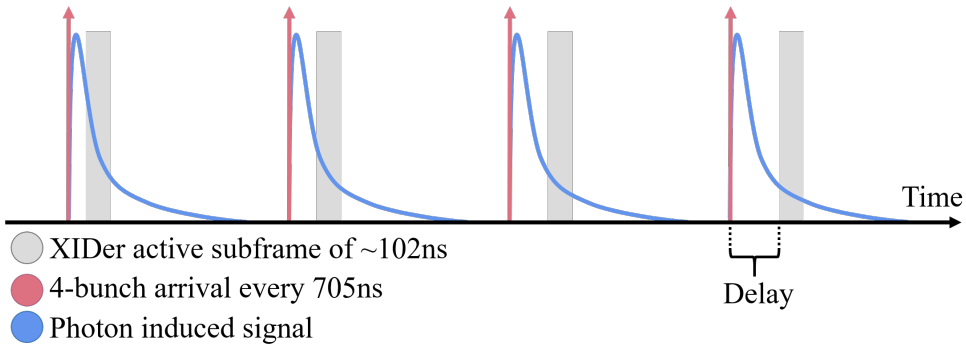


Figure 8.8: Orbit-scan measurement pattern. With the ESRF-designed Bunch Clock Delay Unit (BCDU8), XIDer's (sub)frame start is shifted along the synchrotron orbit. [99]

(sub)frames of the detector have to synchronized to the orbit frequency of the electron bunches. Only then, one can ensure that X-ray pulses hit the detector at a determined instant of time in the (sub)frame window.

In terms of XIDer, this synchronisation is achieved by deriving the ASIC root clock from the synchrotron's RF clock as described in section 6.1.3. By correct choice of the (sub)frame length via the front-end sequencer configuration as well as the amount of IDLE words in the telegram protocol, (sub)frames can be aligned with the X-ray pulse structure (see sections 6.3.3.1 and 6.3.3.2). The following presentations are loosely based on the contents of [99].
The goals of this measurement are:

- Verify that XIDer can be operated synchronously to the electron bunch orbit.
- Verify that XIDer is capable of resolving single X-ray pulses generated by single electron bunches in pulsed modes.

In order to do so, the measurement pattern depicted in figure 8.8 has been applied. Performed with the ESRF's 4-bunch mode[5], the pattern's idea is to shift the (sub)frame starting point along the pulse train. For each of the start-shift settings, XIDer is read out. When sweeping the length of this shift over a whole orbit period, the 4 pulses with a $\approx$ 705 ns-spacing should be resolved. As depicted in the figure, the chosen effective (sub)frame length is 102 ns.

Technically, the (sub)frame shift is implemented with an RF clock-synchronous trigger which is provided by the ESRF-designed Bunch Clock Delay Unit (BCDU8). The timing of this trigger can be programmed in multiples of the RF clock period. With a Verilog module implemented on the ASIC-control FPGA, the trigger signal is used to start XIDer's data acquisition. With the monochromator, an energy of 30 keV has been chosen for the X-ray photons incident to the mesurement set-up. The employed XIDer prototype assembly used a T4 ASIC and an ohmic CdTe sensor and was calibrated for 30 keV photons. In addition, a Basler camera has been used to ensure the beamline uniformity across the XIDer assembly. The detector prototype was operated at a system frequency of 440 MHz with a charge pump clock frequency of $\approx$88 MHz.

Figure 8.9 shows the result this so-called *orbit-scan* measurement. Each of the data points is represented by an x and shows the mean of roughly 8000 measurements with a

[5]Equal to the 16-bunch mode, but with 4 electron bunches in the storage ring

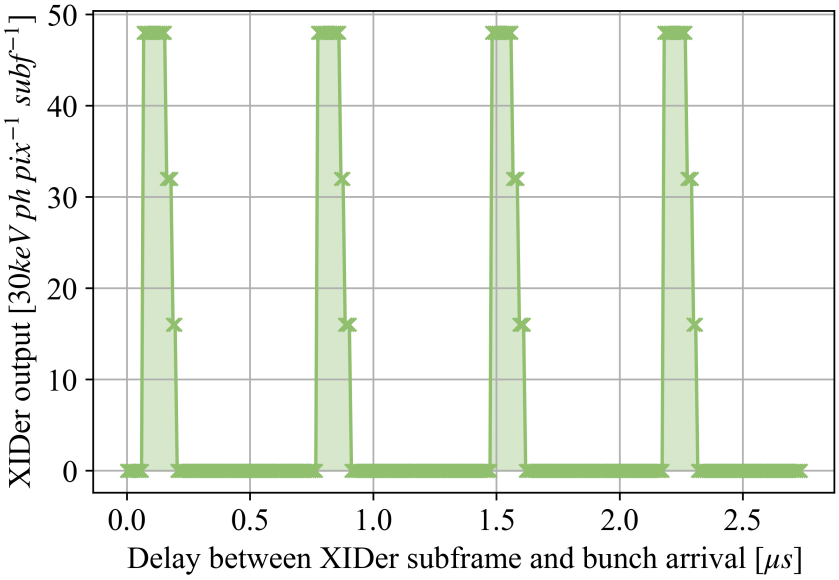


Figure 8.9: Orbit scan of the ESRF's 4-bunch mode performed with a XIDer prototype assembly. The assembly was equipped with an ohmic CdTe sensor.[99]

single XIDer front-end in the same setting. Due to calibration issues that led to unreliable fine stage counts, the measurement has only been performed with the front-end's coarse stage which is why count values only appear in multiples of 8. The x-axis shows the corresponding (sub)frame shift setting with a chosen step size of 8.5 ns. The maximum shift setting is given by the storage ring orbit period which is roughly 2.8 µs.

As depicted, the pulses generated by the 4 electron bunches in the synchrotron storage ring are clearly seperated. Estimating the mean time difference of the rising edges yields a distance of (707 ± 4) ns which is in agreement with the actual bunch separation of roughly 705 ns.

As a summary, this measurement fulfills its goals as it demonstrates that XIDer has been synchronised to the storage ring successfully and that XIDer can indeed resolve single X-ray pulses generated by single electron bunches. However, it also points at the current measurement set-up limitations. Due to the innovative and unconventional approach of the analog front-end, the automated calibration has to overcome unforeseen challenges. Since this was one of the first beamlines that utilised the newly developed calibration procedure, it also served as a means to test the procedure's performance. For the presented measurement, the fine stage calibration proved to be unreliable which is why it has been excluded in the data analysis. Using the data acquired in this beamline, the automated calibration is currently under investigation.

Additionally, the ASIC root clock has not yet been increased to the aimed for 880 MHz. With a frequency of 440 MHz, the output data rate of T4's serializer is not high enough to read out the 4x4 matrix in the ≈ 705 ns time window between the bunches. The achieved data rate of 220 Mbit s^{-1} only suffices for continuously reading out every second of the bunches.

Only running at 440 MHz was a decision made prior to the most recent beamtime where this measurement has been recorded. Due to substantial technical changes in the measurement set-up, this decision has been made as a safety precaution. From an ASIC-point of view, no evidence has been found that the root frequency could not be increased beyond 440 MHz, yet. Further investigations are necessary.

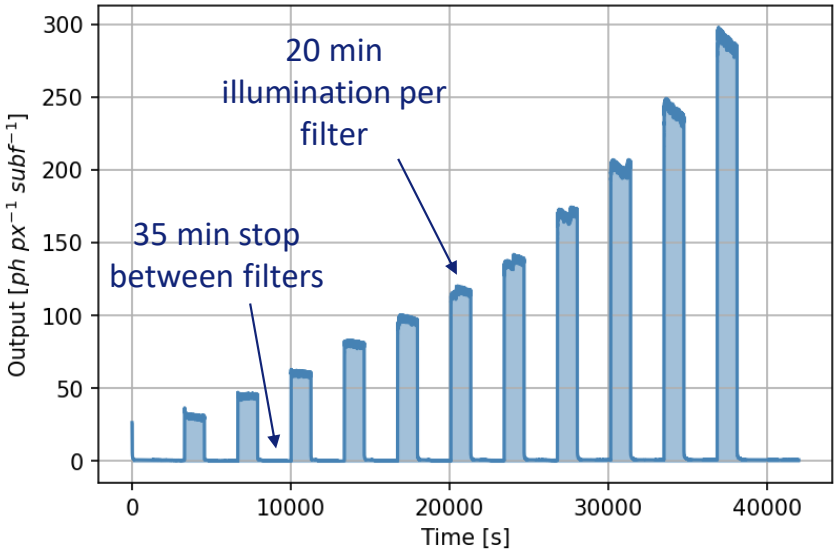


Figure 8.10: Flux pattern recorded with a T4-CdTe assembly with 200 µm pixel pitch. Taken from [98]

A few side notes: T6 features a 14 Gbit s^{-1} serializer IP provided by STFC to increase XIDer's output data rates. A final chip iteration with thousand of pixels will features several instances of this IP. However, there has not been a decision on how many data links the final ASIC detector will have. Additionally, the continuous readout mode at a frame-rate used in the presented measurement is not a foreseen use-case for the final detector. The detector's requirement for continuous frame readout is in the order of 100 kHz. This is more than one order of magnitude below the 1.4 MHz repetition rate of X-ray pulses in the 4-bunch mode.

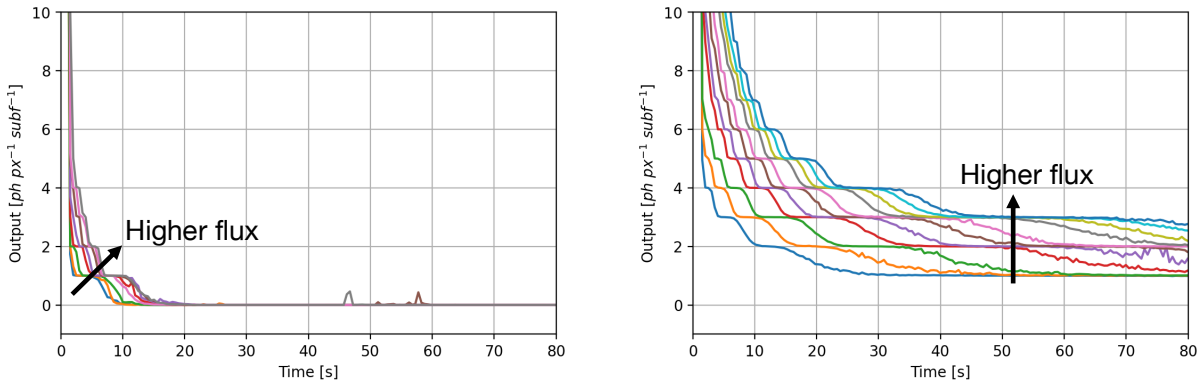
8.3.2.4 Afterglow

As described in section 3, the charge trapping and releasing properties of high-Z materials are origin to several signal afterglow tails with different time constants. Especially for CdTe, some of these time constants can be in the order of µs up to h[6] which is orders of magnitude longer than the x-ray pulse spacing in pulsed bunch-modes. Subsequently, measurements with CdTe and CZT are always dependent on the properties of previous illumination. XIDer assemblies are used to gain insight into the sensor dynamics, in order to feed the design of leakage or long-afterglow compensation circuits.

This subsection presents an example of such a measurement. It has been performed with the ESRF's 7/8+1 bunch mode. With an X-ray beam energy of 30 keV, T4-CdTe assemblies with a 100 µm and 200 µm pixel pitch have been tested with the pattern depicted in figure 8.10.

The plot shows the single channel output of one of the assemblies over the whole measurement period. Each data point in this plot corresponds to a 2 µs (sub)frame with an active integration time of 1.65 µs. After an idle time of 35 min where the beam shutter is closed, the assembly is illuminated for 20 min. For each illumination period a different filter setting is chosen where the incident flux is increased in each setting. After data acquisition, the time evolution of the afterglow signal processed by XIDer's readout ASIC for each filter setting is compared. Figures 8.11a and 8.11b show the results of this comparison for

[6]This depends greatly on the quality of the material



(a) 100 µm pixel pitch

(b) 200 µm pixel pitch

Figure 8.11: Preliminary afterglow measurements with T4-CdTe assemblies [98]

a the 100 µm and 200 µm sensor, respectively. The steps in the measurements stem from XIDer's digitization in the readout process.

While the presented results are preliminary and under investigation, a few qualitative conclusions can be made. As expected, smaller pixel pitches, i.e. smaller pixel sizes, exhibit much less afterglow. This is due to the fact that the smaller pixel surface area leads to a smaller volume which in turn leads to smaller number of traps per pixel. Combined with the digitizing nature of the digital integration scheme, the decreased afterglow signal amplitude leads to an easier afterglow discrimination with the comparator threshold. Subsequently, in terms of afterglow suppression the performance of a 100 µm pixel pitch detector is better than that of an otherwise equal 200 µm pitch detector.

Additionally, a higher flux leads to a larger initial amplitude in the afterglow. This, however, is expected to only be true, as long as there are traps to fill in the sensor material. At a high enough flux, all of the traps are expected to be filled and the initial afterglow amplitude is expected to saturate. In the presented measurement, this behaviour has not been observed.

For a 200 µm pixel pitch and the highest flux settings, afterglow was visible even a minute after illumniation. In addition to CdTe, XIDer has also been used to measure the afterglow of sensors made from the much more promising CZT material. However, all of the results are highly preliminary. The data analysis has not been finished when this work has been compiled.

In this context, it is important to note that section 6.1.5 explains a novel leakage/long-afterglow compensation scheme which is planned to be implemented in future chip iterations. The presented scheme is designed to handle afterglow components with long time constants as exhibited by CdTe. Current on-going measurements, also performed with CZT, are supposed to provide further insight for the necessary design parameters for the proposed scheme.

8.4 Reflections on Assembly Measurements

From the beginning of the XIDer collaboration, ASIC and sensor design have been pursued in parallel. A very early decision foresaw performing the readout of sensor characterisation measurements with ASIC prototypes designed in the XIDer collaboration.

Subsequently, the first T2-CdTe prototype was functional only two years after the start of the collaboration. The presented qualitative measurements with this prototype

that has been irradiated with a laser verified the functionality of the chosen adhesive low-temperature bump-bonding procedure. Also, for the first time, this measurement demonstrated that the analog front-end was and is capable of reading out the electronic signal of a CdTe sensor.

Besides the general assembly functionality, the presented measurements verify that the designed readout ASIC is capable of operating in a beamline environment. First dynamic range measurements show a maximum achievable photon count rate of $6.5 \times 10^7\,\mathrm{ph\,s^{-1}}$. With a pixel pitch of 100 µm, this corresponds to a photon flux of $6.5 \times 10^9\,\mathrm{ph\,s^{-1}\,mm^{-2}}$. Admittedly, this measured value is still too low by one and a half orders of magnitude compared to the aimed for $1 \times 10^{11}\,\mathrm{ph\,s^{-1}\,mm^{-2}}$. But, as discussed, the measured rate is currently not limited by the ASIC or detector itself but by the measurement procedure. A measurement with a detector that is synchronised to the storage ring orbit frequency is expected to greatly improve on the measured upper photon flux limit. An important point to mention is, that even with the current limitation in the measurement set-up, the measured photon count rate is already competitive with existing state-of-the-art synchrotron X-ray detectors (see section 5.3.1).

With the orbit scan measurement, the ASIC has been verified to be capable of operating synchronous to the ESRF's storage ring orbit. In the presented measurement, single x-ray pulses of the ESRF's 4-bunch mode have been resolved. Their measured spacing of (707 ± 4) ns lies in agreement with their actual spacing of roughly 705 ns. With achieving this synchronicity, the dynamic range measurement has been repeated. However, the corresponding data has not yet been fully analysed or published.

Finally, the presented preliminary afterglow measurements show that the readout ASIC can also be used to study the dynamics of CdTe sensor prototypes. As shown, larger pixel pitches lead to higher afterglow amplitudes. The quantitative analysis of the acquired data will be put to use in the design of leakage[7] compensation circuits.

Finally, with the current beamline set-up iteration, the measurements show promising results for the readout ASIC performance. Future assembly characterisations will be concerned with optimizing the automated calibration and increasing the system frequency. This will hopefully give more insight into the front-end's dynamic range, linearity and output data rate. At the same time, further afterglow as well as high-flux polarisation studies are planned for both CdTe and CZT sensors.

[7] Throughout the project, the term *leakage* is used synonymously for the long afterglow components of CdTe sensors.

9 Conclusion

This work presents the from-scratch design process and performance verification of the readout ASIC for the XIDer project with a focus on the analog domain. The aim of this R&D project is to verify the feasibility of an X-ray diffraction detector with the requirements imposed by a storage ring based fourth-generation synchrotron light source like the ESRF. The most challenging of these requirements is a dynamic photon counting range up to a photon flux of 1×10^{11} ph s^{-1} mm^{-2} while maintaining single photon sensitivity. Another challenging requirement is a time resolution, i.e. (sub)frame length, of 175 ns to resolve single bunches in the ESRF's 16-bunch mode. At the same time, the detector has to be as flexible as possible to enable its usage in many different experiments with different conditions and readout modes. In addition, due to the envisaged energy range of 30 keV to 100 keV, high-Z compound semiconductors have to be used as the sensor material to maintain high photon absorption efficiency. The complicated charge trapping and detrapping dynamics of such materials pose an additional challenge in the signal readout.

9.1 Current State of XIDer and the Readout ASIC

The chosen detector concept is a 2D hybrid pixelated structure with a 100 µm pitch where each sensor pixel is read out in parallel by an associated ASIC channel. In order to overcome the challenges, XIDer's readout ASIC employs novel concepts including the pipelined continuous conversion approach, the digital integration readout scheme, as well as the telegram protocol and interface.

Since the foundation of XIDer in 2018, six ASIC iterations have been submitted. The latest iteration is a large scale integration test for future engineering runs. Its 16x16 channel matrix is built from 4x4 sub-modules, which can be assembled to form larger matrices with an arbitrary size.[1]

Characterisation measurements of ASIC prototypes have been performed both in an isolated laboratory environment and with bump-bonded CdTe and CZT sensors at the ESRF's BM05 beamline. Table 9.1 summarizes XIDer's current state of performance, which is further discussed below. All of the measurements demonstrate the functionality of the analog front-end, the digital control blocks including the slow control, the sequencer and the telegram interface, as well as the measurement set-up, firmware and software. On a quantitative level, they are in good agreement with the corresponding simulations.

As a device that counts absorbed photons, a good counting linearity is a crucial property for XIDer's readout ASIC. In a linearity measurement with the on-chip test charge injection circuit in which all of the (sub)frame's charge is injected at once at the beginning, the conditions of the ESRF's most challenging 16-bunch mode have been emulated. By sweeping the injected input charge, the front-end has been confirmed to exhibit a remarkable linearity. Over a charge injection range 0 to 162 equivalent 30 keV photons, a maximum systematic deviation of 1 photon has been measured. The upper limit of this charge range is given by the charge injection circuit rather than the front-end.

[1] In multiples of 4x4

With an improvement of the injection circuit, future measurements are planned to verify that the front-end manages to achieve the requirement of 200 30 keV photons per X-ray pulse in the 16-bunch mode.

Measured at an input capacitance of 200 fF, the coarse-to-fine charge transfer time is expected to allow a possible photon count rate of roughly $0.9 \times 10^{11}\,\mathrm{ph\,s^{-1}\,mm^{-2}}$ in the most challenging 16-bunch mode, i.e. at a (sub)frame length of 175 ns. With a target of $1 \times 10^{11}\,\mathrm{ph\,s^{-1}\,mm^{-2}}$ for the XIDer detector, the bare ASIC is thus close to achieving the aimed for performance. The maximum count rate achieved by the analog front-end depends on the (sub)frame length. The 16-bunch mode's 175 ns is the shortest (sub)frame XIDer is designed for. Subsequently, it acts as a benchmark. For longer (sub)frames, timing constraints are relaxed and the ASIC can achieve higher count rates. At (sub)frames longer than 185 ns, the transfer time measurement predicts that the current front-end is capable of reach the required count rate of $1 \times 10^{11}\,\mathrm{ph\,s^{-1}\,mm^{2}}$.

Actual rate measurements with a bump-bonded sensor in the beamline have achieved a maximum count rate of $6.5 \times 10^{9}\,\mathrm{ph\,s^{-1}\,mm^{-2}}$ at a (sub)frame length of 2 µs up to this point. This, however, is currently limited by the beamline measurement set-up. The verified synchronisation with the storage ring in the presented orbit scan measurement is expected to enable utilising the ASIC's full count rate capability. Further assembly measurements will need to be performed for verification.

Besides the maximum count rate, the measurements verify that the ASIC is indeed capable of providing the required single photon sensitivity[2]. In an isolated environment and with an input capacitance of 200 fF, the baseline of the front-end under test has been measured to vary with a standard deviation of $(307.5 \pm 1.6)\,\mathrm{e^-}$. Subsequently, for the average charge generated by a 30 keV photon, the ASIC achieves a signal to noise ratio of roughly 22.[3]

In addition to the high signal to noise ratio, the low baseline noise leads to a low dark count rate. Simulations predict that the measured baseline noise leads to a dark count rate in the order of $1\,\mathrm{ph\,h^{-1}\,pix^{-1}}$ in XIDer's foreseen measurement conditions and at an incident photon energy of 20 keV. At higher energies, the dark count rate is expected to decrease further because of the increased comparator threshold voltage in the fine stage. This performance has been deemed to be more than sufficient for the experiments that XIDer is to be used in [8]. Actual dark count rate measurements with ASIC-sensor assemblies are currently being analysed. Results will be published in [93] where the additional influence of sensor leakage currents on the dark count rate is studied.

Furthermore, the statistical counting fluctuation of the observed front-end has been measured. The fluctuation has been verified to increase with the amount of total counted photons. This is expected because of the charge pumps' increased noise contribution with each applied charge package. Up to a value of roughly 45 equivalent injected 30 keV photons, no counting variation has been recorded, with the exception of two values. Increasing from 45 to 162 total counted photons, a maximum standard deviation of only 0.4 photons has been evaluated. With this, the counting fluctuations caused by the electronics readout noise are expected to be negligible in comparison to the Poissonian counting statistics which scale with the square root of the photon count.

While not being listed in the table, the functionality of the in-channel data pre processing functions and the telegram interface has been verified in a dedicated test for the histogram

[2] i.e. in the energy range of 30 keV to 100 keV with CdTe and CZT sensors

[3] in CdTe, a 30 keV photon generates roughly 6800 electron-hole-pairs on average. Since XIDer only reads out electrons, this corresponds to a charge of $6800\,\mathrm{e^-}$.

[4] dark count rate

Parameter	Device	Value	Comment
Counting Linearity	ASIC	$\leq 1\,\mathrm{ph}$ systematic error in range $0\,\mathrm{ph}$ to $162\,\mathrm{ph}$	$30\,\mathrm{keV}$ photons, conditions in text
Max. Count Rate per area in 16-bunch mode ($100\,\mu\mathrm{m}$ pitch)	ASIC Assembly	$(0.90 \pm 0.05) \times 10^{11}\ \frac{\mathrm{ph}}{\mathrm{s\,mm^2}}$ $\approx 6.5 \times 10^{9}\ \frac{\mathrm{ph}}{\mathrm{s\,mm^2}}$	Deriv. from transf. time Limited by set-up
Max. Count Rate per area @ subframe length $> 185\,\mathrm{ns}$ ($100\,\mu\mathrm{m}$ pitch)	ASIC	$1 \times 10^{11}\ \frac{\mathrm{ph}}{\mathrm{s\,mm^2}}$	Deriv. from transf. time, conditions in text
Input Referred Baseline Noise @$200\,\mathrm{fF}$ input cap.	ASIC	$(307.5 \pm 1.6)\,\mathrm{e^-}$	Expected to translate to DCR[4] of less than $1\ \frac{\mathrm{ph}}{\mathrm{h\,pix}}$, conditions in text
Counting Noise	ASIC	$\leq 0.4\,\mathrm{ph}$ standard deviation in range $0\,\mathrm{ph}$ to $162\,\mathrm{ph}$	$30\,\mathrm{keV}$ photons, conditions in text
Power Cons.	ASIC an. ASIC dig.	$\approx 240\ \frac{\mu\mathrm{W}}{\mathrm{pix}}$ $(300 \pm 100)\ \frac{\mu\mathrm{W}}{\mathrm{pix}}$	Analog, simulated Digital, measured, depends on mode, see text

Table 9.1: Performance summary of XIDer in its current state. The column *Device* denotes, whether the corresponding value has been evaluated for a bare ASIC or an ASIC-sensor assembly.

readout mode. The ASIC channel under test has succesfully stored a photon count distribution in its RAM storage which has been generated with the on-chip data processing functions. This demonstrates the ASIC's flexibility in terms of data taking and data readout modes. A test of the histogram mode with actual charge signals is planned.

In all of these measurements, the analog front-end has been operated with the default bias settings. While the actual power consumption of the analog front-end has not yet been measured, simulations predict a value of $240\,\mu\mathrm{W\,pix^{-1}}$ in this configuration. Besides the coarse and fine stage CSAs, this includes the comparators and charge pumps for both stages, as well as auxiliary buffer blocks. Except for the CSAs, none of the included modules have yet been optimized for low power consumption. The power consumption

of the digital control block depends on the operational mode. In a typical configuration with a system frequency of 440 MHz and a (sub)frame length of roughly 1 µs, the chip's digital power consumption has been measured as $(300 \pm 100)\,\mu W\,pix^{-1}$. This, however, includes the power consumption of the global control blocks which are instantiated only once per ASIC. And since this measurement has been performed with a T5 ASIC which has a small 4x4 channel matrix, the power consmuption of the global blocks per channel is overestimated. Additional measurements with the larger matrix of T6 are planned.

The overall ASIC design process shows that XIDer's requirements prove to be as challenging as expected. However, in terms of front-end functionality, noise performance, single photon sensitivity, and counting linearity, the ASIC already meets the majority of the requirements. Obviously, the conclusions made here have to be taken with caution with respect to the expected performance of a fully assembled final detector with millions of pixels, where contributions beyond that of individual readout channels influence the detector performance. For this reason, larger channel matrices have been implemented on the most recent ASIC iteration and will be tested in combination with larger sensor pixel matrices in the near future.

9.2 Outlook

With promising results, the initial R&D phase of XIDer is concluding by the end of 2023. While the analog front-end of the ASIC prototypes manages to fulfill almost all of the requirements, there are a few properties left that require more optimisation. For example, the transfer time of the residual charge from the coarse to the fine stage turns out to be a limitation for the maximum achievable count rate at the short (sub)frame length of the ESRF's 16-bunch mode. In order to cope with this, future design iterations are planned to trade the transfer charge gain with a faster transfer speed by decreasing the transfer capacitor size. Another example is the current front-end's large power consumption stemming from the non-optimised comparator, charge pump, and buffer designs. A planned low-power optimisation should simplify fitting the front-end into large scale matrices regarding supply voltage drop and heat dissipation.

In terms of sensor characterisation, the trapping and detrapping dynamics of the high-Z materials like CdTe and CZT need to be studied in more detail. Insights gained in these studies are necessary for the development of an effective leakage and long afterglow compensation circuit. In addition, the test set-up has to be improved to probe XIDer's upper counting rate limit beyond the measured $6.5 \times 10^9\,ph\,s^{-1}\,mm^{-2}$ in a beamline environment.

Besides these low-level improvements, the next step in the ASIC development and characterisation is to verify its performance in a large scale design. Channel-to-channel variations and crosstalk between channels, as well as between the analog and digital domain, need to be studied in more detail. This is the purpose of the most recent iteration, T6. With a 16x16 matrix, it is the first prototype that features more than 16 channels. In addition, it is the first iteration that includes fine trim circuitry to mitigate channel-to-channel variations. By the time this work has been compiled, its fully assembled test set-up has just arrived at the laboratory and measurements are being prepared. Furthermore, high-level questions like managing the data readout and power supply of a large chip are currently under investigation.

On a higher, organisational level, the project's future lies in a currently forming collaboration with the STFC under the name of XIDyn. The collaboration is a merge of XIDer

and a similar detector design by the STFC for the Diamond Light Source. Due to their similarity, the XIDyn collaboration aims to fulfill the requirements of both the Diamond Light Source and the ESRF. A common ASIC design is planned as a basis. Whether all the requirements can be met with a single ASIC or whether different flavours are necessary, is currently being discussed.

9.3 Summary of Author Contributions

In this section, the author's contributions to the XIDer project are listed and summarized:

- **Conceptual design of the readout ASIC:** Starting from an initial adaptation of available circuit blocks like the sequencer and the JTAG interface from the DSSC project, the author has provided major contributions to the fully independent concept design of the readout ASIC for XIDer.
- **Analog front-end design concept:** Major contributions to the development of the novel design concept for the analog front-end. The result is the proposed and implemened pipelined continuous conversion approach which is the first to utilize the novel digital integration scheme.
- **Analog circuit design:** Design of the analog front-end circuit blocks. A special focus was put on the charge sensitive amplifier (CSA) and the charge pump to optimise the front-end for counting linearity, low noise and, in the case of the CSA, low power consumption.
- **Analog design verification and simulation:** System theoretical calculations and simulations to study and test design concepts and optimise their performance before manufacturing. These range from simple functionality tests to detailed dc, transient, and ac simulations, including noise and Monte Carlo analysis. As a result, the analog front-end has been optimised to fulfill almost all of the ESRF's design constraints.
- **Full-custom layout:** Implementation and optimisation of the full-custom physical layout of the analog front-end and peripheral circuitry, such as I/O pads and buffers. In its most recent iteration, the front-end layout has been minimized to a size of $100\,\mu m \times 25\,\mu m$ to fit in the 4×4 pixel matrix module. With this step, the layout is ready for integration in large scale designs.
- **Digital design concepts:** Conceptual input and definition of requirements for the digital part of XIDer's readout ASIC.
- **Analog-to-digital interface and mixed-signal verification:** In cooperation with digital designers, the interface between the analog and digital domains has been designed an implemented. For full-system verifications, the author has performed and analysed mixed-signal simulations.
- **Full chip floorplans:** Execution of and contribution to layout of full chip floorplans for all of the test chips.
- **ASIC Design Submissions:** Six test chips with increasing complexity have been designed in the TSMC 65 nm technology and submitted for manufacturing. Prior to submission, full-chip layouts have been verified via DRC, LVS and ESD checks.

- **Design of ASIC-specific characterisation set-ups:** Design and preparation of characterisation set-ups for every ASIC prototype iteration. This includes the design of dedicated ASIC carrier PCBs with integrated circuitry, the test set-up control FPGA firmware as well as a software framework for the ASIC control and data readout with a graphical user interface. Beyond the ASIC-specific characterisation, the firmware and the framework have also been used as a basis for assembly prototype measurements at ESRF beamlines.

- **ASIC characterisation measurements:** Execution and in-depth analysis of isolated test chip characterisation measurements. Furthermore, the author has supported and participated in laboratory tests of ASICs at the ESRF and the corresponding data analysis. The performed measurements allowed the verification of the performance of the implemented circuit modules. In addition, valuable insight for the optimisation of the front-end performance has been gathered.

- **Prototype ASIC-sensor assembly verification:** For the very first ASIC-sensor assemblies, a laser-based test set-up has been designed and functional tests have been performed.

- **Design of beamline-specific characterisation set-ups:** Contribution and support for the design of test set-ups for ASIC-sensor assemblies at ESRF-beamlines.

- **ESRF beamline measurements:** Contribution to the preparation and execution of several characterisation tests of assemblies with CdTe and CZT sensors at the ESRF's BM05 beamline. Furthermore, the author participated in and supported the analysis of the acquired data with ASIC-specific insight.

- **Representation through publications and participation at conferences:** First authorship of two publications [73] and [87] and co-authorship in several other publications. In addition, the author represented the XIDer collaboration with several talk and poster contributions at conferences like IEEE and ULITIMA.

A Additions to System Theory

A.1 The Impulse Response

System theory aims to find a general expression for the transformation performed by a system. The following explanations and derivations are supposed to provide an intuitive understanding of how this goal is achieved.

The starting point is an arbitrary LTI system as shown in figure A.1. If the system is provided with a rectangular input signal $s_0(t)$ of width T_0 and amplitude $\frac{1}{T_0}$, its output signal response $g_0(t)$ is shaped as depicted on the right-hand side. The width and amplitude of the rectangular pulse are chosen such that its time integral as well as the integral of output response are constant. As depicted in figure A.2, one can use $s_0(t)$ to approximate an arbitrary input signal $s(t)$. In this approximation, a sum of time-shifted versions of $s_0(t)$ is applied to reconstruct the course of $s(t)$ via a step function $s_a(t)$:

$$s(t) \approx s_a(t) = \sum_{n=-\infty}^{\infty} s(nT_0)s_0(t - nT_0)T_0. \tag{A.1}$$

Since the width of a single rectangular pulse is given by T_0, the individual pulses are shifted by an integer multiple n of T_0. In order to correctly approximate the amplitude of $s(t)$ at $t = nT_0$, the normalized rectangular pulse with the amplitude $\frac{1}{T_0}$ has to be multiplied with T_0 as well as $s(nT_0)$.

Due to the fact that LTI systems are linear and time-invariant, the system response $g(t)$ to $s(t)$ can now be approximated as a sum of responses to the individual rectangular pulses. The result is

$$g(t) \approx g_a(t) = \sum_{-\infty}^{\infty} s(nT_0)g_0(t - nT_0)T_0. \tag{A.2}$$

Intuitively, it is obvious that decreasing T_0 will result in a more accurate approximation of the input signal $s(t)$. This is due to the fact that a smaller T_0 causes narrower individual rectangular pulses. Approaching the limit $T_0 \to 0$, the rectangular pulse turns into the dirac delta distribution $\delta(t)$. Since this turns the sum in equation A.1 into a summation

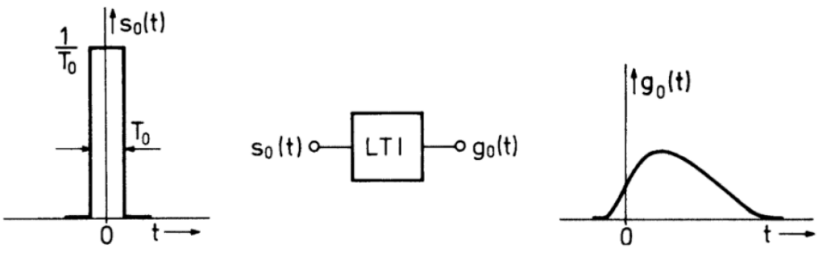


Figure A.1: Arbitrary LTI system with a normalized rectangular input pulse $s_0(t)$ and its corresponding response $g_0(t)$ on the left- and right-hand sides. [57].

of infinitesimally narrow pulses, it can be rewritten as an integration:

$$s(t) = \int_{-\infty}^{\infty} s(\tau)\delta(t-\tau)d\tau \tag{A.3}$$

with the substitutions $nT_0 \to \tau$, $T_0 \to d\tau$ and $s_0(t) \to \delta(t)$. Doing the same for $g_a(t)$ results in

$$g(t) = \int_{-\infty}^{\infty} s(\tau)h(t-\tau)d\tau \tag{A.4}$$

in which $g_0(t) \to h(t)$. The function $h(t)$ is called *impulse response* as it describes the circuit's reaction to an input dirac delta pulse $\delta(t)$. And as shown in equation A.4 it allows an exact description of the circuit's response to any input signal $s(t)$. Due to this, both $h(t)$ and $\delta(t)$ are of outstanding importance for system theoretical predictions and calculations regarding electronic circuits and LTI systems in general. Deriving the impulse response allows a complete characterisation of the system of interest.

There are a few more remarks to make about the equations A.3 and A.4 before moving on. Firstly, the dirac delta distribution has great relevance beyond the field of system theory. Its mode of action can be described via the integral

$$\int_{-\infty}^{\infty} x(t) \cdot \delta(t)dt = x(0) \tag{A.5}$$

which is often used as the definition of $\delta(t)$. However, in a mathematical sense this is not a classical Riemann integral. There is no locally integrable function $\delta(t)$ that actually fulfills this condition. In fact, equation A.5 is a symbolic way of describing the evaluation of $x(t)$ at $t = 0$. And in the case of equation A.3 it describes the evaluation of $s(\tau)$ at the time $\tau = t$ which demonstrates that the result of the integral is indeed a perfect reconstruction of $s(t)$. For further reading on properties of the dirac delta distribution, the reader is referred to [100].

Secondly, the integrals used in the evaluation of $s(t)$ and $g(t)$ are known as *convolution integrals*. As an abbreviation the following notation is used:

$$c(t) = \int_{-\infty}^{\infty} a(\tau)b(t-\tau)d\tau = a(t) * b(t) \tag{A.6}$$

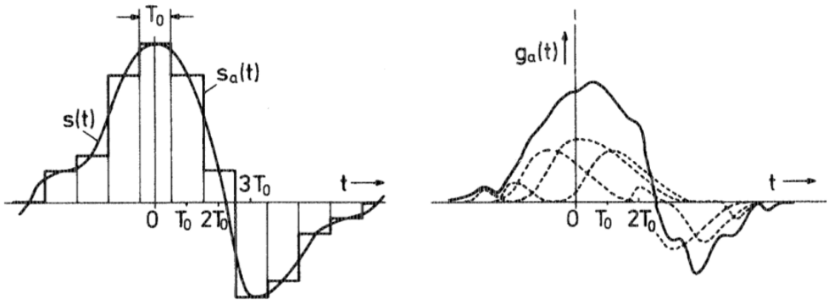


Figure A.2: Left-hand side: Approximation of an arbitrary input signal by using a linear combination of time shifted versions of the rectangular pulse $s_0(t)$ depicted in figure A.1 with different amplitudes. Right-hand side: Output response of the arbitrary LTI system to the approximated input signal [57].

in which $a(t)$, $b(t)$ and $c(t)$ are signals. As illustrated, a convolution maps two input functions, in this case signals, $a(t)$ and $b(t)$ onto an third output function. An exhaustive mathematical description of this operation is beyond the scope of this thesis. Instead, the following list provides a few of its properties which are most important to its application in system theory with LTI systems:

- The dirac delta function $\delta(t)$ acts as the identity element of convolution such that for a signal $s(t)$:
$$s(t) = s(t) * \delta(t) \tag{A.7}$$

- The convolution is a commutative operation such that for two signals $a(t)$ and $b(t)$
$$a(t) * b(t) = b(t) * a(t). \tag{A.8}$$
This can be proven easily by substituting τ with $t - \Theta$ in equation A.4:
$$g(t) = \int_{\infty}^{-\infty} s(t-\Theta)h(\Theta)(-d\Theta) = \int_{-\infty}^{\infty} h(\Theta)s(t-\Theta)d\Theta \tag{A.9}$$
As a result, there is no difference between using the input signal $s(t)$ to stimulate a system with the impulse response $h(t)$ and using an input signal $h(t)$ to stimulate a system with the impulse response $s(t)$. In both cases, the result is the same.

- Convolutions are an associative operation. The convolution of three signals $a(t)$, $b(t)$ and $c(t)$ starts with convolving two of the three signals followed by a second convolution with the remaining signal. The actual order does not affect the result:
$$[a(t) * b(t)] * c(t) = a(t) * [b(t) * c(t)] = [a(t) * c(t)] * b(t). \tag{A.10}$$

- Distributivity: The convolution of a signal $a(t)$ with the sum of other signals $b(t)$ and $c(t)$ is equal to the sum of $a(t) * b(t)$ and $a(t) * c(t)$:
$$a(t) * (b(t) + c(t)) = a(t) * b(t) + a(t) * c(t) \tag{A.11}$$

A more thorough discussion of convolutions can be found in [101].

Finally, as stated before, the impulse response $h(t)$ is the sought for function that allows predicting and calculating a system's reaction to an arbitrary input. However, due to practical reasons, system theoretical calculations with LTI systems usually seek to find the system's *transfer function* which is the Laplace transform of $h(t)$.

A.2 Table of Common Laplace Transforms

$f(t)$	$F(s) = \mathcal{L}_1(f(t))$
$\delta(t)$	1
1	$\frac{1}{s}$
t	$\frac{1}{s^2}$
e^{-at}	$\frac{1}{s+a}$
$\frac{1}{T}e^{-t/T}$	$\frac{1}{Ts+1}$
te^{-at}	$\frac{1}{(s+a)^2}$
$1-e^{-t/T}$	$\frac{1}{s(Ts+1)}$
$sin(\omega t)$	$\frac{\omega}{s^2+\omega^2}$
$e^{-at}sin(\omega t)$	$\frac{\omega}{(s+a)^2+\omega^2}$

Table A.1: List of common one-sided Laplace transforms where the time domain function $f(t) = 0$ for $t < 0$. Taken from [58].

B Basic Analog Circuits

Complex analog circuits are usually built from smaller compartments and subcircuits. This modularisation enables the design and optimisation of circuit compartments with very specific tasks. In some cases, subcircuits can be as small as single transistors biassed in a particular operation region. The following sections introduce basic building blocks that have been used in the design of XIDer's readout ASIC. Their description is based on the references [61] and [60], if not stated otherwise.

B.1 Switches

The task of a switch is to provide an option whether to connect or disconnect two nodes A and B as depicted in figure B.1. On silicon, the simplest implementation of a switch is given by a single transistor in triode region. As discussed in section 4.2.2, the gate-source voltage of the transistor defines whether the switch is closed, i.e. on, or open, i.e. off. If $V_{GS} > V_{th}$, the switch is considered on, otherwise it is considered off. The most important parameters of a switch are its on- and off-resistances r_{on} and r_{off}, where the values of an ideal switch are $r_{on} = 0$ and $r_{off} \to \infty$. In reality though, these values can not be reached. For the single transistor, this is evident from equation 4.44 which describes r_{on} related to its device parameters.

However, the equation shows how to tune those parameters to make r_{on} as small as possible. Firstly, the process parameters μ_n and C_{ox} have to be as big as possible. Secondly, the switch has to be controlled with the largest possible gate voltage to achieve a large V_{GS}. And lastly, the transistor has to have a large W/L ratio. In order to illustrate this, figure B.2 shows an n-MOSFET's r_{on} vs. the applied gate-source voltage for different values of W/L. As a result, the optimal gate voltage for the on-state of an n-MOSFET switch is the highest available level, i.e. $V_{G,on} = V_{supply}$.

When the MOSFET switch is off, i.e. $V_{GS} < V_{th}$, the drain current I_D is mainly dominated by the subthreshold leakage which is $\propto e^{V_{GS}}$. As a result, the corresponding control voltage for the switch's off state $V_{G,off}$ should be chosen as low as possible to increase r_{off} as far as possible. In most cases, the ground level suffices.

Whether an n-type MOSFET is a good choice for the implementation of a switch depends on the application. It can only effectively drive voltages from A to B or vice versa, in a range from V_{gnd} to $V_{G,on} - V_{th} = V_{supply} - V_{th}$ which limits its dynamic range. Thus, in some cases it might be better to use a p-MOSFET switch which can drive voltages from $V_{gnd} + V_{th}$ to V_{supply}. In other cases, one might need the whole range from V_{gnd} to V_{supply}. Then, a parallel combination of an n- and a p-MOSFET should be used. This so-called *transmission gate* is depicted in figure B.3a.

On another note, switches built from MOSFETs suffer from an effect called *clock feedthrough* or *charge injection*. Charge injection finds its origin in the charge $Q_{channel}$

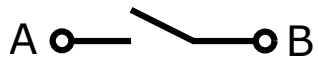


Figure B.1: Schematic symbol of a switch.

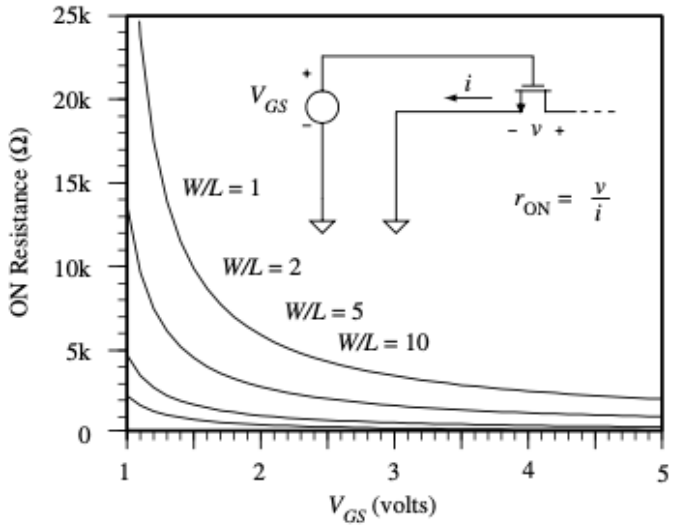
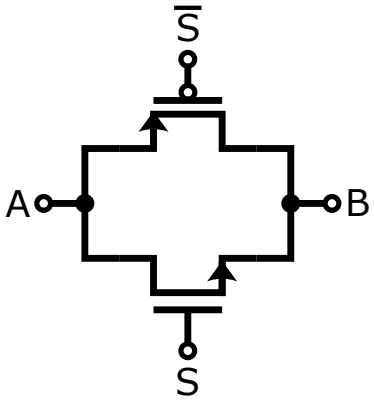
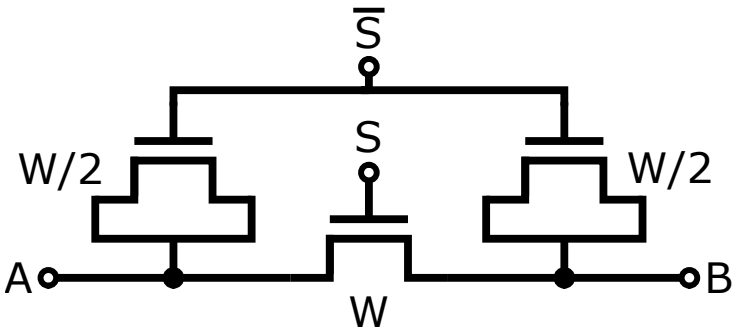


Figure B.2: Resistance of an n-MOSFET switch in its conducting state vs. the applied gate-source voltage for different values of W/L [61].



(a) Transmission gate: the control signal S has to be inverted for the p-MOSFET.



(b) Charge injection cancellation approach with two n-MOSFETs that have half the size of the switch transistor. The gates of the charge cancellation transistors are connected to the inversion of the control signal S.

Figure B.3: Advanced switch circuit diagrams.

that is stored in the transistor's conductive channel, when $V_{GS} > V_{th}$. In order to turn the switch on or off, $Q_{channel}$ has to either be taken from or released to the surrounding nodes. The size of $Q_{channel}$ is proportional to W, L and C_{ox} of the transistor as well as the gate voltages in the switch's on and off state $V_{G,on}$ and $V_{G,off}$. In most cases, $Q_{channel}$ is assumed to split equally between the drain and source terminals. Subsequently, the approach shown in figure B.3b is the default circuit to compensate for charge injection. It uses a MOSFET on either side of the switch with half the switch's size. With their gates connected to the inverted control signal of the switch, they inject a charge of opposite polarity through their parasitic gate-source and gate-drain capacitances. And due to their chosen size, this charge equals to $-\frac{1}{2}Q_{channel}$ per transistor. In general, the assumption of an equal charge split between the drain and the gain is not necessarily true and it depends on the application whether this approach leads to the desired results. As a side note: Since the transmission gate features two charge injections of opposite polarity through the n- and the p-MOSFET, it naturally comes with a clock feedthough suppression. However, in order for this to work, both MOSFETs need to be matched. While theoretically W/L can be chosen equal for both transistors in the design, their different type pronounces process uncertainties which will complicate their matching in a real design.

B.2 Current Mirrors & Cascodes

In order to operate at the desired operating point, many circuits need bias currents. Thus, current sources that generate these biasses are an important and necessary compartment in the design of analog circuitry. A perfect current source is characterized by an infinite output resistance. This is evident from the requirement, that the current generated by the source should not change with the applied voltage. In reality of course, such a source does not exist. However, thanks to the high output resistance r_{out} (see section 4.2.2), a MOSFET in saturation region can fulfill the task of a current source quite well. The idea is shown in figure B.4a for an n-MOSFET. In saturation, the output current I_{out} only slightly depends on the applied V_{out}. In fact, it mostly depends on the applied gate-source voltage. Here, the transistor's source is pinned to the ground potential. Due to this, $V_G (= V_{GS})$ alone has to be tuned such that the drain current has the desired value.

Since the output resistance $r_{out} \propto L/I_D$ (see equation 4.46), the transistor length L has to be chosen large. At the same time, the current source should have a large dynamic range, i.e. a large range for V_{out} in which the transistor remains in saturation region. This is achieved by a low saturation voltage $V_{DS,Sat}$. And as $V_{DS,Sat} = V_{GS} - V_{th} = V_G - V_{th}$, this means that the gate voltage V_G for the desired current has to be low. And in order to accomplish this, the transistor needs to have a large W/L as is evident from equation 4.40. However, due to the fact that L should be chosen large for a large output resistance, designers can only increase W to achieve a decently low saturation voltage.

In order to generate the correct gate voltage for the desired current, a *current mirror* as depicted in figure B.4a is used. Current mirrors are based on the fact that the drain currents of two equal MOSFETs with the same gate-source voltage are equal. To conduct the current I_{in}, the diode-connected input transistor M_1 has to raise its drain- and gate-voltages to the corresponding value following equation 4.40. And with the assumption that μ_n and C_{ox} are equal for both M_1 and M_2, the output current is then given by

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} \cdot I_{in}. \tag{B.1}$$

(a) Simple (b) Cascoded

Figure B.4: Current mirror circuit diagrams

This equation illustrates two important features of the current mirror. Firstly, when ignoring the channel-length modulation, then the ratio I_{out}/I_{in} only depends on the ratio ${}^{(W/L)_2}/_{(W/L)_1}$. As a result, the current mirror can not only generate a one-to-one copy $I_{out} = I_{in}$, but it can also multiply or divide the input current. And the factor for this multiplication/division can be tuned via the transistor dimensions. Secondly, the channel-length modulation adds a V_{DS} dependency to this factor. This is due to the fact that, in general, $V_{DS1} \neq V_{DS2}$. Subsequently, the actual mirrored current I_{out} is off by the factor $(1 + \lambda V_{DS2})/(1 + \lambda V_{DS1})$. And since V_{DS2} is the circuit's output voltage, this means that output resistance of the current mirror is deteriorated by the channel-length modulation. Due to the fact that $\lambda \propto 1/L$, M_1 and M_2 have to be chosen long to minimize the influence of this effect.

Another tool to cope with the channel-length modulation, is the so-called *cascode*. The idea of a cascode is to pin the drain voltages of M_1 and M_2 to the same voltage to ensure that $V_{DS1} = V_{DS2}$. Its implementation is depicted by transistor M_3 in figure B.4b. If M_3 is operated in saturation region, its large-signal source voltage is given by

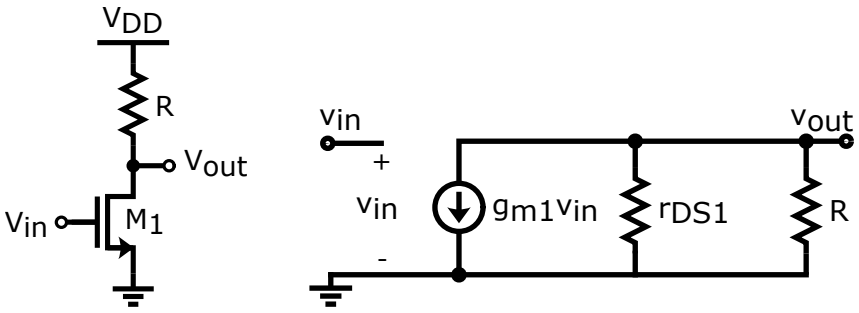
$$V_{S3} = V_{DS2} = V_{casc} - V_{th_3} - \sqrt{I_{in}\frac{2}{\mu_n C_{ox}}\frac{L_3}{W_3}} = V_{casc} - V_{th_3} - V_{DS,Sat3}, \tag{B.2}$$

where V_{casc} is the cascode bias or gate voltage. With a high W and a small L, the last term in this equation can be neglected and since V_{th} is a constant, V_{DS2} is solely $\propto V_{casc}$. In order to match V_{DS1} and V_{DS2}, the cascode bias voltage has to be chosen such that $V_{DS1} = V_{casc} - V_{th}$.

In the small-signal model, the cascode causes an increase of the current mirror's output resistance

$$r_{out,CM,casc} = \frac{v_{out}}{i_{out}} = r_{out3} + r_{out2} + g_{m3} r_{out3} r_{out2} \approx g_{m3} r_{out3} r_{out2} \tag{B.3}$$

in which r_{outi} and g_{mi} are the drain-source as well as the transconductances of the corresponding transistors M_i. Since in general, $r_{outi} << g_{m3} r_{out3} r_{out2}$, the equation above is dominated by the last term. Subsequently, in order to achieve a high output resistance $r_{out,CM,casc}$, the cascode needs to have a large transconductance. Thus, the same conclusion can be made as for equation B.2: $(W/L)_3$ has to be chosen large. In addition, L_2 and L_3 should be chosen large to achieve high source-drain resistances r_{out2} and r_{out3} respectively.



(a) Schematic drawing.

(b) Small-signal equivalent excluding parasitic capacitances.

Figure B.5: Common-source amplifier stage with resistive loading. The supply voltage is denoted as V_{DD}.

The choice of the bias cascode bias V_{casc} is a task on its own. There is a wide variety of automated biassing circuits to fulfill this function. For more details on these as well as more advanced current mirror and cascode circuits, the reader is referred to analog electronics design literature like [60].

B.3 Voltage Amplifiers

In almost every sensor readout chip, there is some sort of amplification circuit. The most common use case is the amplification of the analog sensor output signal to prepare it for further processing by subsequent circuitry. And in most cases, these amplifiers have to meet many requirements at once to fulfill the ever-growing demands of state-of-the-art detectors. Large gain, low noise, high bandwidth, high dynamic range and low power consumption are a few very common examples. While this section discusses only very basic amplifier structures, the presented concepts are necessary in the understanding of the actually employed, more complex designs.

B.3.1 Single-Ended

One of the simplest voltage amplifier stages in CMOS is the single-ended common-source stage with a resistive load as depicted in figure B.5a. Understanding its operation principle provides a very intuitive view on how amplifiers work in general. The starting point is the input voltage V_{in} which is supposed to be amplified. It is connected to the gate of the input transistor M_1. Since M_1's source is connected to the fixed ground potential, V_{in} is its gate-source voltage V_{GS1}. From the small-signal model, it is known that a MOSFET transistor, such as M_1 in the diagram, converts changes in its gate-source voltage V_{GS} to changes in its drain current I_D. The factor related to this conversion is the transconductance g_{m1}, such that the generated small-signal current i_D is given by $i_D = g_m v_{GS}$. i_D, in turn, flows through the resistor R at the top of the circuit which converts the current back to a voltage – the output voltage $v_{out} = R \cdot i_D$. From this intuitive view, one can already make the assumption that the gain has to be related to a multiplication of the conversion factors of both components in action: $(v_{out}/v_{in})_{assumed} \propto g_{M1} \cdot R$. Here, M_1 is assumed to be in the saturation region.

The small signal model allows calculating the actual gain $(v_{out}/v_{in})_{res}$ with the corresponding equivalent circuit diagram drawn in figure B.5b. For now, parasitic capacitances

are excluded. With Kirchhoff's laws, the gain can be determined as

$$\left(\frac{v_{out}}{v_{in}}\right)_{res} = -g_{M1}(r_{DS1} \parallel R) = -g_{M1}\frac{r_{DS1}R}{r_{DS1}+R} = g_{M1}R_{tot}. \tag{B.4}$$

So indeed, the gain is related to a multiplication of the two conversion factors g_{M1} and R. However, the transistor's source-drain resistance r_{DS1} acts in parallel to R. As a result, the conversion of the drain current to the output voltage is performed by $R_{tot} = (r_{DS1} \parallel R)$ instead of only R.

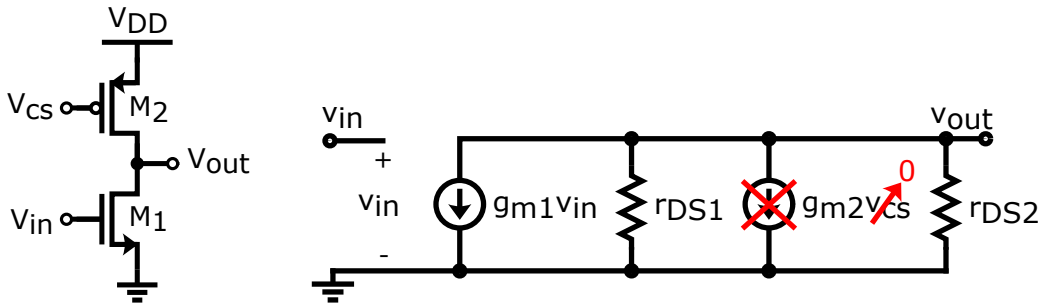
The actual fabrication of a resistor with a well-defined and tightly-controlled resistance proves to be difficult in most CMOS technologies. In order to cope with this, designers usually use active loads which can be implemented via a single transistor or additional subcircuits. Due to the design philosophy of XIDer's readout ASIC, its analog part mostly features current-source loads as depicted in figure B.6a, where the current source is implemented by a p-MOSFET M_2. As a side note: This topology can also be used with a p-MOSFET as the input transistor and an n-MOSFET as the current source.

The corresponding small signal circuit diagram is illustrated in figure B.6b. Just like M_1, the additional transistor M_2 is supposed to be in saturation region. Since the gate-source voltage of the current-source transistor M_2 is constant, its small-signal value v_{CS} is considered 0.[1] As a result, the transconductance g_{M2} of M_2 can be neglected in the calculation. Thus, M_2 only affects the circuit's gain via r_{DS2} and the circuit boils down to the known case of a resistive-loaded gain stage. Following equation B.4, the gain is given by:

$$\left(\frac{v_{out}}{v_{in}}\right)_{cs} = -g_{M1}(r_{DS1} \parallel r_{DS2}) = -g_{M1}\frac{r_{DS1}r_{DS2}}{r_{DS1}+r_{DS2}} \tag{B.5}$$

Increasing the gain of this stage can be achieved by either increasing g_{M1}, r_{DS1} or r_{DS2}. The design parameter dependencies of g_{M1} and r_{DS1} however, prevent a simultaneous increase of both quantities in most cases. Due to this, M_1 is usually tuned for a big g_{M1}, i.e. a large $(W/L)_1$ with a high drain current I_D. And at the same time, M_2 is tuned to have a high output resistance r_{DS2}. If an even higher gain is needed, cascodes can be applied to both M_1 an M_2 to achive higher effective output resistivities as described section B.2.

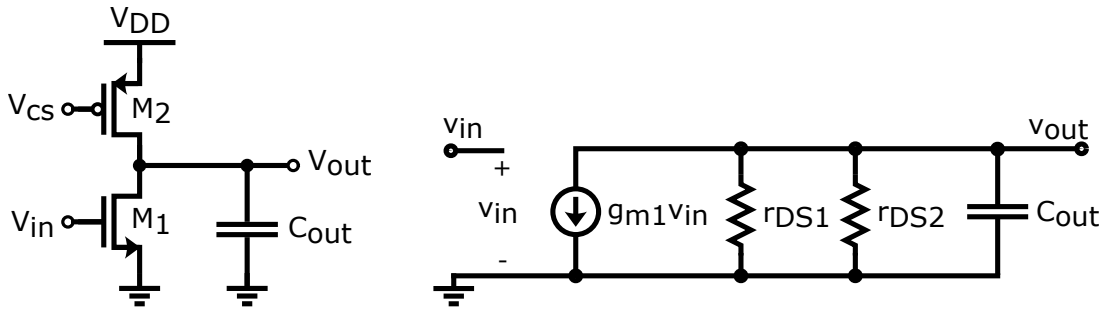
[1] Small-signal quantities represent small variations from their corresponding large signal values (in this case V_{GS2}) which the circuit is biased at. If a voltage is considered constant, there is no variation and its small-signal equivalent vanishes.



(a) Schematic drawing.

(b) Small-signal equivalent excluding parasitic capacitances.

Figure B.6: Common-source amplifier stage actively loaded with a current source.



(a) Schematic drawing.

(b) Small-signal equivalent excluding parasitic capacitances.

Figure B.7: Common-source amplifier stage actively loaded with a current source and an output capacitance.

Frequency-Dependent Behaviour

Up to this point, the common source gain stage has only been examined in the DC case. A very common configuration in actual circuits is the one shown in figure B.7a, where the amplifier has to drive a capacitive load C_{out} at its output. When moving to higher frequencies, this output capacitor starts affecting the circuit's performance. This influence can be studied by deriving the system's transfer function $H_{cs}(s)$. It can be calculated by applying Kirchhoff's current law at the v_{out}-node in the small-signal circuit diagram as shown in figure B.7b:

$$g_{M1}v_{in} = -\frac{v_{out}}{r_{DS1} \parallel r_{DS2} \parallel Z_{C_{out}}},$$

where $Z_{C_{out}} = 1/(sC_{out})$. With this, $H_{cs}(s)$ is given as

$$H_{cs}(s) = \frac{v_{out}(s)}{v_{in}(s)} = -\frac{g_{M1}r_{out}}{1 + sr_{out}C_{out}}, \qquad r_{out} = (r_{DS1} \parallel r_{DS2}). \tag{B.6}$$

As can be seen, for low frequencies, i.e. $H_{cs}(0)$, the circuit exhibits the same gain $|H_{cs}(0)| = g_{M1}r_{out} = g_{M1}(r_{DS1} \parallel r_{DS2})$ as in the previous discussion. But the equation also shows that this circuit behaves like an RC-lowpass with a single pole at $s_P = 1/(r_{out}C_{out})$. As discussed in section 4.1.3.2, this means that the gain of the circuit starts dropping significantly for frequencies higher than s_P. In equivalence to the RC lowpass (see equations 4.32 and 4.33), the gain and phase are

$$|H_{cs}(j\omega)| = \frac{g_{M1}r_{out}}{\sqrt{1 + (\omega r_{out}C_{out})^2}} = \frac{g_{M1}}{C_{out}}\sqrt{\frac{1}{(1/r_{out}C_{out})^2 + \omega^2}} \tag{B.7}$$

$$\phi_{cs}(j\omega) = arctan(-\omega C_{out}r_{out}). \tag{B.8}$$

As a result, this circuit's frequency response is equal to that of an RC lowpass with two exceptions. First, it exhibits a dc gain of $g_{M1}r_{out}$, instead of just 1. As a result, an amplifier's bandwidth can also be characterised by the frequency at which its gain has dropped to 1, instead of the 3dB frequency. This is the so-called *unity gain bandwidth*. In case of the discussed amplifier structure, the unity gain bandwidth equals the so-called *gain-bandwidth-product*:

$$GBW = \omega_P|H_{cs}(0)| = \frac{g_{M1}}{C_{out}}, \tag{B.9}$$

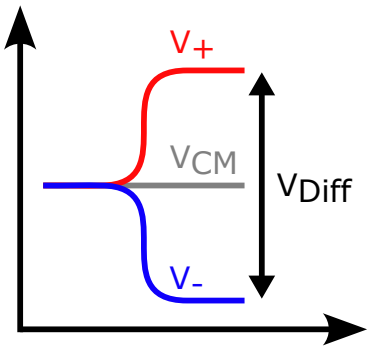


Figure B.8: Differential signalling

where ω_P is the angular pole frequency.

Second, the output voltage of amplifiers with this architecture is inverted with respect to v_{in}. This is evident from the negative sign in the transfer function (equation B.6). As a result, there is an additional phase shift of -180° in addition to the value of $\phi_{cs}(j\omega)$.

B.3.2 Differential

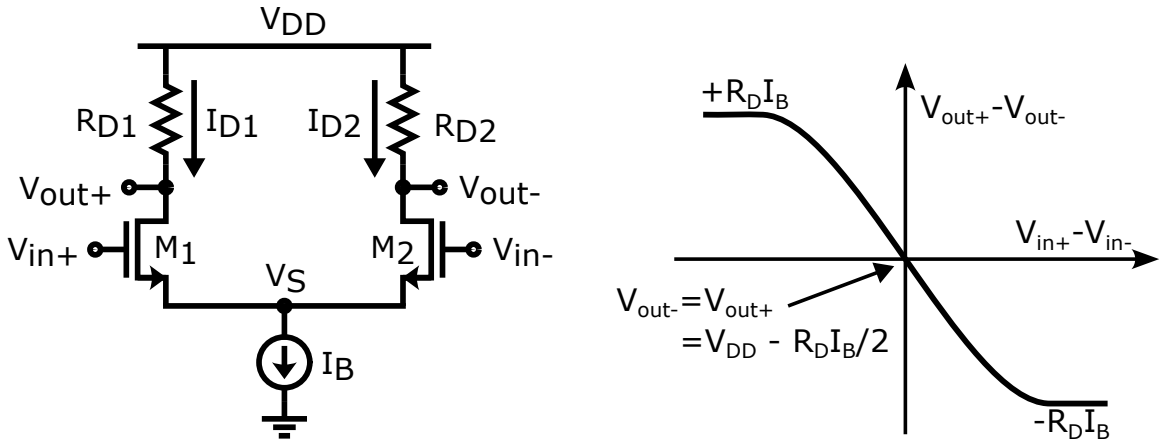
Instead of single-ended circuits, the analog part of XIDer's readout ASICs is almost fully designed with differential implementations. In differential designs, signals are not measured in reference to a fixed value, such as the ground potential for voltages. Instead, differential signals are defined as the difference of the values of two signals V_+ and V_- on seperate nodes or wires: $V_{Diff} = V_+ - V_-$. On top, a differential signal exhibits a so-called *common-mode* level $V_{CM} = (V_+ + V_-)/2$ which can be understood as a center potential. Both V_+ and V_- evolve around the common-mode level with amplitudes of equal size but opposite polarity. As depicted in figure B.8, they act like mirrored version of each other.

Differential designs usually hold several advantages compared to the single-ended approach. One of these is the so-called *common-mode rejection*. Whether a signal is transferred from one circuit to the next via a long connection or it is processed in a circuit, several noise sources can affect its actual value. In a differential design however, both V_+ and V_- are affected. And since the noise coupling usually acts with the same polarity on V_+ and V_- its effect is less pronounced in V_{Diff}. Ideally, the noise couples equally into both V_+ and V_-. Then, the differential signal itself is unaffected by this so-called *common-mode noise*. Other advantages of differential signals are the availability of larger voltage swings and simpler biassing.

One of the simplest differential amplifier architectures in CMOS technology is the *differential pair* shown in figure B.9a. As with the single-ended amplifier, this circuit can also be implemented with p-MOSFETs. For clarity however, the following descriptions focus on the depicted n-MOSFET configuration.

In the illustrated circuit, M_1 and M_2 act as the input transistors for the differential signal $V_{in,diff} = V_{in+} - V_{in-}$. The sources of M_1 and M_2 are shorted and connected to a current source driving the current I_B. Both sides are loaded with the load resistors R_{D1} and R_{D2}, respectively, which are chosen to be equal $R_{D1} = R_{D2} = R_D$. And finally, the amplifier's differential output $V_{out,diff}$ is given by the difference of the MOSFETs' drain voltages V_{out+} and V_{out-}.

The idea of this circuit is to share the current I_B between both sides. In the special case that $V_{in+} = V_{in-}$, i.e. $V_{in,diff} = 0\,\mathrm{V}$, I_B is shared equally with $I_B/2$ flowing through both M_1 and M_2. Subsequently, the voltage drop on the resistors R_{D1} and R_{D2} is equal:



(a) Circuit diagram. (b) Input-output voltage characteristics.

Figure B.9: Differential pair

$V_{R_D} = R_D I_B/2$. And as a result, $V_{out+} = V_{out-} = V_{DD} - V_{R_D} = V_{DD} - R_D I_B/2$ which leads to a differential output voltage of $V_{out,diff} = 0\,\mathrm{V}$. Thus, if the amplitude of the differential input signal is 0 V, so is the amplitude of the output. This state is depicted in the middle of the voltage input-output characteristics of the differential pair in figure B.9b.

If $V_{in,diff} \neq 0\,\mathrm{V}$, e.g. such that $V_{in+} > V_{in-}$, then the gate-source voltage of M_1 is larger with respect to that of M_2. As a result, M_1's current I_{D1} rises, while M_2's current I_{D2} is lowered. Subsequently V_{out+} decreases, while V_{out-} increases. At high enough values of $V_{in,diff}$, i.e. if V_{in-} is small enough, M_2 turns off. When neglecting subthreshold currents, this means that M_1 conducts all the available current, i.e. $I_{D1} = I_B$ and $I_{D2} = 0\,\mathrm{A}$. Due to the fact, that increasing $V_{in,diff}$ above this point will not result in a further change of I_{D1} or I_{D2}, this state marks the maximum differential output voltage amplitude that can be achieved with this circuit. Since M_2 is off, V_{out-} is equal to the supply voltage V_{DD}. At the same time, V_{out+} is given by the voltage drop generated by the current I_B flowing through the resistor $R_{D1} = R_D$: $V_{out+} = V_{DD} - R_D I_B$. Subsequently, the maximum differential output amplitude is given by:

$$|V_{out,diff}|_{max} = R_D I_B. \tag{B.10}$$

As a side note: Whether the circuit can actually reach $|V_{out,diff}|_{max}$ depends on the input common mode $V_{in,CM}$. This is due to the fact that in the desired operation region, i.e. M_1 and M_2 are in saturation, the voltage of node S, V_S, is dictated by $V_{in,CM}$. Since the voltages of the two output nodes can not be smaller than V_S, the actual value of $|V_{out,diff}|_{max}$ is given by $min[R_D I_B,\ V_{DD} - V_S \approx V_{DD} - (V_{in,CM} - V_{th})]$.

As can be seen in figure B.9b, there is a *linear region* around $V_{in,diff} = 0\,\mathrm{V}$, in which the gain is maximized. It turns out that this is where both M_1 and M_2 are in saturation region. Since the gain is maximized in the linear region, this is the desired operation region of the differential pair. Thus, for further small-signal calculations, the circuit is assumed to be biassed at $V_{in,diff} = 0$.

Small-Signal Gain

There are several ways to determine the small-signal gain of this circuit. One of these is the *half-circuit* method which splits the differential pair into two equal, symmetric sides as depicted in figure B.10. The half-circuit method relies on the fact that the V_S acts as a

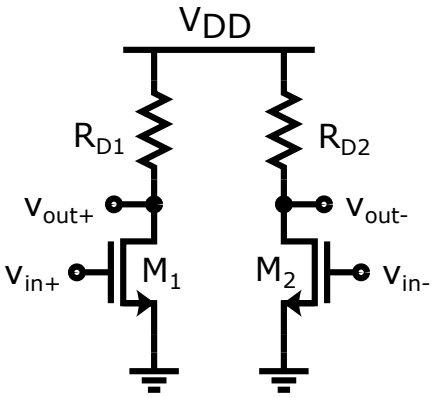


Figure B.10: Differential pair split into two common-source stages after applying the half-circuit method.

fixed voltage in the linear region, as long as the channel-length modulation is neglected. Subsequently, it can be considered a (virtual) ground for small-signal calculations. As demonstrated, this splits the differential pair into two common-source amplifiers, one for each half. As a result, the voltage gain of the differential pair can easily be found by the use of equation B.4. For the left hand side, the gain is

$$\left(\frac{v_{out+}}{v_{in+}}\right)_{cs,left} = -g_{m1}(R_{D1} \parallel r_{DS1}) = -g_{m1}R_{tot1},$$

while for the right hand side, it is given as

$$\left(\frac{v_{out-}}{v_{in-}}\right)_{cs,right} = -g_{m2}(R_{D2} \parallel r_{DS2}) = -g_{m2}R_{tot2}.$$

With the simplifications $g_{m1} = g_{m2} = g_m$ and $R_{tot1} = R_{tot2} = R_{tot}$, the total differential gain can be calculated via:

$$\frac{v_{out+} - v_{out-}}{v_{in+} - v_{in-}} = \frac{v_{out+} - v_{out-}}{2v_{in+}} = \frac{v_{out+}}{2v_{in+}} - \frac{v_{out-}}{-2v_{in-}} = -g_m R_{tot}. \tag{B.11}$$

At first glance, the gain of the differential pair seems to be equal to that of a single ended common-source amplifier. However, as stated before, the differential pair exhibits its maximum gain at $V_{in,diff} = 0$. At this point, the current $I_{D,diff} = I_{D1} = I_{D2}$ flowing through either transistor is $I_B/2$. Subsequently, with equation 4.45, the differential pair's transconductance is only

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_{D,diff}} = \sqrt{\mu_n C_{ox}\frac{W}{L}I_B}. \tag{B.12}$$

As a result, for the same current consumption, the effective transconductance and thus the gain of a differential pair are reduced by the factor $1/\sqrt{2}$ compared to its single-ended counterpart.

Active Current-Mirror Load

In actual circuits, the current source at the bottom of the differential pair is implemented via a current-source transistor. And just as for the single-ended common-source stage,

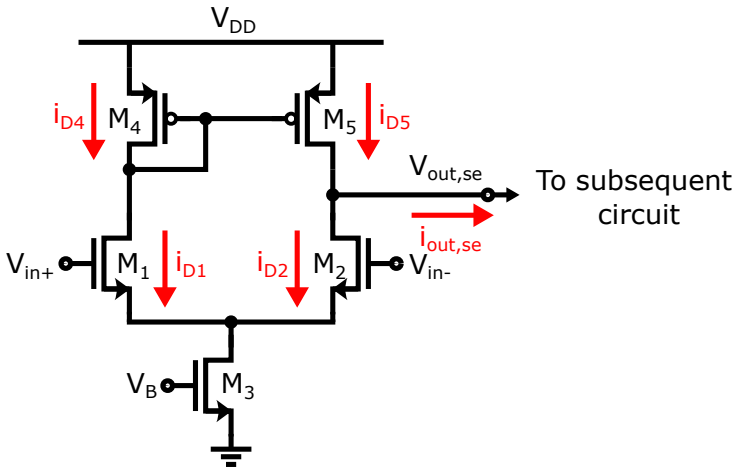


Figure B.11: Differential pair with an active current mirror load converting the differential to a single-ended output. Small-signal currents are indicated in red.

instead of resistors, designers use a wide variety of different subcircuits to implement the loads of the differential pair. Besides the aforementioned staticly biassed current-source transistors, a commonly used approach in the design of XIDer's readout ASIC is the active current-mirror load as depicted in figure B.11. The reason for using this approach for XIDer is that in most cases, the analog front-end only requires a single node of the differential pair's output for further processing. And instead of discarding the signal on the other unused node, the active current mirror uses it to boost the amplifier's gain. In the depicted circuit, this is implemented with the two p-MOSFETs M_4 and M_5. In order to understand the effect of the active current mirror, the depicted circuit diagram also features the small-signal currents flowing through M_1, M_2, M_4 and M_5. For the sake of simplicity, the current source M_3 is assumed to be perfect, i.e. $r_{out3} \to \infty$.

Each M_1 and M_2 experience a small-signal input voltage with half the amplitude of the differential input signal $v_{in,diff}$. As a result, with the assumption that $g_{m1} = g_{m2}$, the small-signal drain currents generated from this voltage are given by

$$i_{D1/2} = \pm\frac{g_{m1}}{2} v_{in,diff}. \tag{B.13}$$

In turn, the current flowing through M_4 is equal to that flowing through M_1:

$$i_{D4} = i_{D1} = \frac{g_{m1}}{2} v_{in,diff}. \tag{B.14}$$

And assuming that M_4 and M_5 have equal device parameters, M_4's drain current is mirrored to M_5, such that $i_{D4} = i_{D5}$.

Since the drain current of M_2 is fixed to i_{D2}, the excess current can only leave the amplifier through the $v_{out,se}$-node. In turn, the amplifier's output current $i_{out,se}$ is

$$i_{out,se} = i_{D5} - i_{D2} = i_{D1} - i_{D2} = g_{m1} v_{in,diff}. \tag{B.15}$$

Thus, from comparison with equation B.13, the effective transconductance for single-ended output operation is doubled by the addition of the active current mirror load. With the actual application of the small-signal model as well as elaborate calculations, the

low-frequency gain can be determined as

$$\frac{v_{out,se}}{v_{in,diff}} = g_{m1}(r_{DS2} \parallel r_{DS4}). \tag{B.16}$$

Here, $v_{out,se}$ is the single-ended output voltage and $v_{in,diff}$ is the differential input voltage.

As a summary, the differential pair loaded with an active current mirror can be used to convert a differential voltage into an amplified single-ended version. The differential-to-single-ended voltage gain achieved in this operation is equal to the differential-to-differential voltage gain of a differential pair with resistive loading. However, in both the differential and the single-ended output case, the effective transconductance is reduced by a factor of $1/\sqrt{2}$ compared to a common source stage with equal current consumption.

The core amplifier of XIDer's analog front-end uses a structure which is similar to the differential pair with active current mirror loading. Section 6.2.1 provides a more thorough study including the actual frequency response to gain more insight into the important device parameters.

C Front-End Amplifier Small-Signal Calculation Add-Ons

C.1 Open-Loop DC Voltage Gain

For the DC voltage gain, the circuit has to be substituted with a small-signal model. A simple approximation can be done in a very similar way to what has been shown for the differential pair with an active current mirror load but without the folded cascodes in section B.3.2. In order to calculate the gain $A_v = v_{out}/v_{in}$, the amplifier's transconductance $g_{mA} = i_{out}/v_{in}$ as well as its output resistance $r_{outA} = v_{out}/i_{out}$ have to be determined. With these A_v is given as

$$A_v = -g_{mA} r_{outA}. \tag{C.1}$$

With figure C.1, the calculation of g_{mA} works as follows: As before, the circuit is biassed at $V_{ref} = V_{in}$. A small-signal voltage v_{in} at the input node leads to a small-signal drain current i_{D2} in M_2. Since V_{ref} is a fixed bias voltage, its corresponding small-signal voltage is $v_{ref} = 0\,\mathrm{V}$ and no small-signal current is generated in M_1. Due to this, the assumption that the input of a differential circuit is given by a differential signal with a fixed common-mode voltage no longer holds. In this configuration, the common-mode voltage of the differential input actually moves with the input signal. As a result, the amplitude of v_{in} splits up into two parts: a differential component

$$v_{in,d} = \frac{v_{in} - v_{ref}}{2} = \frac{v_{in}}{2} \tag{C.2}$$

and a common-mode component

$$v_{in,cm} = \frac{v_{in} + v_{ref}}{2} = \frac{v_{in}}{2}. \tag{C.3}$$

Subsequently, half of the input voltage contributes differentially to an output voltage $v_{out,d}$ with the gain $A_{v,d}$. The other half contributes with a common-mode shift, generating a voltage $v_{out,cm}$ via the gain $A_{v,cm}$ at the output. In the end, the total small-signal output voltage is given by

$$v_{out,tot} = v_{out,d} + v_{out,cm} = A_{v,d} v_{in,d} + A_{v,cm} v_{in,cm} = (A_{v,cm} + A_{v,d}) \frac{v_{in}}{2}. \tag{C.4}$$

The calculation of $A_{v,d} = -g_{mA} r_{outA}$ is performed with the help of figure C.1. The differential component $v_{in,d}$ causes a current $i_{D1} = g_{mA,d} v_{in,d}$ in the input transistor M_2. Due to the high drain-source resistance of M_5, the current i_{D5} is fixed. Thus, in order to fulfill Kirchhoff's current law: $i_{D1} = -i_{D2}$ At V_M, the current splits into a component i_{casc} that flows through the folded cascode and another one i_{D3} through M_3. The folded cascode and M_3 are in parallel connection which is why the i_{casc} can be determined via

$$i_{casc} = \frac{r_{ds3}}{\frac{1}{g_{m6}} + r_{ds3}} i_{D1}. \tag{C.5}$$

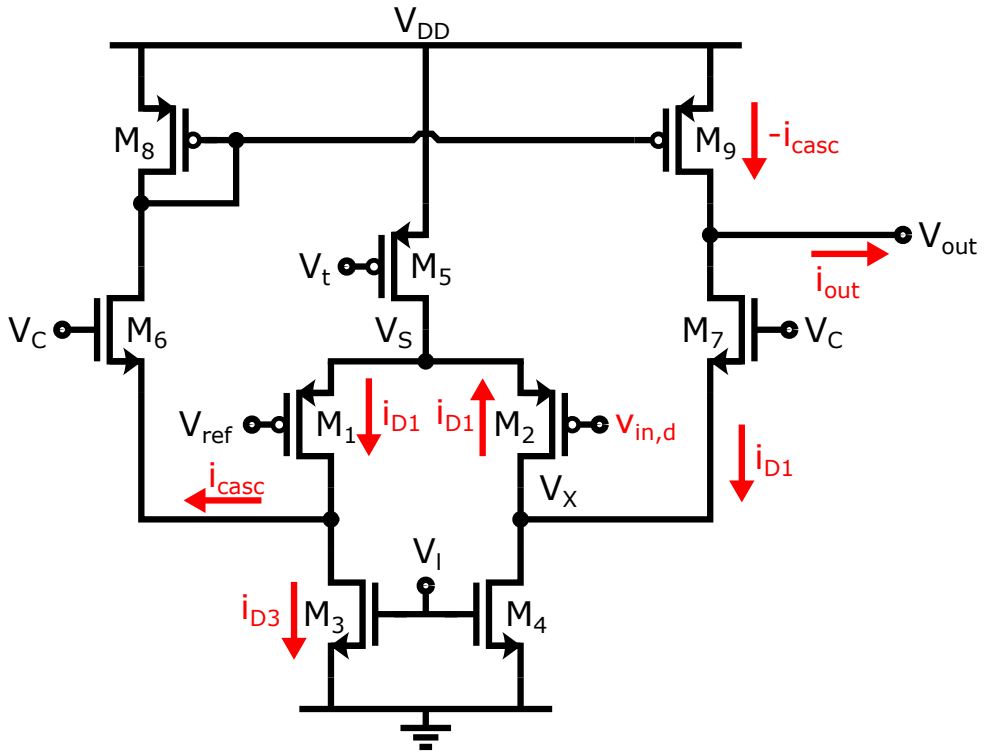


Figure C.1: Differential amplifier in the CSA of XIDer's front-end stage with small signal currents as a reaction to the differential component $v_{in,d}$ of the input voltage v_{in}.

If r_{ds3} is large enough, then $i_{casc} = -i_{D1}$. At last, the active current mirror mirrors i_{casc} from the folded cascode on the left to the folded cascode on the right, such that $i_{D9} = -i_{casc}$. As a result, the circuit's output current is given as

$$i_{out,d} = i_{D9} - i_{D1} = -i_{casc} - i_{D1} = -\left(\frac{r_{ds3}}{\frac{1}{g_{m6}} + r_{ds3}} + 1\right) i_{D1} = -\left(\frac{r_{ds3}}{\frac{1}{g_{m6}} + r_{ds3}} + 1\right) g_{m2} v_{in,d}. \tag{C.6}$$

Hence, with $g_{m2} = g_{m1}$, g_{mA} can be determined as

$$g_{mA,d} = \left(\frac{r_{ds3}}{\frac{1}{g_{m6}} + r_{ds3}} + 1\right) g_{m1} \approx 2 g_{m1}, \tag{C.7}$$

where the final approximation holds, if $r_{ds3} \gg \frac{1}{g_{m6}}$.

The amplifier's output resistance r_{outA} can be estimated with the known behaviour of cascodes. r_{outA} is formed by a parallel connection of r_{ds9} with the cascoded parallel connection of r_{ds2} and r_{ds4}. Subsequently r_{outA} is calculated via

$$r_{outA} \approx r_{ds8} \parallel g_{m6} r_{ds6} (r_{ds1} \parallel r_{ds3}) \tag{C.8}$$

$$\tag{C.9}$$

$$\approx \frac{g_{m6} r_{ds1} r_{ds3} r_{ds6} r_{ds8}}{g_{m6} r_{ds1} r_{ds3} r_{ds6} + r_{ds3} r_{ds8}} \tag{C.10}$$

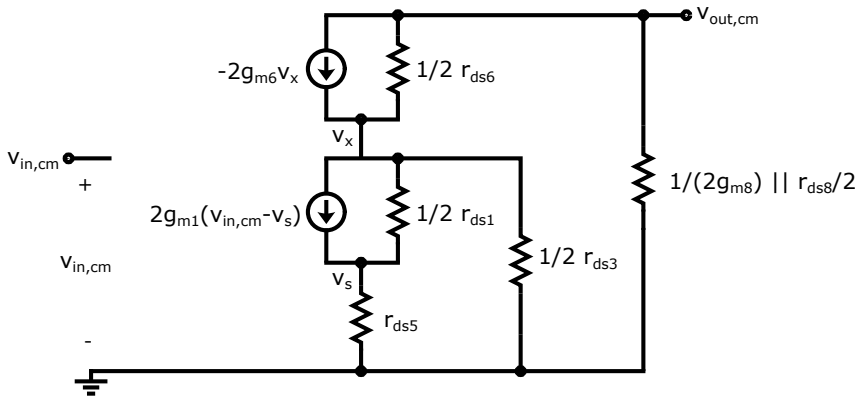


Figure C.2: Small-signal model equivalent of the differential amplifier in the CSA of XIDer's front-end for the calculation of the common mode gain $A_{v,cm}$.

with $r_{ds8} = r_{ds9}$, $r_{ds6} = r_{ds7}$, $r_{ds3} = r_{ds4}$ and $g_{m6} = g_{m7}$. As a result, $A_{v,d}$ is given as

$$A_{v,d} = -g_{mA,d} r_{outA} \approx -\frac{g_{m1} g_{m6} r_{ds1} r_{ds3}^2 r_{ds6} r_{ds8}}{(1/g_{m6} + r_{ds3})(g_{m6} r_{ds1} r_{ds3} r_{ds6} + (r_{ds1} + r_{ds3}) r_{ds8})} \propto -\frac{\sqrt{I_T}}{I_T/2 - I_L} \tag{C.11}$$

The calculation of $A_{v,cm}$ on the other hand can be performed with figure C.2 as a basis. Following the example of the common mode gain calculataion on p. 155 in [60] for a similar circuit, the displayed equivalent circuit relies on the assumption that a shift in the common mode affects both circuit sides symmetrically. Thus, the drain nodes of M_8 and M_9 as well as those of M_1 and M_2 are considered shorted. With Kirchhoff's current law, the following set of equations can be found at the nodes $v_{out,cm}$, v_x and v_s:

$$\frac{v_{out,cm}}{\frac{1}{2g_{m8}} \parallel \frac{r_{ds8}}{2}} = -2g_{m6} v_x + 2\frac{v_{out,cm} - v_x}{r_{ds6}} \tag{C.12}$$

$$\tag{C.13}$$

$$-2g_{m6} v_x + 2\frac{v_{out,cm} - v_x}{r_{ds6}} = \frac{v_s}{r_{ds5}} + 2\frac{v_x}{r_{ds3}} \tag{C.14}$$

$$\tag{C.15}$$

$$2g_{m1}(v_{in,cm} - v_s) + 2\frac{v_x - v_s}{r_{ds1}} = \frac{v_s}{r_{ds5}} \tag{C.16}$$

Solving this set of equations leads to

$$A_{v,cm} \approx \frac{2g_{m6} r_{ds3}}{g_{m8} r_{ds5} + g_{m6} g_{m8} r_{ds3} r_{ds5}} \tag{C.17}$$

As expected from the semi-differential structure of the amplifier the common-mode gain $A_{v,cm}$ is very small compared to $A_{v,d}$. For realistic designs, the *common-mode rejection ratio* (CMRR) is in the order of a few hundred: $|A_{v,d}/A_{v,cm}| \approx O(10^2)$. While $A_{v,cm}$ remains an important quantity that should be minimized for the rejection of common-mode noise, it can be neglected in equation C.4 such that

$$v_{out,tot} \approx A_{v,d} \frac{v_{in}}{2}. \tag{C.18}$$

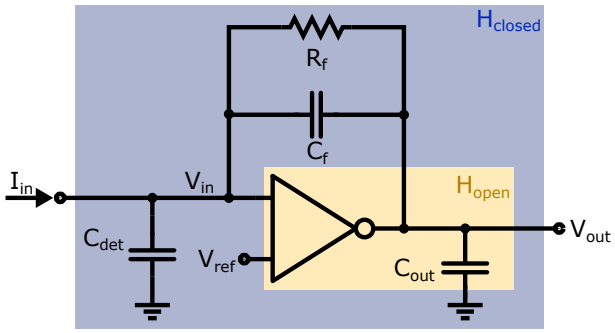


Figure C.3: Charge Sensitive amplifier with a differential amplifier and a feedback capacitor C_f. The reset switch is represented by its resistance R_f which opens a second feedback path parallel to C_f.

and thus

$$A_{v,tot} = \frac{v_{out,tot}}{v_{in}} \approx \frac{A_{v,d}}{2} \approx -\frac{1}{2} g_{m,A} r_{outA} \approx -g_{m1}(r_{ds8} \parallel g_{m6} r_{ds6}(r_{ds1} \parallel r_{ds3})). \tag{C.19}$$

C.2 Closed-Loop Transfer Function

This section gives a motivation for the closed loop transfer function of the CSA in the front-end of XIDer's readout ASIC. For the sake of brevity, it does not feature every single step. Instead, it uses references to text-book examples with similar structures to motivate the most important results.

The final aim of this evaluation is to understand how to increase and optimise the amplifier's speed. In order to achieve this, a good approximation for the closed-loop transfer function $H_{closed}(s)$ that describes the CSA's AC-behaviour has to be found. Figure C.3 is used as a basis for this analysis. It shows the differential amplifier in the CSA's negative feedback scheme. In addition to C_f, there is a feedback path through the resistor R_f which represents the resistance of the reset switch. If the switch is open, R_f is assumed to approach infinity.

For a fed back system like the CSA, it is advisable to first find the open loop transfer function $H_{open}(s)$ ignoring the feedback paths. Here, $H_{open}(s)$ is given by the transfer function of the amplifier. In order to determine $H_{open}(s)$, figure C.4 is used. There are two important and defining capacitors for the ac behaviour. The first one is the output capacitance C_{out} which is a sum of the output load C_{load} as well as the gate-drain capacitances of M_7 and M_9. Since, M_7 and M_9 act in saturation, though, $C_{gd7/9}$ can be neglected and $C_{out} \approx C_{load}$. The second important capacitor is C_{mirr} which is the parasitic capacitance at the gate contact of M_8 and M_9. Its most important contributors are the gate-source capacitances C_{gs8} and C_{gs9}. With the assumption that $C_{gs8} = C_{gs9}$, it can be approximated as $C_{mirr} \approx 2C_{gs8}$.

In good approximation, the amplifier acts like a two-pole system in which both C_{out} and C_{mirr} are responsible for one of the poles, respectively. This is evident from the small-signal analysis of a similar circuit presented on page 190 ff. in [60]. The pole frequencies can be approximated via

$$s_{p,mirr} \approx \frac{g_{m8}}{2C_{mirr}}, \tag{C.20}$$

$$s_{p,out} \approx \frac{1}{r_{out} C_{out}} \approx \frac{1}{r_{ds8} \parallel (g_{m6} r_{ds6}(r_{ds1} \parallel r_{ds3}))C_{out}}, \tag{C.21}$$

where r_{out} is the amplifier's output resistance. As mentioned in the DC analysis, it is given as $r_{out} = r_{ds8} \parallel (g_{m6} r_{ds6}(r_{ds1} \parallel r_{ds3}))$. Since the dc gain has already been approximated in

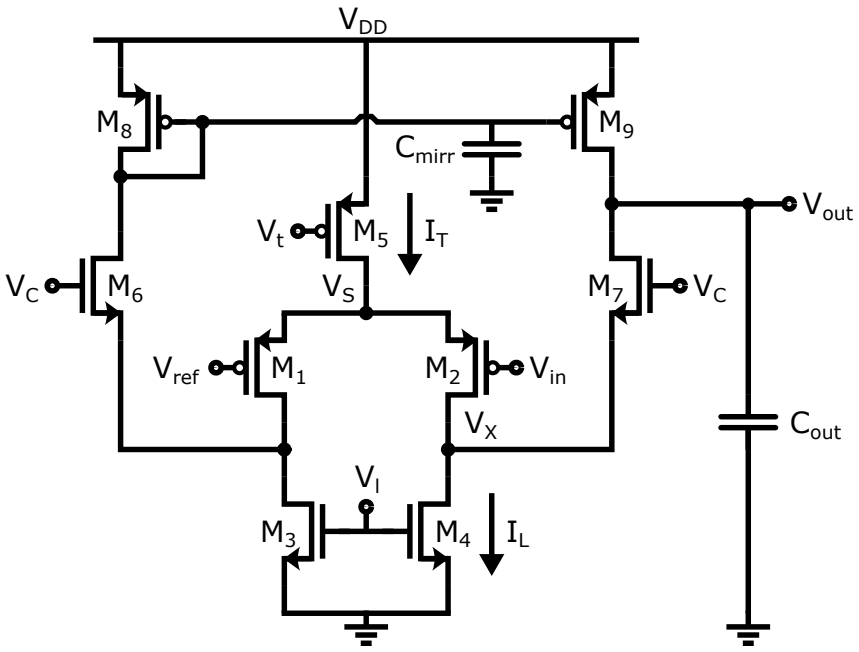


Figure C.4: Circuit diagram of the differential amplifier with the most important capacitors for the approximation of the open-loop transfer function $H_{open}(s)$.

equation 6.19, the amplifier's transfer function can be approximated via

$$H_{open}(s) = \frac{v_{out}(s)}{v_{in}(s)} \approx \frac{A_v}{(1 + \frac{s}{s_{p,mirr}})(1 + \frac{s}{s_{p,out}})}. \tag{C.22}$$

As a sanity check, the plot in figure C.5a shows a comparison of the amplifier's open-loop gain-frequency-dependence from a full-blown analog simulation vs. $|H_{open}(j\omega)|$. As demonstrated, the approximated calculation lies in good agreement with the simulation.

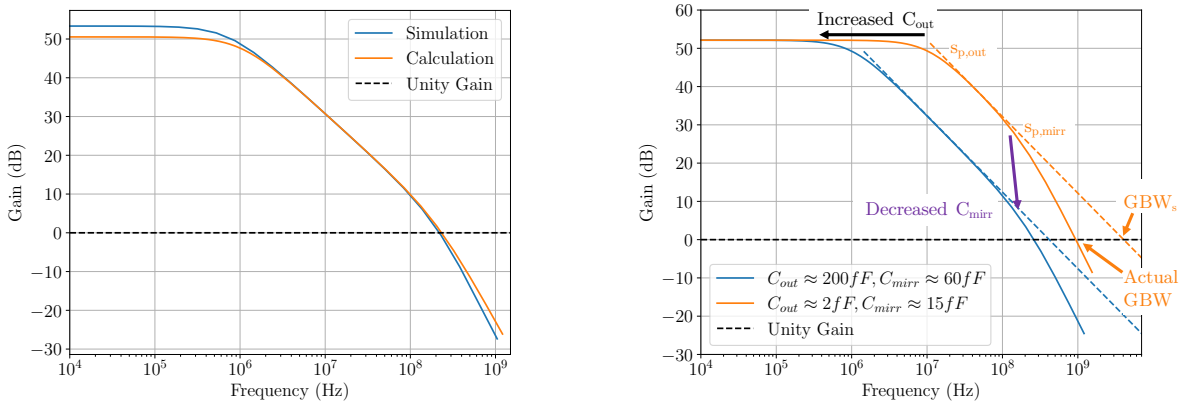
Next to it, figure C.5b shows the calculated transfer function for different values of C_{mirr} and C_{out}. As can be seen, $s_{p,out}$ and $s_{p,mirr}$ are decreased with higher higher capacitor values.

As a result, one can draw the following conclusions for the optimisation of the amplifier's speed: Since

$$g_{m8} \propto \sqrt{\frac{W_8}{L_8} I_{D8}} = \sqrt{\frac{W_8}{L_8}\left(I_L - \frac{I_T}{2}\right)}$$

a large W_8/L_8-ratio as well as a large bias current difference $I_L - \frac{I_T}{2}$ leads to a high amplifier speed.[1] On top, increasing $s_{p,out}$ by decreasing C_{out} and r_{out} also helps increasing the amplifier speed. Except for decreasing C_{out}, however, all of the measures mentioned above conflict the requirements for high gain. First of all, since $r_{ds8} \propto L_8$, a high gain demands a large L_8. A large W_8/L_8 however, dictates a low L_8 with respect to W_8. So, one has to make a tradeoff between gain and bandwidth by finding an optimum value for L_8. Another option would be to choose a large L_8 for a high gain and increase W_8 along with it to obtain a high bandwidth alongside. But, choosing both W_8 and L_8 large also results in a large C_{mirr} which, in turn, decreases $s_{p,mirr}$.
Second, decreasing r_{out} also decreases the gain which results in the same tradeoff between gain and bandwidth. Trading these quantities against each other to arrive at the desired

[1] This is only true, if I_L is increased and $I_T/2$ is kept constant. Otherwise g_{m1} decreases.



(a) Comparison of the simulated and calculated transfer function. The approximated calculation closely reconstructs the simulation.

(b) Calculated transfer function for different values of C_{out} and C_{mirr}. Depending on the size of $s_{p,mirr}$, the circuit's unity gain bandwidth can be largely deteriorated.

Figure C.5: Transfer function H_{open} of the CSA's differential amplifier without feedback. For the calculated transfer functions, the corresponding transistor small-signal quantities (g_{mi}, r_{dsi}, ...) have been extracted from an analog simulation.

circuit performance is a crucial part of the optimisation process.

With $H_{open}(s)$ determined, the next step is finding the closed-loop transfer function $H_{closed}(s)$ of the CSA with both C_f and R_f in action. The purpose of this step is to understand how the open-loop characteristics transfer to the closed-loop case. Since the input signal from the pixel sensor is a current rather than a voltage, this transfer function has to describe a current-to-voltage conversion

$$H_{closed}(s) = \frac{v_{out}(s)}{i_{in}(s)} \tag{C.23}$$

as indicated in figure 6.16. With Kirchhoff's current law and the assumption that the input capacitance of the amplifier can be neglected vs. C_{det}, the current flowing into the input node can be described via

$$i_{in}(s) = sC_{det}v_{in}(s) + (v_{in}(s) - v_{out}(s))\left(\frac{1}{R_f} + sC_f\right). \tag{C.24}$$

The substitution of $v_{in}(s) \approx v_{out}(s)/H_{open}(s)$ yields

$$H_{closed}(s) \approx \frac{v_{out}(s)}{i_{in}(s)} = \frac{1}{\frac{sC_{det}}{H_{open}(s)} + \left(\frac{1}{H_{open}(s)} - 1\right)\left(\frac{1}{R_f} + sC_f\right)}. \tag{C.25}$$

The determination of meaningful formula requires excessive simplification with the help of a few assumptions. For example, the capacitor sizes can be assumed such that [42]

$$A_v C_f \gg C_{det} \gg C_f \tag{C.26}$$

with $A_v \gg 1$. Additionally, R_f is assumed to be large such that $1/R_f \ll 1$. With these in

play, a lengthy and elaborate calculation reveals that $H_{closed}(s)$ can be approximated by

$$H_{closed}(s) \approx \frac{H_{closed}(0)}{(1+\frac{s}{s_{p,fb}})(1+\frac{s}{s_{p,amp+}})(1+\frac{s}{s_{p,amp-}})} \tag{C.27}$$

with a single real pole at

$$s_{p,fb} = \frac{1}{R_f C_f} \tag{C.28}$$

and a complex conjugate pole pair at

$$s_{p,amp+/-} = \left(\frac{1}{2}(s_{p,mirr} + s_{p,out}) \pm \sqrt{s_{p,mirr} s_{p,out} \frac{C_f}{C_{det}} A_v}\right). \tag{C.29}$$

The transfer function's dc value is given as $H_{closed}(0) = \frac{A_v R_f}{1-A_v} \approx R_f$.

D Lists

D.1 List of Figures

D.2 List of Tables

E Author Publications

The author contributed to the following list of publications which have been used as references in this thesis.

First Authorship

[73] D. Schimansky et al. "Concepts for the data flow control on the XIDer readout ASIC". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 1057 (Dec. 2023), p. 168720. ISSN: 0168-9002. DOI: 10.1016/j.nima.2023.168720. URL: https://www.sciencedirect.com/science/article/pii/S0168900223007118.

[87] D. Schimansky et al. "Concepts for the XIDer readout ASIC incorporating a pipelined ADC with very low dead time". In: *Journal of Instrumentation* 16.03 (Mar. 2021), P03023. DOI: 10.1088/1748-0221/16/03/P03023. URL: https://dx.doi.org/10.1088/1748-0221/16/03/P03023.

Co-Authorship

[7] M. Williams et al. "XIDER: First Prototypes and Results with the Digital Integration Readout Scheme". In: *IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*. Oct. 2021, pp. 1–4. DOI: 10.1109/NSS/MIC44867.2021.9875717. URL: https://ieeexplore.ieee.org/document/9875717.

[10] P. Fajardo et al. "Digital integration: a novel readout concept for XIDER, an X-ray detector for the next generation of synchrotron radiation sources". In: *Journal of Instrumentation* 15.01 (Jan. 2020), p. C01040. DOI: 10.1088/1748-0221/15/01/C01040. URL: https://dx.doi.org/10.1088/1748-0221/15/01/C01040.

[51] M Williams et al. "XIDER: a novel X-ray detector for the next generation of high-energy synchrotron radiation sources". In: *Journal of Physics: Conference Series* 2380.1 (Dec. 2022), p. 012091. DOI: 10.1088/1742-6596/2380/1/012091. URL: https://dx.doi.org/10.1088/1742-6596/2380/1/012091.

[99] M. Williams et al. "Exploring the time-resolving capabilities of XIDer assemblies". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* (Dec. 2023). ISSN: 0168-9002. DOI: 10.1016/j.nima.2023.168688. URL: https://www.sciencedirect.com/science/article/pii/S0168900223006782.

F Bibliography

[1] S.M. White et al. "Commissioning and Restart of ESRF-EBS". In: *Proc. IPAC'21* (Campinas, SP, Brazil). Aug. 2021, pp. 1–6. ISBN: 978-3-95450-214-1. DOI: 10.18429/JACoW-IPAC2021-MOXA01. URL: https://jacow.org/ipac2021/papers/moxa01.pdf.

[2] J.-L. Revol et al. "ESRF-EBS: Implementation, Performance and Restart of User Operation". In: *Proc. IPAC'21* (Campinas, SP, Brazil). Aug. 2021, pp. 3929–3932. ISBN: 978-3-95450-214-1. DOI: 10.18429/JACoW-IPAC2021-THPAB074. URL: https://jacow.org/ipac2021/papers/thpab074.pdf.

[3] S. Henderson. "Status of the APS Upgrade Project". In: *Proc. IPAC'15* (Richmond, VA, USA). June 2015, pp. 1791–1793. ISBN: 978-3-95450-168-7. DOI: https://doi.org/10.18429/JACoW-IPAC2015-TUPJE067. URL: http://jacow.org/ipac2015/papers/tupje067.pdf.

[4] H. Tanaka et al. "SPring-8 Upgrade Project". In: *Proc. IPAC'16* (Busan, Korea). June 2016, pp. 2867–2870. ISBN: 978-3-95450-147-2. DOI: doi:10.18429/JACoW-IPAC2016-WEPOW019. URL: http://jacow.org/ipac2016/papers/wepow019.pdf.

[5] I.V. Agapov et al. "Status of the PETRA IV project". In: *Proc. IPAC'19* (Melbourne, Australia). June 2019, pp. 1404–1407. ISBN: 978-3-95450-208-0. DOI: doi:10.18429/JACoW-IPAC2019-TUPGW011. URL: http://jacow.org/ipac2019/papers/tupgw011.pdf.

[6] Yi Jiao et al. "The HEPS project". In: *Journal of Synchrotron Radiation* 25 (Nov. 2018), pp. 1611–1618. DOI: 10.1107/S1600577518012110. URL: https://doi.org/10.1107/S1600577518012110.

[7] M. Williams et al. "XIDER: First Prototypes and Results with the Digital Integration Readout Scheme". In: *IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*. Oct. 2021, pp. 1–4. DOI: 10.1109/NSS/MIC44867.2021.9875717. URL: https://ieeexplore.ieee.org/document/9875717.

[8] M. Collonge et al. "Monte Carlo simulations for XIDer, a novel digital integration X-ray detector for the next generation of synchrotron radiation sources". In: *Journal of Instrumentation* 17.01 (Jan. 2022), p. C01037. DOI: 10.1088/1748-0221/17/01/C01037. URL: https://dx.doi.org/10.1088/1748-0221/17/01/C01037.

[9] H.T. Philipp et al. "High dynamic range CdTe mixed-mode pixel array detector (MM-PAD) for kilohertz imaging of hard x-rays". In: *Journal of Instrumentation* 15.06 (June 2020), P06025. DOI: 10.1088/1748-0221/15/06/P06025. URL: https://dx.doi.org/10.1088/1748-0221/15/06/P06025.

[10] P. Fajardo et al. "Digital integration: a novel readout concept for XIDER, an X-ray detector for the next generation of synchrotron radiation sources". In: *Journal of Instrumentation* 15.01 (Jan. 2020), p. C01040. DOI: 10.1088/1748-0221/15/01/C01040. URL: https://dx.doi.org/10.1088/1748-0221/15/01/C01040.

[11] Joao P. B. Brito, Rafael P. Bernar, and Luis C. B. Crispino. "Synchrotron geodesic radiation in Schwarzschild–de Sitter spacetime". In: *Physical Review D* 101.12 (June 2020). DOI: 10.1103/physrevd.101.124019. URL: https://doi.org/10.1103%2Fphysrevd.101.124019.

[12] Settimio Mobilio, ed. *Synchrotron Radiation. Basics, Methods and Applications*. eng. Berlin, Heidelberg: Springer, 2015. ISBN: 978-364-25531-5-8. DOI: 10.1007/978-3-642-55315-8. URL: http://dx.doi.org/10.1007/978-3-642-55315-8.

[13] Donald H Bilderback, Pascal Elleaume, and Edgar Weckert. "Review of third and next generation synchrotron light sources". In: *Journal of Physics B: Atomic, Molecular and Optical Physics* 38.9 (Apr. 2005), S773. DOI: 10.1088/0953-4075/38/9/022. URL: https://dx.doi.org/10.1088/0953-4075/38/9/022.

[14] Sylvain Aumonier et al. "Millisecond time-resolved serial oscillation crystallography of a blue-light photoreceptor at a synchrotron". In: *IUCrJ* 7.4 (July 2020), pp. 728–736. DOI: 10.1107/S2052252520007411. URL: https://doi.org/10.1107/S2052252520007411.

[15] Marine Cotte et al. "New Opportunities Offered by the ESRF to the Cultural and Natural Heritage Communities". In: *Synchrotron Radiation News* 35 (Nov. 2022), pp. 1–7. DOI: 10.1080/08940886.2022.2135958. URL: https://doi.org/10.1080/08940886.2022.2135958.

[16] D. Phil Woodruff. *Synchrotron Radiation: Sources and Applications to the Structural and Electronic Properties of Materials*. Cambridge University Press, 2021. DOI: 10.1017/9781316995747.

[17] Julian Schwinger. "On the Classical Radiation of Accelerated Electrons". In: *Phys. Rev.* 75 (12 June 1949), pp. 1912–1925. DOI: 10.1103/PhysRev.75.1912. URL: https://link.aps.org/doi/10.1103/PhysRev.75.1912.

[18] Eduard Prat. *Synchrotron light sources and X-ray free-electron-lasers*. July 2021. arXiv: 2107.09131. URL: https://doi.org/10.48550/arXiv.2107.09131.

[19] Eberhard J. Jaeschke et al., eds. *Synchrotron Light Sources and Free-Electron Lasers. Accelerator Physics, Instrumentation and Science Applications*. eng. second edition. Springer eBook Collection. Cham, Switzerland: Springer, 2020. ISBN: 978-3-030-23201-6. DOI: 10.1007/978-3-030-23201-6. URL: https://doi.org/10.1007/978-3-030-23201-6.

[20] Bryce Jacobson, John Madey, and Pardis Niknejadi. "Design and Commissioning of Chasman-Green Double Bend Achromatic Lattice Linear Transport Line at the University of Hawai'i MkV Accelerator Facility". In: *Proc. IPAC'13*. 2013, WEPWA072.

[21] R. Chasman, G. K. Green, and E. M. Rowe. "Preliminary Design of a Dedicated Synchrotron Radiation Facility". In: *IEEE Transactions on Nuclear Science* 22.3 (1975), pp. 1765–1767. DOI: 10.1109/TNS.1975.4327987.

[22] Mikael Eriksson. "The multi-bend achromat storage rings". In: *AIP Conference Proceedings* 1741.1 (2016), p. 020001. DOI: 10.1063/1.4952780. URL: https://aip.scitation.org/doi/abs/10.1063/1.4952780.

[23] Ali Akbar Fakhri et al. "An analytical study of double bend achromat lattice". In: *Review of Scientific Instruments* 86.3 (2015), p. 033304. DOI: 10.1063/1.4914389. URL: https://doi.org/10.1063/1.4914389.

[24] S. C. Leemann et al. “Beam dynamics and expected performance of Sweden’s new storage-ring light source: MAX IV”. In: *Phys. Rev. ST Accel. Beams* 12 (12 Dec. 2009), p. 120701. DOI: 10.1103/PhysRevSTAB.12.120701. URL: https://link.aps.org/doi/10.1103/PhysRevSTAB.12.120701.

[25] *ESRF webpage: Parameters*. https://www.esrf.fr/home/UsersAndScience/Accelerators/parameters.html. Accessed: 11.04.2023.

[26] Valerio Cerantola et al. “New frontiers in extreme conditions science at synchrotrons and free electron lasers”. In: *Journal of Physics: Condensed Matter* 33.27 (May 2021), p. 274003. DOI: 10.1088/1361-648X/abfd50. URL: https://dx.doi.org/10.1088/1361-648X/abfd50.

[27] Pooria Sedigh Rahimabadi, Mehdi Khodaei, and Kaveenga R. Koswattage. “Review on applications of synchrotron-based X-ray techniques in materials characterization”. In: *X-Ray Spectrometry* 49.3 (2020), pp. 348–373. DOI: https://doi.org/10.1002/xrs.3141. URL: https://analyticalsciencejournals.onlinelibrary.wiley.com/doi/abs/10.1002/xrs.3141.

[28] P. Tafforeau et al. “Applications of X-ray synchrotron microtomography for non-destructive 3D studies of paleontological specimens”. In: *Applied Physics A* 83.2 (2006), pp. 195–202. DOI: 10.1007/s00339-006-3507-2. URL: https://doi.org/10.1007/s00339-006-3507-2.

[29] Fred A. Stevie and Carrie L. Donley. “Introduction to x-ray photoelectron spectroscopy”. In: *Journal of Vacuum Science & Technology A* 38.6 (2020). DOI: 10.1116/6.0000412. URL: https://doi.org/10.1116/6.0000412.

[30] Vitalij K. Pecharsky and Peter Y. Zavalij. *Fundamentals of powder diffraction and structural characterization of materials*. eng. Boston, MA: Springer US, 2005. ISBN: 978-0-387-24567-6. DOI: 10.1007/b106242. URL: http://dx.doi.org/10.1007/b106242.

[31] Siegfried Hunklinger and Christian Enss. *Solid state physics*. eng. Berlin ; Boston: De Gruyter, 2022. ISBN: 978-3-11-066650-2 and 978-3-11-066708-0. DOI: 10.1515/9783110666502. URL: https://doi.org/10.1515/9783110666502.

[32] “Small Angle X-ray Scattering for Nanoparticle Research”. In: *Chemical Reviews* 116.18 (Sept. 2016), pp. 11128–11180. DOI: 10.1021/acs.chemrev.5b00690. URL: https://doi.org/10.1021/acs.chemrev.5b00690.

[33] Tobias W. Gräwert and Dmitri I. Svergun. “Structural Modeling Using Solution Small-Angle X-ray Scattering (SAXS)”. In: *Journal of Molecular Biology* 432.9 (2020). Integrative Biophysics: Protein Interaction and Disorder, pp. 3078–3092. ISSN: 0022-2836. DOI: https://doi.org/10.1016/j.jmb.2020.01.030. URL: https://www.sciencedirect.com/science/article/pii/S0022283620300942.

[34] *ESRF webpage: About Us*. https://www.esrf.fr/about. Accessed: 14.04.2023.

[35] *ESRF Highlights 2022*. https://www.esrf.fr/Apache_files/Highlights/2022/index.html. Accessed: 17.04.2023.

[36] T P Perron et al. “New Preinjector for the ESRF Linac”. In: *Proc. EPAC’08, Genoa, Italy*. 2008, pp. 2195–2197. URL: https://accelconf.web.cern.ch/e08/papers/wepc087.pdf.

[37] *ESRF webpage: Filling Modes*. https://www.esrf.fr/Accelerators/Operation/Modes. Accessed: 02.05.2023.

[38] S. M. Sze and Ming-Kwei Lee. *Semiconductor devices. physics and technology ; international student version*. eng. 3. ed., international student version. Hoboken, NJ: Wiley, 2013, IX, 582 S. ISBN: 0-470-87367-1 and 978-0-470-87367-0.

[39] Glenn F. Knoll. *Radiation detection and measurement*. eng. 4th ed. Hoboken, NJ: Wiley, 2010, XXVI, 830 S. ISBN: 978-0-470-13148-0.

[40] Rudolf Gross and Achim Marx. *Festkörperphysik*. ger. 4., aktualisierte Auflage. De Gruyter Studium. Berlin ; Boston: De Gruyter, 2023, p. 1067. ISBN: 978-3-11-078264-6 and 978-3-11-078239-4. DOI: 10.1515/9783110782394.

[41] Helmuth Spieler. *Semiconductor detector systems*. eng. Repr. Series on semiconductor science and technology. Oxford [u.a.]: Oxford Univ. Press, 2008, XVI, 489 S. ISBN: 978-0-19-852784-8.

[42] *Pixel detectors. from fundamentals to applications*. eng. Particle acceleration and detection. Berlin ; Heidelberg [u.a.]: Springer, 2006, X, 304 S. ISBN: 3-540-28332-3 and 978-3-540-28332-4.

[43] J.H. Hubbell and S.M. Seltzer. *Tables of X-Ray Mass Attenuation Coefficients and Mass Energy-Absorption Coefficients (version 1.4)*. Tech. rep. Gaithersburg, MD: National Institute of Standards and Technology, May 1995, last update: July 2004. DOI: 10.18434/T4D01F.

[44] L. A. Kosyachenko et al. "Band gap of CdTe and Cd0.9Zn0.1Te crystals". In: *Semiconductors* 45.10 (2011), pp. 1273–1280. DOI: 10.1134/S1063782611100137. URL: https://doi.org/10.1134/S1063782611100137.

[45] Salah Awadalla. *Solid-State Radiation Detectors. Technology and Applications*. English. Ed. by Salah Awadalla, Salah Awadalla, and Krzysztof Iniewski. 1st ed. Devices, circuits, and systems. United States: CRC Press, 2015, 384 S. ISBN: 1482262215 and 9781482262216 and 1482262207 and 9781482262209 and 9781315215013 and 1315215012 and 1482262215 and 9781482262216.

[46] Hamna F. Haneef, Andrew M. Zeidell, and Oana D. Jurchescu. "Charge carrier traps in organic semiconductors: a review on the underlying physics and impact on electronic devices". In: *J. Mater. Chem. C* 8 (3 2020), pp. 759–787. DOI: 10.1039/C9TC05695E. URL: http://dx.doi.org/10.1039/C9TC05695E.

[47] Xavier Mathew. "Photo-induced current transient spectroscopic study of the traps in CdTe". In: *Solar Energy Materials and Solar Cells* 76.3 (2003). CANCUN 2001 Nanoscale materials & devices, pp. 225–242. ISSN: 0927-0248. DOI: https://doi.org/10.1016/S0927-0248(02)00276-3. URL: https://www.sciencedirect.com/science/article/pii/S0927024802002763.

[48] W. Shockley and W. T. Read. "Statistics of the Recombinations of Holes and Electrons". In: *Phys. Rev.* 87 (5 Sept. 1952), pp. 835–842. DOI: 10.1103/PhysRev.87.835. URL: https://link.aps.org/doi/10.1103/PhysRev.87.835.

[49] R. N. Hall. "Electron-Hole Recombination in Germanium". In: *Phys. Rev.* 87 (2 July 1952), pp. 387–387. DOI: 10.1103/PhysRev.87.387. URL: https://link.aps.org/doi/10.1103/PhysRev.87.387.

[50] J Franc et al. “CdTe and CdZnTe crystals for room temperature gamma-ray detectors”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 434.1 (1999), pp. 146–151. ISSN: 0168-9002. DOI: https://doi.org/10.1016/S0168-9002(99)00448-9. URL: https://www.sciencedirect.com/science/article/pii/S0168900299004489.

[51] M Williams et al. “XIDER: a novel X-ray detector for the next generation of high-energy synchrotron radiation sources”. In: *Journal of Physics: Conference Series* 2380.1 (Dec. 2022), p. 012091. DOI: 10.1088/1742-6596/2380/1/012091. URL: https://dx.doi.org/10.1088/1742-6596/2380/1/012091.

[52] Adriano Cola and Isabella Farella. “The polarization mechanism in CdTe Schottky detectors”. In: *Applied Physics Letters* 94 (Mar. 2009), pp. 102113–102113. DOI: 10.1063/1.3099051. URL: https://doi.org/10.1063/1.3099051.

[53] Derek S. Bale and Csaba Szeles. “Nature of polarization in wide-bandgap semiconductor detectors under high-flux irradiation: Application to semi-insulating $Cd_{1-x}Zn_xTe$”. In: *Phys. Rev. B* 77 (3 Jan. 2008), p. 035205. DOI: 10.1103/PhysRevB.77.035205. URL: https://link.aps.org/doi/10.1103/PhysRevB.77.035205.

[54] Michael Prokesch et al. “CdZnTe Detectors Operating at X-ray Fluxes of 100 Million Photons/(mm^2·sec)”. In: *IEEE Transactions on Nuclear Science* 63.3 (2016), pp. 1854–1859. DOI: 10.1109/TNS.2016.2556318. URL: https://ieeexplore.ieee.org/document/7497721.

[55] *Redlen Technology webpage*. https://www.redlen.com. Accessed: 13.09.2023.

[56] B. Thomas et al. “Characterisation of Redlen high-flux CdZnTe”. In: *Journal of Instrumentation* 12.12 (Dec. 2017), p. C12045. DOI: 10.1088/1748-0221/12/12/C12045. URL: https://dx.doi.org/10.1088/1748-0221/12/12/C12045.

[57] Jens-Rainer Ohm and Hans Dieter Lüke. *Signalübertragung. Grundlagen der digitalen und analogen Nachrichtenübertragungssysteme*. ger. 11., neu bearbeitete und erweiterte Auflage. Berlin ; Heidelberg ; Dordrecht ; London ; New York: Springer, 2010, pp. XV, 513. ISBN: 978-3-642-10199-1.

[58] Jan Lunze. *Regelungstechnik 1. systemtheoretische Grundlagen, Analyse und Entwurf einschleifiger Regelungen : mit 77 Beispielen, 186 Übungsaufgaben sowie einer Einführung in das Programmsystem MATLAB*. ger. 12., überarbeitete Auflage. Berlin ; [Heidelberg]: Springer Vieweg, 2020. ISBN: 978-3-662-60746-6. DOI: 10.1007/978-3-662-60746-6. URL: https://doi.org/10.1007/978-3-662-60746-6.

[59] Tony Chan Carusone. *Analog integrated circuit design*. eng. Ed. by David Johns and Kenneth W Martin. 2nd ed. Hoboken, NJ: J. Wiley & Sons, 2012. URL: https://learning.oreilly.com/library/view/-/9780470770108/?ar.

[60] Behzad Razavi. *Design of analog CMOS integrated circuits*. eng. International ed. Electrical engineering series. Boston, Mass. [u.a.]: McGraw-Hill, 2001, XX, 684 S. ISBN: 0-07-118839-8 and 0-07-118815-0 and 978-0-07-118839-5 and 978-0-07-118815-9.

[61] Phillip E. Allen and Douglas R. Holberg. *CMOS analog circuit design*. eng. International third edition. New York ; Oxford: Oxford University Press, 2012, xv, p. 590. ISBN: 978-0-19-993742-4.

[62] Angsuman Sarkar et al. *Low Power VLSI Design. fundamentals*. eng. Berlin ; Boston: De Gruyter Oldenbourg, 2016, XIV, 310 S. ISBN: 978-3-11-045526-7 and 978-3-11-045555-7 and 3-11-045526-9.

[63] Gavin B. M. Vaughan et al. "ID15A at the ESRF – a beamline for high speed operando X-ray diffraction, diffraction tomography and total scattering". In: *Journal of Synchrotron Radiation* 27.2 (Mar. 2020), pp. 515–528. DOI: 10.1107/S1600577519016813. URL: https://doi.org/10.1107/S1600577519016813.

[64] Jean Susini et al. "New challenges in beamline instrumentation for the ESRF Upgrade Programme Phase II". In: *Journal of Synchrotron Radiation* 21.5 (Sept. 2014), pp. 986–995. DOI: 10.1107/S1600577514015951. URL: https://doi.org/10.1107/S1600577514015951.

[65] Eberhard Jaeschke et al., eds. *Synchrotron Light Sources and Free-Electron Lasers. Accelerator Physics, Instrumentation and Science Applications*. eng. Springer Nature Living Reference : Physics and Astronomy. Cham: Springer, 2019, p. 1400. ISBN: 978-3-319-04507-8. DOI: 10.1007/978-3-319-04507-8. URL: https://doi.org/10.1007/978-3-319-04507-8.

[66] Takaki Hatsui and Heinz Graafsma. "X-ray imaging detectors for synchrotron and XFEL sources". In: *IUCrJ* 2.3 (May 2015), pp. 371–383. DOI: 10.1107/S205225251500010X. URL: https://doi.org/10.1107/S205225251500010X.

[67] *Technical Specifications: DECTRIS EIGER2 XE CdTe 16M*. https://media.dectris.com/230216-Technical_Specifications-DECTRIS_EIGER2_XE_CdTe_16M.pdf. Accessed: 27.09.2023.

[68] *European XFEL website*. https://www.xfel.eu. Accessed: 28.09.2023.

[69] B. Henrich et al. "The adaptive gain integrating pixel detector AGIPD a detector for the European XFEL". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 633 (2011). 11th International Workshop on Radiation Imaging Detectors (IWORID), S11–S14. ISSN: 0168-9002. DOI: https://doi.org/10.1016/j.nima.2010.06.107. URL: https://www.sciencedirect.com/science/article/pii/S0168900210012970.

[70] J. H. Jungmann-Smith et al. "Towards hybrid pixel detectors for energy-dispersive or soft X-ray photon science". In: *Journal of Synchrotron Radiation* 23.2 (Mar. 2016), pp. 385–394. DOI: 10.1107/S1600577515023541. URL: https://doi.org/10.1107/S1600577515023541.

[71] Tim Brandt van Driel et al. "The ePix10k 2-megapixel hard X-ray detector at LCLS". In: *Journal of Synchrotron Radiation* 27.3 (May 2020), pp. 608–615. DOI: 10.1107/S1600577520004257. URL: https://doi.org/10.1107/S1600577520004257.

[72] Katherine S. Shanks et al. "The MM-PAD-2.1: A Wide-Dynamic-Range Detector For High-Energy X-ray Imaging". In: *2020 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*. 2020, pp. 1–2. DOI: 10.1109/NSS/MIC42677.2020.9507923. URL: https://ieeexplore.ieee.org/document/9507923.

[73] D. Schimansky et al. "Concepts for the data flow control on the XIDer readout ASIC". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 1057 (Dec. 2023), p. 168720. ISSN: 0168-9002. DOI: 10.1016/j.nima.2023.168720. URL: https://www.sciencedirect.com/science/article/pii/S0168900223007118.

[74] *Cadence website*. https://www.cadence.com/en_US/home.html. Accessed: 08.05.2023.

[75] *Cadence website: Virtuoso Studio*. https://www.cadence.com/en_US/home/tools/custom-ic-analog-rf-design/virtuoso-studio.html. Accessed: 08.05.2023.

[76] *Cadence website: Innovus Implementation System*. https://www.cadence.com/en_US/home/tools/digital-design-and-signoff/soc-implementation-and-floorplanning/innovus-implementation-system.html. Accessed: 08.05.2023.

[77] *Cadence website: Xcelium Logic Simulator*. https://www.cadence.com/ko_KR/home/tools/system-design-and-verification/simulation-and-testbench-verification/xcelium-simulator.html. Accessed: 08.05.2023.

[78] *Wolfram Mathematica website*. https://www.wolfram.com/mathematica/. Accessed: 08.05.2023.

[79] *TSMC 65nm Technology webpage*. https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_65nm. Accessed: 11.10.2023.

[80] *STFC website*. https://www.ukri.org/councils/stfc/. Accessed: 09.10.2023.

[81] Ulrich Tietze, Christoph Schenk, and Eberhard Gamm. *Halbleiter-Schaltungstechnik*. ger. 14., überarb. und erw. Aufl. Literaturverz. S. [1763] - 1766. Berlin ; Heidelberg: Springer-Vieweg, 2012, XXXVII, 1807 S. ISBN: 3-642-31025-7 and 978-3-642-31025-6.

[82] "IEEE Standard for Test Access Port and Boundary-Scan Architecture". In: *IEEE Std 1149.1-2013 (Revision of IEEE Std 1149.1-2001)* (May 2013), pp. 1–444. DOI: 10.1109/IEEESTD.2013.6515989. URL: https://ieeexplore.ieee.org/document/6515989.

[83] Florian Erdinger. *Design of front end electronics and a full scale 4k pixel readout ASIC for the DSSC X-ray detector at the European XFEL*. eng. PhD thesis. Heidelberg, 2016, p. 163. DOI: 10.11588/heidok.00022273. URL: http://nbn-resolving.de/urn:nbn:de:bsz:16-heidok-222733.

[84] Alan Owens and A. Peacock. "Compound semiconductor radiation detectors". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 531.1 (2004). Proceedings of the 5th International Workshop on Radiation Imaging Detectors, pp. 18–37. ISSN: 0168-9002. DOI: https://doi.org/10.1016/j.nima.2004.05.071. URL: https://www.sciencedirect.com/science/article/pii/S0168900204010575.

[85] *Diamond Light Source website*. https://www.diamond.ac.uk/. Accessed: 10.10.2023.

[86] *Accellera Webpage: About Verilog-AMS*. https://www.accellera.org/activities/working-groups/systemverilog-ams/verilog-ams/about. Accessed: 08.08.2023.

[87] D. Schimansky et al. "Concepts for the XIDer readout ASIC incorporating a pipelined ADC with very low dead time". In: *Journal of Instrumentation* 16.03 (Mar. 2021), P03023. DOI: 10.1088/1748-0221/16/03/P03023. URL: https://dx.doi.org/10.1088/1748-0221/16/03/P03023.

[88] *Xilinx 7 Series FPGAs Data Sheet: Overview*. https://docs.xilinx.com/v/u/en-US/ds180_7Series_Overview. Accessed: 02.10.2023.

[89] *Python Webpage*. https://www.python.org/. Accessed: 04.09.2023.

[90] *PyQt5 Documentation*. https://www.riverbankcomputing.com/software/pyqt/. Accessed: 04.09.2023.

[91] D. Schimansky et al. "XIDer: a Novel X-ray Detector for Next- Generation High-Energy Synchrotron Radiation Sources". Presented at the 2023 ULITIMA at SLAC, Menlo Park, California, USA. Mar. 13-16, 2023. URL: https://indico.slac.stanford.edu/event/7076/contributions/4185/.

[92] D. Schimansky. "Update on: XIDer – an X-ray Integrating Detector for the ESRF-EBS Upgrade". Presented in the HighRR Bi-Weekly Seminar, Heidelberg, Germany. 10.03.2021. URL: https://indico.cern.ch/event/951974/.

[93] Marin Collonge. *Study and Application of the Incremental Digital Integration: a Novel X-ray Detector Readout For Synchrotron Applications*. eng. PhD thesis. Heidelberg, to be published.

[94] *Acrorad webpage*. https://www.acrorad.co.jp. Accessed: 12.09.2023.

[95] *Due2lab webpage*. https://www.due2lab.com/en/. Accessed: 12.09.2023.

[96] *Polymer Assembly Technology webpage*. https://www.polymerassemblytech.com. Accessed: 12.09.2023.

[97] *Tomsk State University*. https://en.tsu.ru. Accessed: 21.09.2023.

[98] M. Collonge et al. "New Results with XIDER: a Novel High Dynamic Range X-ray Integrating Detector". Presented at the 2022 IEEE-NSS-RTSD, Milano, Italy. Nov. 05-12, 2022. URL: https://www.eventclass.org/contxt_ieee2022/scientific/online-program/session?s=124#e223.

[99] M. Williams et al. "Exploring the time-resolving capabilities of XIDer assemblies". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* (Dec. 2023). ISSN: 0168-9002. DOI: 10.1016/j.nima.2023.168688. URL: https://www.sciencedirect.com/science/article/pii/S0168900223006782.

[100] Christian B. Lang and Norbert Pucker. *Mathematische Methoden in der Physik*. ger. 3. Aufl. 2016. Berlin ; Heidelberg: Springer Spektrum, 2016. ISBN: 978-3-662-49313-7. DOI: 10.1007/978-3-662-49313-7. URL: http://dx.doi.org/10.1007/978-3-662-49313-7.

[101] Philippe Blanchard and Erwin Brüning. *Mathematical Methods in Physics. Distributions, Hilbert Space Operators, Variational Methods, and Applications in Quantum Physics*. eng. 2nd ed. 2015. Cham [u.a.]: Birkhäuser, 2015. ISBN: 978-3-319-14045-2. DOI: 10.1007/978-3-319-14045-2. URL: http://dx.doi.org/10.1007/978-3-319-14045-2.

[102] Philip Willmott. *An introduction to synchrotron radiation: techniques and applications*. John Wiley & Sons, 2019.

[103] C. Pellegrini, A. Marinelli, and S. Reiche. "The physics of x-ray free-electron lasers". In: *Rev. Mod. Phys.* 88 (1 Mar. 2016), p. 015006. DOI: 10.1103/RevModPhys.88.015006. URL: https://link.aps.org/doi/10.1103/RevModPhys.88.015006.

[104] F. R. Elder et al. "Radiation from Electrons in a Synchrotron". In: *Phys. Rev.* 71 (11 June 1947), pp. 829–830. DOI: 10.1103/PhysRev.71.829.5. URL: https://link.aps.org/doi/10.1103/PhysRev.71.829.5.

[105] EM Rowe and Frederick E Mills. "Tantalus. 1. A dedicated storage ring synchrotron radiation source". In: *Part. Accel.* 4 (1973), pp. 211–227.

[106] Nils Martensson and Mikael Eriksson. "The saga of MAX IV, the first multi-bend achromat synchrotron light source". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 907 (2018). Advances in Instrumentation and Experimental Methods (Special Issue in Honour of Kai Siegbahn), pp. 97–104. ISSN: 0168-9002. DOI: https://doi.org/10.1016/j.nima.2018.03.018. URL: https://www.sciencedirect.com/science/article/pii/S016890021830353X.

[107] Dieter Einfeld, Mark Plesko, and Joachim Schaper. "First multi-bend achromat lattice consideration". In: *Journal of synchrotron radiation* 21 (Sept. 2014), pp. 856–861. DOI: 10.1107/S160057751401193X. URL: https://doi.org/10.1107/S160057751401193X.

[108] Egor Sobolev et al. "Megahertz single-particle imaging at the European XFEL". In: *Communications Physics* 3.1 (May 2020), p. 97. DOI: 10.1038/s42005-020-0362-y. URL: https://doi.org/10.1038/s42005-020-0362-y.

[109] P. Raimondi et al. "Commissioning of the hybrid multibend achromat lattice at the European Synchrotron Radiation Facility". In: *Phys. Rev. Accel. Beams* 24 (11 Nov. 2021), p. 110701. DOI: 10.1103/PhysRevAccelBeams.24.110701. URL: https://link.aps.org/doi/10.1103/PhysRevAccelBeams.24.110701.

[110] I. K. Robinson. "Crystal truncation rods and surface roughness". In: *Phys. Rev. B* 33 (6 Mar. 1986), pp. 3830–3836. DOI: 10.1103/PhysRevB.33.3830. URL: https://link.aps.org/doi/10.1103/PhysRevB.33.3830.

[111] Kaan Orhan, ed. *Micro-computed Tomography (micro-CT) in Medicine and Engineering*. eng. 1st ed. 2020. Springer eBook Collection. Springer, 2020. ISBN: 978-3-030-16641-0. DOI: 10.1007/978-3-030-16641-0.

[112] Junko Yano and Vittal K. Yachandra. "X-ray absorption spectroscopy". In: *Photosynthesis Research* 102.2 (2009), pp. 241–254. DOI: 10.1007/s11120-009-9473-8. URL: https://doi.org/10.1007/s11120-009-9473-8.

[113] Jose M. Martin-Garcia et al. "Serial millisecond crystallography of membrane and soluble protein microcrystals using synchrotron radiation". In: *IUCrJ* 4.4 (July 2017), pp. 439–454. DOI: 10.1107/S205225251700570X. URL: https://doi.org/10.1107/S205225251700570X.

[114] Klaus Giewekemeyer et al. "High-dynamic-range coherent diffractive imaging: ptychography using the mixed-mode pixel array detector". In: *Journal of Synchrotron Radiation* 21.5 (Sept. 2014), pp. 1167–1174. DOI: 10.1107/S1600577514013411. URL: https://doi.org/10.1107/S1600577514013411.

[115] Cyril Ponchut, Nicola Tartoni, and David Pennicard. "X-ray imaging at synchrotron research facilities". In: *Radiation Measurements* 140 (2021), p. 106459. ISSN: 1350-4487. DOI: https://doi.org/10.1016/j.radmeas.2020.106459. URL: https://www.sciencedirect.com/science/article/pii/S1350448720302377.

[116] Christian Brönnimann and Peter Trüb. "Hybrid Pixel Photon Counting X-Ray Detectors for Synchrotron Radiation". In: *Synchrotron Light Sources and Free-Electron Lasers: Accelerator Physics, Instrumentation and Science Applications*. Ed. by Eberhard J. Jaeschke et al. Cham: Springer International Publishing, 2020, pp. 1191–1223. ISBN: 978-3-030-23201-6. DOI: 10.1007/978-3-030-23201-6_36. URL: https://doi.org/10.1007/978-3-030-23201-6_36.

[117] Silah Lee et al. "Direct Thermal Growth of Large Scale Cl-doped CdTe Film for Low Voltage High Resolution X-ray Image Sensor". In: *Scientific Reports* 8.1 (2018), p. 14810. DOI: 10.1038/s41598-018-33240-1. URL: https://doi.org/10.1038/s41598-018-33240-1.

[118] G. Prekas et al. "Direct and indirect detectors for X-ray photon counting systems". In: *2011 IEEE Nuclear Science Symposium Conference Record*. 2011, pp. 1487–1493. DOI: 10.1109/NSSMIC.2011.6154354.

[119] *Chair of Circuit Design website*. http://sus.ziti.uni-heidelberg.de/?lang=en. Accessed: 08.05.2023.

[120] D.S. McGregor and H. Hermon. "Room-temperature compound semiconductor radiation detectors". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 395.1 (1997). Proceedings of the Fourth International Workshop on GaAs Detectors and Related Compounds, pp. 101–124. ISSN: 0168-9002. DOI: https://doi.org/10.1016/S0168-9002(97)00620-7. URL: https://www.sciencedirect.com/science/article/pii/S0168900297006207.

[121] Angelo Rivetti. *CMOS*. eng. 1st edition. Devices, circuits, and systems. Online resource; Title from title page (viewed September 3, 2018). CRC Press, 2018, 1 online resource (726 pages). ISBN: 978-1-4665-6311-7. URL: https://learning.oreilly.com/library/view/-/9781466563117/?ar.

[122] Changliang Li, Chao Feng, and Bocheng Jiang. "Extremely bright coherent synchrotron radiation production in a diffraction-limited storage ring using an angular dispersion-induced microbunching scheme". In: *Phys. Rev. Accel. Beams* 23 (11 Nov. 2020), p. 110701. DOI: 10.1103/PhysRevAccelBeams.23.110701. URL: https://link.aps.org/doi/10.1103/PhysRevAccelBeams.23.110701.

[123] Michael Fiederle et al. "Overview of GaAs und CdTe Pixel Detectors Using Medipix Electronics". In: *Crystal Research and Technology* 55.9 (2020). DOI: https://doi.org/10.1002/crat.202000021. URL: https://onlinelibrary.wiley.com/doi/abs/10.1002/crat.202000021.

Danksagungen

Zum Abschluss dieser Arbeit möchte ich mich bei allen bedanken, die mich auf meinem Weg durch die Promotion begleitet haben.
Allen voran danke ich meinem Doktorvater Prof. Peter Fischer für die Aufnahme in seine Arbeitsgruppe, das entgegengebrachte Vertrauen und die Unterstützung bei meiner Forschungsarbeit. Vielen Dank für die vielen Ratschläge und die konstruktiven Diskussionen, sowie das offene, freundliche Klima, in dem ich die Freiheit hatte, selbstbestimmt zu forschen und zu entwickeln. Ich danke außerdem Prof. André Schöning für die Übernahme des Zweitgutachtens.
Weiterhin möchte ich allen aktuellen, sowie mittlerweile ehemaligen Mitgliedern der Arbeitsgruppe Schaltungstechnik und Simulation am ZITI danken. Ich bedanke mich bei Florian Erdinger für die großartige Betreuung und Zusammenarbeit in den ersten beiden Jahren meiner Arbeit. Ich danke Christian Kreidl für die Hilfe in technischen Fragen, für das Drahtbonden zahlreicher Prototypen, sowie für die tatkräftige Unterstützung bei der Planung und den Zusammenbau unseres ersten ASIC-Sensor-Prototypen. Außerdem danke ich Michael Ritzert für die konstruktive Zusammenarbeit und für die Geduld bei meinen endlosen Fragen. Danke auch an Michael Keller für die vielen hilfreichen Diskussionen und zahlreichen Kaffeepausen.
Weiterer Dank gilt meinen Kollegen vom ESRF in Frankreich, insbesondere Pablo Fajardo, Paolo Busca, Morag Williams, Marin Collonge und Marie Ruat für die konstruktive aber besonders auch lockere und unterhaltsame Zusammenarbeit. Die vielen Stunden (teilweise bis spät in die Nacht), die wir zusammen bei Charakterisierungsmessungen an Beamlines verbracht haben, werden mir für immer in Erinnerung bleiben. Ebenfalls danke an die Mitglieder der ASIC Labor Gruppe am KIP und PI, allen voran Markus Dorn und Ralf Achenbach, für die Unterstützung bei Chip-Submissions und bei dem Zusammenbau unseres ersten ASIC-Sensor-Prototypen. Danke auch an alle, die Teile dieser Arbeit gegengelesen und mir hilfreiches Feedback gegeben haben. Dabei danke ich vor allem Morag Williams, Pablo Fajardo, Florian Erdinger, Jonas Große Sundrup und Michael Ritzert.
Ein besonderer Dank gilt außerdem meiner Partnerin Emma, die mir vor allem in den schwierigen Phasen dieser Arbeit mit viel Geduld und Verständnis zur Seite stand. Auch möchte ich meiner Familie, Freunden und Freundinnen danken, die mir meine akademische Laufbahn erst ermöglicht und mich auf meinem Weg bis hierhin unterstützt haben.

The XIDer project was initiated in the framework of the ESRF Extremely Brilliant Source Upgrade Programme (ESRF-EBS) funded by the ESRF Members and Associated Countries and has received financial support from the ATTRACT project funded by the EC under Grant Agreement 777222.