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Development and Characterisation of the Radiation tolerant HELIX128-2 Readout Chip for the HERA-*B* Microstrip Detectors

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DISSERTATION
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Development and Characterisation of the Radiation tolerant HELIX128-2 Readout Chip for the HERA-*B* Microstrip Detectors

presented by
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Abstract

Within this doctoral thesis work, major parts of the preamplifier and readout chip HELIX128-2 have been developed. Among others these circuits included the "Bias Generator" part, which uses digital-to-analogue converters to provide bias currents and control voltages for the amplifier stages of the chip, and a serial interface for programming all the chips operational parameters.

Furthermore, a complete characterisation of the chip, also under irradiation with a ^{137}Cs-source was performed.

Deficiencies found during the necessary tests and measurements resulted in an improvement of the chip within several revision steps: 2.2, 2.3, 3.0, 3.1 and 3.1a.

The modifications required therefore, included all parts of the circuit, except for the frontend and multiplexer. Especially the pipeline r/w logic control has been improved within this work.

HELIX128-2 is a low noise VLSI readout chip for 128 channels of silicon strip detectors or Microstrip Gaseous Chambers ($\overline{ENC} = 462\mathrm{e}^- + 35.4\mathrm{e}^-/\mathrm{pF}$ for a new chip and $571\mathrm{e}^- + 52.0\mathrm{e}^-/\mathrm{pF}$ at 3.9kGy[1]). Its architecture implements besides an analogue readout path similar to the CERN RD20/FElix chip (Charge sensitive preamplifier, shaper, analogue memory and serial readout of a triggered samples' channel data) also an undelayed binary readout path. The latter is intended for trigger applications and uses individual comparators following each channel's frontend, and a combination of their data in groups of four channels.

The two parts of this thesis are: A description of the HELIX128-2 with a special emphasis on the circuits' implementation. The second part presents the characterisation results of the chip including the chip performance after irradiation doses up to 3.9kGy.

[1] Under the conditions at HERA-B (i.e. $t_{\mathrm{fall}} \approx 100\mathrm{ns}$ at $C_{\mathrm{p}} = 16.3\mathrm{pF}$ and $I_{\mathrm{pre}} = 350\mu\mathrm{A}$)

Zusammenfassung

Entwicklung und Charakterisierung des strahlungstoleranten HELIX128-2 Auslesechips für die HERA-*B* Mikrostreifenzähler

In der vorliegenden Doktorarbeit wurden große Teile der Schaltung des Verstärker- und Auslesechips HELIX128-2 entwickelt. Dazu gehörten unter anderem der "Bias Generator", eine Schaltung zur Einstellung der Ruheströme und Kontrollspannungen der Verstärkerstufen mit Digital-zu-Analog Wandlern, sowie eine serielle Schnittstelle zum Programmieren der Betriebsparameter des Chips.

Des weiteren wurde eine vollständige Charakterisierung des Chips, einschließlich der Bestrahlung mit einer ^{137}Cs-Quelle durchgeführt.

Die bei den dazu notwendigen Tests und Messungen gefundenen Unzulänglichkeiten führten zu einer Weiterentwicklung des Chips in verschiedenen Revisionsstufen: 2.2, 2.3, 3.0, 3.1 und 3.1a.

Die dabei eingeflossenen Modifikationen betrafen mit Ausnahme von Eingangsstufe und Multiplexer alle Schaltungsteile. Insbesondere an der Pipeline Schreib-/Lesesteuerung wurden im Rahmen dieser Arbeit Verbesserungen vorgenommen.

HELIX128-2 ist eine rauscharme ($\overline{ENC} = 462\mathrm{e}^- + 35.4\mathrm{e}^-/\mathrm{pF}$ für einen neuen Chip, $\overline{ENC} = 571\mathrm{e}^- + 52.0\mathrm{e}^-/\mathrm{pF}$ nach 3.9kGy[2]) VLSI-Schaltung zur Auslese von 128 Kanälen eines Silizium-Streifenzählers oder einer MSGC[3]. Die Architektur implementiert neben einem analogen Auslesepfad, der dem Konzept des CERN RD20/FElix Chip folgt (Ladungsverstärker, Pulsformer, analoger Zwischenspeicher und serielle Auslese der Kanäle getriggerter Daten) auch über einen unverzögerten binären Datenpfad. Er ist für Triggeranwendungen gedacht und über der Eingangsstufe folgende Komparatoren realisiert, deren Signale in Gruppen von vier Kanälen zusammengefaßt werden.

Die vorliegende Arbeit gliedert sich daher in zwei Teile: Der erste Teil ist die Beschreibung des HELIX128-2 mit besonderem Schwerpunkt auf der Schaltungsimplementation. Der zweite Teil gibt die Ergebnisse der Charakterisierung des Chips wieder und beinhaltet die Chipeigenschaften unter Bestrahlung bis 3.9kGy.

[2] Unter den Bedingungen des HERA-*B* Experiments ($t_{\mathrm{fall}} \approx 100\mathrm{ns}$ bei $C_{\mathrm{p}} = 16.3\mathrm{pF}$ und $I_{\mathrm{pre}} = 350\mu\mathrm{A}$)

[3] Mikrostreifen–Proportionalzähler

Contents

Introduction

Todays physics provides us with a broad knowledge about the formation of the universe and the structure of matter. Concerning the latter, the *standard model of electroweak interaction* has proven incredibly successful by predicting the existence not only of the Z^0-boson but also of the b- and t-quark . One also knows how to create matter from energy by applying $E = m \cdot c^2$, the famous equation found by Albert Einstein in 1905 [Ein05], but due to the conservation of momentum, charge etc. one can only create *pairs* of particles – one will always be the anti-particle of the other. If an elementary particle meets its anti-particle, they annihilate and revert to energy again.... Thus the fact that the whole universe known to us only consists of matter and lacks any sizable amount of antimatter is still a – admittedly very fortunate – mystery, not yet solved by physics.

There is a glimpse of understanding this paradox: A small asymmetry in mixing and decay of the $K^0/\overline{K^0}$-mesons, known as $\mathcal{CP}$-Violation [Chr64]. In certain decay channels of their heavier relatives, the $B^0/\overline{B^0}$-mesons, this effect is expected to be much larger. Thus it is feasible to study the $\mathcal{CP}$-Violation in the system of the B-mesons to extend our knowledge.

The HERA-B experiment [HB93] [HB95] will accomplish this task but has to face some obstacles: Due to their higher mass the cross section for the production of B^0-$\overline{B^0}$-pairs with a hadron accelerator is much lower than for K-mesons, higher centre of mass energy allows more concurrent processes producing a higher background of unwanted particles , finally their lifetime is shorter, which makes them travel less before decaying into other particles.

HERA-B therefore has to run at a rather high interaction rate to collect enough statistics in a finite time, it needs a very high spatial resolution to find the (secondary) vertices of the decaying B-mesons, and a very sophisticated trigger algorithm to suppress the high background of concurrent processes. In turn the required high-rate, high-resolution detector components, especially silicon microstrip detectors and microstrip gaseous chambers, need highly integrated high-speed readout electronics. Furthermore, the detector system will collect irradiation doses that put further demands and restrictions on the materials and technologies used. Commercial CMOS *ASIC*[4] technology and a sophisticated design allowed the realisation of the HELIX128 readout chip especially tailored to meet all these demands, at moderate cost.

The construction and performance of HELIX128 are presented in this work.

[4] Application Specific Integrated Circuit

Chapter 1

$\mathcal{CP}$-Violation

For a long time it was assumed that all weak interaction processes are invariant under the following operations:

- Charge conjugation[1] $\mathcal{C}$
- Parity transformation[2] $\mathcal{P}$
- Time-reversal[3] $\mathcal{T}$

Studies of weak decays of nuclei [Wu57] and of pions and muons [Gar57][Fri57] showed that $\mathcal{C}$ as well as $\mathcal{P}$-symmetry was not conserved. This can be visualised by applying $\mathcal{C}$ or $\mathcal{P}$ transformation on a left-handed[4] neutrino ν_L:

$$\nu_L \xrightarrow{\mathcal{P}} \nu_R$$
$$\nu_L \xrightarrow{\mathcal{C}} \overline{\nu}_L$$

Neither the right-handed[5] neutrino nor the left-handed antineutrino have been observed. In turn it was believed that symmetry under the product $\mathcal{CP}$ of both transformations was still conserved, since its result is a right-handed antineutrino – an existing particle:

$$\nu_L \xrightarrow{\mathcal{CP}} \overline{\nu}_R$$

For the K^0-mesons it made up this simplified scenario: While produced as strangeness eigenstates $K^0(s = +1)$ and $\overline{K^0}(s = -1)$ with $\mathcal{CP}|K^0\rangle = |\overline{K^0}\rangle = -1 \cdot |K^0\rangle$, one of the preferred hadronic decay modes is $K_S^0 \to \pi^+\pi^-$ (lifetime $\approx 10^{-10}$s). For the latter, $\mathcal{CP}|K_S^0\rangle = |K_S^0\rangle$ had to be valid, since $\mathcal{CP}|\pi^+\pi^-\rangle = |\pi^+\pi^-\rangle$. The K_S^0 had to be a mixture of $K^0$and $\overline{K^0}$, and Gell-Mann and Pais

[1] particle is replaced by its antiparticle
[2] space reflection, this is needed to reverse all radial-vector like properties
[3] inversion of the direction of time (in the 4-dimensional time-space continuum)
[4] antiparallel orientation of spin and momentum vectors
[5] parallel orientation of spin and momentum vectors

[Gell55] postulated a long-lived K_L^0which had to be the other linear combination of $K^0$and $\overline{K^0}$, orthogonal w.r.t. K_S^0:

$$\mathcal{CP}\left|K_S^0\right\rangle = \mathcal{CP}\left|(K^0+\overline{K^0})/\sqrt{2}\right\rangle = \left|(\overline{K^0}+K^0)/\sqrt{2}\right\rangle = \left|K_S^0\right\rangle \quad (1.1)$$

$$\mathcal{CP}\left|K_L^0\right\rangle = \mathcal{CP}\left|(K^0-\overline{K^0})/\sqrt{2}\right\rangle = \left|(\overline{K^0}-K^0)/\sqrt{2}\right\rangle = -\left|K_L^0\right\rangle \quad (1.2)$$

In 1964 Christenson et al. [Chr64] discovered an anomaly in the decay of K_L^0-mesons: With the apparatus depicted in fig. 1.1 they found besides the preferred decay mode of the K_L^0-mesons

$$K_L^0 \longrightarrow \pi^0\pi^+\pi^-,$$

which conserves $\mathcal{CP}$ symmetry, approximately 50 $\mathcal{CP}$-violating events with

$$K_L^0 \longrightarrow \pi^+\pi^-.$$

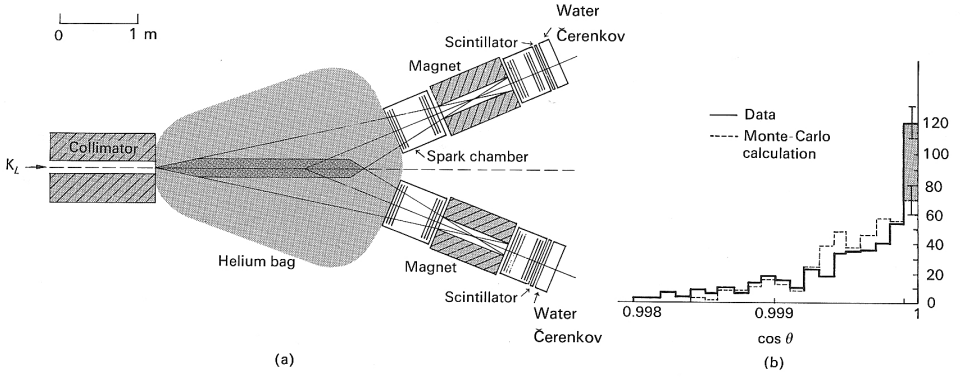


Figure 1.1: (a) Experimental setup of Christenson et al. (1964) demonstrating the decay $K_L \to \pi^+\pi^-$. Rare two-pion decays are distinguished from three-pion and leptonic decays by the invariant mass of the pair and the direction θ of their resultant momentum vector wrt. the K_L beam axis. (b) $\cos(\theta)$ distribution of events with 490 MeV $< M_{\pi\pi} <$ 510 MeV. The shaded deviation from the distribution expected for three-body decays of about 50 events collinear with the beam is due to the $\mathcal{CP}$-violating $\pi^+\pi^-$ decay mode [Per82].

The model of weak interaction – a unitary 2×2 matrix parametrised by the *Cabbibo Angle* Θ_C – could not describe this phenomenon since the matrix elements had to be real numbers. A unitary 3×3 matrix (now parametrised by 3 angles $\Theta_1, \Theta_2, \Theta_3$ and a complex phase δ, which describes the $\mathcal{CP}$-violation) was proposed by Kobayashi and Maskawa in 1973 [Kob73]. It also postulated the existence of a 3$^{\text{rd}}$ family of quarks (consisting of *top* and *bottom*), which was

found later. This Cabbibo-Kobayashi-Maskawa (*CKM*) matrix is an important part of today's *Standard Model of Electroweak Interaction*:

$$\begin{pmatrix} |d\prime\rangle \\ |s\prime\rangle \\ |b'\rangle \end{pmatrix} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \cdot \begin{pmatrix} |u\rangle \\ |c\rangle \\ |t\rangle \end{pmatrix} \tag{1.3}$$

The transition of a quark $|q\rangle$ into another quark $|q'\rangle$ is proportional to $\left|{V_{qq'}}^2\right|$, the squared element of the *CKM* matrix[6]. For $\mathcal{CP}$-violating transitions $\left|{V_{qq'}}^2\right| \neq \left|{V_{\overline{q}\,\overline{q'}}}^2\right| = \left|{V^*_{qq'}}^2\right|$ has to be valid, i.e. $\Im(V_{qq'}) \neq 0$.
A widely used parametrisation of the *CKM* matrix was suggested by Wolfenstein [Wol83] which uses real parameters λ, A, ρ and η, where $\lambda = \sin\Theta_C$:

$$\mathbf{V} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} = \begin{pmatrix} 1-\frac{\lambda^2}{2} & \lambda & \lambda^3 A(\rho - \imath\eta) \\ -\lambda & 1-\frac{\lambda^2}{2} & \lambda^2 A \\ \lambda^3 A(1-\rho-\imath\eta) & -\lambda^2 A & 1 \end{pmatrix} \tag{1.4}$$

Any of the six unitarity conditions, esp.

$$V_{ud}V^*_{ub} + V_{cd}V^*_{cb} + V_{td}V^*_{tb} = 0$$

is represented by the so called *Unitarity Triangle* [Cha84] [Jar88] in the (ρ, η) plane of the Wolfenstein parametrisation (fig. 1.2). While two corners of this triangle are fixed at $(0,0)$ and $(1,0)$, the tip is given by (ρ, η) and the sides are $\propto V_{ub}$ and $\propto V_{td}$. $\mathcal{CP}$-violation is possible if the area of the triangle is different from zero, i.e. $\eta \neq 0$.

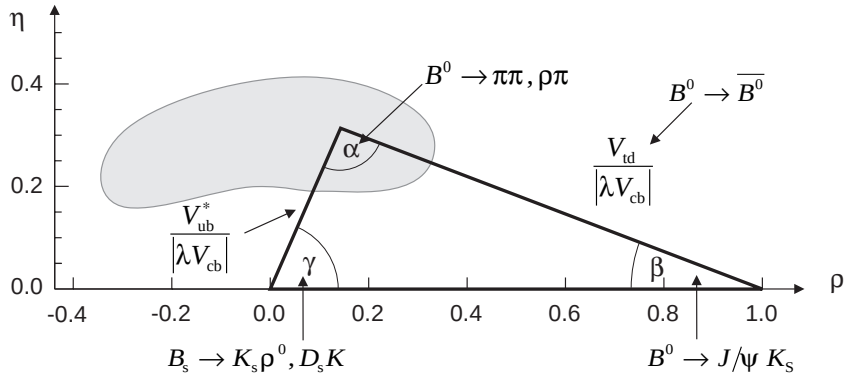


Figure 1.2: *Unitarity Triangle* in the $\rho - \eta$ plane of the Wolfenstein parametrisation of the *CKM* matrix. The $(1-\sigma)$ contour shown constrains the position of the triangle's tip by data given in [Ali93].

Decays of $B^0/\overline{B^0}$mesons into a $\mathcal{CP}$ eigenstate X via a single transition amplitude are predicted to exhibit strong $\mathcal{CP}$ asymmetries directly related to the

[6]Another interpretation of this matrix is a base transformation from the eigenstates of the electroweak interaction to the mass eigenstates of the quarks [Per82].

shape of the *Unitarity Triangle*, independent from poorly known hadronic amplitudes [HB93] [Big89]. Therefore the measurement of these decay modes is very suitable to broaden the understanding of $\mathcal{CP}$-violation. The particle-antiparticle asymmetry in these decay modes arises from the interference of the direct decay $B^0 \to X$ and the decay through mixing $B^0 \to \overline{B^0} \to X$. Examples for these decay modes are $B^0 \to \pi^+\pi^-$ (providing α in fig. 1.2), $B^0 \to J/\Psi K_S^0$ (providing β) and $B_s \to \rho^0 K_S^0$ (providing γ). E.g. for the decay $B^0 \to J/\Psi K_S^0$ (also called *"gold plated"* decay mode) the relation to β is given by the decay rates

$$n_{B^0 \to J/\Psi + K_S^0}(t) \propto e^{-t}(1 + \sin 2\beta \sin xt) \tag{1.5}$$

$$\overline{n}_{\overline{B^0} \to J/\Psi + K_S^0}(t) \propto e^{-t}(1 - \sin 2\beta \sin xt). \tag{1.6}$$

The measurement of this $\mathcal{CP}$ asymmetry in the *gold plated* decay of the neutral B-mesons is the primary objective of the HERA-B experiment.

Chapter 2

The HERA-*B* Experiment

*"HERA-*B *is an experiment designed primarily to search for $\mathcal{CP}$-violation in decays of B mesons into the* "gold plated" *decay mode $B \to J/\psi + K_S^0$. The B mesons are produced in interactions of 820GeV protons in the HERA proton beam with an internal wire target in the beam halo. The use of a halo target results in a minimal disturbance of the ep luminosity operation of HERA and allows the parallel operation of both the ep collider experiments and of HERA-*B*. Despite the small B meson production cross section, the experiment can accumulate sufficient statistics to detect the rare $\mathcal{CP}$-violating B decays, by running at high interaction rates – between 30 and 50MHz – for several years of HERA operation. Among the strong background of "ordinary" proton-nucleus interactions, B-decay candidates are selected by requiring a dilepton in the J/ψ mass range already at the first trigger level, and refining the signature at higher trigger levels. The detector covers almost 4π in the rest frame of the reaction and allows the efficient detection and identification of reaction products. While optimised for the study of the $B \to J/\psi K_S^0$ mode, the detector and its trigger system are flexible enough to access a wide range of additional physics topics, ranging from B_s mixing and B hadron spectroscopy to the very detailed investigation of heavy-quark, J/ψ and Υ production mechanisms, and to high-statistics investigations of rare charm decay modes."*[HB95]

For a long time hadron accelerators have been known to be heavy quark factories, and not only the J/Ψ but also the Υ resonances have been discovered in hadron experiments. Even in the range of modest energies available for fixed target experiments the production rates of charm and beauty quarks exceed the rates available at e^+e^- storage rings. Unfortunately this advantage is bought by the large background of other (undesired) hadronic interactions.

For the HERA-*B* experiment [HB93] [HB95] an *internal* target has been chosen. It consists of eight individually adjustable target wires, interacting with the *halo* (the less populated outer regions) of the 920GeV HERA proton beam. By only using the halo of the proton beam, the luminosity operation of the two *ep* collider experiments H1 and ZEUS is not restricted. The usage of eight separate target wires enables the experiment to run at event rates of up to 40MHz by allowing on average 4 interactions per *bunch crossing* (every 96ns). This is necessary since only one $B^0/\overline{B^0}$ pair is produced in $1.3 \cdot 10^6$ collisions. And only one out of $2.3 \cdot 10^3$ B^0-mesons decays into the *gold plated*

decay channel. Taking inefficiencies of the detector system into account, this yields about $3 \cdot 10^{11}$ collisions to be observed in order to find one B^0 decaying into that channel. For a measurement of $sin2\beta$ with an error $\Delta sin2\beta \approx 0.1$ about 2500 decays of B^0 into the *gold plated* channel

$$B^0 \longrightarrow J/\Psi + K_S^0 \quad \longrightarrow l^- + l^+ + \pi^+ + \pi^- \tag{2.1}$$

$$\overline{B^0} \longrightarrow J/\Psi + K_S^0 \quad \longrightarrow l^- + l^+ + \pi^+ + \pi^- \tag{2.2}$$

$l^- + l^+$ = lepton pair (i.e. $e^- + e^+$ or $\mu^- + \mu^+$)

have to be observed. Running at an event rate of ≈40MHz this corresponds to almost one year (i.e. 10^7s) of data taking.

Since the final states in eq. 2.1 and 2.2 are the same, *B-tagging* has to be used to identify the initial particle. b-quarks are always produced as $b/\overline{b}$-pairs, thus the flavour of the first quark can be determined from the flavour of the second one.

The setup of the HERA-B experiment as a forward spectrometer is depicted in fig. 2.1. To cover about 90% of the 4π solid angle in the rest frame of the B-mesons, a geometric acceptance of 220mrad horizontal and 160mrad vertical is required. The detector components downstream of the target are the following:

- **The silicon vertex detector** (VDS[1]). It uses 16 planes of double-sided silicon detectors with a strip pitch of 51.7µm and 54.6µm (cf. section 2.2). Its main purpose is the reconstruction of the B-mesons decay vertices to separate them from the background of other events. On average the B-mesons travel about 9mm downstream from the target before decaying. The resolution required to reconstruct B mesons is about 10% of that value. The detailed description of the vertex detector is given in section 2.1. 147,456 channels have to be read out.

- **The dipole magnet** of the HERA-B spectrometer is located 4.5m downstream of the target. Due to the Lorentz-force, charged particles traversing the 2.2Tm field of the spectrometer magnet experience a momentum dependent deflection in the horizontal plane. The direction of the deflection depends on the sign of the particle's charge.

- **The inner tracking system** (ITR) is described in section 2.3 and reconstructs the tracks of charged particles between the end of the *vertex detector* (about 2.5m from target) and the *electromagnetic calorimeter* (about 13.25m downstream wrt. the target). Besides its primary objective of particle tracking, the ITR in conjunction with the magnet also provides a momentum measurement, since charged tracks experience a momentum-dependent deflection in the magnetic field. It covers the area from 10mrad up to 25cm from the beam. In addition to the 18,400 trigger outputs about 135,000 channels of MSGC-GEM[2] detectors (described in section 2.5) have to be read out.

[1] Vertex Detector System
[2] Microstrip Gaseous Chamber with Gas Electron Multiplier

- **The outer tracking system** (OTR) [Ber99] accomplishes the track reconstruction in the area outside the inner tracking system, i.e. distances from 25cm of the beam to the 220mrad horizontal and 160mrad vertical acceptance of the detector. Like the inner tracking systemthe detector planes are grouped in 11 superlayers. About 96,000 channels of proportional drift tubes with hexagonal cross section have to be read out. The minimum diameter of the drift tubes is restricted to 5mm, a compromise between moderate occupancies and the safety margin for high-voltage arcovers. The intrinsic resolution of the drift tubes is limited to $\approx$200µm by the inhomogeneous field near the anodes and the position of the wires. The fill gas is a mixture of Ar, CF_4 and CO_2.

- **The high p_T trigger chambers** [HB95] are located in and behind the magnet. Three layers of gas-pixel chambers (inner region) and straw chambers with pad readout are used to detect pion pairs with a transverse momentum $p_T \geq 1.5$GeV/c. This allows HERA-B to trigger $B^0 \to \pi^+\pi^-$ decays, enabling the measurement of α in fig. 1.2. About 27,000 channels have to be read out.

- **The ring image Čerenkov detector** (RICH) [Ham95] serves the purpose of particle identification: Particles traversing a medium at a velocity higher than the speed of light in that particular medium emit photons in the UV or visible region, the so called Čerenkov light. The opening angle of the light cone depends on the particle velocity and the refractive index of the medium. The light cone of a particle is projected as a ring onto a photon detection plane by mirrors. From the diameter of the ring, which is proportional to the opening of the light cone, the particle's velocity can be calculated. Together with the measurement of its energy or momentum, the mass and in turn the particle type can be determined. The distinction of K-mesons from pions by the RICH is of prime importance to tag B decays in the *gold plated* channel. The HERA-B RICH is located between 8.5m and 12m from the target and uses C_4F_{10} as radiator gas. The photon detection plane is equipped with Hamamatsu H6568 16-anode photomultiplier tubes. Approximately 28,000 channels have to be read out.

- **The transition radiation detector** (TRD) [Sav98], 12.0m downstream of the target provides an additional instrument for particle identification. Its particular task is hadron rejection in the central area of the electromagnetic calorimeter. Elementary particles emit transition radiation in the soft x-ray region, when crossing the interface between materials of different refractive indices. The X-ray photons are detected by straw tubes filled with a gas mixture based on krypton. The HERA-B TRD has an active area of $(134 \times 89)\text{cm}^2$ and 36 radiator and straw tube layers. About 7,300 channels have to be read out.

- **The electromagnetic calorimeter** (ECAL) [Zoc00] is located 13.25m from the target. It is a Shashlik-calorimeter made of alternating layers of

lead resp. tungsten absorber and scintillator material. Incident photons produce a shower of electron-positron pairs and photons. The energy deposited in the scintillators by these secondary particles is converted into UV light which in turn is converted into visible light by shashlik-type wave length shifting fibers and read out with photomultipliers. The main purpose of the ECAL is the detection of electron/positron pairs as "track seeds", i.e. initial points for the track reconstruction. Furthermore it has to provide a hadron/$e^{\pm}$ discrimination at the level of $\approx$100. The spatial resolution of the calorimeter, which covers an energy range of 2...500GeV, decreases from 2.5mm in the inner region to 17mm for the outer region. The number of readout channels is 6,500.

- **The muon system** (MUON) [Buc99] consists of 3 hadron absorber layers made of iron and armoured concrete. The detector layers behind each absorber are composed of a central gas-pixel detector and outer proportional tubes with and without pad readout. A fourth detector layer without absorber provides tracking information not deteriorated by muon deflection in the absorber material. The gas mixture used is based on argon. In total 29,500 channels have to be read out.

The trigger system consists of four stages. The **first level trigger** (FLT) [Ful98] looks for track seeds in the MUON ($J/\Psi \rightarrow \mu^+\mu^-$), ECAL ($J/\Psi \rightarrow e^+e^-$) and High pT ($B \rightarrow \pi^+\pi^-$) systems. These track candidates are extrapolated and fitted though the ITR and OTR detectors with a *Kalman Filter* algorithm. The kinematic parameters of the fitted tracks in the vertex are extracted. The decision of the FLT is finally based on the invariant mass of possible track pair combinations. The decision of the FLT has to be taken within 12µs since the detector components can only keep their data pipelined for 128 *bunch crossings*. Due to the 50kHz input rate of the 2$^{\text{nd}}$ level trigger and the input frequency of 10MHz (i.e. the HERA *bunch crossing* frequency) a suppression of background events by a factor of $\gtrsim$200 has to be achieved. The hardware implementation uses LUTs[3] and PLDs[4].

At the **second level trigger** (SLT) [Ger00] stage the data of the Vertex detector as well as the analogue data of the tracking detectors is available. From this data the exact decay vertices and momentum vectors of J/Ψ-candidates are calculated. The decision of the SLT is based on the parallelity of the momentum vector and the displacement of the B-vertex wrt. the target. Furthermore the quality of the track fit is taken into account. A rate reduction of $\approx$ 100 within an average latency of 7ms has to be accomplished. It's implementation does no longer use the ADSP21060 (SHARC™) DSPs[5] of the DAQ[6] system as proposed in [HB95], but a farm of 240 commercial personal computers running *Linux*, which it shares with the third level trigger.

[3] Look Up Tables
[4] Programmable Logic Devices
[5] Digital Signal Processor
[6] Data Aquisition

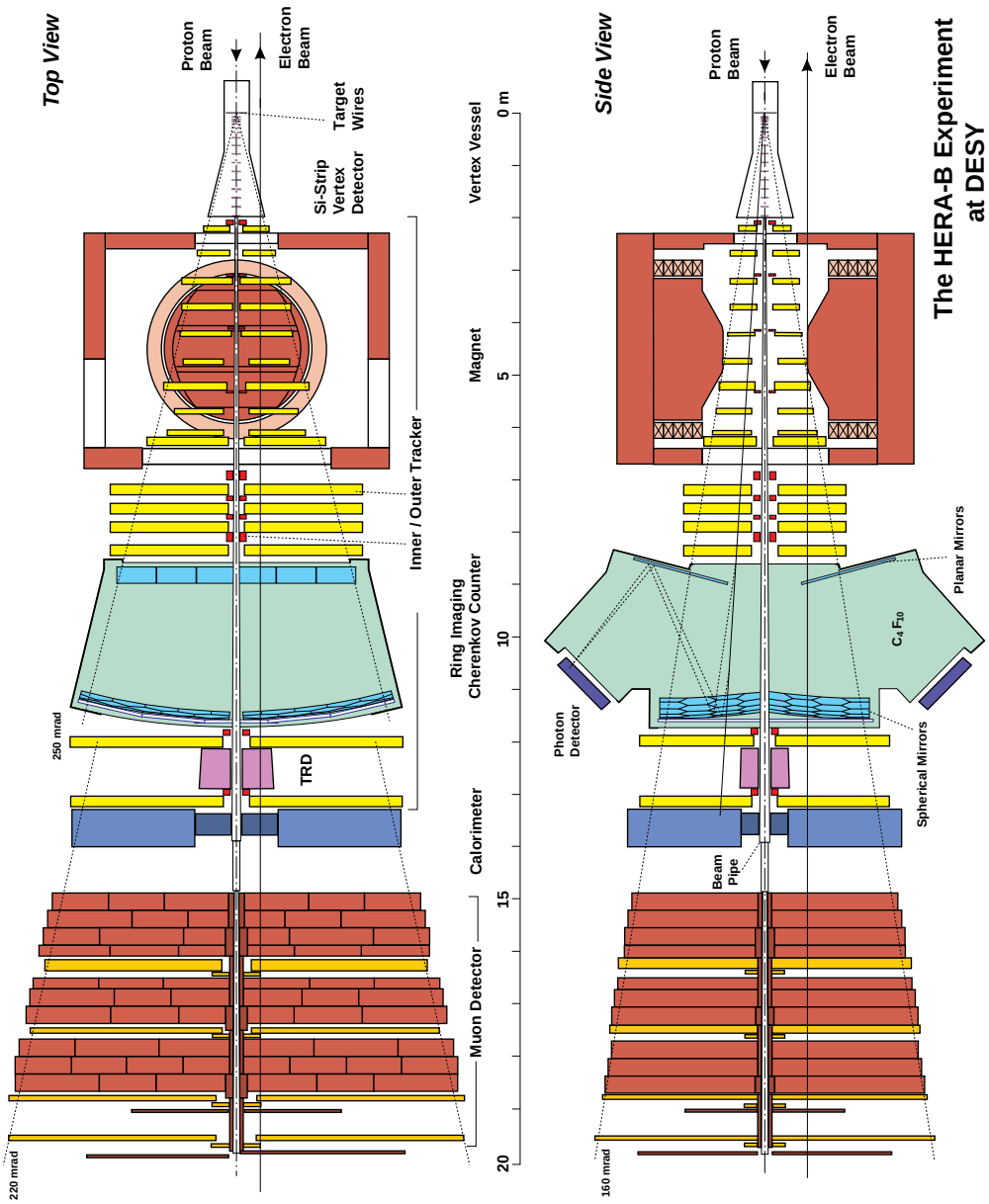


Figure 2.1: HERA-B detector (taken from [HB95])

The **third level trigger** (TLT) runs on the same farm of commercial personal computers as the SLT. Large parts of the TLTs decision are based on information not directly associated with the tracking data, thus enabling triggers for physics outside $\mathcal{CP}$-Violation (e.g B_s mixing). A reduction by a factor of 10 within a latency of 100ms is required to meet the 50Hz input rate of the 4LT.

The **fourth level trigger** (4LT) is also a software implementation. It runs on a dedicated PC farm consisting of 200 CPUs and performs a full event reconstruction, also including the derivation of calibration data. The actual 4^{th} level trigger decision is based on the event classification performed during event reconstruction. The 4LTs decision takes 4s on average, yielding a reduction by 2.5. Finally the data is written to disk or tape at a rate of about 20Hz.

2.1 The Silicon Vertex Detector System of HERA-B

The task of the silicon vertex detector (VDS) is to measure the displacement of the B-meson decay vertices with resolutions of $\leq$500µm in z (beam) direction and $\leq$25µm in the $x-y$ (transverse) plane. A detailed description is given in [Knö98], [Bau98] and [Bau00]. The HERA-B VDS subsystem is read out by HELIX128-2.2[7] chips.

2.1.1 Design Considerations

The final limit for the resolution of tracking detectors is not only restricted by their intrinsic resolution, but also by multiple scattering, i.e. a particle does not have to cross all tracking layers on a straight line. In particular a deflection of the particle before or when hitting the first plane of the detector has a deteriorating effect on the vertex resolution. Therefore the thickness of the material traversed by a particle has to be minimised. A straightforward approach to eliminate this problem is to mount target and vertex detector in a common vacuum vessel, which in case of HERA-B would be a part of the HERA proton ring. However, the necessity to shield the detectors from the fields of the beam mirror current and the wake fields in such a *vertex vessel* (resonant cavity!) prevents the realisation of this solution. Folding a thin shielding around the detector modules as depicted in fig. 2.2 while still placing the detectors in a secondary vacuum leads to the *Roman Pot* [Bat85] configuration. The shielding can be aligned perpendicular to the detector planes and it can be as thin as 100µm, since there is no pressure drop across the shielding. This way the amount of radiation length the particle has to pass through is kept minimal. The rather high impedance of the *vertex vessel* has to be short-circuited for the high beam mirror current ($\geq 2\text{A}_{\text{peak}}$ [Sch]) by some additional shielding, to suppress wake fields and their detrimental effects on the beam.

A retractable Roman Pot system, as implemented in the P238 detector at CERN Sp$\overline{\text{p}}$S [Bra88] provides further improvements, since the detector can be

[7]First HELIX128-3.1 and HELIX128-3.1a equipped detector modules are expected be installed by the end of 2000 (cf. appendix B and E).

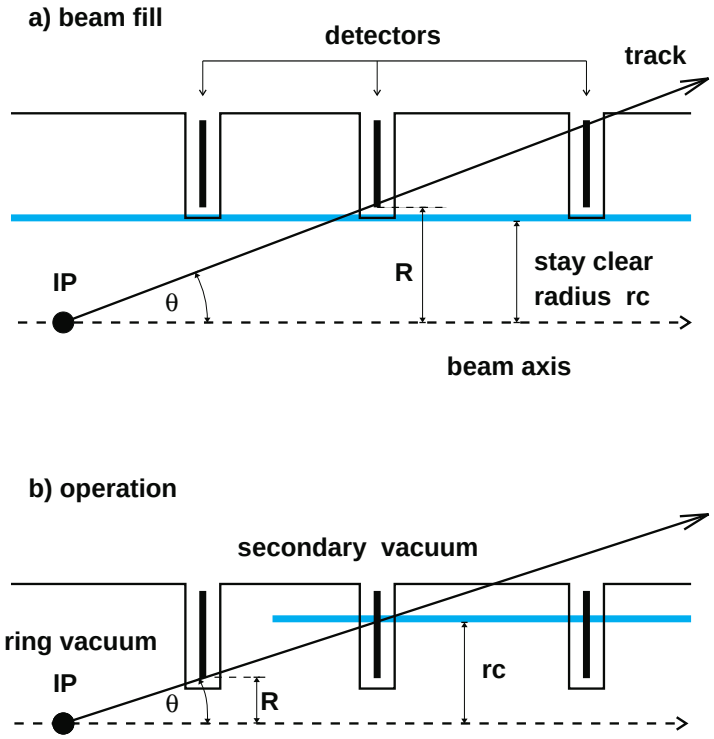


Figure 2.2: Schematic view of a forward vertex detector in a Roman Pot system. The beam pipe is "folded" around the detectors. A retractable Roman Pot system, can be moved closer to the beam during data taking than the *stay clear radius* required for beam fills. Operation close to the beam is required to reach the necessary acceptance for B-meson decays. [Knö98].

retracted to a "save" position while filling the accelerator ring. It can be moved very close to the beam during data taking, thus increasing the resolution of the detector system.

2.1.2 Geometry and Layout

The HERA-B VDS depicted in fig 2.3 provides an angular coverage from 10mrad to 250mrad – consistent with the overall acceptance of the HERA-B detector. It covers 90% of the 4π solid angle in the rest frame of the B mesons. Consisting of eight superlayers, made of two double-sided silicon strip detectors per quadrant, the HERA-B VDS typically provides 4 views per superlayer (cf. fig. 2.4). The detectors are $7\times5\text{cm}^2$, so they can be cut from 4" wafers. To suppress ambiguities in the track reconstruction, views with a small stereo angle are required. Therefore the strips of the silicon detectors are tilted by 2.5°wrt. the detector edges and the two detectors of a superlayer are mounted with the p-sides facing each other. This results in views of ±2.5°, 87.5°and 92.5°.

The detectors of the HERA-B VDS can be retracted from the beam axis during fills as shown in fig 2.5. This is necessary to avoid disturbances during

the filling of the ring and to prevent undue radiation damage during that phase. To increase detector lifetime by distributing radiation damage and accumulated dose more evenly, the detectors can be also moved perpendicular to beam and retraction axes into two working positions, which is also depicted in fig. 2.5.

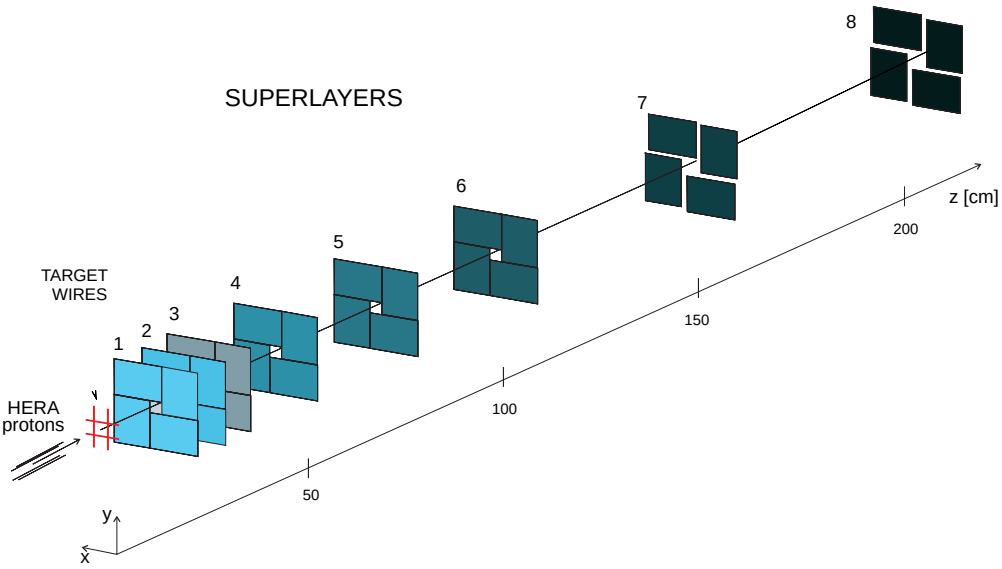


Figure 2.3: Isometric view of the VDS's eight superlayers (taken from [Abt00]).

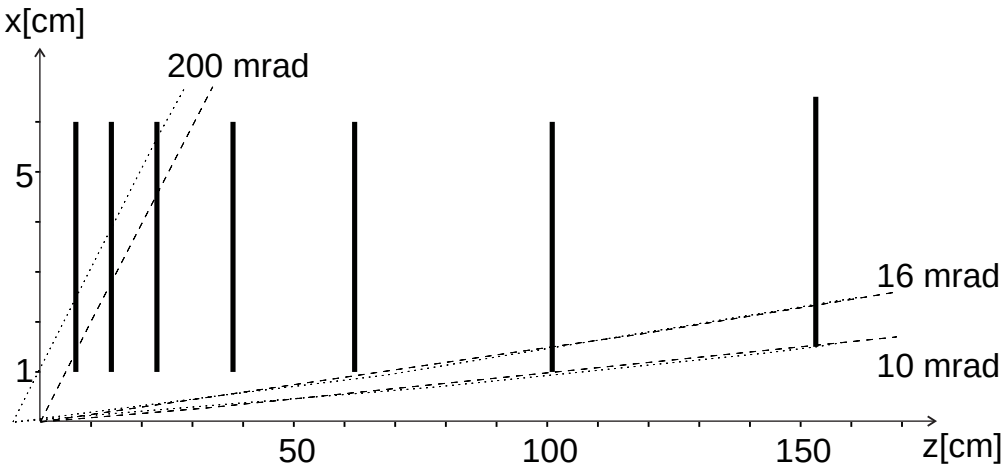


Figure 2.4: Acceptance of the HERA-B silicon vertex detector (taken from [Rie98]). Only the 7 superlayers inside the vessel are shown.

Cooling of the detectors is required to suppress leakage currents (producing noise) and the "reverse annealing" process in the detectors. Furthermore the heat of the readout electronics, dissipating about 10W per quadrant and superlayer, has to be removed .

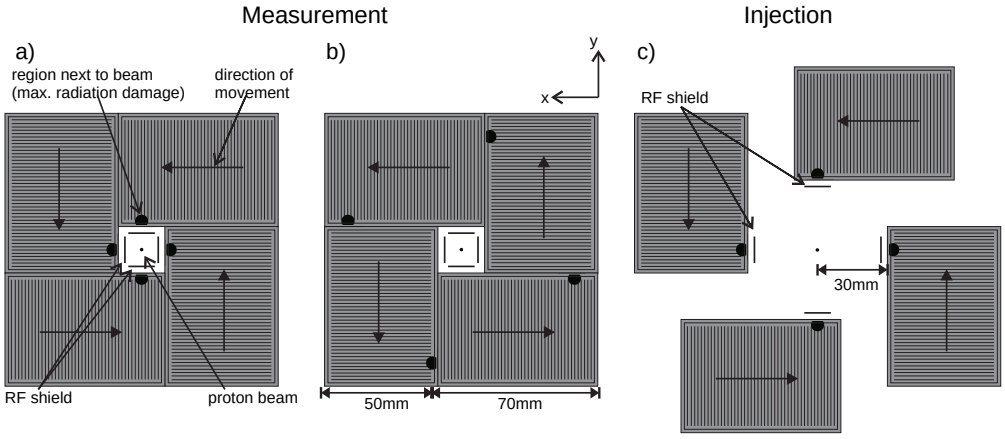


Figure 2.5: Arrangement and retraction schema for the 4 detector elements of a sublayer: a) Detector positions for data taking. b) Alternative detector layout. It is obtained from a) by a 5cm clockwise shift of the detectors. It is intended to increase the lifetime of the detectors by evenly distributing radiation damage. c) Retracted detector positions during beam fills.

2.1.3 Mechanics and Construction

The mechanical backbone of the HERA-B VDS is the conically shaped *vertex vessel* made of stainless steel. A Schematic is shown in fig. 2.6. The length of the vessel, which also contains the eight wire targets is about 2.5m. Its maximum diameter is 1.16m at the rear end, governed by the 250mrad acceptance of the detector. The upstream end of the *vertex vessel* flanges to the HERA proton beam line system. The rear end is closed with a spherically shaped exit window made of aluminium. The exit window is only 3mm thick and welded to the 0.5mm thick beam pipe running through all other parts of the HERA-B experiment to minimise radiation length. Four flanges per quadrant allow the Roman Pots containing the silicon detectors to protrude into the beam region. Retraction and tangential movement of the detectors is accomplished by bellows and spindle gear driven linear bearings attached to the vessel. Detector positions are controlled by commercial electromechanic linear gauges [Brä]. The vacuum inside the vessel is $< 10^{-8}$mbar, while the secondary vacuum inside the Roman Pots is 10^{-6}mbar. Four bands made of aluminum coated stainless steel foil running along the beam from the target to the exit window carry the beam mirror current. They provide suppression of wake fields inside the *vertex vessel* and are retracted together with the detectors during beam fills. The bands are only 5µm thick, but amount to a radiation length of $X/X_0 \approx 3\%$ at 10mrad, i.e. in the worst case.

The detector modules of the 8th superlayer are mounted on the rear end of the *vertex vessel*, outside the exit window. Since they are mounted outside the beam pipe, a retraction mechanism is not required.

Detectors of one quadrant of the first three superlayers are depicted in fig. 2.7.

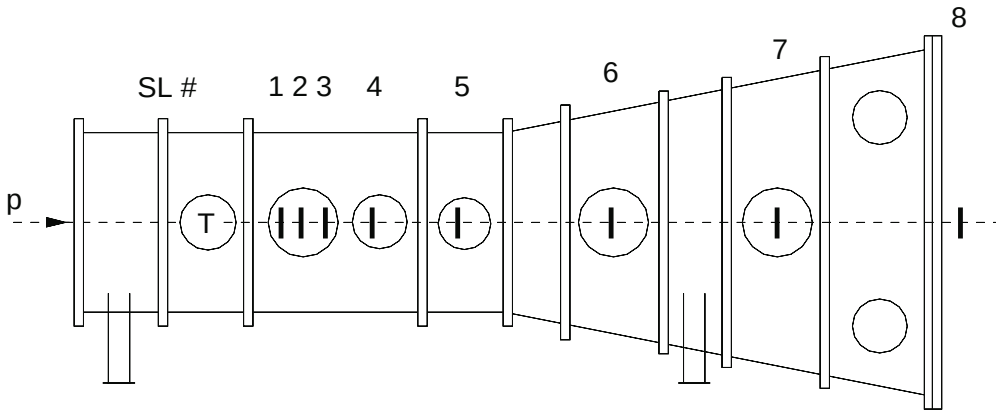


Figure 2.6: Drawing of the *vertex vessel*. The target (T) and the detectors' (I) Roman Pots protrude into the vessel through flanges, which are also located on the top and bottom sides of the vessel.

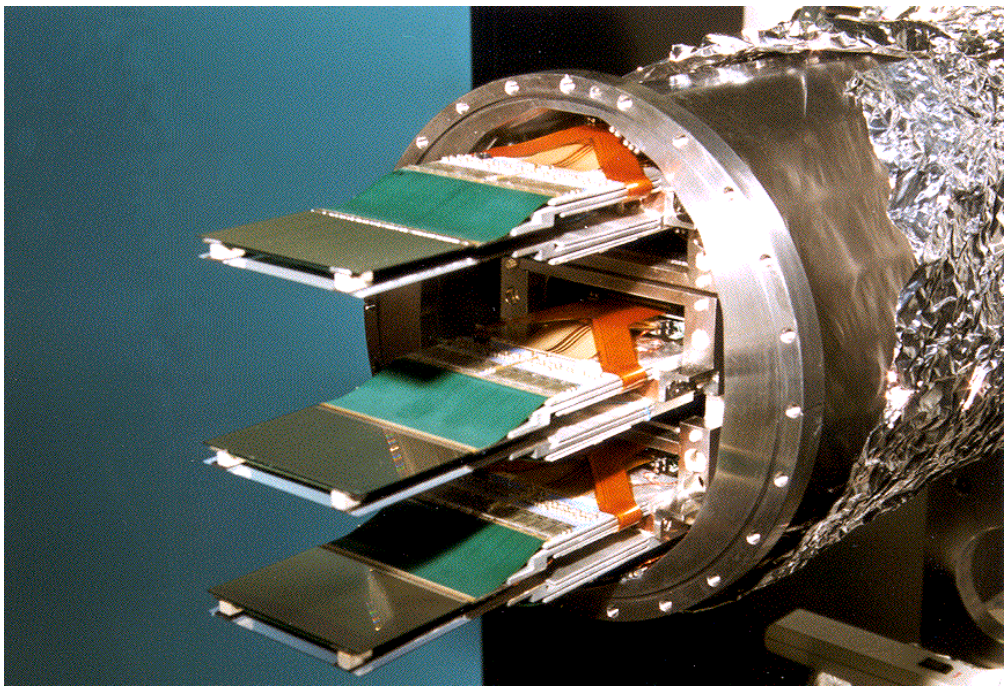


Figure 2.7: Detector modules (one quadrant of the first three superlayers) with two double-sided strip detectors per superlayer. The length of the carbon fibre carriers varies from 150mm for the detectors next to the target (shown) to 430mm for the most downstream ones, which also have separated Roman Pots.

2.2 Silicon Strip Detectors

Besides silicon, there are only a few other materials which might be used for a high resolution tracking detector like the HERA-B VDS. The alternatives are gallium-arsenide (GaAs) (or other III-V semiconductors) and diamond. Besides their higher cost, their primary ionisation per radiation length is smaller than $7800\frac{e^-/\text{hole pairs}}{0.1\%\text{X}_0\ MIP}$ [PDG96] generated in silicon.

2.2.1 Charge Generation

Charged elementary particles traversing matter interact with the electrons and nuclei contained therein. This fact on the one hand enables us to build detectors for these particles, on the other hand, it sets a limit for the spatial resolution of these detectors, as already pointed out in sect. 2.1.1. There are two categories of energy loss a charged elementary particle experiences when interacting with matter:

- Non-ionising energy loss like Čerenkov radiation, Bremsstrahlung and Pair Production in the relativistic energy range and Phonon Excitation at lower energies.
- Ionising energy loss.

For all electromagnetically interacting particles, ionisation is the main contribution to their energy loss.
The mean ionising energy loss per unit path length, also called *stopping power* is given by the Bethe-Bloch formula [Bet33][PDG00]:

$$\left\langle \frac{\partial E}{\partial x}(E) \right\rangle = 4\pi r_e^2 m_e c^2 N_\text{A} \frac{Z}{A} \rho \frac{z^2}{\beta^2} \left(\ln \left(\frac{2m_e c^2 \beta^2}{I(1-\beta^2)} \right) - \beta^2 \right) \tag{2.3}$$

E = projectile energy (in keV)

$\beta = v/c$ projectile velocity

z = projectile charge (in e)

x = path length (in cm)

$r_e = 2.82 \cdot 10^{-13}\text{cm}$ = classical electron radius

$m_e = 511\text{keV/c}^2$ = electron rest mass

$N_\text{A} = 6.02 \cdot 10^{23}\text{mol}^{-1}$ = Avogadro's number

Z = atomic number of the medium (Si: $Z = 14$)

A = atomic weight of the medium (Si: $A = 28.1\text{u} = 28.1\text{g/mol}$)

ρ = mass density of the medium (Si: $\rho = 2.7\text{g/cm}^3$)

I = average ionisation potential (Si: $I = 172\text{eV}$)

Fig. 2.8 shows the specific energy loss of silicon. As expected from eq. 2.3, the energy loss shows a $1/\beta^2$ increase at low energies. This behaviour causes the so-called *Bragg-peak*: A particle stopped in the material has lost most of

its energy at the very end of the track. At relativistic energies the $ln\left(\frac{\beta^2}{1-\beta^2}\right)$ term in eq. 2.3 causes the specific energy loss to increase again. A particle with an energy corresponding to the minimum of the curve is called a *minimum ionising particle* (*MIP*). Most particles encountered in HERA-B are in that energy region.

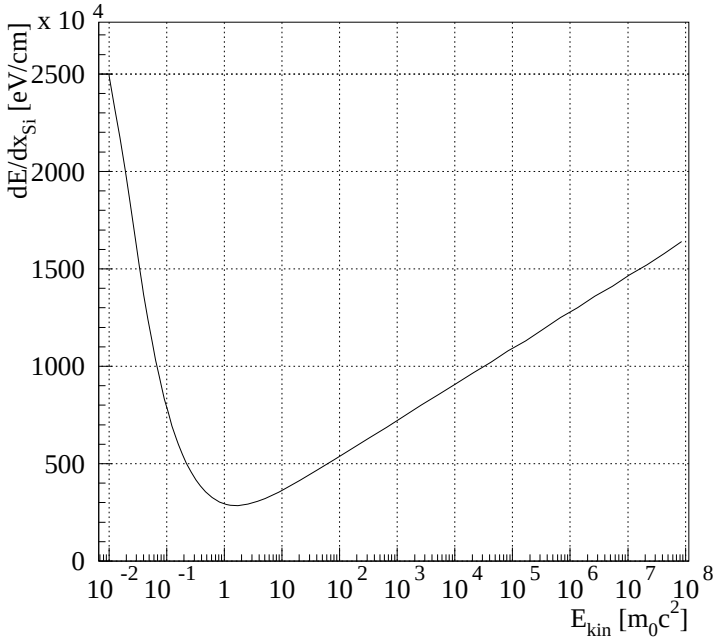


Figure 2.8: *Stopping Power* (energy loss per unit length) of Silicon (eq. 2.3).

The distribution of the energy loss per unit path length $\frac{\partial E}{\partial x}$ is described by the Landau distribution [Lan44], which is highly asymmetric and shows a long tail at high energies. The shape of the distribution arises from so-called δ-electrons, which occasionally receive a high momentum transfer from the incident particle. These δ-electrons can travel some 10µm in silicon, causing secondary ionisation along their path and thus deteriorating the spatial resolution of a detector. The variance (i.e. width) of the Landau distribution is much smaller than the $\sqrt{n_e}$ variance of the Poisson distribution (n_e = number of electron/hole pairs produced), which describes counting processes. The variance of the Landau distribution can be related to the variance of the Poisson distribution by the *Fano-factor* F [Kno97]:

$$var\,(Q) = \quad \sigma^2\,(Q) = \; F\,\langle Q\rangle = F\frac{\langle E\rangle}{\epsilon}\cdot(2q_e)^2 \tag{2.4}$$

$$\Longleftrightarrow \qquad \sigma\,(Q) = \sqrt{F\cdot\langle Q\rangle} = \sqrt{F\cdot\overline{n_e}}\cdot 2q_e \tag{2.5}$$

$\langle E\rangle$ = mean energy loss of the projectile

$\langle Q\rangle$ = mean charge induced by the projectile

F = Fano-factor (Si: $F = 0.084\ldots0.143$)

ϵ = energy to create one electron-hole pair (Si: $\epsilon = 3.6$eV)

$q_e = 1.602\cdot10^{-19}$C = elementary charge

$\overline{n_e}$ = mean number of electron-hole pairs produced

The mean energy loss per unit path of a minimum ionising particle of elementary charge q_e (e.g. a 1...2MeV electron) in silicon is $\left\langle\frac{\partial E}{\partial x}\right\rangle$ ≈390eV/µm [PDG84] or 110 e^--hole pairs per µm on average. Due to the large asymmetry of the Landau distribution, the most probable energy loss per unit path length is 290eV/µm or 82 e^--hole pairs per µm. In 300µm of silicon, which is the usual thickness of commercial wafers, this amounts to 88keV or 24600 e^--hole pairs. It should be mentioned that the average energy ϵ to create an electron-hole pair is 3.6eV, which is larger than the bandgap of 1.12eV.

2.2.2 Charge Detection

To separate electrons and holes an electric field has to be present. Otherwise electrons and holes will recombine again, creating photons and phonons. Unfortunately applying a voltage to intrinsic silicon causes a significant current superimposed to the signal of the detected particle. It is mainly due to charge carrier injection at the contacts,but there is also a thermally generated population of electrons in the conduction band (cf. tab. 2.1) and the same number of holes in the valence band, contributing to conductivity.

Atomic Weight	28.09u
Crystal Lattice	diamond
Lattice Constant	5.43Å
Relative Dielectric Constant ϵ_r	11.9
Breakdown Field Strength	$\approx 3\cdot10^7$V/m
Bandgap ($T = 300$K)	1.12eV
Intrinsic Charge Carrier Density ($T = 300$K)	$1.45\cdot10^{10}$cm^{-3}
n-Substrate Doping Concentration	$1.5\ldots2\cdot10^{12}$cm^{-3}
Electron Mobility μ_e ($T = 300$K)	1380cm^2/Vs
Electron Diffusion Constant D_n ($T = 300$K)	$\approx$ 35cm^2/s
Hole Mobility μ_p ($T = 300$K)	450cm^2/Vs
Hole Diffusion Constant D_p ($T = 300$K)	$\approx$ 11cm^2/s

Table 2.1: Properties of silicon used for Detectors [Sze81]

To suppress this current, contacts to the intrinsic silicon have to be doped, i.e. some silicon atoms are replaced with elements having a different number of electrons in their outermost shell. Doping with elements of the III$^{\text{rd}}$ main group in the periodic table of elements ("acceptors" like boron) will cause holes in the valence band (p-type silicon) and those of the V$^{\text{th}}$ main group ("donors" like arsenic and phosphorus) will create electrons in the conduction band (n-type silicon). The charge carriers created by doping the silicon (majority carriers) will outnumber the carriers of opposite charge intrinsic to the silicon (minority carriers) by several orders of magnitude. As a result the minority carriers will (almost) completely recombine, leaving only the majority carriers for conduction.
Applying a positive voltage to the n-doped part of the diode depicted in fig. 2.9 causes a region of the depth d, the so-called pn-junction, to be depleted from all charge carriers [Ash81]:

$$d_{\text{p,n}} = \sqrt{\frac{2\epsilon_0\epsilon_{\text{r}}(V_0 - V_{\text{D}})}{q_e(n_{\text{D}} + n_{\text{A}})}\frac{n_{\text{A}}}{n_{\text{D}}}} \tag{2.6}$$

$d_{\text{p,n}}$ = depth of the depletion layer (in n and p doped regions)

$\epsilon_0\epsilon_{\text{r}}$ = dielectric constant

n_{A} = acceptor concentration

n_{D} = donor concentration

V_{D} = diffusion voltage

V_0 = external voltage

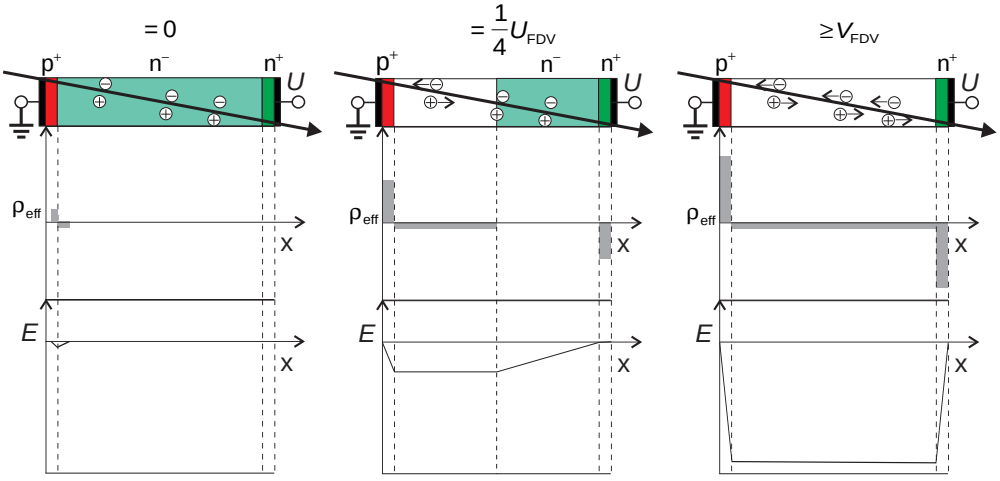


Figure 2.9: Principle, effective space charge density ρ_{eff} and electric field E of a silicon detector (pin-diode) for different bias voltages. Only the electron-hole pairs generated in the depleted region ($E \neq 0$) are separated and cause a signal. V_{FDV} is the full depletion voltage.

E.g. for p-type silicon ($n_\mathrm{A} \gg n_\mathrm{D}$, $V_0 \gg V_\mathrm{D}$) using the specific resistivity

$$\rho_\mathrm{n} = \frac{1}{q_e \overline{\mu}_\mathrm{n} n_\mathrm{D}} \tag{2.7}$$

$\overline{\mu}_\mathrm{n}$ = electron mobility

eq. 2.6 can be simplified:

$$d_\mathrm{n} = \sqrt{\frac{2\epsilon_0 \epsilon_\mathrm{r} V_0}{q_e n_\mathrm{D}}} = \sqrt{2\epsilon_0 \epsilon_\mathrm{r} \overline{\mu}_\mathrm{n} \rho_\mathrm{n} V_0} \tag{2.8}$$

The depletion grows proportional to the square root of the reverse voltage V_0 and the capacitance of the pn-junction decreases $C_\mathrm{pn} \propto 1/\sqrt{V_0}$ [8]. To fully deplete a silicon wafer of 300µm thickness about 40...140V are required. Assuming a homogeneous charge distribution along the particles track, the signal of a silicon detector can be approximated by the superposition of two rectangular current pulses: A short one (≈175nA×10ns) caused by the electrons and a long one (≈70nA×25ns) due to the holes [PDG00]. Since the signal is a current the depletion voltage has to be supplied via bias resistors, which leads to the equivalent circuit depicted in fig. 2.10.

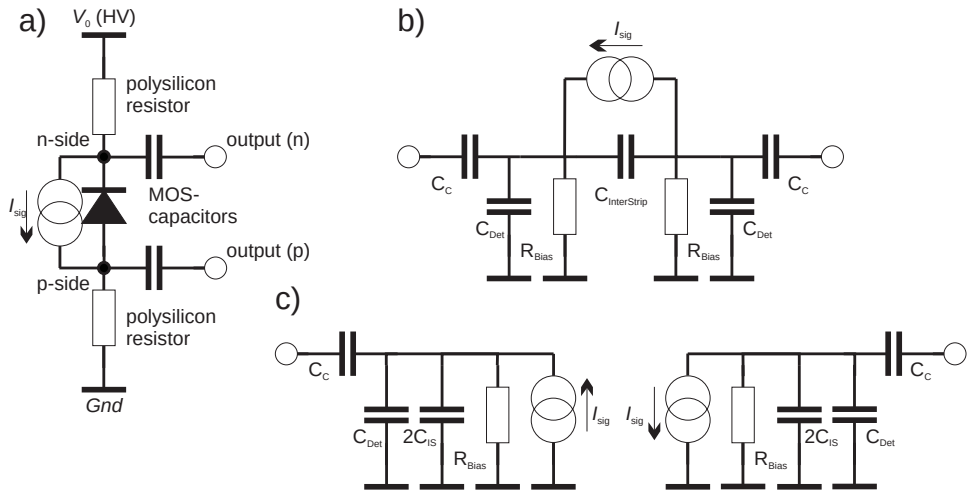


Figure 2.10: a) Equivalent circuit of a silicon detector with bias resistors and AC coupling. The change in the voltage drop over R_bias due to radiation damage requires AC coupling of the readout electronics. b), c) small signal models of a)

Due to radiation damage (cf. chapter 4) the n^- substrate of detectors used in HERA-B turns into p^- silicon when subjected to a fluence $\Phi \gtrsim 3.5 \cdot 10^{12}\mathrm{cm}^{-2}$ [Rie98]. Furthermore radiation damage also increases the leakage current ($I_\mathrm{leak} \propto \Phi$ [Lut99]), which is removed by AC-coupling of the readout electronics. The leakage current is the only *intrinsic* noise source of a silicon

[8] This dependency is used e.g. for voltage controlled oscillators or filters (VCO, VCF).

detector, but the detector capacitance together with the principle of a charge sensitive amplifier accounts for an additional noise contribution (cf. eq. 3.16).

2.2.3 Spatial Resolution

To obtain a spatial resolution from a silicon detector, the heavily doped contacts have to be segmented. E.g. dividing the n^+ and p^+-implants into orthogonal strips results in a double-sided silicon strip detector as the ones used in the HERA-B VDS depicted in fig. 2.11. It should be denoted that the e.g. for detectors made from an n-type wafer, the region between the n^+ implants can not be depleted. Thus the strips have to be isolated by an additional p-implant.

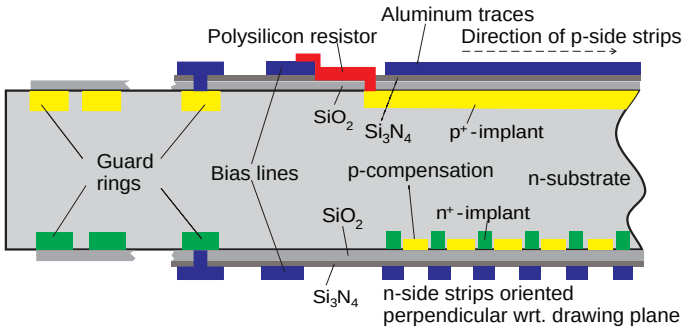


Figure 2.11: Cross section of a silicon strip detector (not to scale) taken from [Rie98].

The spatial resolution of such a detector for single strip hits is given by [Lut87]:

$$\sigma_x = \frac{\Delta x}{\sqrt{12}} \tag{2.9}$$

Δx = strip pitch

Fortunately the charge is usually distributed among two or more strips, enabling interpolation by calculating the charges' centre of gravity. Assuming a rectangular charge distribution having a width equal to the strip pitch Δx and a finite signal to noise ratio, interpolation over n strips yields a resolution of [Lut87]:

$$\sigma_x^2 = \left(\frac{\Delta x}{S/N}\right)^2 \sum_{i=1}^{n} \left(\frac{x_1 - \overline{x}}{\Delta x}(i-1)\right)^2 \tag{2.10}$$

Δx = strip pitch

S/N = signal to noise ratio

x_1 = position of the 1st strip used for calculation

$\overline{x}$ = calculated centre of gravity

The best resolution is obtained when the particle hits exactly between two adjacent strips with only their signals evaluated. Eq. 2.10 then yields

$$\sigma_x = \frac{\Delta x}{\sqrt{2} \cdot S/N}. \tag{2.11}$$

For a strip pitch of 50µm and a S/N = 20 the calculated resolution is $\sigma_x = \frac{50\mu\text{m}}{\sqrt{2}\cdot 20} = 1.8\mu\text{m}$. However, inclined tracks, the Landau-distributed charge generation and quantisation errors of ADCs employed in subsequent DAQ stages have not been taken into account for this calculation. In practical detector operation resolutions of $\lesssim 10\mu$m are reached.

2.3 The Inner Tracking System of HERA-*B*

The track information of the inner tracking system is used to connect hits in the calorimeter to the vertex detector, and thus has to provide binary information for the L1 trigger as well as (higher resolution) analogue data required for tracking and momentum measurement.

The inner tracking detector is divided into 48 layers, 36 between the silicon vertex detector and the RICH, the remaining 12 between RICH and the calorimeter (cf. fig. 2.1). Each of these layers consists of four MSGC-GEM detectors, each covering one quadrant around the beam pipe [HB95].

The mechanical structure of the ITR consists of carbon fibre composite plates attached to the support structure of the OTR, with an MSGC-GEM detector on either side. Since these detectors cover the same quadrant, four of these plates form two layers of the ITR. Besides the detectors, the carrier plates also hold HV supply circuitry and gas supply tubing. For detector readout three readout boards, each equipped with two HELIX128 chips, connect to one MSGC. These six readout boards together with the subsequent "trigger driver board" are also mounted to the support plates.

2.4 Microstrip Gaseous Chamber Detectors

Microstrip Gaseous Chambers (MSGC) [Oed88] are derived from MWPCs[9] [Cha70] [Cha68] and share the same principle of operation. The difference is that the anode wires of the proportional chamber are replaced by a planar anode structure on top of an insulating substrate. Created with photolithographic techniques, structures having an anode strip pitch of $\leq 300\mu$m can be produced.

Eq. 2.3 describes the ionisation caused by a particle traversing matter. In case of gaseous media, electrons and ions are created. Despite the relatively low ionisation energies of typical fill gases ($I_{\text{Ar/CH}_4} \approx 30$eV), the low density of the media reduces the primary ionisation to about $8.5e^-$-ion pairs per mm. Applying a constant electric field $\vec{E}$, electrons and ions will drift towards anode

[9] Multi Wire Proportional Chamber

or drift electrode with a constant velocity given by [Sau91]:

$$\vec{v}_{\mathrm{d}} = \frac{q_e \vec{E}}{\sqrt{2m}\rho\sigma(\overline{\epsilon})\sqrt{\overline{\epsilon}}} \tag{2.12}$$

$\vec{E}$ = electric field

m = mass of the ion or electron

ρ = molecular density of the gas

$\sigma(\overline{\epsilon})$ = cross section for scattering

$\overline{\epsilon}$ = mean energy of the ion or electron

In the vicinity of the anodes the electric field is strong enough for secondary ionsation, causing an avalanche of electrons and ions. The electric field in this region can be approximated by a cylindrical capacitor ($E(r) = \frac{1}{\ln(r_{\mathrm{a}}/r_{\mathrm{b}})}\frac{V_{\mathrm{a}}}{r}$) with radii r_{a}(inner) and r_{b}(outer). The multiplication of the small initial charges by secondary ionisation in the region of the very high electric field near the anodes is given by the the Diethorn-formula [Die56]:

$$a = \exp\left[\frac{V_{\mathrm{a}}}{\ln\left(r_{\mathrm{b}}/r_{\mathrm{a}}\right)}\frac{\ln 2}{\Delta V}\ln\left(\frac{V_{\mathrm{a}}}{p r_{\mathrm{a}} K \ln\left(r_{\mathrm{a}}/r_{\mathrm{b}}\right)}\right)\right] \tag{2.13}$$

V_{a} = applied high Voltage

r_{a} = anode radius ($r_{\mathrm{a}} \approx 10\mu$m for MSGCs)

r_{b} = cathode radius ($r_{\mathrm{b}} \leq 120\mu$m for MSGCs)

p = gas pressure

$\Delta V, K$ = gas parameters

Usual values for a are in the order of several thousands.

The secondary ionisation process also causes UV-light due to the de-excitation of freshly ionised atoms. To avoid ionisation by these UV photons, which would cause an avalanche of ionisation filling (and probably destroying) the whole detector, the photons have to be absorbed by a "quencher" gas (e.g. CH_4) added to the gas mixture.

In case of a proportional detector, the signal to noise ratio does not only depend on the Landau-distributed primary charge, but also on the Polya-distribution describing fluctuations in the gas multiplication (i.e. the avalanche size). According to [Kno97] the Polya-distribution can also be related to Poisson statistics:

$$S/N = \frac{Q}{\sigma(Q)} = \frac{\sqrt{n}}{\sqrt{F+b}} \tag{2.14}$$

n = number of primary electron-ion pairs (≈ 25 for an MSGC)

F = Fano-factor ($F \approx 0.17$)

b = factor for Polya-distribution ($b \approx 0.5$)

Applying eq. 2.10 to the values given above yields S/N of about 6, and a spatial resolution of about 35µm for an MSGC with 300µm anode pitch.

2.5 Microstrip Gaseous Chamber Detectors with Gas Electron Multiplier

Not only for HERA-B[HB93] [HB95] but also for many other experiments (e.g. [CMS94]) MSGCs were considered the optimum replacement for MWPCs in high-rate hadronic environments or when fast readout was required. But the first tests with "larger" detectors ($(12.5 \times 12.5)\text{cm}^2$) showed that the concept failed in a hadronic environment [Vis96] [Hot97] [Bre97]: To achieve electron multiplication by $a \approx 4000$ a rather high electric field in the vicinity of the anode strips was required. The primary ionisation of heavy or slow particles (e.g. nuclear fragments) together with this high field caused sparks and arcovers, which in turn produced open circuits on the anode strips due to spark erosion. For that reason other experiments (e.g. CMS) abandoned their plans to use MSGCs.

In theory one can overcome this sparking problem by reducing the anode voltage and hence the electron multiplication in the anode region. For a practical realisation, one would have to employ some kind of "electron premultiplier" to achieve the required gain and S/N figures. The *Gas Electron Multiplier* (GEM) proposed by F. Sauli [Sau96] [Sau97] is such a device: It consists of a Kapton foil with copper coating on both sides, through which holes of 55µm diameter are etched. The pitch of the hexagonally arranged holes is 140µm. When a high voltage is applied between top and bottom side of the GEM foil, all field lines have to pass through the holes. The field can be chosen high enough to cause electron multiplication inside the holes. Fig. 2.12 shows a schematic drawing of a MSGC-GEM including a few field lines, while fig. 2.13 shows a $25 \times 25\text{cm}^2$ MSGC-GEM used in the HERA-B inner tracking system.

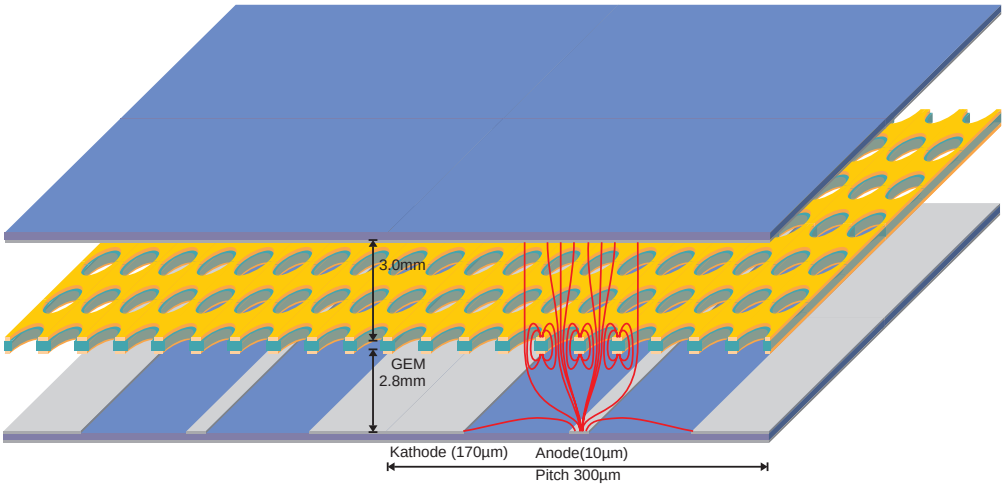


Figure 2.12: Schematic drawing of a MSGC-GEM. The electron multiplication process is split between the GEM foil (centre plane with holes) and the anode strips (on bottom plane). This greatly reduces the risk of discharges and arcovers. The dector is only sensitive to primary ionisation in the volume between the drift electrode (top plane) and the GEM-foil, since only charges generated there are multiplied by the GEM.

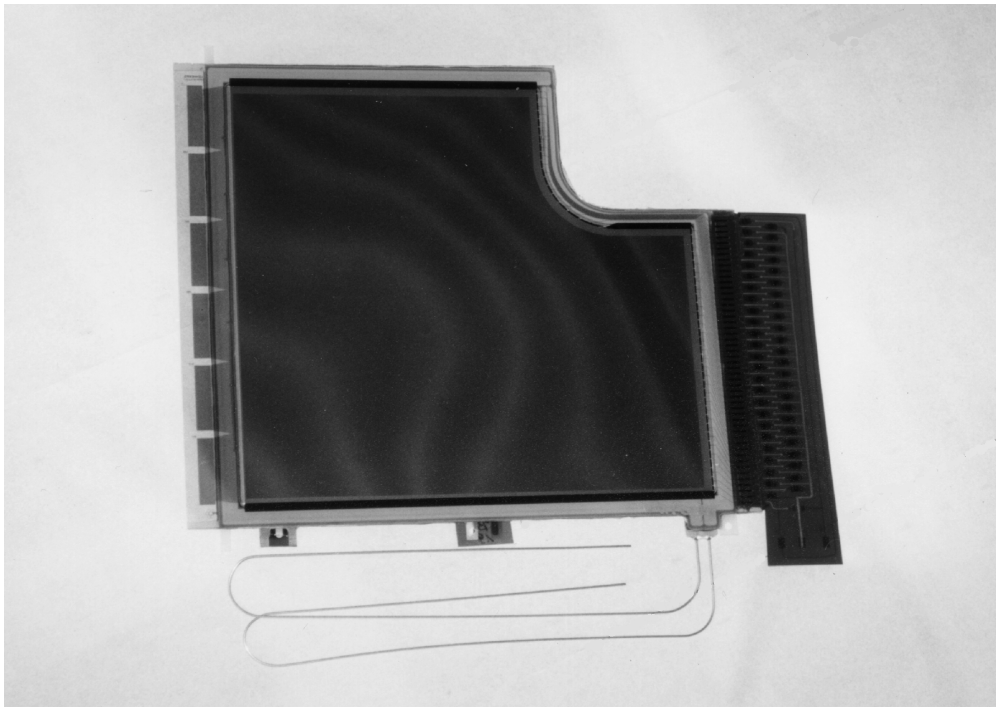


Figure 2.13: Photography of a MSGC-GEM detector used in the HERA-B inner tracking system. The anode strips are horizontally aligned and the readout electronics are connected to the left-hand side of the detector (6 HELIX128 chips, i.e one per connector group). The PCB on the right-hand side contains the cathode biasing circuits. The HERA proton beam pipe passes through the cut out top left edge of the detector.

Chapter 3

The HELIX128-2.2 Readout Chip

3.1 Requirements

To comply with the requirements of the HERA-B experiment, a readout chip for the silicon vertex detector and inner tracking system had to be built to the following specifications, which are mainly taken from [HB93] and [HB95]:

- **Number of channels:** 128 (plus an additional frontend-only test channel for detector studies, which is not required but would be a nice add on.)
- **Noise:** For new chips a noise figure better than $400e^- + 40e^-/pF$ is required to achieve a signal-to-noise ratio of $\geq$20 with detector capacitances of 20pF and signals of $24 \cdot 10^3 e^-$. After 2kGy accumulated dose, a S/N ratio $\geq$13 under the same conditions was required. The *wear limit* for irradiated detector modules given in [Rie98] is S/N $\leq$ 7 to remain operational with a reasonable safety margin.
- **Signal shape:** For a chip using peak sampling mode, rise and fall times $\leq$96ns (the HERA *bunch crossing* frequency) are needed. A remainder or undershoot in the following sample would seriously deteriorate the trigger performance of the chip and therefore has to be $\leq$5%.
- **Leakage current compatible charge sensitive amplifier:** For DC-coupling to an MSGC detector, the charge sensitive amplifier must be able to sink the leakage current of an anode strip ($I_{\text{leak}} \leq$ 50nA [Zie]).
- **Input protection:** The gates of the input transistor have to be protected from voltages $\geq$ 15V when MSGCs are read out. The protection must not deteriorate the noise performance of silicon strip detectors. Internal protection diodes and external series resistors only present in MSGC systems are the most feasible solution.
- **Sampling frequency:** The sampling frequency is given by the 10.4MHz *bunch crossing* frequency of the HERA accelerator ring.

- **Latency:** The decision of the first level trigger in HERA-B is available after 12µs. This requires a storage depth of about 128 samples.

- **Analogue readout:** The 128 channels of one chip can't be read out in parallel. Therefore they have to be multiplexed to a single line.

- **Readout architecture** is governed by the 50kHz L1 trigger rate and the requirement of dead-time free operation (i.e. simultaneous sampling and readout) in HERA-B. To minimise common mode noise, the readout frequency should be an (preferably even) integer multiple of the sampling frequency. Including a 100% safety margin for the trigger rate, this leads to 20.8MHz for single chip readout and 31.2MHz (41.6MHz) for the daisy chained readout of two chips. The latter reduces the number of channels in the subsequent DAQ stage by a factor of two. Therefore daisy chained readout was considered a requirement. To avoid dead time introduced by fluctuations of the trigger rate, a derandomiser buffer for 8 triggers was demanded.

- **Trigger signals:** HERA-B's L1 trigger relies on track data from the inner tracking systemand OTR. To obtain this information from the ITR, all channels have to be equipped with discriminators sharing a common threshold level and feeding their outputs to a second, undelayed readout path. The required resolution is 96ns in the time domain and better than 2400e^- in amplitude. The required spatial resolution is in the order of 1.5mm, which allows to combine (i.e. logical OR) the signals of four channels (cf. section 2.3). Open drain outputs of the trigger signals are feasible, since in HERA-B the data of two MSGCs are `or`ed together. Though not required for HERA-B, the polarity of the discriminator outputs was made switchable to allow use of the trigger outputs also with double-sided silicon detectors.

- **Geometry:** To comply with the 50µm readout pitch of silicon strip detectors, the width of the chip is restricted to 6.4mm. The requirement was set to 6.2mm to cover inaccuracies in the dice cutting and chip placement processes.

- **Radiation tolerance:** The detector modules of the HERA-B silicon vertex detector have to be replaced after about one year of operation. This is due to the deterioration of the silicon strip detectors by radiation damage. Since the readout chips can not be disconnected from detectors and reused, they will be replaced within the same intervals. The required radiation tolerance for the readout chips given in [HB93] and [HB95] is 2kGy/a. In the final design of the vertex detector the chips are mounted at $r_\perp$ =10cm instead of $r_\perp$ =7cm as claimed in [HB93], which reduces the annual dose by a factor of two. It is however advisable to provide a safety margin of at least 100% (cf. chapter 5).

- **Power dissipation:** The cooling system for the readout chips of the silicon vertex detector, which are mounted in the vacuum vessel, has been

built to handle up to about 14W per quadrant and superlayer [Sey97] $((1280\text{ch} + 1024\text{ch}) \cdot 2 = 4608\text{ch})$ [Sey97]. Therefore the power dissipation has to be less than 3.0mW per channel.

- **Remote control:** The chips are inaccessibly mounted inside the detector or inside a vacuum vessel. Therefore the remote adjustment of all parameters that might need to be changed (e.g. bias currents or control voltages) is mandatory. On the other hand the number of control lines for the chip has to be kept at as small as possible.

These specifications are very close to those of the CERN RD20 [Gad92] [Bin93] [Bre94/1] [Bre94/2] FElix chip and its derivatives [Fre95] [APV6] [Fre96] developed for experiments at the future CERN LHC accelerator. Unfortunately did these chips neither fulfill all the requirements of the HERA-B experiment (esp. concerning sampling frequency, subsequent triggers, trigger outputs and the ability to read out MSGCs) nor were these chips available in quantities in 1995, when the development of the HELIX128 started. Except for the deconvolution filter, which is not required at 10MHz sampling frequency, the HELIX' analogue signal path very closely resembles the RD20 concept, while the HELIX' Pointer/FIFO based implementation of the storage/readout control circuit is completely different from the shift register based solution implemented on the RD20 FElix chip.

3.2 Overview

The block schematic of the HELIX128-2.2[1] is depicted in fig. 3.1. Its deduction from the requirements is rather straight-forward: Each channel's readout path splits after the front end. The output of each front end channel is sampled onto a pipeline storage capacitor and in parallel it is AC-coupled to a comparator. This AC-coupling removes the individual offset voltage of each frontend channel and permits a common threshold voltage for all 128 channels. The comparator outputs run through an XOR gate enabling a polarity reversal before being ORed together in groups of four adjacent channels. These 32 signals are then latched with a clock signal independent from the analogue sampling process. The outputs of these latches connect to open drain output pads.

The sampled analogue signal has to be kept for up to 128 clock cycles before it is either overwritten or marked for readout by a trigger signal. The oldest triggered samples are read out with a resetable charge sensitive amplifier and multiplexed together with some digital information to a single line. The signal of this line is driven off-chip by a current buffer. This storage/readout sequence is controlled by a digital circuit, which can also handle up to 8 subsequent triggered samples and the daisy chained readout of two or more chips (i.e. they subsequently multiplex their analogue data to the same readout line).

[1] This description also covers all subsequent versions (i.e. HELIX128-2.2 also covers the HELIX128-3.0, HELIX128-3.1 and HELIX128-3.1a chips) unless otherwise denoted (cf. appendix B and E).

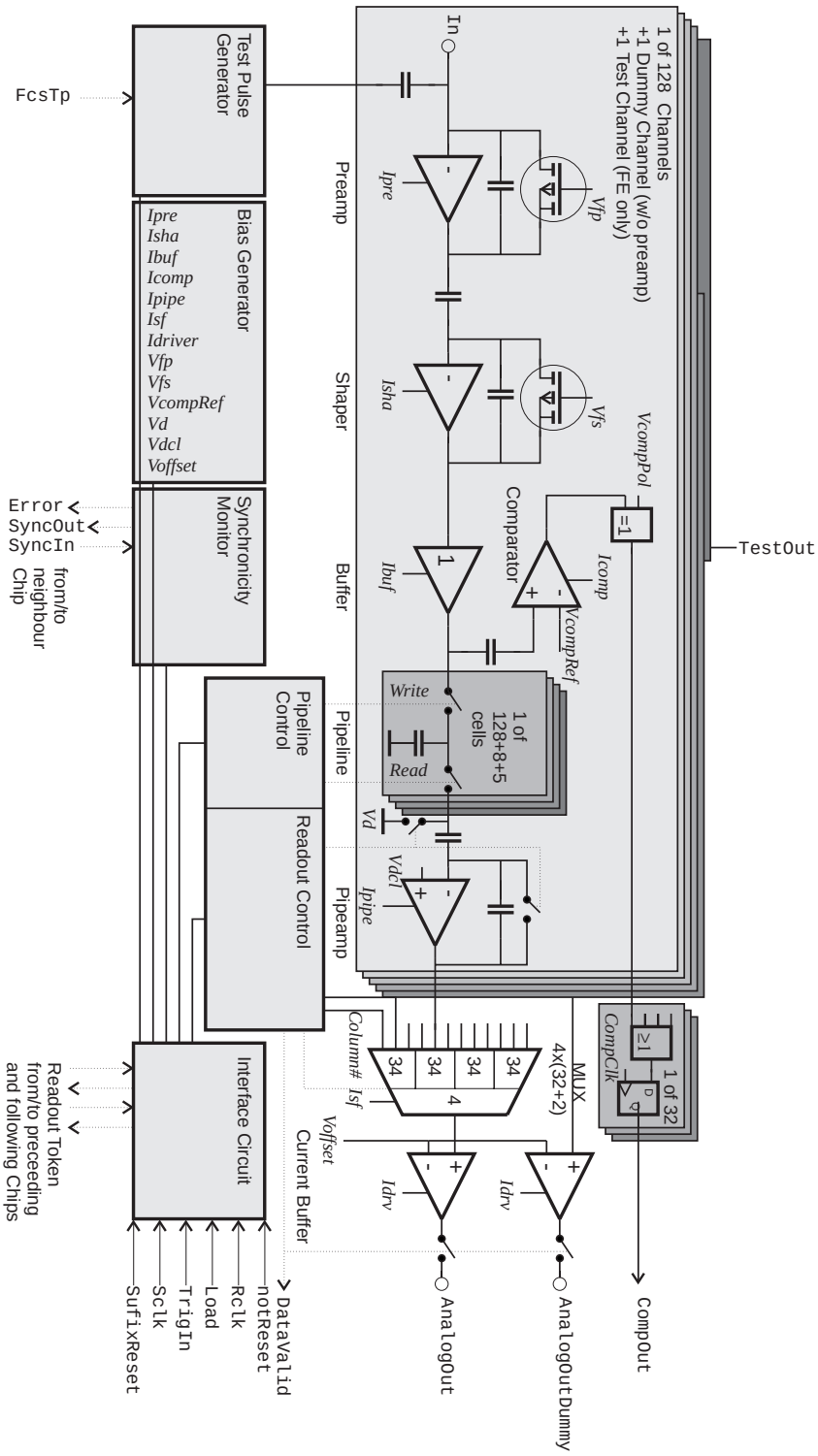


Figure 3.1: Block schematic of the HELIX128-2.2 and later chips.

Remote control is accomplished via the trigger input and a dedicated `load` signal[2], allowing the adjustment of bias currents, control voltages, trigger latency and other parameters.

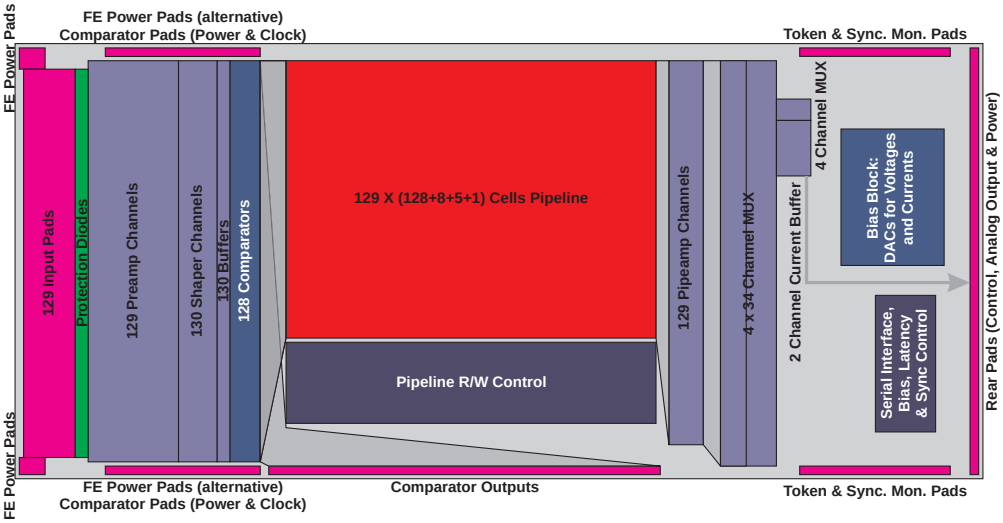


Figure 3.2: Layout floorplan of the HELIX128-2.2 and later chips. The relaxed spacing of the building blocks on the right-hand side of the chip is due to the space required by the token and synchronicity monitoring pads.

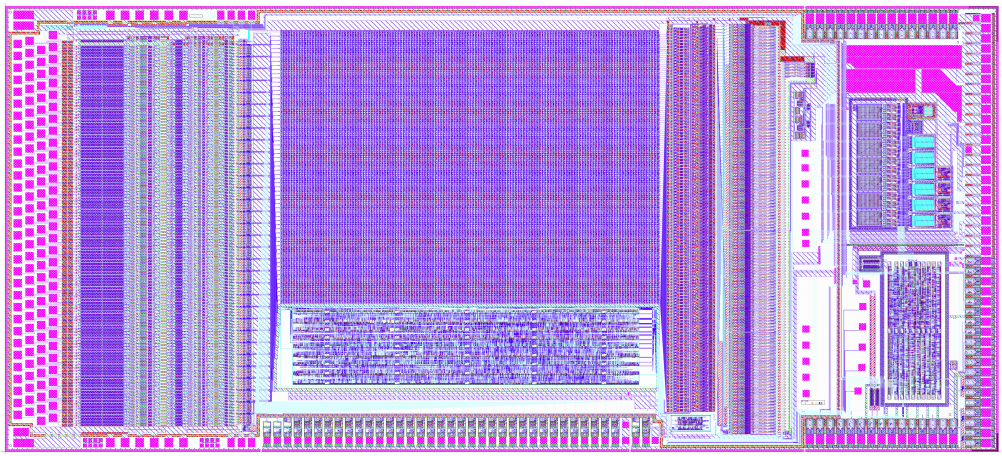


Figure 3.3: Layout of the HELIX128-3.0 chip. It differs from HELIX128-2.2 only in only very few details. The colour scheme of the layers is explained in fig. 4.1.

The layout floorplan of the $(6.2 \times 14.2)\text{mm}^2$ chip is shown in fig. 3.2. It is governed by the attempt to separate the noisy (i.e. digital) components from the sensitive ones (esp. the frontend) while keeping related or interacting parts as close together as possible. Fig. 3.3 shows the layout of the chip.

[2]HELIX128-2.0 and 2.1 use a dedicated 3-line interface instead.

3.3 Frontend

The frontend of a readout chip for silicon strip detectors or Microstrip Gaseous Chambers has to consist of a charge sensitive or current sensitive preamplifier and a filter circuit. The decision upon the principle of the preamplifier can be either based on the expected noise performance for a given detector capacitance and bandwidth or the chip technology used. In case of microstrip detectors and 10MHz signal rate the decision has to be in favour of a charge sensitive amplifier [Fal98] from the noise performance point of view:

$$q_{\mathrm{ineq}}^2 = 4kT\frac{1}{(R_{\mathrm{p}} \parallel R_{\mathrm{fb}})|\imath\omega|^2} + \frac{i_{\mathrm{p}}^2}{|\imath\omega|^2} + e_{\mathrm{s}}^2 \cdot \left(C_{\mathrm{p}}^2 + C_{\mathrm{fb}}^2\right) \ [\mathrm{C}^2/\mathrm{Hz}] \quad (3.1)$$

q_{ineq} = equivalent spectral input noise charge density (cf. sect. 3.3.1) [$\mathrm{C}/\sqrt{\mathrm{Hz}}$]

i_{p} = (parallel) current noise density [$\mathrm{A}/\sqrt{\mathrm{Hz}}$]

e_{s} = (series) voltage noise density [$\mathrm{V}/\sqrt{\mathrm{Hz}}$]

k = Boltzmann's constant ($1.38 \cdot 10^{-23}\mathrm{J/K}$)

T = absolute temperature [K]

ω = angular velocity equivalent to the system bandwidth [s^{-1}]

R_{p} = resistance on amplifier input node (i.e resistance of the detector, $\geq$ 10MΩ for MSGs or silicon strip detectors) [Ω]

R_{fb} = feedback resistance of the amplifier ($\leq$ 1MΩ for a current sensitive amplifier, $\geq$ 10MΩ for a charge sensitive amplifier) [Ω]

C_{p} = capacitance on amplifier input node (i.e capacitance of the detector, $\approx$ 20pF for MSGCs or silicon strip detectors) [F]

C_{fb} = feedback capacitance ($\approx$ 0 for a current sensitive amplifier, $\approx$ 300fF for a charge sensitive amplifier) [F]

While the first term in eq. 3.1 is increased for a current sensitive amplifier due to the lower values of R_{fb} required, the finite contribution of C_{fb} to the last term for the charge sensitive amplifier can be still neglected. For microstrip detectors C_{fb} is smaller than C_{p} by about two orders of magnitude. Therefore a charge sensitive amplifier is feasible. For C_{p} comparable to C_{fb} (e.g. for pixel detectors) and increased system bandwidth (supressing the first two terms in eq. 3.1) the current sensitive amplifier takes over.

Concerning the chip technology a charge sensitive amplifier is feasible when implemented in CMOS technology:

The polysilicon feedback capacitor governing the behaviour of a charge sensitive amplifier is a nearly ideal, extremely accurate and well matching device, while linear resistors required for current sensitive amplifiers are suffer from by bad accuracy, poor matching and large parasitics in CMOS processes. In a bipolar process a current sensitive amplifier can make use of a common base circuit, which eliminates the feedback resistor and takes advantage of the higher transconductance of bipolar transistors.

The HELIX128 is manufactured in AMS' CYE (0.8µm CMOS) process [AMS97/2] and consequently a charge sensitive amplifier was chosen.

The pulse shaping circuit is a band pass filter. Possible implementations on integrated circuits include the "classic" continuous (i.e. $CR-(RC)^n$) implementation, switched capacitor (SC) techniques like double or quadruple correlated sampling and the deconvolution method, which implements a combination of both. The expected noise performance of various filter implementations is given in tab. 3.1.

Pulse processing		Noise ($\overline{ENC^2}$)		Comment
Sampling	Filter	parallel	series	
single	none	$\frac{i_{\mathrm{np}}^2}{2} \cdot 0.535\, T_{\mathrm{meas}}$	∞	1, 2
single	$CR-RC$	$\frac{i_{\mathrm{np}}^2}{2} \cdot 0.475\, T_{\mathrm{meas}}$	$\frac{e_{\mathrm{ns}}^2}{2} C_{\mathrm{p}} \cdot 7.18/T_{meas}$	
double	none	$\frac{i_{\mathrm{np}}^2}{2} \cdot 0.750\, T_{\mathrm{meas}}$	$\frac{e_{\mathrm{ns}}^2}{2} C_{\mathrm{p}} \cdot 2.54/T_{meas}$	1, 3, 4
double	$CR-RC$	$\frac{i_{\mathrm{np}}^2}{2} \cdot 0.238\, T_{\mathrm{meas}}$	$\frac{e_{\mathrm{ns}}^2}{2} C_{\mathrm{p}} \cdot 15.2/T_{\mathrm{meas}}$	3, 4
quad	none	$\frac{i_{\mathrm{np}}^2}{2} \cdot 0.731\, T_{\mathrm{meas}}$	$\frac{e_{\mathrm{ns}}^2}{2} C_{\mathrm{p}} \cdot 2.68/T_{\mathrm{meas}}$	1, 3, 5
deconvolution		$\frac{i_{\mathrm{np}}^2}{2} \cdot 0.786\, T_{\mathrm{meas}}$	$\frac{e_{\mathrm{ns}}^2}{2} C_{\mathrm{p}} \cdot 1.80/T_{\mathrm{meas}}$	3, 6

1. Preamplifier implementation difficult due to the high gain required in real world applications. In turn the preamp has a restricted dynamic range and is prone to pile-up (cf. sect. 3.3.2).
2. Poor pulse separation
3. Implementation of trigger comparators requires the reuse of samples and pulse processing already in the frontend.
4. Without reuse of samples dead time of 1 sample after readout
5. Without reuse of samples dead time of 3 samples after readout
6. Without reuse of samples dead time of 2 samples after readout. Timing jitter will deteriorate noise performance.

Table 3.1: $\overline{ENC^2}$ (Equivalent Noise Charge) values for different signal processing techniques [Fal98]. The output of the charge sensitive preamplifier is sampled if there is no filter present. A common time consumption for the measurement T_{meas} was enforced. $i_{\mathrm{np}}^2 = 2eI_0 + \frac{4kT}{R_{\mathrm{p}}}$, $e_{\mathrm{ns}}^2 = 4kTR_{\mathrm{s}}$ are the spectral noise densities (cf. sect. 3.3.1).

The best results are achieved with a combination of double correlated sampling and $RC-CR$ filtering if parallel noise is the dominant contribtion. For applications dominated by series noise the deconvolution method is the optimum solution.

The requirements to generate L1 trigger signals and to provide a dead-time free operation severely restrict the choice of the shaping circuit. In this case all SC implementations have to use their samples more than once (reuse of samples). Furthermore the generation of a L1 trigger signal requires that all the pulse processing takes place already in the front end and at the nominal

sampling frequency. It is evident that this concept is prone to clock feedthrough and charge injection, which both have an impairing effect on the noise performance. Due to the poor results from other SC circuits in a low-noise environment [Bec96] a SC filter based solution was not considered an option. Instead the well proven CR-RC filter solution, built around an amplifier core ([Gad92], [Nyg91]) was chosen.

3.3.1 Noise in Amplifiers

The term noise originates from the hissing sound a loudspeaker produces when it is connected to a "noisy" amplifier. It was adopted to the source of this noisy sound: The (statistical) fluctuation of a device's output signal not caused by a change on one of its inputs. In the context of electronics a *device* can be anything from a simple resistor up to a complex system, e.g. a satellite communications link.

For signal transmitting systems like amplifiers or links, it is common to assign the noise to the input node. The so-called equivalent input noise is the input signal amplitude that will cause an output signal of the same amplitude as the noise. The major advantage of this method is the convenient calculation of the signal-to-noise ratio, especially for compound systems and systems with variable gain.

Speaking in statistical terms, noise is the width (i.e. the variance) of the output signal distribution:

$$\sigma^2(v) = \overline{e_\mathrm{n}^2} = \lim_{T\to\infty} \int_{-T}^{T} (v(t) - v_0(t))^2 \, dt \;\; [V^2] \tag{3.2}$$

$v(t)$ = output signal

$v_0(t)$ = noiseless output signal

Which for $v_0(t) = 0$ becomes

$$\sigma^2(v) = \overline{v_\mathrm{n}^2} = \lim_{T\to\infty} \int_{-T}^{T} v^2(t) \, dt \;\; [V^2] \tag{3.3}$$

Introducing the (unilateral) spectral noise density $e_\mathrm{n}(f)$ $(e_\mathrm{n}(f) = 0 \; \forall f \leq 0)$ [Hin96] [Mül89] noise phenomena can be also treated in the frequency domain:

$$\sigma^2(v) = \overline{v_\mathrm{n}^2} = \int_{0}^{\infty} e_\mathrm{n}^2(f) \, df \;\; [V^2] \tag{3.4}$$

Types of Noise Sources

In pure electronic systems (i.e. not taking into account sensors and actuators) there are three types of noise sources.

Thermal Noise (sometimes also called *Johnson Noise* or *Nyquist Noise*) originates from fluctuations of the charge distribution in a conductor caused by thermal movement of the charge carriers. As such it is very similar to

the Brownian Movement of molecules in a gas. The instantaneous electric field becomes non-zero and an AC voltage drop can be measured across the conductor. The mean electric field and therefore the DC voltage drop has to be zero; otherwise it would be a *Perpetuum Mobile* of the 2nd type. The mean squared noise according to [Joh28] and [Nyq28] is given by:

$$\overline{v^2} = 4kTR\Delta f \ \left[\mathrm{V}^2\right] \tag{3.5}$$

$$\overline{i^2} = \frac{4kT}{R}\Delta f \ \left[\mathrm{A}^2\right] \tag{3.6}$$

k = Boltzmann's constant ($1.38 \cdot 10^{-23}$J/K)

T = absolute temperature [K]

Δf = system bandwidth [Hz]

R = resistance [Ω]

It is obvious that differentiating eqs. 3.5 and 3.6 wrt. Δf yields the spectral noise densities:

$$e_\mathrm{n} = \sqrt{4kTR} \ \left[\mathrm{V}/\sqrt{\mathrm{Hz}}\right] \tag{3.7}$$

$$i_\mathrm{n} = \sqrt{\frac{4kT}{R}} \ \left[\mathrm{A}/\sqrt{\mathrm{Hz}}\right] \tag{3.8}$$

The spectral density of thermal noise is independent from frequency. Noise with a frequency-independent spectral density is commonly designated as *white noise*.

Shot Noise is caused by the discrete nature of the charge carriers. The best analogue for shot noise phenomena are not shot grains hitting a surface, which is what the name suggests, but a bathroom shower:

- The noise is the "patter" of the water drops hitting the surface of the water in the shower base – the interface of a conductor.
- The noise increases (linearly) with the size of the drops – it is proportional to the elementary charge.
- The noise increases (linearly) with the flow rate of the water – it is proportional to the DC current.
- The water drops have to traverse a (gravitational) difference of potential – the charge carriers have to pass a voltage threshold.

In mathematical terms this is a Poisson process and the charge carriers pass the voltage threshold with temporal fluctuations. The mean squared shot noise current is given by:

$$\overline{\Delta i^2} = 2q_e I_0 \Delta f \ \left[\mathrm{A}^2\right] \tag{3.9}$$

I_0 = DC current

The spectral density of the shot noise is given by $i_n = \sqrt{2q_e I_0}$ (in $[\mathrm{A}/\sqrt{\mathrm{Hz}}]$), i.e. the shot noise also has a *white* spectrum. Detailed descriptions can be found in [Mül89] and [Zie86].

Flicker Noise is very often also called $1/f$-noise, due to the $1/f^\alpha$ dependent spectral noise density, with α being always very close to 1. The causes of the flicker noise are various and not completely understood yet, but flicker noise is mainly observed in active devices [Zie86].

Flicker noise in CMOS devices contributes to the total noise only in the kHz region. Therefore it will not be considered in further calculations.

Series Noise and Parallel Noise

For convenience and simplicity of noise calculations, the noisy real-world components are usually split into ideal (i.e. noiseless) components and dedicated noise sources, represented by a voltage source or current source in the equivalent schematic. For a resistor this is quite obvious: A current noise source of the spectral noise density given in eq. 3.8 in parallel to a noiseless resistor R causes the voltage drop given by eq. 3.7 across the resistor. In turn will a voltage noise source with the noise density given in 3.7 in series with R force a noise current given by eq. 3.8 into the resistor.

This concept becomes very handy when describing transmission circuits like amplifiers: Their noise performance is characterised by a series noise (voltage) source e_{ns} and a parallel (current) noise source i_{np}. While the series noise source is the only active source in case of a short circuited input, the parallel source is the only contribution under open-circuit conditions as depicted in fig. 3.4. Knowing these two noise sources the S/N ratio of a transmission circuit can be calculated for an arbitrary impedance connected to the input.

In case of a charge sensitive amplifier and a microstrip detector the input load consists of a capacitor in parallel with a resistor. The capacitance C_{p} is dominated by the strip capacitance C_{Strip}, while the resistance is given by the resistance of the detector's biasing network and the amplifier feedback resistance ($R_{\mathrm{p}} = R_{\mathrm{Bias}} \| R_{\mathrm{fb}}$). Inductances (e.g. of bond wires) can be neglected, in microstrip detectors they only contribute for frequencies well above 100MHz.

To calculate the equivalent input noise, the voltage drop across the input load has to be determined [Rad74][Far83]:

$$V_{\mathrm{ns}}(t) = R_{\mathrm{p}} \cdot I_{\mathrm{R}}(t) \tag{3.10}$$

$$\dot{V}_{\mathrm{ns}}(t) = \frac{I_C(t)}{C_{\mathrm{p}}} \tag{3.11}$$

The (noise) current through the input load therefore becomes:

$$I_{\mathrm{ns}}(t) = I_R(t) + I_C(t) = C_{\mathrm{p}} \cdot \left(\dot{V}_{\mathrm{ns}}(t) + \frac{V_{\mathrm{ns}}(t)}{R_{\mathrm{p}} \cdot C_{\mathrm{p}}} \right) \tag{3.12}$$

Assuming that a series of δ-shaped pulses describes $V(t)$ we can substitute

$$V(t) = V \cdot \delta(t) \tag{3.13}$$

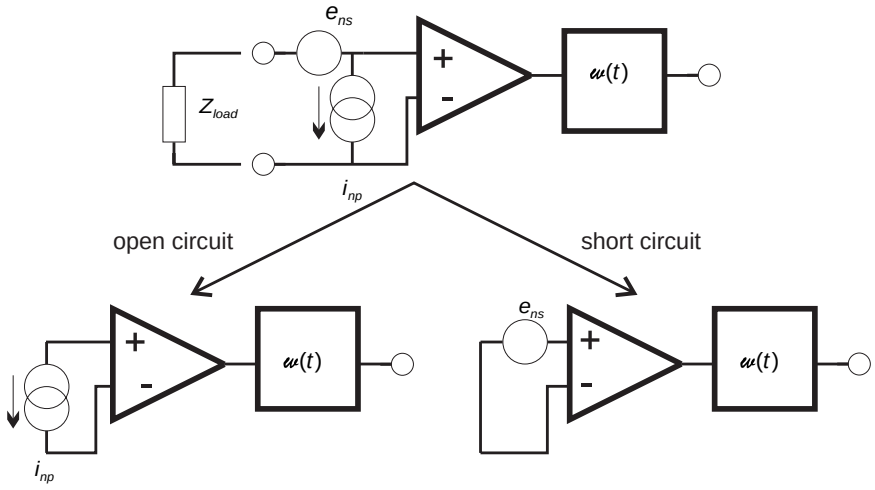


Figure 3.4: Concept of series and parallel noise: For an open input only the parallel noise contributes (e_{ns} open), while for a short circuited input only the series noise is active (i_{np} shorted). The filter's transfer function $w(t)$ limits the bandwidth of the ideal amplifier depicted.

and arrive at:

$$I(t) \quad = \quad V \cdot C_{\mathrm{p}} \cdot \left(\dot{\delta}(t) + \frac{\delta(t)}{R_{\mathrm{p}} \cdot C_{\mathrm{p}}} \right) \tag{3.14}$$

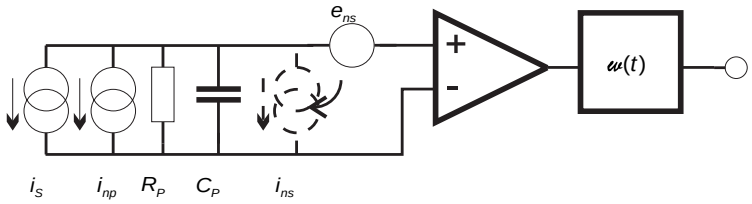


Figure 3.5: Equivalent circuit of a noisy amplifier chain. The real components have been replaced with noiseless ones and dedicated noise sources. The source of the series noise voltage can be transformed into a (parallel) current noise source, which enables the calculation of $V_{C_{\mathrm{p}}}$.

In real-world systems the bandwith Δf has to be replaced by the integral of the normalised (i.e. $\max w(f) = 1$) transfer function $w(f)$. Moving to the time domain, we end up with $w(t)$ being the pulse response of the system, giving rise to the time dependency in 3.4 even in case of only *white noise* sources. With

the δ-functions in eq. 3.13 and 3.14 the transformation into the time domain can be executed and the equivalent noise charges become [Rad74][Far83]:

$$\overline{ENC_{\mathrm{p}}^2} = \frac{1}{2}\left(\overline{i_{\mathrm{n}}^2} + \frac{4kT}{R_{\mathrm{p}}}\right) \cdot \int_{-\infty}^{\infty} w^2(t)\,dt \tag{3.15}$$

$$\overline{ENC_{s}^2} = \frac{1}{2}\overline{e_{\mathrm{n}}^2} \cdot C_{\mathrm{p}}^2 \cdot \int_{-\infty}^{\infty} \left(\dot{w}^2(t) + \frac{w^2(t)}{R_{\mathrm{p}}^2 \cdot C_{\mathrm{p}}^2}\right) dt \tag{3.16}$$

i_{n} = (parallel) current noise density of the system without input load [A/$\sqrt{\mathrm{Hz}}$]

e_{n} = (series) voltage noise density without input load [V/$\sqrt{\mathrm{Hz}}$]

It should be noted that despite their common origin the components of the series noise in eq. 3.16 are statistically independent and the mixed term $2\frac{\dot{w}(t)\cdot w(t)}{R_{\mathrm{p}}\cdot C_{\mathrm{p}}}$ vanishes.

The Spectral Noise Density of the first stages' input device governs the noise of any amplifier chain. When calculating the equivalent input noise, the contributions of subsequent stages are suppressed by the gain factors of the preceding ones and usually it is sufficient, to take the first stages' noise into account. For the first amplifier stage using a FET the spectral noise densities are given by [Zie76]:

$$\overline{e_{\mathrm{n}}^2} = \frac{2\,(1+\eta)}{3} \cdot \frac{4kT}{g_{\mathrm{m}}} \tag{3.17}$$

$$\overline{i_{\mathrm{n}}^2} = \frac{4}{15} \cdot \frac{\omega^2 C_{\mathrm{GD}}^2}{g_{\mathrm{m}}} \cdot 4kT + 2q_e I_{\mathrm{G}} \tag{3.18}$$

η = "Bulk Factor" = $\frac{g_{\mathrm{mBS}}}{g_m}$ ($\eta \approx 0.125$ for AMS CYE 0.8µm CMOS)

g_{m} = transconductance [A/V]

ω = angular frequency = $2\pi f$ ($\approx \sqrt{2}\frac{\pi}{t_{\mathrm{rise}}+t_{\mathrm{fall}}}$ for CR-RC shaping)

C_{GD} = gate-drain capacitance (*Miller capacitance*) of the FET

I_{G} = gate leakage current

Eq. 3.17 represents the noise contribution arising from thermal fluctuations of the transconductance g_{m}. The dependence of the drain current from the substrate's potential is described by the *Bulk Factor* η (cf. section 4.2). The second addend in 3.18 is the shot noise of the gate leakage current, which can be neglected for MOS transistors. The first term arises from the feedback of the channel's thermal noise to the amplifier input via the *Miller Capacitance* C_{GD} (cf. eq. 3.35 and fig. 3.6). It should be denoted that this contribution has no white spectrum and therefore should be part of the integral in eq. 3.15. Since the noise of a charge sensitive amplifier is dominated by the parallel contribution, in case of $CR-(RC)^n$ shaping ω is related to the centre frequency of the filter $\left(\omega \approx \frac{1}{\tau_1} + \frac{1}{\tau_2} \text{ for } n = 1\right)$ and pulled out of the integration.

The Transfer Function is mainly determined by the $CR-(RC)^n$ shaper, which forms a bandpass filter of the order $n+1$. Obviously that filter has $n+1$ independent parameters $\tau_i = R_i C_i$ $(i = 1 \ldots n+1)$. For a 2^{nd} order band pass filter the two time constants determine the centre frequency $f_{\text{m}} = \frac{1}{4\pi}\left(\frac{1}{\tau_1} + \frac{1}{\tau_2}\right)$ and the quality factor $Q = \sqrt{\frac{1}{2} \cdot \frac{\tau_1 \tau_2}{\tau_1^2 + \tau_2^2}}$. The Q factor also determines the bandwidth of a 2^{nd} order bandpass filter. In the s domain of the Laplace Transformation the transfer function is represented by the following:

$$w_{\text{Sha}}(s) = -\frac{s}{(s+\beta)^2 + \alpha^2} \tag{3.19}$$

$$w_{\text{FE}}(s) = \frac{s}{(s+\beta)^2 + \alpha^2} \cdot \frac{1}{s} \tag{3.20}$$

$w_{\text{Sha}}(s)$ = Pulse response of a CR-RC shaper, i.e. the transfer function of the shaper.

$w_{\text{FE}}(s)$ = Step response of a CR-RC shaper, i.e. the transfer function of a CR-RC shaper connected to an ideal charge amplifier.

$\beta = \frac{1}{2}\left(\frac{1}{\tau_1} + \frac{1}{\tau_2}\right)$ "centre frequency" parameter ($f_{\text{m}} = \frac{\beta}{2\pi}$) of the filter. [$\text{s}^{-1}$]

$\alpha = \frac{1}{2}\sqrt{\left(\frac{1}{\tau_1} - \frac{1}{\tau_2}\right)^2}$ "Bandwidth" parameter ($\Delta f = \frac{\alpha}{\pi}$), related to the filter's quality factor $Q = \frac{1}{2}\sqrt{\frac{\beta^2+\alpha^2}{\beta^2-\alpha^2}}$. [$\text{s}^{-1}$]

Transforming eq. 3.20 back to the time domain yields:

$$w_{\text{FE}}(t) = \frac{1}{\alpha} \cdot \sin(\alpha t) \cdot e^{-\beta t} \tag{3.21}$$

The peak time t_{peak} $(0 \ldots 100\%)$ and the pulse length t_{pulse} ($t = 0$ to the first zero crossing) of the shape defined by eq. 3.21 can be calculated analytically:

$$t_{\text{peak}} = \frac{1}{\alpha} \arctan\left(\frac{\alpha}{\beta}\right) \tag{3.22}$$

$$t_{\text{pulse}} = t_{\text{peak}} + t_{\text{fall}} = \frac{\pi}{\alpha} \tag{3.23}$$

For $\alpha \gg \beta$ eq. 3.21 shows the behaviour of a damped oscillation. Going to the *aperiodic limit* ($Q = 1/2$), which is equivalent to $\alpha = 0$ or $\tau_1 = \tau_2$ results in

$$w(t) = \lim_{\alpha \to 0} \frac{1}{\alpha} \cdot \sin(\alpha t) \cdot e^{-\beta t} = t \cdot e^{-\beta t}, \tag{3.24}$$

the so-called *Semi-Gaussian shaping*. Now the peak time is defined by $t_{\text{peak}} = \frac{1}{\beta}$, while t_{pulse} becomes ∞ due to the exponential decay of eq. 3.24.

Taking the transfer function of a realistic preamplifier given by

$$w_{\text{Pre}}(s) = -\frac{\gamma - \delta}{(s+\gamma) \cdot (s+\delta)} \tag{3.25}$$

$\gamma = \frac{1}{\tau_{\text{fall(Pre)}}}$ Parameter depending on the RC decay time constant of the preamplifier [s^{-1}]

$\delta = \frac{1}{\tau_{\text{rise(Pre)}}} + \frac{1}{\tau_{\text{fall(Pre)}}}$ Parameter depending on the rise time of the preamp [s^{-1}]

into account, one has to to convolute eq. 3.19 with eq. 3.25. Transforming eq. 3.25 back into the time domain, we obtain

$$w_{\mathrm{Pre}}(t) \quad \propto \quad e^{-\gamma t} - e^{-\delta t} \tag{3.26}$$

and can solve the convolution integral given by:

$$w_{\mathrm{PreSha}}(t) \propto \int_0^t \left(e^{-\gamma(t-t')} - e^{-\delta(t-t')}\right) \cdot \left(\cos(\alpha t') - \frac{\beta}{\alpha}\sin(\alpha t')\right) \cdot e^{-\beta t'}\, dt' \tag{3.27}$$

$$\begin{aligned} w_{\mathrm{PreSha}}(t) \propto & \left[\left(\frac{\left(\alpha^2+\beta^2\right)(\gamma-\beta-\delta)+\beta\gamma\delta}{\alpha}\right)\sin(\alpha t) - \left(\alpha^2+\beta^2+\gamma\delta\right)\cos(\alpha t)\right] e^{-\beta t} \\ & +\gamma\frac{\alpha^2+(\beta-\delta)^2}{\delta-\gamma}e^{-\gamma t} - \delta\frac{\alpha^2+(\beta-\gamma)^2}{\delta-\gamma}e^{-\delta t} \end{aligned} \tag{3.28}$$

Unfortunately there is no analytic solution for the maximum of eq. 3.28, which prevents the normalisation of the equation required for noise calculations. Further problems arise when fitting eq. 3.28 to measured pulse shapes:

- The first line contains a periodic function, which causes ambiguities.
- The first line also bears a phase depending on the fit parameters.
- The two exponential terms in the 2$^{\mathrm{nd}}$ line are strongly correlated.

These complications prevented the fit of eq. 3.28 to measured data[3]. The values can be obtained from numeric simulations however [Fal98].

Since there are only small differences between the pulse shapes defined by eq. 3.28 and eq. 3.21, the latter is used for further calculations. Normalisation of eq. 3.21 to $\max w(t) = 1$ yields:

$$w(t) \quad = \quad \sqrt{1+\frac{\beta^2}{\alpha^2}} \cdot e^{\frac{\beta}{\alpha}\arctan\left(\frac{\alpha}{\beta}\right)} \cdot \sin(\alpha t) \cdot e^{-\beta t} \tag{3.29}$$

$$\dot{w}(t) \quad = \quad \sqrt{1+\frac{\beta^2}{\alpha^2}} \cdot e^{\frac{\beta}{\alpha}\arctan\left(\frac{\alpha}{\beta}\right)} \cdot (\alpha\cos(\alpha t) - \beta\sin(\alpha t)) \cdot e^{-\beta t} \tag{3.30}$$

These equations together can be substituted into eq. 3.15 and 3.16:

$$\overline{ENC_{\mathrm{p}}^2} \quad = \quad \frac{1}{8\beta}\left(\overline{i_{\mathrm{n}}^2} + \frac{4kT}{R_{\mathrm{p}}}\right) \cdot e^{\frac{2\beta}{\alpha}\arctan\left(\frac{\alpha}{\beta}\right)} \tag{3.31}$$

$$\overline{ENC_s^2} \quad = \quad \frac{1}{8\beta} \cdot \overline{e_{\mathrm{n}}^2} \cdot C_{\mathrm{p}}^2 \cdot \left(\alpha^2+\beta^2+\frac{1}{R_{\mathrm{p}}^2 \cdot C_{\mathrm{p}}^2}\right) \cdot e^{\frac{2\beta}{\alpha}\arctan\left(\frac{\alpha}{\beta}\right)} \tag{3.32}$$

[3]While the problem of the periodic function can be overcome by fixing the origin of the fit, the phase in the first line of eq. 3.28 as well as the strong correlation of the two exponential terms independently caused PAW's *Minuit* routine [PAW93] to fail due to a non positive definite error matrix.

By substituting eqs. 3.17 and 3.18 into eqs. 3.31 and 3.32 we can calculate the equivalent noise charge of a charge sensitive amplifier frontend with $CR-RC$ shaping for any impedance connected to the input. To quote the usual figures describing the noise of a charge sensitive amplifier – shaper frontend, one has to evaluate eqs. 3.31 and 3.32 for $C_\mathrm{p}=0$ to obtain the *noise offset* (or *noise pedestal*) and calculate $\frac{d\overline{ENC}}{dC_\mathrm{p}}$ from eq. 3.32 to obtain the *noise slope* by neglecting terms of higher order in C_p:

$$\frac{d\overline{ENC}}{dC_\mathrm{p}} = \frac{1}{2\sqrt{2}}\sqrt{\overline{e_\mathrm{n}^2}}\cdot\sqrt{\frac{\alpha^2}{\beta}+\beta}\cdot e^{\frac{\beta}{\alpha}\arctan\left(\frac{\alpha}{\beta}\right)} \tag{3.33}$$

3.3.2 The Charge Sensitive Preamplifier

The conversion from a charge to a voltage signal can be easily accomplished by transferring the charge onto a capacitor and evaluating the voltage drop. Therefore a charge sensitive amplifier could be made of a voltage amplifier with a capacitor in parallel to the amplifier input. The *sensitivity* of this system will be:

$$A_Q = \frac{1}{C}\cdot A_\mathrm{V} \quad [\mathrm{V/C}] \tag{3.34}$$

A_V = voltage gain of the amplifier

Obviously parasitic capacitances (e.g. of the wiring) and the capacitance of the charge source (i.e. C_Strip in case of a microstrip detector) contribute to C in eq. 3.34. To suppress the gain's dependency on the parasitic capacitances, $C_\mathrm{int} \gg C_\mathrm{parasitic}+C_\mathrm{Strip}$ is required, while for a sensitive amplifier a high gain A_Q and in turn very small values of C_int are favourable. The (usually detrimental) *Miller Effect* provides a solution of this dilemma: As shown in fig. 3.6 a virtual impedance to ground given by the impedance between input and output node shows up on the input node of an inverting amplifier:

$$Z_\mathrm{in} = \frac{Z_\mathrm{fb}}{-A_0} \tag{3.35}$$

Z_in = input impedance (to ground) of the amplifier.

Z_fb = impedance between input node and output of the amp.

A_0 = *open loop* voltage *gain*[4] of the amplifier.

A charge sensitive amplifier made of an amplifier core with gain A_0 and a feedback capacitor C_fb will have a dynamic input capacitance of

$$C_\mathrm{p} = -\Re(A_0)C_\mathrm{fb} \tag{3.36}$$

[4]The *open loop gain* is the voltage gain of the amplifier core cell without external feedback components. The gain is defined by $U_\mathrm{out} = A_0 U_\mathrm{in}$ and usually a complex number due to the phase shift between U_in and U_out. Consequently A_0 is negative for an inverting amplifier.

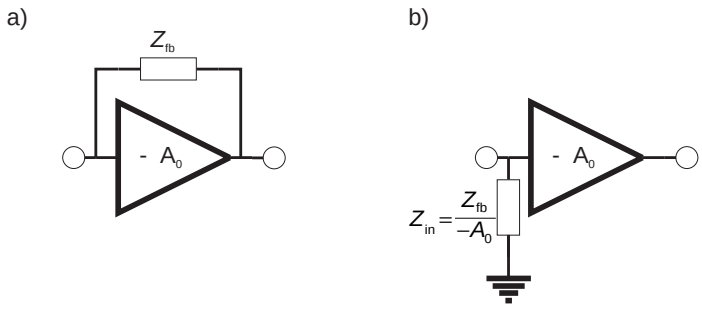


Figure 3.6: *Miller Effect*: a) Amplifier with feedback impedance Z_{fb} b) Transformation of Z_{fb} to the amplifier input due to the *Miller Effect*

and a sensitivity of

$$A_Q = \frac{-1}{C_{\mathrm{fb}}}, \tag{3.37}$$

if all input charge is collected on C_{fb}. For practical application of a charge sensitive amplifier a (large) resistor R_{fb} in parallel with C_{fb} discharges the capacitor and ensures that the output is not driven against the power supply rails. The input charge rate $\frac{dQ}{dt} \leq \frac{\max U_{\mathrm{out}}}{R_{\mathrm{fb}}}$ is limited by this resistor, which together with C_{fb} also determines the fall time (i.e. $\gamma = \frac{1}{\tau_{\mathrm{fall}}} = \frac{1}{R_{\mathrm{fb}} C_{\mathrm{fb}}}$ in eq. 3.26) of the charge sensitive amplifier. Since C_{fb} has to be charged up via the amplifier core's internal resistance Z_{out} the rise time constant (in eq. 3.26) is $\tau_{\mathrm{rise}} \approx \Re(Z_{\mathrm{out}}) C_{\mathrm{fb}}$.

Substituting typical values (e.g $A_{\mathrm{Q}} = -3\frac{\mathrm{V}}{\mathrm{pC}}$ and $C_{\mathrm{Strip}} = 35\mathrm{pF}$) in eqs. 3.36 and 3.37 and requiring 99% of the input charge to be collected on C_{fb} we end up with $C_{\mathrm{fb}} \approx 330\mathrm{fF}$ and $|A_0| \geq 100\frac{C_{\mathrm{Strip}}}{C_{\mathrm{fb}}} \approx 10^4$ for the open loop gain of the amplifier core.

The *Folded Cascode* Amplifier Core

Besides the requirement for an open loop gain of $|A_0| \approx 10^4$ for microstrip detector readout the amplifier core of a charge sensitive amplifier has to be stable at unity gain: In case of an open input (and when neglecting parasitics) the feedback impedance $Z_{\mathrm{fb}} = R_{\mathrm{fb}} \| C_{\mathrm{fb}}$ becomes ineffective and the amplifier operates at a (voltage) gain of $-A_{\mathrm{V}} \leq 1$. A simplification of the *Nyquist Criterion* [Nyq32] leads to

$$-1 \leq \Re(-k \cdot A_0(f)) \quad (\forall f \geq 0)\,, \tag{3.38}$$

k = feedback factor (i.e. the fraction of the output signal fed back to the input) ($k \in \mathbb{C}$).

which says that the negative feedback must not turn into a positive one for $|kA_0| \geq 0$ (i.e. for a *loop gain* $|A_{\mathrm{L}}| \geq 1$).

A simple amplifier stage (e.g. the common source circuit depicted in fig. 3.7a) consists of an active device (e.g. FET) Q_1 and a load resistor R_{a}. The gain is given by

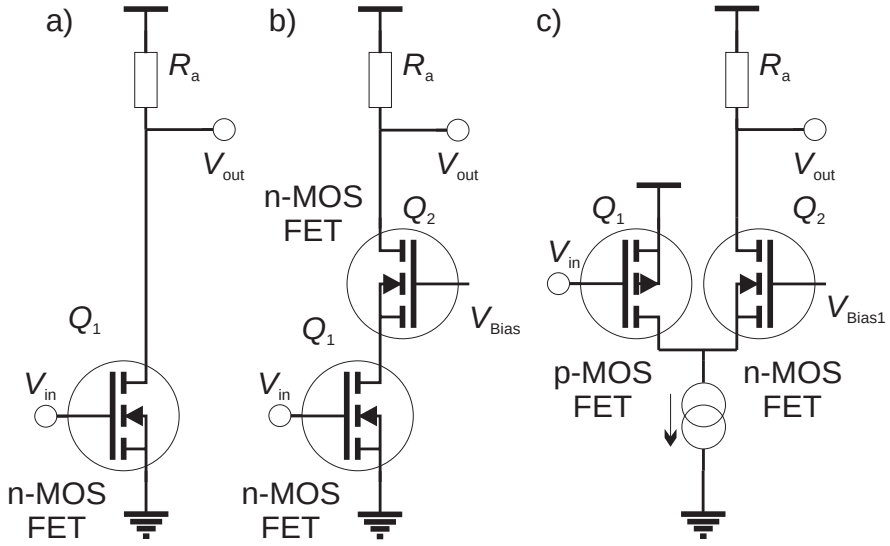


Figure 3.7: Amplifier stages: a) common source b) (linear) cascode c) *folded cascode*

$$A_V = -g_m \cdot R_a. \tag{3.39}$$

g_m = transconductance of the active device (FET, bipolar transistor etc.) [A/V].

R_a = load resistance of the active device [Ω].

In the frequency domain the common source circuit forms a 1st order low pass filter, whose corner frequency is $f_3 = \frac{1}{2\pi C_{GD} R_a}$, where C_{GD} is the *Miller Capacity* (between drain and gate of the FET Q_1 in fig. 3.7a)[5]. Thus a single amplifier stage causes an additional phase shift of up to 90° for frequencies $f \gg f_3$.

Due to the phase shift the option of a two (or more) stage amplifier core (e.g. $A_0 = {A'_0}^2 \approx 10^4$ or $A'_0 \approx 100$, which can be easily realised) is not viable due to possible phase shifts $\geq 90°$, which would lead to the violation of the stability criterion given in eq. 3.38. Furthermore a two stage design would imply a lower transconductance of the input stage (e.g. $g'_m = \sqrt{g_m}$), which has a detrimental effect on the noise performance. Therefore a single stage amplifier core has to be chosen.

Spending almost one third of the allowed power dissipation in the charge sensitive amplifier, a drain current of $I_D \approx 200\mu A$ at a power supply voltage of $V_{cc} = 4V$ can be chosen[6]. Attempting to build a common source circuit as depicted in fig. 3.7a with these figures we come up with the following dimensions: $R_a = 10k\Omega$ from letting $U = \frac{V_{cc}}{2}$ drop across the resistor to ensure an optimum dynamic range. From $|A_0| \approx 10^4$ we conclude $g_m = 1000mA/V$ using eq. 3.39.

[5]Since the low pass characteristic is a property of the amplifiers' *output*, the *Miller Capacitance* C_{GD} is *not* multiplied with A_0 here.

[6]V_{cc} = 4V was selected to provide some safety margin against the 5V limit for the power supply voltage given in the process parameters of AMS' CYE CMOS process chosen [AMS97/2].

Applying eq. 4.4 and AMS' process parameters [AMS97/2] we end up with $\frac{W}{L} = \frac{56\text{m}}{0.8\mu\text{m}}$ [7] and $C_{\text{GD}} \approx 50\text{nF}$ for a p-channel FET. Even ignoring the gate area of 44.8mm^2 which prevents the realisation of the device, the gate–drain capacitance of $C_{\text{GD}} \approx 50\text{nF}$ dominating C_{fb} causes the sensitivity of the charge sensitive amplifier to drop to $|A_{\text{Q}}| = 2 \cdot 10^{-5} \frac{\text{V}}{\text{pC}}$, which is too low by five orders of magnitude.

The effect of C_{GD} can be eliminated by using a second transistor (Q_2) in series with Q_1 as depicted in fig. 3.7b. Q_2 in the linear (or regular) *cascode circuit* works as a *source follower*[8] fixing V_{DS} of Q_1 to V_{Bias}. Thus C_{GD} is taken out of the feedback path by eliminating the *Miller Effect*. Building a linear cascode amplifier to the above specifications results in the following parameters: $R_{\text{a}} = 6.6\text{k}\Omega$, since we restrict the voltage drop to $U = \frac{V_{\text{cc}}}{3}$. Therefore the transconductance has to be $g_{\text{m}} = 1500\text{mA/V}$ and in turn $\frac{W}{L} = \frac{124\text{m}}{0.8\mu\text{m}}$ for a p-MOS transistor. Q_1's gate area of 99.2mm^2 and $C_{\text{GD}} = C_{\text{p}} \approx 112\text{nF}$ (which according to eq. 3.32 results in an unacceptable noise performance) prevent the realisation of a linear cascode amplifier core.

Splitting the cascode circuit into an active branch and a load branch by employing a current source, which keeps the sum of the currents in the two branches constant, results in the *folded cascode circuit* [Beu90] [Nyg91] depicted in fig. 3.7c. The lower limit for g_{m} is now put up by the noise, and R_{a} is selected to match the required gain. Postulating a rise time of $t_{\text{rise}} = 70\text{ns}$ and a *noise slope* of $30e^-/\text{pF}$ and assuming $R_{\text{p}} = \infty$ and Semi-Gaussian shaping ($\alpha = 0$) the transconductance has to be $g_{\text{m}} \approx 7.2\frac{\text{mA}}{\text{V}}$ (applying eq. 3.32). From that we conclude $\frac{W}{L} \approx \frac{3034\mu\text{m}}{0.8\mu\text{m}}$ (i.e a gate area of $\approx 2.43 \cdot 10^{-3}\text{mm}^2$), which was chosen for the HELIX128-2 chip, $R_{\text{a}} = 1.4\text{M}\Omega$ and $C_{\text{GD}} \leq 3.6\text{pF}$.

A further improvement of the *folded cascode* circuit can be achieved by reducing the source voltage of Q_1 in fig. 3.7c to $V_{\text{CC}}/2$. This reduces the power consumption nearly by a factor of 2, since almost the complete bias current runs through Q_1. This improvement also imposes a limitation of the DC input voltage to $V_{\text{in}} < V_{\text{CC}}/2$.

To build a charge sensitive amplifier around this *folded cascode* core, a RC feedback network has to be added. For HELIX128-2 a feedback capacitor of $C_{\text{fb}} = 342\text{fF}$ was selected, while an n-MOS transistor was chosen to implement an adjustable resistor, in turn permitting to tune the feedback's RC time constant. Furthermore a voltage shifter in the DC feedback path is required to bring the input voltage V_{in} below Q_1's source voltage.

The complete schematic of the HELIX128-2 charge sensitive amplifier is shown in fig 3.8. For implementation in a CMOS technology [Gei90] [Cha91] all resistors have been replaced with FETs implementing either active loads[9], current sources or operating in the linear part of their characteristics ($0 < V_{\text{DS}} < V_{\text{GS}} - V_{\text{th}}$ in eq. 4.4). The bias nodes in fig 3.8 are connected to a

[7] The geometrical width W and length L of the gate are the only design variables characterising a FET in a given CMOS technology. Further explanation is given in sect. 4.2

[8] The term *source follower* arises from $V_{\text{GS}} \approx V_{\text{th}}$, i.e the source follows the gate voltage in that distance. The internal resistance of that circuit is $Z_{\text{out}} \approx \frac{1}{g_{\text{m}}}$, i.e. very low.

[9] A FET with drain and gate connected together. Sometimes also referred to as a *diode connected* FET

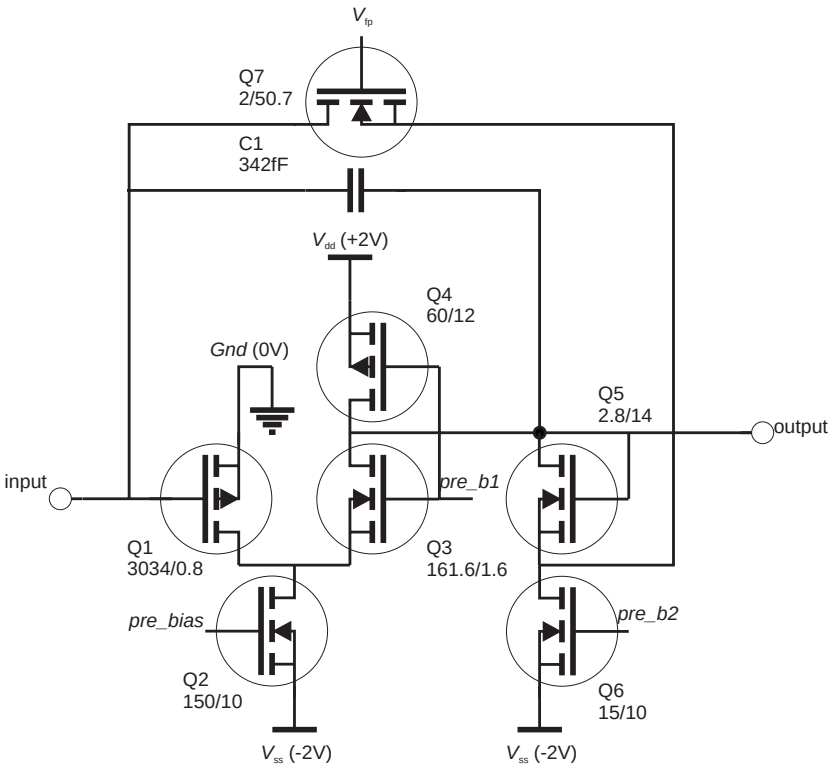


Figure 3.8: Schematic of the HELIX128-2's charge sensitive amplifier. The numbers quoted with the transistor designators are their W/L in [µm].

current mirror network, which resembles the load branch of the *folded cascode* amplifier circuit. The rise and fall time constants in eqs. 3.25 and 3.26 are given by $\tau_{\text{rise}} = \frac{C_{\text{in}}C_{\text{out}}}{-g_{\text{m}}C_{\text{fb}}} = \frac{C_{\text{in}}}{\text{GBW}C_{\text{fb}}}$ and $\tau_{\text{fall}} = C_{\text{fb}}R_{\text{fb}} \approx \frac{C_{\text{l}}}{g_{\text{m}}(\text{Q}_7)}$ (with $C_{\text{in}} = C_{\text{p}} + C_{\text{GD}}(\text{Q}_1) + C_{\text{GS}}(\text{Q}_1) + C_{\text{fb}}$, $C_{\text{out}} = C_{\text{fb}} + C_{\text{load}}$, $g_{\text{m}} = g_{\text{m}}(\text{Q}_1)$ in fig. 3.8 and GBW= $\frac{g_{\text{m}}}{C_{\text{out}}}$ the gain-bandwidth product). The $\approx$ 1V dynamic range together with the $\approx 350\frac{\text{nC}}{\text{s}}$ input charge rate capability of of the amplifier are sufficient to prevent saturation even at occupancies $\geq 10\%$. A detailed calculation of the circuit's parameters and transistor dimensions can be found in [Fal98].

Figure 3.9 shows the response of the HELIX128-2 charge sensitive amplifier to a charge of $24 \cdot 10^3 e^-$ injected to a parallel capacitor of $C_{\text{p}} = 16.3\text{pF}$ (i.e. the conditions found in the HERA-B silicon vertex detector) from a *Spectre*[10] simulation.

3.3.3 The Pulse Shaper Circuit

The signal of the charge sensitive amplifier has to be *shaped*, not only for noise reasons as shown in tab.3.1, but also to separate signals at repetition rates greater than the fall time constant of the preamp. This can be easily accom-

[10]Circuit simulator, part of the *Cadence DFW II™* package used for the development of HELIX128

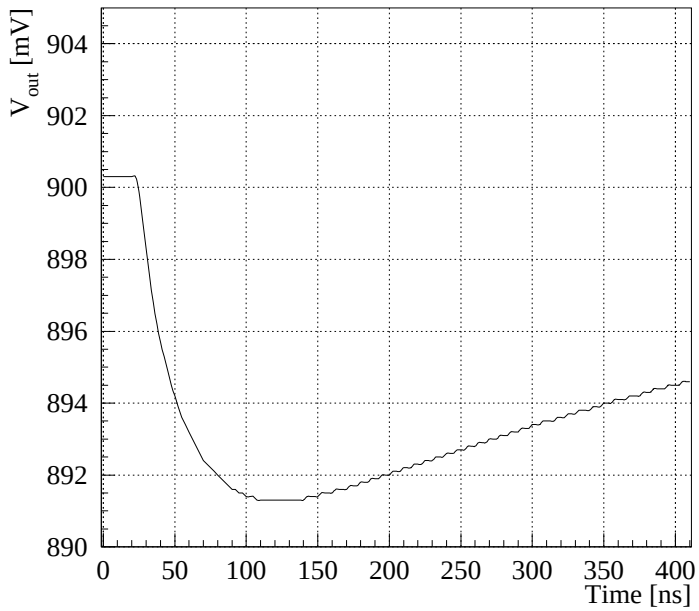


Figure 3.9: *Spectre* Simulation of the HELIX128-2 charge sensitive amplifier's response to a charge of $24 \cdot 10^3 e^-$. The parallel capacitance at the amplifier input is $C_\mathrm{p} = 16.3\mathrm{pF}$ and the bias current $I_\mathrm{pre} = 350\mu\mathrm{A}$.

plished by employing a 2^nd order band pass filter as pointed out in sect. 3.3.1. The simplest implementation of a $CR - RC$ shaper is depicted in fig. 3.10a. Besides the coupling of high and low pass filter, this passive implementation has the big disadvantage of damping the input signal by at least a factor of two. Instead of damping the input signal, a gain of about 10 at the centre frequency of the shaper is desired, since, due to the shorter signal shape, pile up and the resulting limitation of the dynamic range is no longer an issue. One possible solution is the separation of the high pass and low pass filters by a gain stage as depicted in fig. 3.10b, but the relatively large passive components required ($\tau = 50\mathrm{ns} = 1\mathrm{pF} \cdot 50\mathrm{k}\Omega$) make this implementation less feasible in a CMOS process.

The circuit depicted in fig. 3.10a can also be transformed into 3.10c. The transfer function of this circuit is given by:

$$w_{CR-RC}(s) = \frac{1}{1 + \frac{(R_1+R_2)C_2}{R_1C_1} + \frac{1}{sR_1C_1} + sR_2C_2} \tag{3.40}$$

R_i, C_i Taken from fig. 3.10c.

Obviously the two filters decouple for $R_2 \gg R_1$ and the second addend in the denominator of eq. 3.40 becomes $\frac{R_2C_2}{R_1C_1}$, i.e. the transfer function turns into that of fig. 3.10b. The undershoot wrt. the peak of the transfer function given by

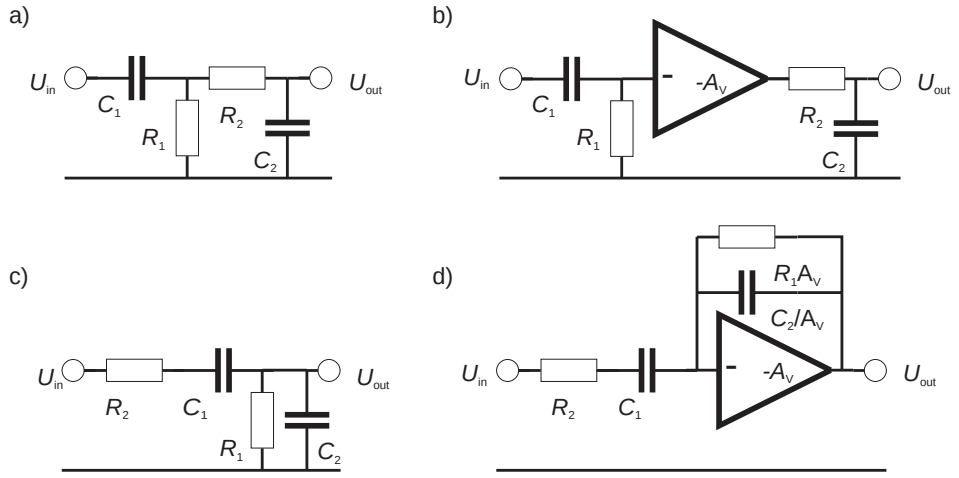


Figure 3.10: Equivalent schematic of a 2$^{\text{nd}}$ order band pass filter: a) Series of high and low pass filter. b) Decoupling of the filters in a) by an amplifier. c) Equivalent circuit of a) with $R_1 \| C_2$. d) Active implementation of c).

eq. 3.21 (which also represents 3.40 in the time domain) is given by $e^{-\frac{\beta}{\alpha}\pi}$. Since $\frac{\beta}{\alpha} \sim \frac{R_1}{R_2} + R_2 + \text{const.}$ the undershoot ratio will become independent from R_1 for $R_2 \gg R_1$. Fig. 3.10d shows an active implementation of fig. 3.10c. Besides an arbitrary gain at the centre frequency of the filter, this solution can easily fulfill the $R_2 \gg R_1$ requirement: Due to the *Miller Effect* $R_1 = R_{\text{fb}}/A_0$ i.e. R_1 becomes very small.

The amplifier core should have no impact on the filter properties. Therefore the gain-bandwith-product has to be GBW $\gg f_{\text{centre}} \cdot A_{\text{V}}(f_{\text{centre}})$. In turn stability at unity gain has to be required, since then $A_{\text{V}} \cdot f_{\text{centre}} \approx f_t \ll \text{GBW}$, which is the transit frequency of a (single stage) amplifier core. For that reason a *folded cascode* amplifier is again the preferred solution. The schematic of the pulse shaper circuit, excluding R_2 is depicted in fig. 3.11, while the detailed calculation of the circuits' parameters can be found in [Fal98]. Connecting the charge sensitive amplifier (fig. 3.8) to the shaper (fig. 3.11) there is no dedicated device representing R_2 in fig. 3.10d; it is determined by the internal resistance of the preamp and therefore adjusted by changing the preamplifier bias current I_{pre}.

The result of a *Spectre* simulation of the complete frontend, including the parasitic capacitances of the circuits' layout, is depicted in fig. 3.12. It only poorly agrees to the measured behaviour of the chip also shown. Especially peak time and the undershoot's length and amplitude do not correspond to the measured data. This discrepancy might originate from the resistances and inductances of the layout's metal and polysilicon lines, which are not calculated during circuit extraction (cf. [AMS_HK]) and therefore are not available to the simulator. The length of the pulse (as defined in eq. 3.23) is however very well represented. Applying eqs. 3.22 and 3.23 to the simulation results yields $\alpha = 23.3 \cdot 10^7 \text{s}^{-1}$ and $\beta = 35.4 \cdot 10^7 \text{s}^{-1}$. Assuming a gain of $A_V = 390$ (cf. [Fal98])

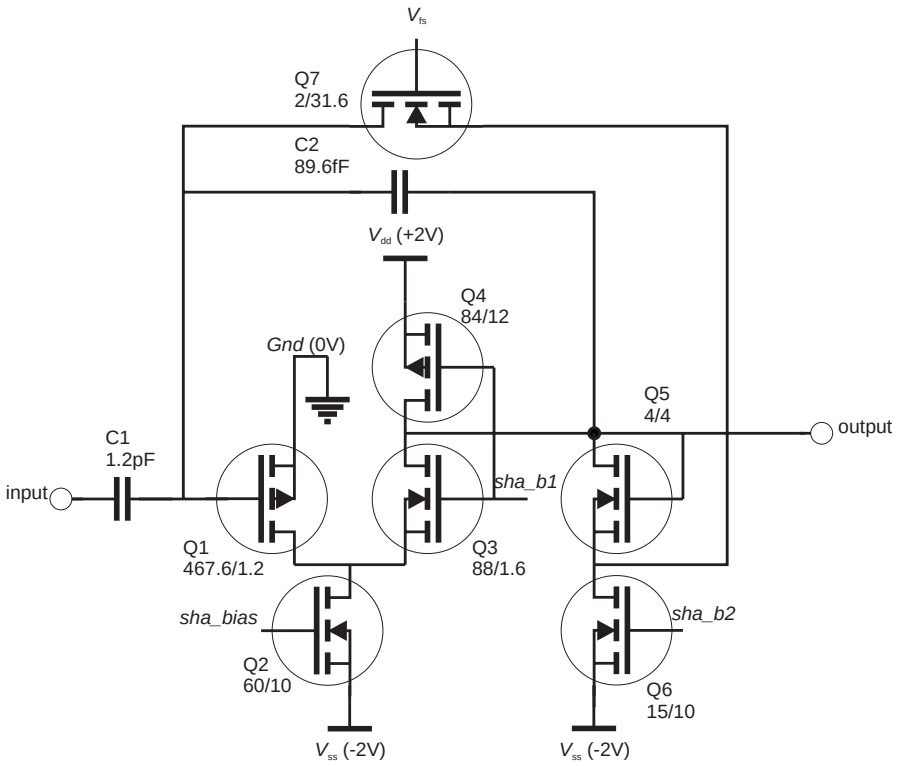


Figure 3.11: Schematic of the HELIX128-2's pulse shaper circuit.

one obtains: $R_2 = 20.0\text{k}\Omega$, $R_1 = 662\Omega$ or $R_{\text{fb}} = 25.8\text{k}\Omega$ at $C_1 = 1.2\text{pF}$ and $C_2 = 35.1\text{pF}$ or $C_{fb} = 90\text{fF}$, which agree within 30% to a manual calculation of R_1 and R_2.

3.3.4 The Frontend Buffer

The frontend has to drive the pipeline as well as a discriminator to derive a L1 trigger signal. The load imposed by these circuits consists of the input capacitance of the discriminator $C_{\text{Discr}} = 59\text{fF}$ [Gla97], the capacitance of a pipeline storage capacitor $C_{\text{Pipe}} = 850\text{fF}$ and the parasitic capacitance $C_{\text{parasitic}} = 2.05\text{pF}$ of the analogue memory's *write line*. In total $C_{load} \approx 3.07\text{pF}$ have to be driven.

The *write* switch of the pipeline is only closed for half a period of the sampling frequency `SClk`[11], i.e $\approx 50\text{ns}$. Therefore the frontend's internal resistance has to be $R_{\text{out}} \leq \frac{t_{\text{on}}}{2\pi C_{\text{load}}} = 2.7\text{k}\Omega$. This is about one order of magnitude lower than the internal resistance of the shaper and therefore a source follower has to be employed. The schematic of the circuit is depicted in fig. 3.13, while the detailed calculation of the parameters can be found in [Fal98]. The internal resistance of the buffer is given by the transconductance of Q_1: $R_{\text{out}} = \frac{1}{-g_{\text{m}}} = 632\Omega$.

[11] The nomenclature of signals is consistent with the HELIX128–2.x manual (apx. C): Names in `typewriter` designate signals that are available outside the chip, i.e connect to a pad. Logical signals in *italics* are internal to the chip and not directly accessible from outside.

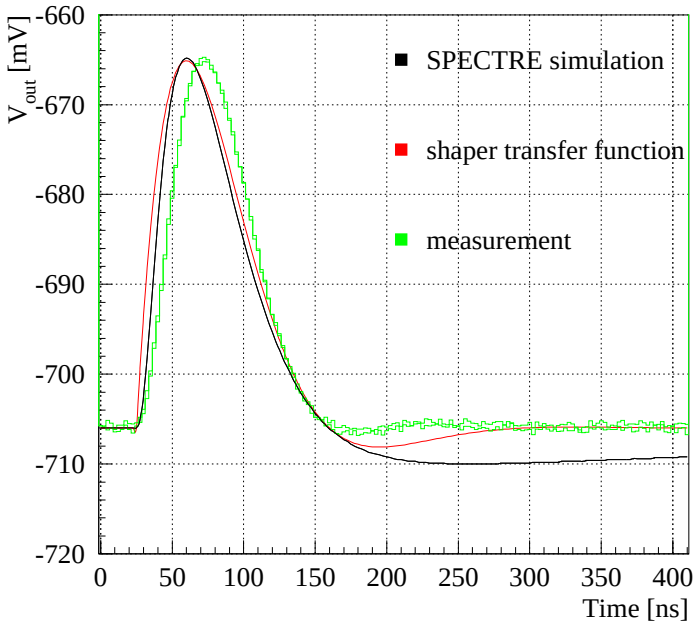


Figure 3.12: *Spectre* simulation of the HELIX128-2 frontend's response to a charge of $24 \cdot 10^3 e^-$. The parallel capacitance to the amplifier input is $C_\mathrm{p} = 16.3\mathrm{pF}$ and the bias current $I_\mathrm{pre} = 350\mu\mathrm{A}$. The second curve shows eq. 3.21 with $\alpha = 23.3 \cdot 10^7 \mathrm{s}^{-1}$ and $\beta = 35.4 \cdot 10^7 \mathrm{s}^{-1}$ taken from a *Spectre* simulation results normalised to fit offset and gain values. The third curve shows the measured pulse shape of the chip (also scaled to fit gain and offset values of the frontend).

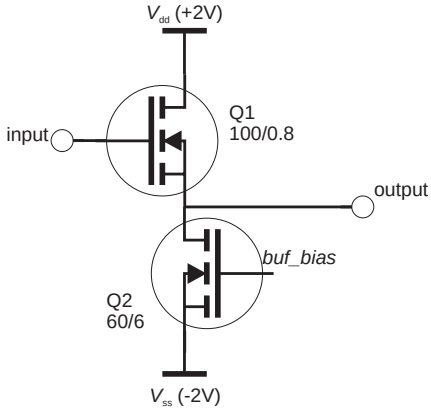


Figure 3.13: Schematic of the HELIX128-2's frontend buffer.

The rise time constant $\tau_\mathrm{rise} = \frac{C_\mathrm{load}}{-g_\mathrm{m}} = 1.9\mathrm{ns}$ applies for the rising edge of the signal only, for the falling edge a constant slope depending on the bias current applies. This is due to Q_1 working as a current sink: $-\frac{dV_{out}}{dt} = \frac{I_\mathrm{bias}}{C_\mathrm{load}} \approx 32.5 \frac{\mathrm{V}}{\mu\mathrm{s}} =$

$1.63\frac{V}{50\text{ns}}$.

The layout of HELIX128-2's frontend, developed by W. Fallot-Burghardt [Fal98] is depicted in fig. 3.14 and shows two adjacent channels.

a)

b)

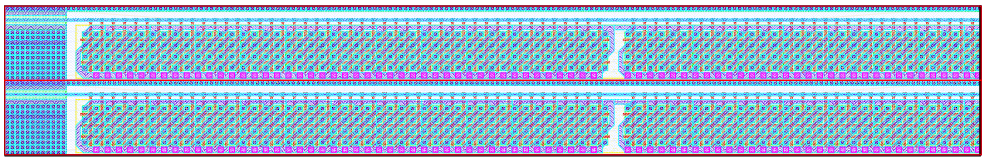
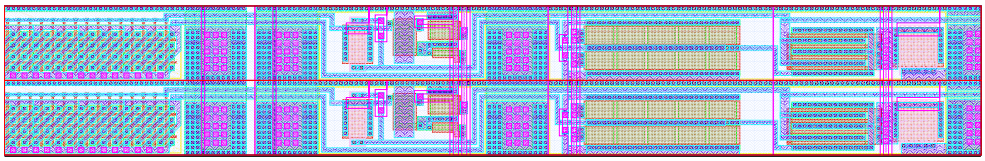
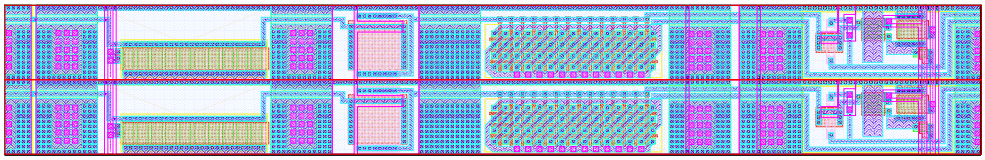


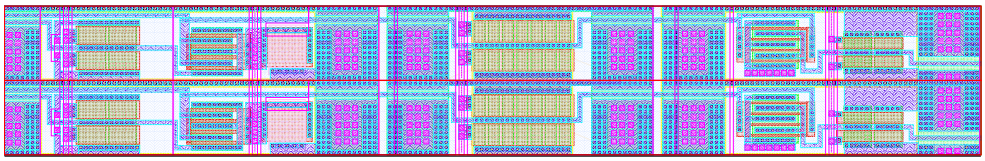
Fig. 3.8: Q_1



Q_1 C_1 Q_7 Q_5 Q_2 Q_3 Q_6



Q_4 Fig. 3.11: C_1 Q_1 C_2 Q_7 Q_5



Q_2 Q_3 Q_6 Q_4 Fig. 3.13: Q_1 Q_2

Figure 3.14: Layout of the HELIX128-2's frontend (designed by W. Fallot-Burghardt [Fal98]). a) Layout of two channels. The size of a single channel is 2140µm×41.2µm. b) Enlarged views of a) with designations of the devices. To minimise the chip area required, Q_1 of the charge sensitive amplifier and shaper are implemented as waffle transistors. The colour scheme of the layers is explained in fig. 4.1.

3.4 The Comparator Circuit

The purpose of the discriminator is to provide a fast trigger signal in case of a hit detector strip. Its implementation on the first HELIX128 readout chip was an (already existing) switching-capacitor type comparator. But this attempt failed due to insufficient sensitivity and excessive switching noise [Bec96].

To overcome this a differential amplifier comparator was implemented on the HELIX128-2.

Before the analogue signals of the frontend can be successfully discriminated, the individual DC offsets of the channels have to be removed by some means of AC coupling. The required time constant has to be $\tau \gg 100\text{ns}$ (cf. sect. 3.1), which excludes the implementation with polysilicon resistors and polysilicon-polysilicon capacitors due to their low specific resistance ($R_{\text{poly2}} = 27\frac{\Omega}{\square}$, the layer with the highest specific resistance in AMS' CYE process [AMS97/2]) and the limited range for capacitances ($\approx$ 10fF ... 10pF limited by parasitics and area) available.

The textbook solution [Lak94] to overcome this problem is to replace the resistor with a transistor switch, that shorts the capacitor to ground during insensitive periods of the input signal. Due to the expected switching noise and the charge injection (caused by C_{GD} of the transistor switch) this approach was not considered an option.

Finally the following implementation of the AC coupling was realised: The resistor was replaced by a series connection of two transistors operating in the linear region (i.e. $V_{\text{GS}} - V_{\text{th}} > V_{\text{DS}}$ in eq. 4.4). This allowed a DC resistance of $R_{\text{C}} \approx 2.4\text{M}\Omega$ and together with $C_{\text{C}} = 1.98\text{pF}$ resulted in $\tau = 4.8\mu\text{s}$. The long time constant also suppresses the detrimental effect of the nonlinear resistor.

To implement a differential amplifier type comparator, there are three different approaches concerning the sizes of the transistors:

- Wide (a few µm) transistors of minimum L (i.e. 0.8µm). Such a circuit provides maximum sensitivity and speed at low power dissipation. The offset voltage between the two inputs is large, due to the bad matching of minimum-L transistors, and thus a common threshold voltage for all 128 channels is not feasible.

- Extremely wide ($\approx$ 100µm) transistors of moderate (few µm) L. Such an implementation provides very low offset voltages on the expense of relatively high power consumption and low speed (due to large parasitics).

- Transistors of moderate W (in the order of 10µm) and L (very few µm). Disadvantage is the moderate gain. Power consumption and offset voltages are low, while the small parasitics still permit high speed switching. A comparator in this configuration was chosen for HELIX128-2.

The schematic of the final implementation (by B. Glass [Gla97]) is depicted in fig. 3.15. For the HELIX128-2 the concept of a differential amplifier type com-

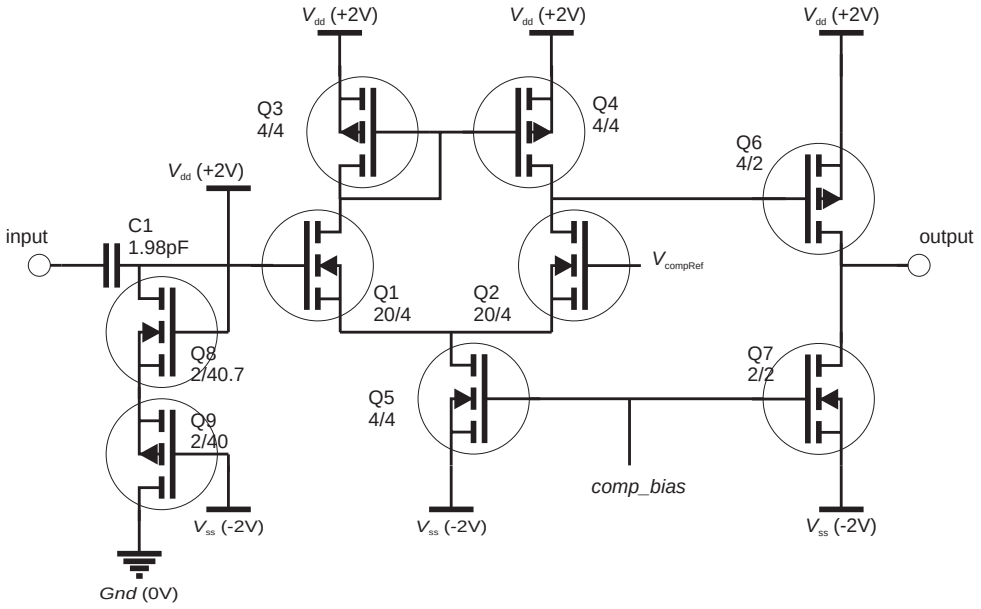


Figure 3.15: Schematic of the HELIX128-2's comparator circuit.

parator was refined by a clever selection of the circuit's operating points: The transistors Q_3 and Q_6 (for $V_{\text{in}} > V_{\text{compRef}}$) or Q_4 and Q_7 (for $V_{\text{in}} < V_{\text{compRef}}$) are driven into the linear region (cf. eq. 4.4) for $V_{\text{in}} \neq V_{\text{compRef}}$. This causes the gain of the comparator to drop from $A_{\text{d}} \approx 6840$ around the trip point (i.e. $V_{\text{in}} \approx V_{\text{compRef}}$) down to $A_{\text{d}} = 1.56$ for $|V_{\text{in}} - V_{\text{compRef}}| \gg 0$. In turn the time constants of the two amplifier stages change: While they are $\tau_1 = 21.7$ns and $\tau_2 = 466$ns around the trip point, they become $\tau_1 = 2.9$ns (i.e. $f_{max} \approx 50$MHz) and $\tau_1 = 2.0$ns for finite offset voltages. This has the drawback of a reduced output voltage swing, which, in the HELIX128's case, is compensated by the voltage gain of the subsequent digital circuits. The small voltage swing of the comparator outputs reduces possible crosstalk of the uncorrelated comparator switching to the frontend.

The measured sensitivity of the comparator [Gla97] is $\sigma(V_{\text{comp}}) \leq 0.5$mV (fig. 3.16), while the measured offset voltage was $|\sigma(V_{\text{offset}})| < 5$mV (fig. 3.17), which is much lower than $|\sigma(V_{\text{offset}})| \approx 16.6$mV expected from [AMS95/1].

The subsequent digital circuits (fig. 3.18) consist of an XOR gate per channel, permitting a polarity reversal, a quad input NOR gate combining the signals of four adjacent channels and a FlipFlop to synchronise the signals with the discriminators' sampling clock `CompClk`.

The open drain pads used to drive the trigger signals off chip turned out to be a major source of crosstalk and disturbances, mainly due to the requirement to sink 4mA per output pad. For HELIX128-2.2 the problem was reduced by employing a separate power supply for the open drain outputs, which was a big improvement wrt. to HELIX128-2.0 and HELIX128-2.1. On HELIX128-3.0 a breakthrough was achieved by a scribeline cut. Further improvement was made by reducing the (parasitic) capacitance of the trigger output's power supply

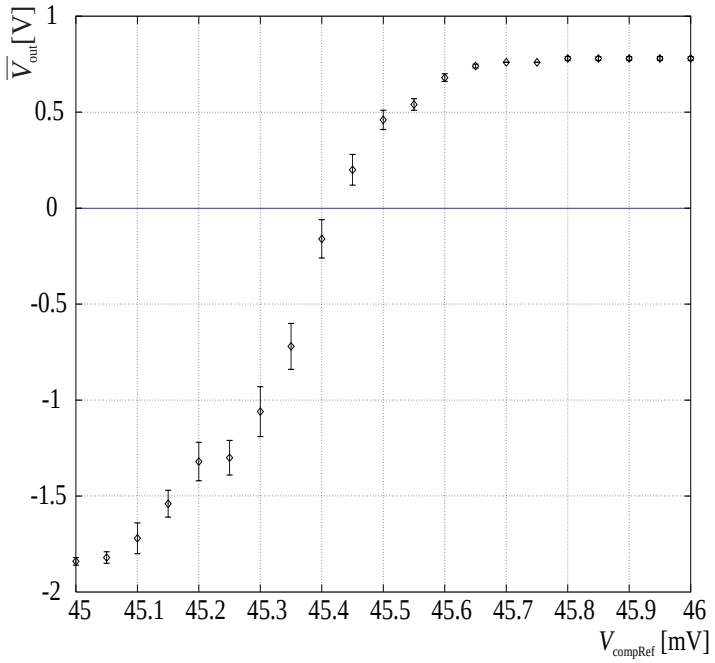


Figure 3.16: Sensitivity of HELIX128-2's comparator circuits. (Measurement results from the IDEFIX test chip) [Gla97]

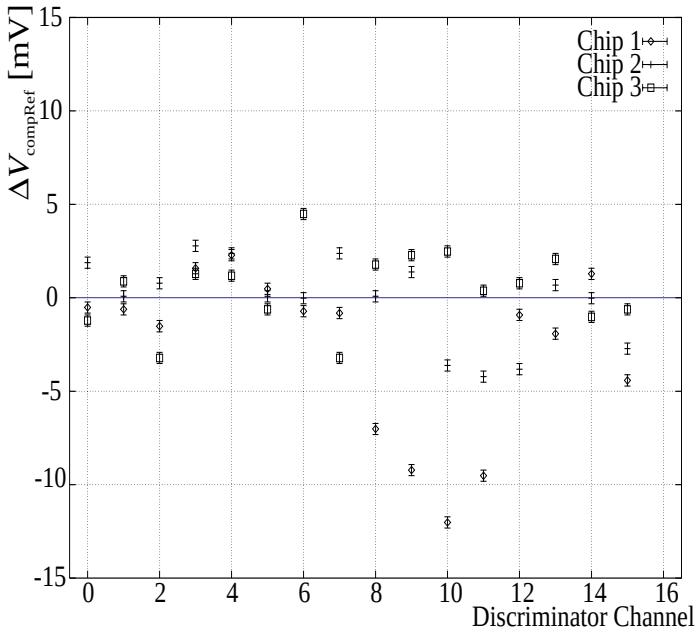


Figure 3.17: Offset voltage of HELIX128-2's comparator circuits. (Measurements from the IDEFIX test chip) [Gla97]

wrt. the substrate. A reduction of the drain resistors' supply voltage and an

improved grounding schema of the HERA-*B* inner tracking system modules also proved highly successfull [Deh].

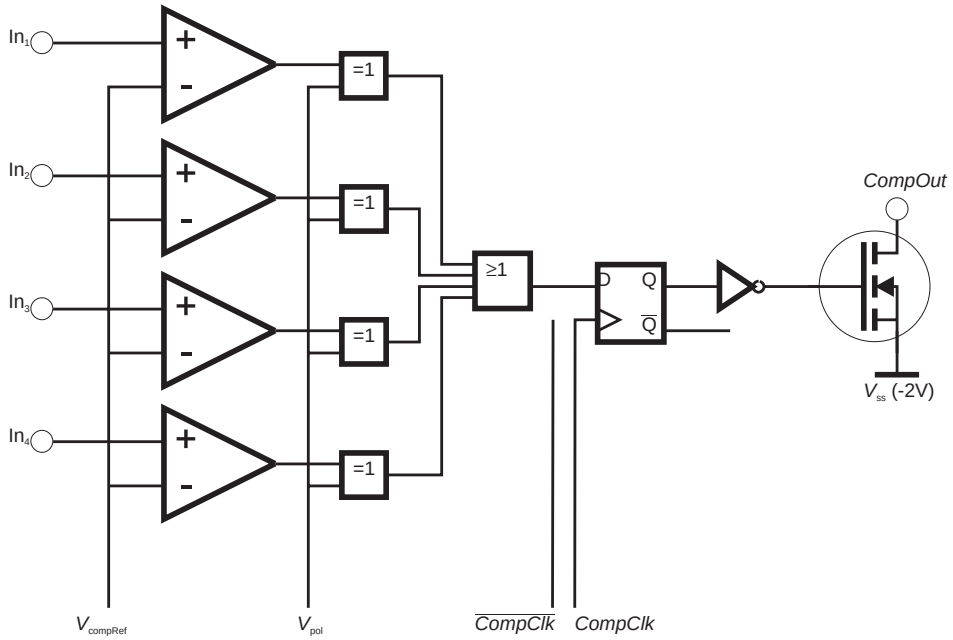


Figure 3.18: Four channels of HELIX128-2's comparator circuits, connecting to an open drain output pad.

The layout of the circuits depicted in fig. 3.18 is shown in fig. 3.19

3.5 *Pipeline* – The Analogue Memory

Since the decision of HERA-*B*'s L1 trigger has a latency of about 12µs, the sampled analogue data has to be stored for at maximum 128 cycles of the sampling clock `SClk`. In addition storage for eight already triggered events has to be provided, to compensate fluctuations of the trigger rate (cf. sect. 3.1). Further 6 samples are required to cover the overhead of the algorithm controlling the pipeline read and write operations. Therefore the analogue memory has to have a depth of $128 + 8 + 6 = 142$ samples[12]. The width is $128 + 1 = 129$ channels, with the additional "shaper only" channel providing offset information for common mode subtraction.

The implementation of a storage cell [Feu] is shown in figs. 3.20 (schematic) and 3.21 (layout). The polysilicon capacitor chosen is $C_{\mathrm{Pipe}} = 850\mathrm{fF}$ and connects to the write and read line via n-MOS transistors of $\frac{W}{L} = \frac{2\mu\mathrm{m}}{0.8\mu\mathrm{m}}$ (i.e. the minimum size in AMS' CYE process). An input signal of $24 \cdot 10^3 e^-$ (i.e. the signal of a *MIP* in a 300µm Si detector) results in $V_{\mathrm{out}} \approx 40\mathrm{mV}$ on the

[12] On HELIX128-3.0 and earlier versions, due to a bug, the implemented depth is only 141 samples. This limits the latency to 127 `SClk` cycles on HELIX128-2.2 and earlier versions (cf. appendix E).

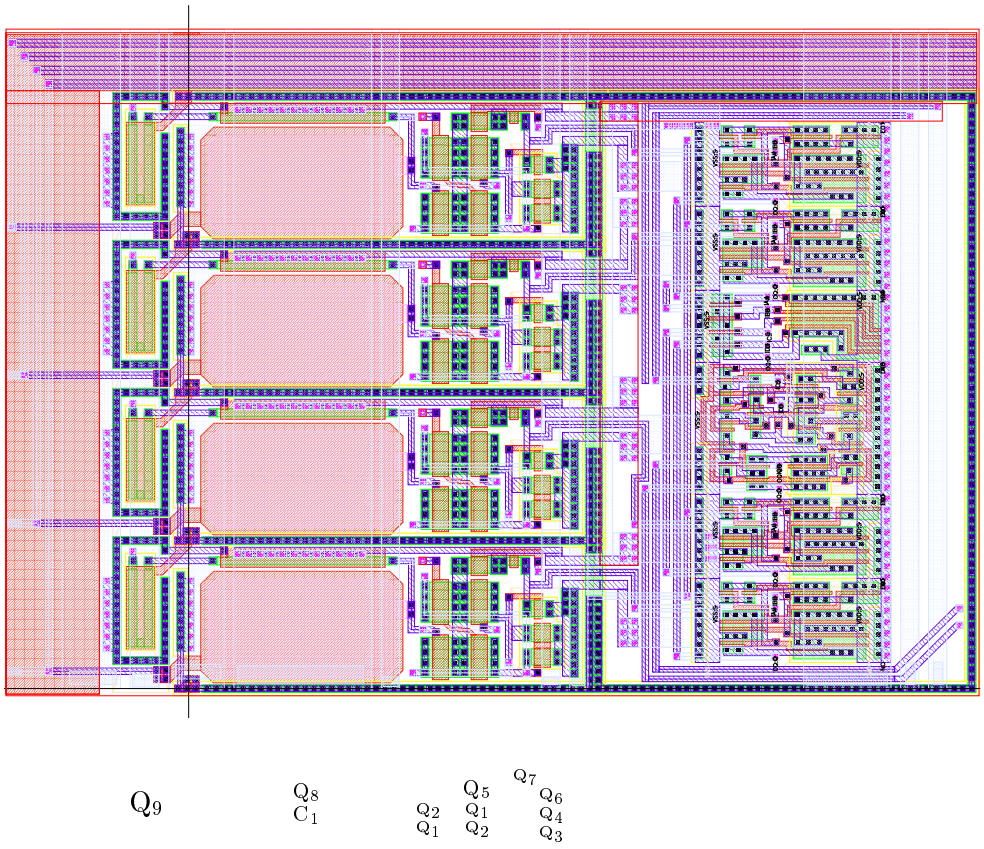


Figure 3.19: Layout of the HELIX128-2's comparator circuit. Four channels together with digital circuits combining their outputs are shown. The designations correspond to the devices in fig. 3.15. The dimensions are 240µm×164.8µm. The colour scheme of the layers is explained in fig. 4.1.

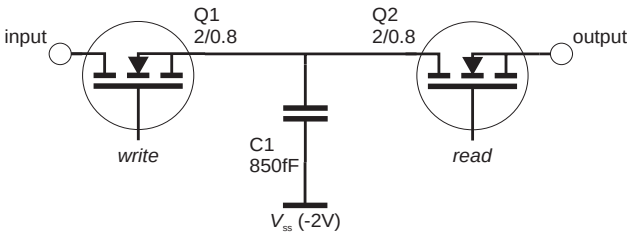


Figure 3.20: Schematic of a HELIX128-2 pipeline (analogue memory) cell.

frontend's output (cf. fig 3.12) and in turn $Q_{\mathrm{Pipe}} = 34\mathrm{fC} = 213 \cdot 10^3 e^-$ on the storage capacitor.

Assuming that the pipeline cell's input voltage does not change in the time needed to turn off the write switch, we can give an estimation for the charge injected due to the switching: The switch actually turns off at $V_{\mathrm{write}} = V_{\mathrm{in}} + V_{\mathrm{th}}$. The total charge injected therefore is:

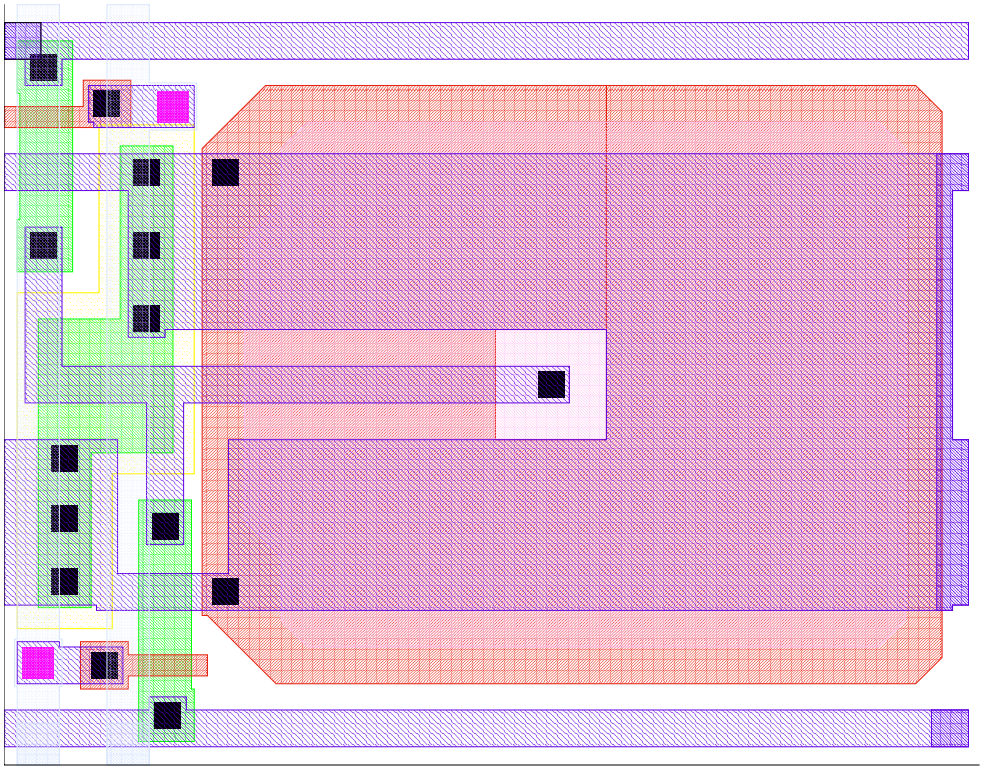


Figure 3.21: Layout of a HELIX128-2 pipeline (analogue memory) cell (designed by M.Feuerstack-Raible [Feu]). The area of the circuit is 36.5µm×29µm. The colour scheme of the layers is explained in fig. 4.1.

$$Q_{\mathrm{SW}} \quad = \quad -\left(V_{\mathrm{in}} + V_{\mathrm{th}}\right) \cdot C_{\mathrm{GD}} \tag{3.41}$$

C_{GD} = Gate-Drain capacitance of the FET switch.

From the data of fig. 3.12 we obtain $Q_{\mathrm{SW}} \approx 0.6\mathrm{fC}$, which is about 2% of *MIP*'s charge on C_{Pipe}. It should also be denoted that, since $Q_{\mathrm{SW}} \propto V_{\mathrm{in}}$, the charge injection causes a decrease of the gain by 0.35%. Unfortunately the switches' charge injection is the dominating contribution to the pipeline's inhomogeneity: The expected matching of the capacitors is $\ll 0.2\%$, while the measured inhomogeneity on HELIX128-1 (which used the same cell layout) was found to be $\approx 0.5\%$ [Sex97].

3.6 The Pipeline Readout Amplifier (*Pipeamp*)

The *pipeamp's* purpose is the retrieval of the charge information stored in a pipeline cell. The most obvious solution is a voltage amplifier, since in that case the signal would become independent from the storage capacitance C_{Cell}. The parasitic capacitance of the pipeline's *read* lines ($C_{\mathrm{par}} \approx 2.05\mathrm{pF}$) and the resulting charge sharing will unfortunately attenuate the frontend's signal at

least by a factor of 3. Furthermore the expected poor noise performance and susceptibility to crosstalk and interference prevent the realisation of this approach. To achieve the optimum noise performance and prevent a deterioration of the frontend's S/N ratio a charge sensitive amplifier had to be chosen [Fal98]. Unlike the frontend, continuous operation and in turn a pulse shaper is not required and consequently a resetable charge sensitive amplifier (to overcome the divergence of eq. 3.16 in tab. 3.1) was chosen. The schematic of the pipeline readout is shown in fig. 3.22. Upon arrival of a trigger or, in case of pending

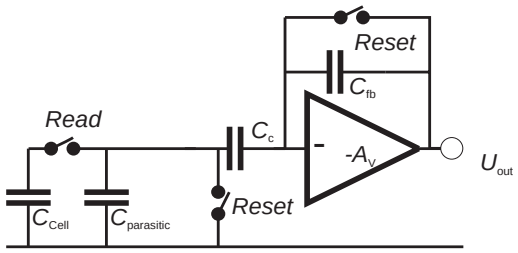


Figure 3.22: Schematic of HELIX128-2's pipeline readout.

triggers, upon the return of the readout token (cf. sect. 3.7.1), the *pipeamp's* feedback capacitor is discharged and the read line is connected to V_{d}, which has to be equal to the frontend's offset voltage (cf. appendix D.7). Then the reset switches are opened again and the sample-and-hold stage following the pipeamp (cf. sect. 3.7) is set into transient mode. Now the *read switch* is closed and the pipeline storage capacitor is connected to the read line. After the pipeamp has integrated the charge on its feedback capacitor, the sample-and-hold stage is switched to *hold* and after that the read switch is opened again. On HELIX128-3.0 and later versions, the reset switch remains closed all the time the pipeamp is idle. The timing diagram is shown in fig. 3.23.

Taking a closer look at fig. 3.22 one notices that charge distribution across the three capacitors C_{Cell}, $C_{\mathrm{parasitic}}$ and C_{c} (which connects to the virtual ground of the amplifier input) takes place. In case of $V_{\mathrm{Cell}} = V_{\mathrm{d}}$ a charge equilibrium is already present when the read switch is closed and no transition on the amplifier output takes place. Since the pipeamp only integrates the charge on C_{c}, neglecting charge injection effects, we end up with:

$$Q_{\mathrm{eff}} = \frac{C_{\mathrm{c}}}{C_{\mathrm{Cell}} + C_{\mathrm{parasitic}} + C_{\mathrm{c}}} \left(V_{\mathrm{offfset}} + V_{\mathrm{signal}} - V_{\mathrm{d}}\right) \cdot C_{\mathrm{cell}} \qquad (3.42)$$

Q_{eff} = charge integrated by the pipeamp.

V_{offset} = offset voltage of the frontend's output.

V_{signal} = (AC) signal voltage of the frontend's output.

This results in $\frac{Q_{\mathrm{eff}}}{Q_{\mathrm{cell}}} = 0.256$ ($C_{\mathrm{parasitic}} = 2.05\mathrm{pF}$) and in turn $\frac{Q_{\mathrm{eff}}}{Q_{\mathrm{in}}} = 2.27$.

The amplifier core cell is a *folded cascode* circuit similar to those of the preamplifier and shaper as depicted in fig. 3.24. The key requirements for this

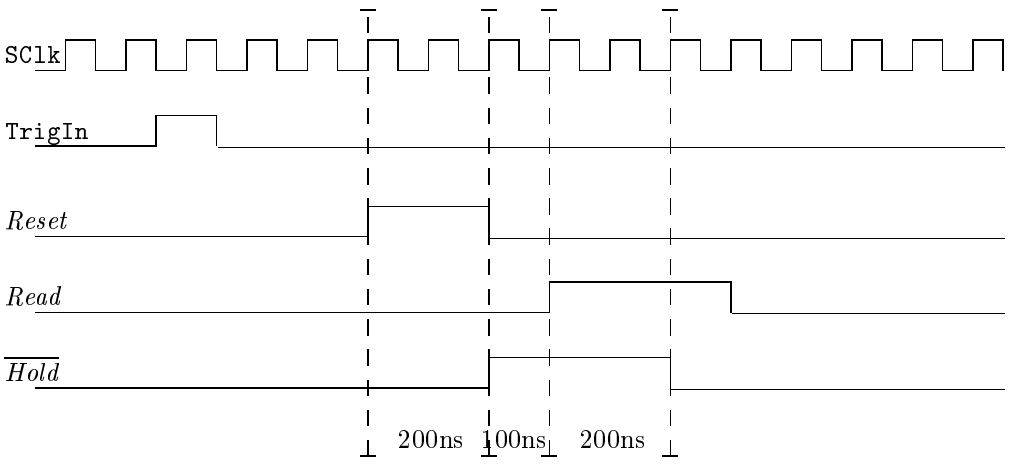


Figure 3.23: Timing diagram of HELIX128-2's pipeline readout amplifier switches. `SClk` is the sampling clock frequency. On HELIX128-3.0 and later chips, "*Reset*" remains "high" all the time the pipeamp is idle and is set to "low" only when "*Read*" or "$\overline{Hold}$" are "high".

amplifier are low noise [13] ($\overline{ENC} \leq 450\mathrm{e}^-$), stability at unity gain[14] (during the reset phase) and a rise time well below 200ns. Furthermore the operating point of the amplifier has to remain the same in closed loop and open loop operation. To ensure this, the source of the input transistor connects to an adjustable voltage V_{dcl}. On HELIX128-2.0 and 2.1, which lacked Q_5 and Q_6 the range of V_{dcl} was found to be insufficient. Thus the radiation tolerance was restricted and all amplifier channels changed their operating points when the "reset" switch was opened. This transition had also an adverse effect on the noise performance. By introducing Q_5 and Q_6 on HELIX128-2.2. the required V_{d} was lowered, which solved the problem (cf. appendix E). The detailed calculation of the transistor sizes and key parameters ($g_{\mathrm{m}} = 437\mu\mathrm{A/V}$, $\tau_{\mathrm{rise}} = 25\mathrm{ns}$) can be found in [Fal98].

The noise can be calculated from the transfer function given by $w(t) = 1 - e^{-\frac{t}{\tau_{rise}}}$. Since the amplifier is only sensitive for a finite time, the divergence in tab. 3.1 does not show up. With $R_{\mathrm{p}} = \infty$ (neglecting leakage currents in Q_{102} and Q_{202} in fig. 3.24) we obtain from eqs. 3.15 and 3.16:

[13] The deterioration of the frontend's noise performance (which was found e.g. on the APV5 readout chip [Fre95]) is given by $\frac{\overline{ENC}_{\mathrm{pipeamp}}}{A_Q \cdot C_{\mathrm{Cell}}}$ and should be $\ll \overline{ENC}_{\mathrm{frontend}}$.

[14] The voltage divider made of Q_5 and Q_6 reduces the loop gain and therefore somewhat relaxes this requirement.

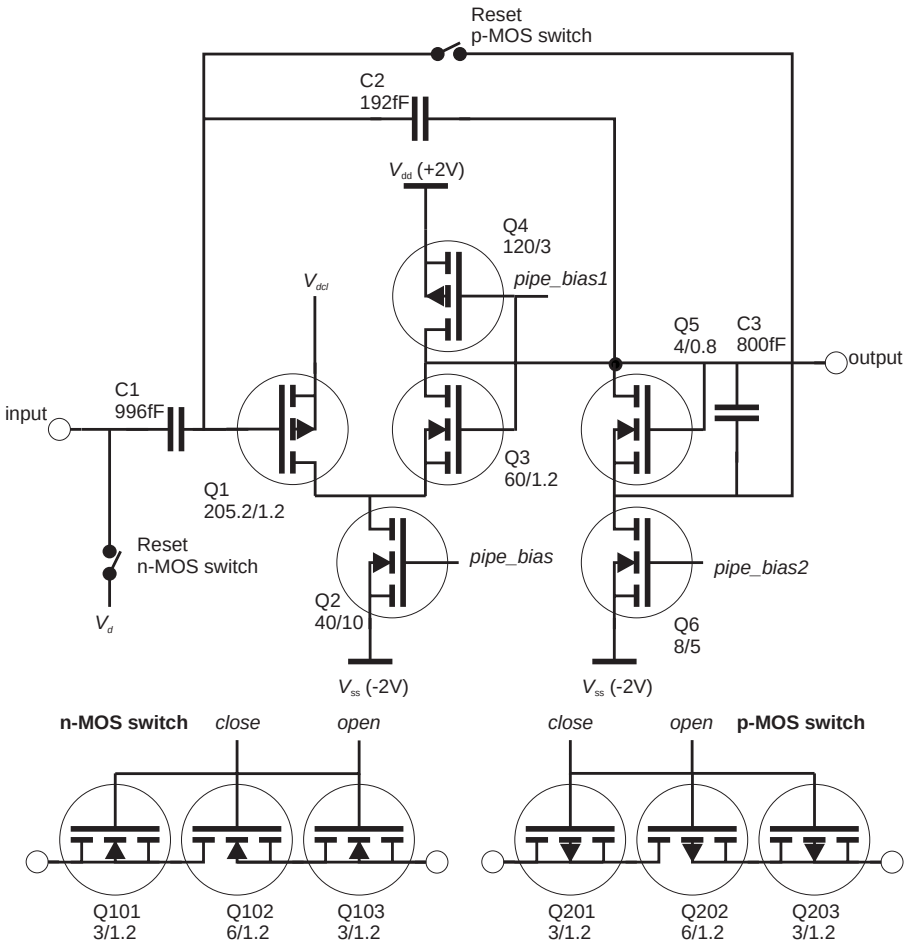


Figure 3.24: Schematic of HELIX128-2's pipeline readout amplifier.

$$\overline{ENC_{\mathrm{p}}^2} = \frac{1}{2}\overline{i_{\mathrm{n}}^2}\int_0^{t_{\mathrm{hold}}} \frac{1-e^{-\frac{t}{\tau_{rise}}}}{1-e^{-\frac{t_{\mathrm{hold}}}{\tau_{rise}}}}\,dt \tag{3.43}$$

$$\overline{ENC_s^2} =$$

$$\frac{1}{2}\overline{e_{\mathrm{n}}^2}\int_0^{t_{\mathrm{hold}}} \frac{-\left(C_{\mathrm{parasitic}}+C_{\mathrm{c}}+C_{\mathrm{cell}}\Theta(t_{\mathrm{on}}-t)\right)^2}{\tau_{\mathrm{rise}}}\cdot\frac{e^{-\frac{t}{\tau_{rise}}}}{1-e^{-\frac{t_{\mathrm{hold}}}{\tau_{rise}}}}\,dt \tag{3.44}$$

t_{hold} = time period the pipeamp is sensitive (i.e from opening the "reset" switch at $t = 0$ to t_{hold} when the sample-and-hold stage is switched to "hold").

t_{on} = time period for which C_{Cell} is connected to the pipeamp.

Substituting the pipeamp's parameters (i.e. $g_{\mathrm{m}} = 473\frac{\mu\mathrm{A}}{V}$, $C_{\mathrm{GD}} = 260\mathrm{fF}$ and $\omega = \frac{1}{2\tau_{\mathrm{rise}}} = 20\cdot 10^6\mathrm{s}^{-1}$) into eqs. 3.43 and 3.44 we obtain $\overline{ENC}_{\mathrm{pipeamp}} =$

$63.5 \cdot 10^{-18}\mathrm{C} = 397\mathrm{e}^-$ which contributes $\overline{ENC} = 175\mathrm{e}^-$ to the noise at the preamplifier input.

The pipeamp's reset switches consist of three transistors each: Short circuited transistors are connected to the source and drain of the switch. Since these transistors are half the size (and therefore half the capacitance) of the switch and operated opposite to it, charge injection is cancelled (cf. fig. 3.24). Figure 3.25 shows the layout of the pipeline readout amplifier.

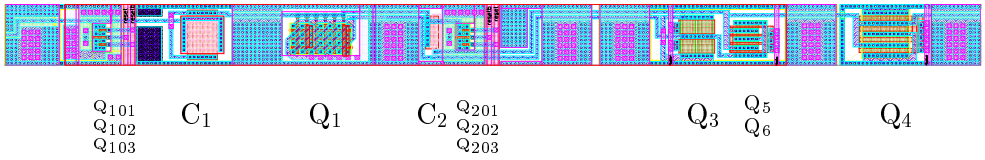


Figure 3.25: Layout of HELIX128-2.2's pipeline readout amplifier. The designators identify the devices with fig 3.24. Dimensions are 659.6µm×41.2µm. The colour scheme of the layers is explained in fig. 4.1.

3.7 The Readout Multiplexer

The Purpose of the multiplexer is to subsequentially switch the signals of the 128 pipeline readout amplifiers to a single output line. The design was derived from a multiplexer designed by J. Kaplon [Kap95], but split into two stages by W. Fallot-Burghardt [Fal98]. In a two-stage multiplexer only the last stage has to run at the full readout speed, while the first stage runs at a lower frequency. On HELIX128 in addition to the signals of the 128 readout channels the 8bit pipeline column number, i.e. the memory address containing the data, is also read out. This allows e.g. for a cell-wise offset subtraction or latency monitoring to detect SEU events (cf. sect 4.6.1). Four 34 channel multiplexers switch the signals of the $128 + 8 = 136$ channels onto four lines at a quarter of the final `RClk` readout clock speed. The second stage then switches these four signals to the output line with the full frequency of `RClk` (i.e. 40MHz). As shown in the schematic depicted in fig. 3.26 the second pair of *MUX34* multiplexers has to be operated with a 180° phase shift to exploit the relaxed timing constraints of the first stage. Fig. 3.27 shows the timing of the multiplexer stages. The first mux stage therefore has to have a rise time $t_{\mathrm{rise}} < 37.5\mathrm{ns}$. As shown in fig. 3.28 the fist multiplexer stage is driven by a source follower, which is part of the sample-and-hold stage latching the signals of the pipeamp (cf. sect. 3.6). It has to drive the parasitic capacitance of the first-stage bus line and the gate-drain capacitances of the 33 remaining switches (i.e. Q_9), which in total amount to $C_{\mathrm{MUX34}} = 5.02\mathrm{pF}$. Since $g_{\mathrm{m}}(Q_7) = 2.0\mathrm{mA/V}$ and $R_{\mathrm{DSon}}(Q_9) = 80\Omega$ the rise time constant of the signal on the *MUX34* bus is $t_{\mathrm{rise}} = 9.1\mathrm{ns}$, which is fast enough for e.g. charge injection induced disturbances and ringing to settle. Ringing and charge injection in the last *MUX4* multiplexer stage is directly visible on the chip's output and therefore has to be avoided. Like

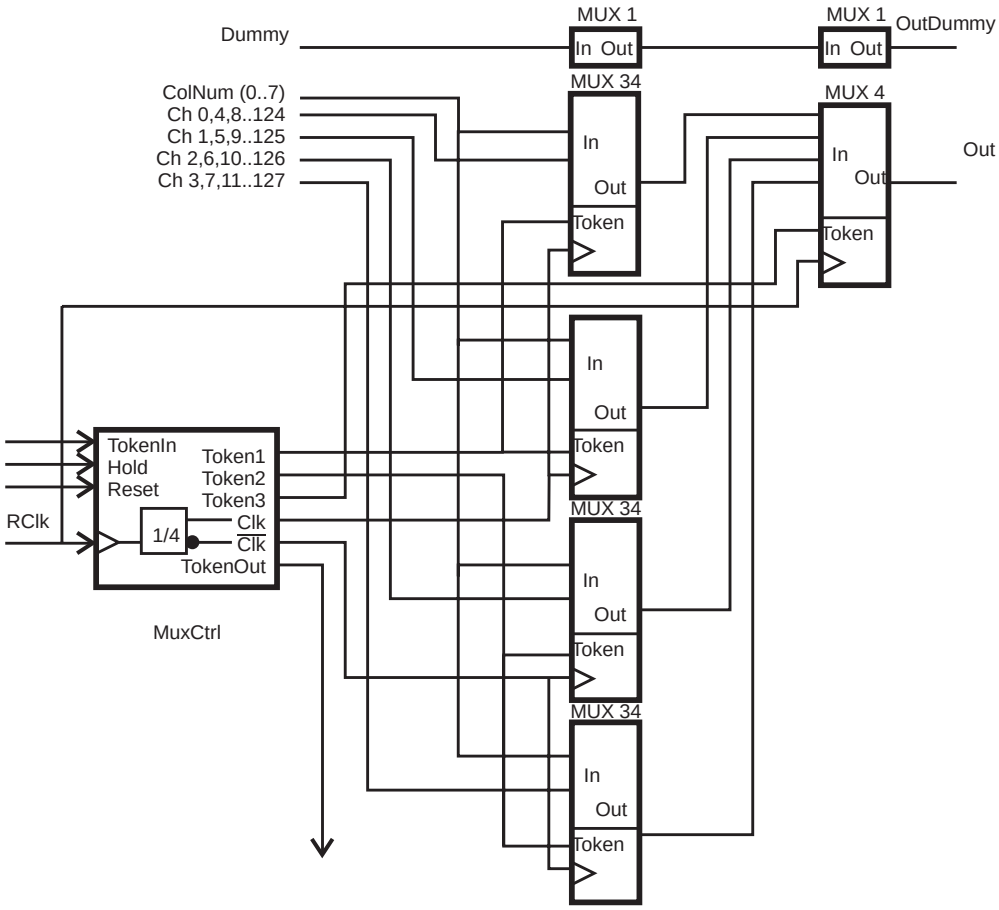


Figure 3.26: Schematic of HELIX128-2's two stage multiplexer.

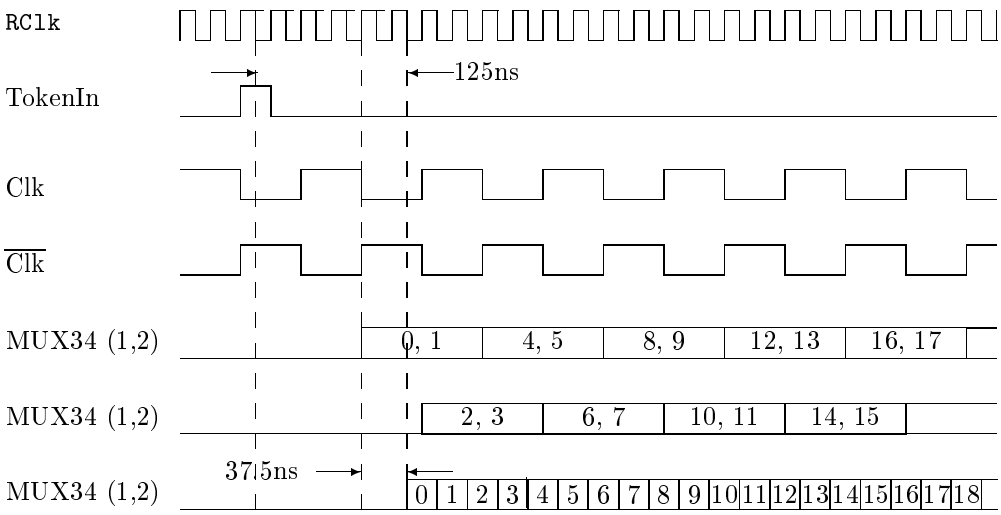


Figure 3.27: Timing diagram of the HELIX128-2's multiplexer.

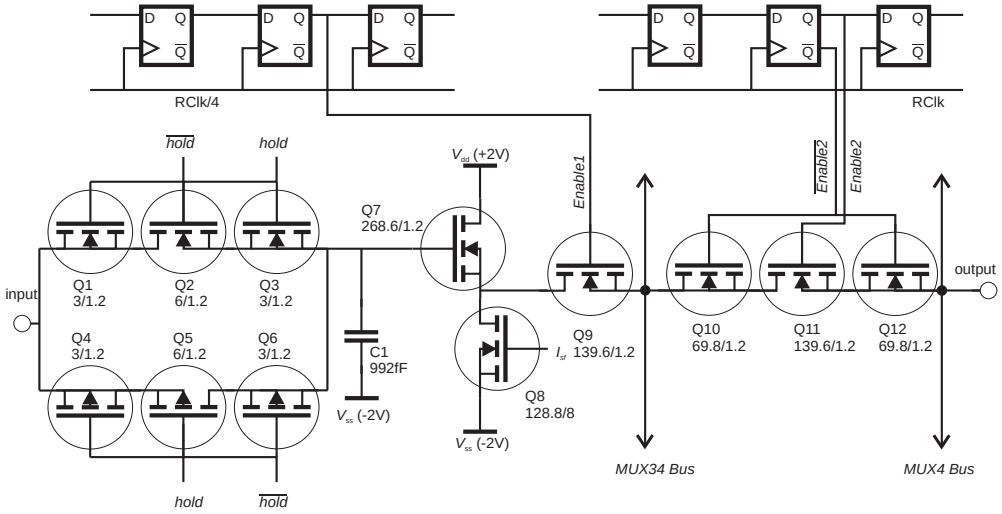


Figure 3.28: Schematic of one HELIX128-2's multiplexer channel.

in the multiplexer's S&H stage and the pipeamp (cf. sect. 3.6) compensated transmission gates were employed to accomplish this.

When driving the *MUX4* output, the parasitic capacitance C_{MUX34} is in parallel with the internal resistance of the source follower, resulting in a lower internal resistance of the driving stage and an even faster rise time of $t_{\mathrm{rise}} = 6.4\mathrm{ns}$ on the multiplexer output.

The layout of a multiplexer channel is depicted in fig. 3.29. Figure 3.30 shows the readout figure of HELIX128128.

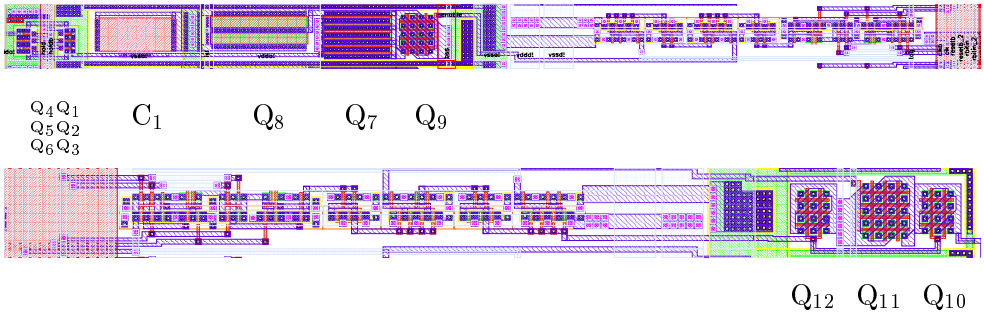


Figure 3.29: Layout of the HELIX128-2's multiplexer [Fal98]: A *MUX32* channel (top) and a *MUX4* channel (bottom). The designations correspond to those in fig. 3.28. The dimensions are 668µm×41.2µm (*MUX32*) and 465µm×41.2µm (*MUX4*). The colour scheme of the layers is explained in fig. 4.1.

3.7.1 *Daisy-Chained* Readout of two or more HELIX128

The digital part of the multiplexer stages is a simple shift register consisting of FlipFlops which use a differential clock and also have a synchronous reset

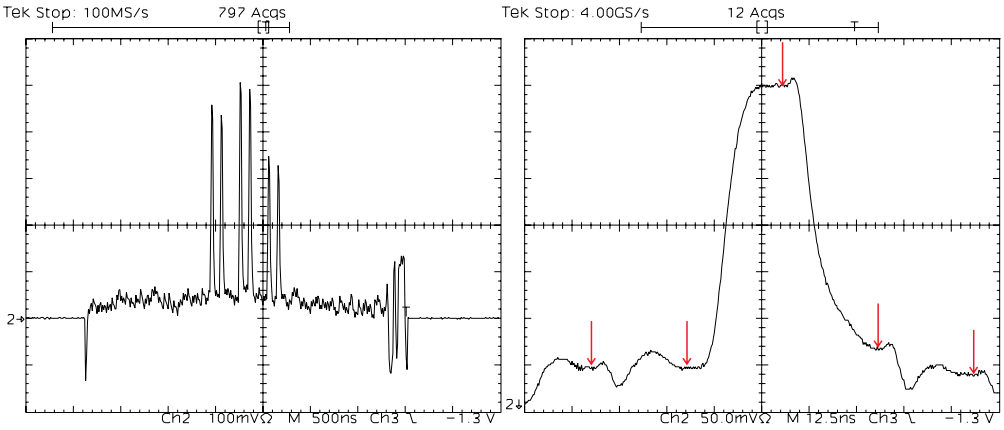


Figure 3.30: Data burst of HELIX128 at `RClk`= 40MHz readout speed. Left: Complete readout figure. A charge of $96 \cdot 10^3 e^-$ ($\equiv 4MIP$) was injected on 6 channels. The last eight "channels" of the burst encode the pipeline column number (i.e. the memory address the data was stored at). Right: Enlarged view of a channel with a $96 \cdot 10^3 e^-$ signal. The signal of the *dummy* (i.e. shaper only) channel `notAnalogOut` was subtracted for offset correction. The arrows indicate the proposed sampling points of the subsequent DAQ stage.

(both not shown in fig. 3.26). The control of these shift registers is done by a sequencer, which besides feeding the initial read bit to all *MUX34* stages and 34 read bits to the *MUX4* stage, also takes care of the operation of the pipeline readout amplifier. Furthermore it generates a `DataValid` signal used to connect the current buffer (cf. sect. 3.8) to the output pad, when the multiplexer is sending data. This signal is also externally available, e.g. to control subsequent DAQ stages. A counter generates a `HelixTokenOut` signal five `RClk` cycles before the end of the readout. It can be sent to a second HELIX128 chip's `HelixTokenIn` pad, which then will immediately send its data after the preceeding one has finished (cf. fig. 3.27). The last chip in such a readout daisy-chain has to feed a signal back to all others. This `ReturnToken` signal is necessary for a synchronous operation of the daisy-chained chips, e.g. to discard the already read out event from the derandomiser buffer. The first chip in a readout daisy-chain has to get it's `HelixTokenIn` from the `SufixTokenOut` pad. This is necessary to send an initial token to the readout chain after a reset of the chip and also allows the insertion of a programmable pause before the start of the next readout burst, which might be required by subsequent DAQ stages (cf. section 3.10.2). If the derandomiser buffer is empty, the token will be kept until the arrival of the next trigger. Besides the obvious `TokenOut-TokenIn` and `ReturnTokenOut-ReturnTokenIn` connections, on HELIX128-2.2 (and preceding versions) a `SufixTokenOut-TokenIn` connection on the first and a `TokenOut-ReturnTokenIn` on the last chip (or both for the readout of a single chip) have to be established.

Fail Safe Token Schema of the HELIX128-3.0

The readout of four HELIX128 chips in a daisy-chain by the ZEUS experiment required the introduction of a fail safe token schema to overcome a potential single chip failure, which would block the whole readout chain. It was implemented on the HELIX128-3.0 chip by introducing a second token path (shown in fig. 3.31), which can be selected by programmable switches. This is depicted in fig. 3.32, which also shows that the `SufixTokenOut-TokenIn` and `TokenOut-ReturnTokenIn` connections can be established by register programmable switches.

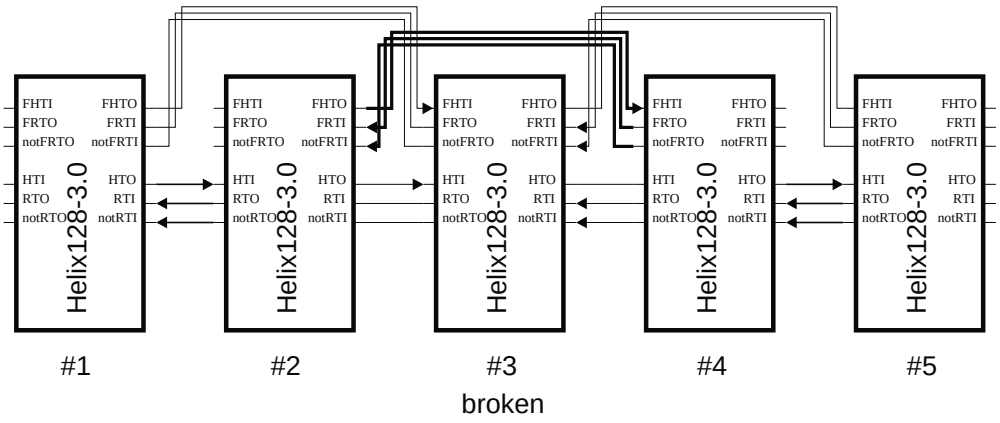


Figure 3.31: HELIX128-2's fail safe token path. The bold lines indicate how the token can bypass the broken chip.

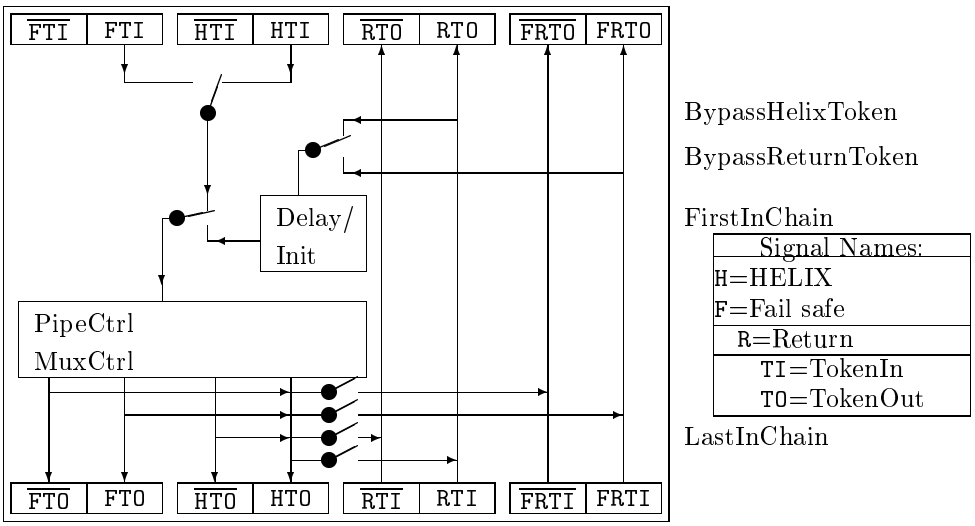


Figure 3.32: Switches for HELIX128-3's internal token routing, implementing a fail safe token schema. The inverted signals are only present to suppress crosstalk.

The implemented fail safe token schema can overcome all 4 possible failures of non-adjacent chips:

- Chip does not accept or pass the token: The chip subsequent to the failing one is set to *BypassToken*. It then uses the token passed from the one preceding the failing one.
- First chip in the chain does not work: Set up second as *FirstInChain*.
- Last chip in the chain does not work: Set up pre-last as *LastInChain*.
- Open or short circuit of the return token line: Set all chips to *BypassReturnToken*. The fail safe return token line is now used instead.

The only single-chip failure not covered by the fail safe token schema is a short of the chip's analogue outputs `AnalogOut` or `AnalogOutDummy`.

To reduce crosstalk, differential signal lines were implemented together with the fail safe token schema. However, only the non-inverted signal inputs are used.

3.8 The Output Transconductance Amplifier

In case of the HERA-*B* silicon vertex detector, the receivers for the HELIX128's 40MHz analogue signals are mounted outside the *vertex vessel*. This connection of about 1m length has an inhomogeneous impedance, due to the various technologies (stripline on ceramic and Kapton substrates, coax cable) and connectors (esp. the vacuum feed through) used. Driven by a voltage amplifier, such a line causes a severe deterioration of the signal by reflections and ringing. Furthermore the capacitance of an unmatched transmission line implies an increase of a voltage amplifier's rise time.

The disadvantageous capacitive load can be circumvented by the use of a current amplifier: Driving a signal current into a zero impedance node does not cause a voltage change, and the signal is not affected by capacitive load. Another favourable side effect of this concept is the reduced power dissipation.

The drain current of a FET is unfortunately proportional to the square of the controlling (gate) voltage (cf. eq. 4.4) and the linearity of the circuit becomes a major problem. However, a series resistor connecting to the source of a FET not only reduces its g_m, it also improves the linearity: If $g_\mathrm{m} \gg \frac{1}{R}$ the system works like a source follower and it becomes $V_\mathrm{R} = V_\mathrm{G} - V_\mathrm{th}$ and in turn we obtain $I_\mathrm{D} \propto \frac{V_\mathrm{G}-V_\mathrm{th}}{R}$. This technique was employed by W. Fallot-Burghardt [Fal98] for the HELIX128 current output driver depicted in fig. 3.33.

The first stage (i.e. $\mathrm{Q}_1 \ldots \mathrm{Q}_5$) is a differential amplifier, but instead of a voltage (like in fig. 3.15), the difference current of the two branches is, together with a bias current from Q_7, fed into Q_6. While the transconductance of the differential amplifier is only 224µA/V, the current mirror consisting of Q_6 and Q_7 provides an additional amplification of the current by 25. The rise time of the circuit is only $t_\mathrm{rise} = 9\mathrm{ns}$, due to the absence of high impedance nodes. Two of these current drivers are implemented on HELIX128: One is fed by

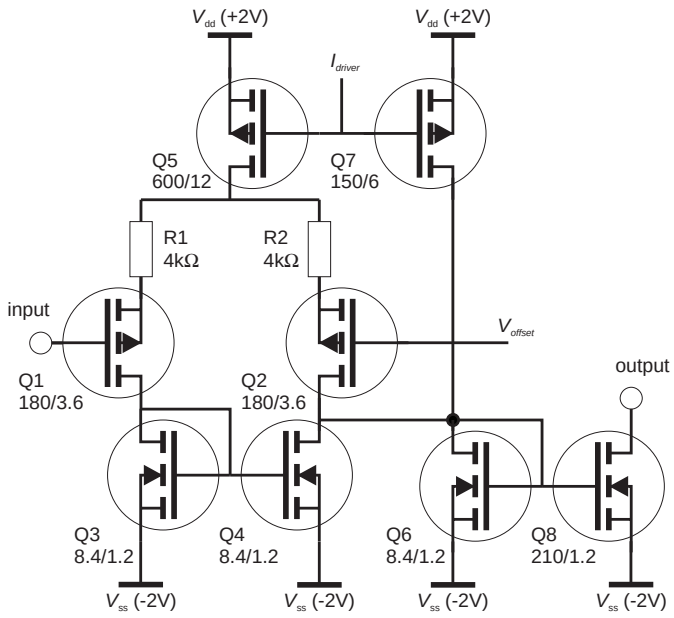


Figure 3.33: Schematic of HELIX128-2's current line driver.

the multiplexer, while the other is driven by the shaper-only `analogOutDummy` channel. The inverting input of both buffers connects to a reference voltage *Voffset*. The main advantage of this schema wrt. a fully differential output is the "visibility" of the pipeamps offset voltage on the output, which allows the tuning of *Vdcl* (cf. appendix D.8).

Fig. 3.34 shows the layout of the HELIX128's output stage.

3.9 Pipeline Control Circuit

To control the pipeline operation, HELIX128 uses a FIFO based circuit instead of the shift register based implementations known from other readout chips [APV6], [Kap98]. It was synthesised from a functional description (written in *Verilog*), which besides scalability and portability resulted in a circuit, that is much smaller (wrt. chip area) than a shift-register based solution. It was originally developed by M. Feuerstack-Raible [Feu], but all improvements implemented on HELIX128-3.1 resulted from testing and debugging done in this thesis.

A big advantage of this circuit, when implemented with standard cells, is that it only grows $\propto \ln(n) \times m$ where n is the latency and m the depth of the derandomiser buffer, which stores triggered events [Feu].

The pipeline control circuit has to accomplish four tasks:

- Write data to the pipeline.
- Accept triggers and protect the corresponding data from being overwritten. This also includes the buffering of up to 8 triggered events waiting

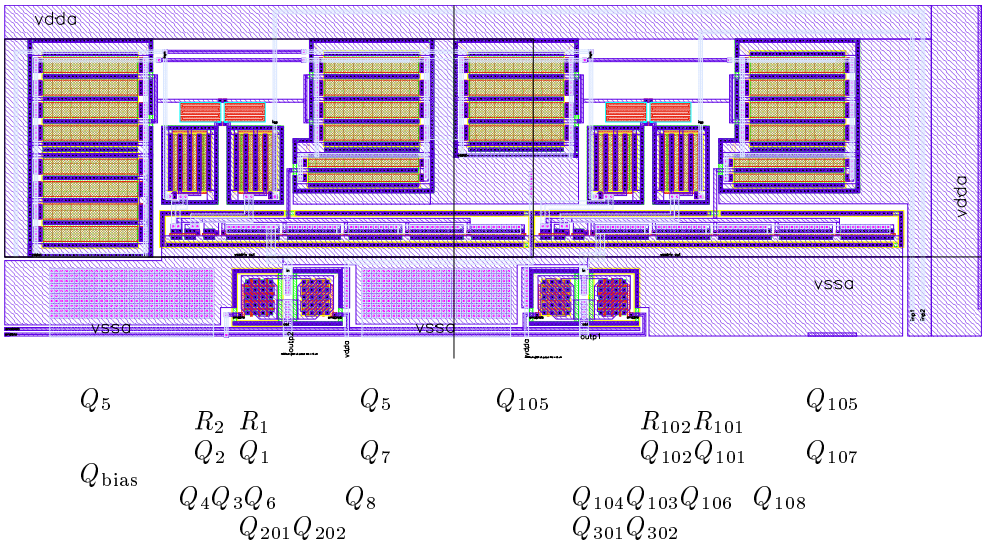


Figure 3.34: Layout of the HELIX128-2's output stage: Two current buffers can be switched to the output lines by the waffle transistors in the bottom row. The designations identify the devices with fig. 3.33 (The $10x$ indices denote the 2^{nd} channel, i.e. `AnalogOutDummy`). The size of the circuit is 780µm×267.5µm. The colour scheme of the layers is explained in fig. 4.1.

for readout and flagging that the chip temporarily can not accept further triggers.

- Initiate the readout of the next triggered data, when the readout of the previous event is finished (i.e. immediately if there is no readout ongoing).
- Free the protected addresses after their data has been read out.

The implementation of the pipeline control circuit on the HELIX128 is split into three parts: The derandomiser buffer and two *incrementers*. The first ("write") *incrementer* provides with each `SClk` cycle the address of the next pipeline column to be overwritten. This address is decoded to operate the pipeline write switches. The second ("trigger") *incrementer* works like the first one, but calculates each `SClk` cycle the "triggerable" address. In fact it calculates the same addresses as the first one, only delayed by the latency. An accepted trigger signal will write this address to the derandomiser buffer. A sequencer in the derandomiser part will initiate the readout of the oldest data referenced by the contents of the buffer. Furthermore it will discard the address from the buffer, after its data has been read out.The algorithm of the pipeline control circuit is depicted in fig. 3.35.

3.9.1 *Incrementer* – Calculator and Buffer for valid Pipeline Addresses

Each `SClk` cycle, the *Incrementer* compares two subsequent pipeline addresses with the contents of the derandomiser buffer. If an address is not marked for

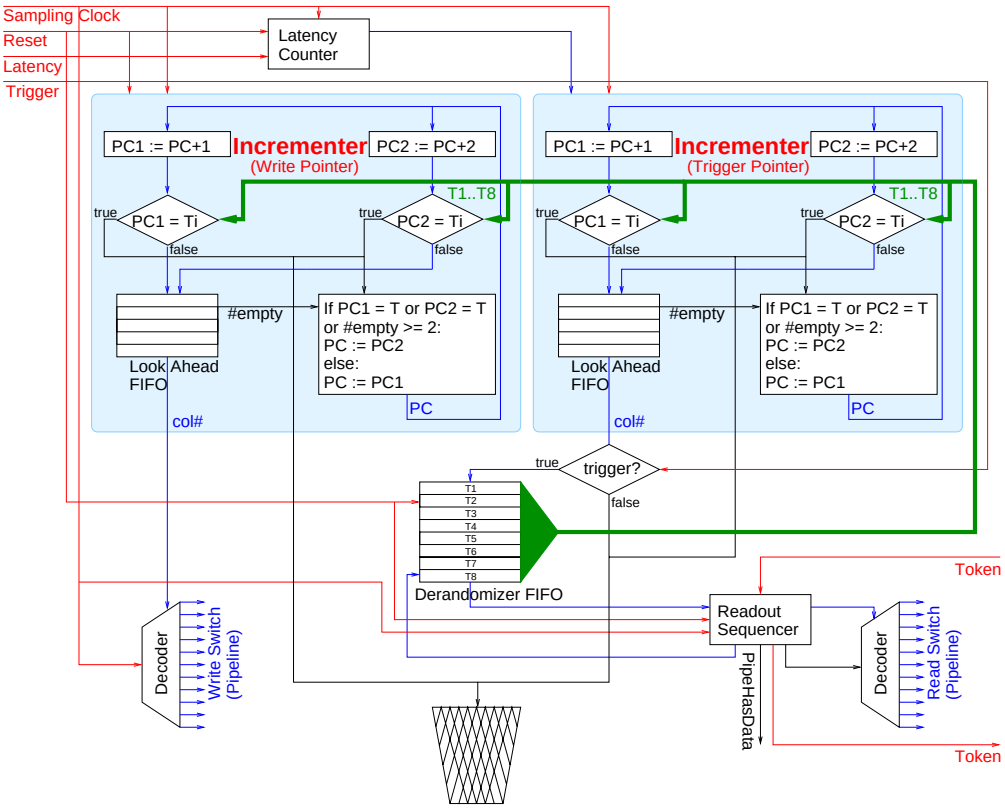


Figure 3.35: Principle of the HELIX128-2's pipeline read/write control circuit.

readout (i.e. not a valid content of the derandomiser's FIFO), it is stored into a *lookAhead FIFO*, provided there is enough space. The pipeline addresses compared in the next clock cycle depend not only on the result of this comparison, but also on the number of free buffers in the *lookAhead* FIFO. Since there is always one free slot, there are six possible results of this calculation, which are given in tab. 3.2. The oldest entry in the *lookAhead* FIFO is the output of the *Incrementer* and pulled from the stack each `SClk` cycle.

It is obvious that the worst case this algorithm has to handle are m subsequent triggered pipeline addresses, where $m = 8$ is the depth of the HELIX' derandomiser FIFO. Since we compare two consecutive addresses each `SCLK` cycle, a naive calculation of the required depth of the *lookAhead* FIFO's results in $n = m/2 + 1 = 5$ addresses. This is the correct result from an incorrect calculation: On the one hand the *lookAhead* FIFO consists of latches and therefore it has an implicit delay of one `SClk` cycle. This reduces its effective depth to $n - 1$ addresses. On the other hand, the usual state of the *Incrementer* is "2" in tab. 3.2 (with 8 subsequent pending triggers, it has to be "2" outside this sequence). Consequently eight subsequent triggered addresses are traversed by the sequence 2-4-6-5-5-3-1-1-2 of the *incrementer's* states, i.e. no valid addresses are calculated for only 3 `SClk` cycles. The sequence 2-6-5-5-5-1-1-1-2 (generated by triggering the address preceding 7 already triggered ones) causes a buffer underrun at the third "5" and has to be avoided. The easiest way to accomplish

State	Number of valid addresses	Number of free *lookAhead* FIFO positions	Action taken	Start address for next calculation (PC)
1	2	≥ 2	store both addresses in *lookAhead* FIFO	$n+2$
2	2	1	store lower address in *lookAhead* FIFO (discard higher one, it will be calculated again in the next cycle)	$n+1$
3	1	≥ 2	store valid addresses in *lookAhead* FIFO	$n+2$
4	1	1	store valid addresses in *lookAhead* FIFO	$n+2$
5	0	≥ 2	none	$n+2$
6	0	1	none	$n+2$

Table 3.2: *Incrementer* states.

this is a pipeline depth of $l + m + m/2 + 2 = 142$ entries (with $l = 128 =$ max. latency and $m = 8 =$ depth of derandomiser FIFO), since it prevents a -2-6- sequence. It was realised on HELIX128-3.1 (cf. appendices C, E). Figure 3.36 visualises the two sequences.

3.9.2 *Multi-Event Buffer* – Derandomiser for Triggered Events

This derandomiser buffer with a depth of 8 entries for pending triggers was implemented to comply with the requirements (cf. sect. 3.1) and provide dead-time free operation. Each entry consists of the pipeline address of the triggered sample and two flag bits, *inhTrig* and *inhWrite*, to validate the entries for comparison by the "write" and "trigger" *Incrementers*. The implementation is a ring buffer with read and write pointers, since the read and write operations to the buffer are in FIFO order, while the final discarding of entries from the buffer can occur in a different order. The operation of the derandomiser buffer is the following:

- *Trigger:* If the HELIX128's `TrigIn` signal is high and the derandomiser's write pointer refers to an empty position, the address generated from the "trigger" *Incrementer* is written to that position of the derandomiser buffer, *inhTrig* and *inhWrite* flags are set and the pointer is forwarded to the next position.
- *Readout:* If the derandomiser's read pointer references an entry with the *inhTrig* and *inhWrite* flags set, the sequencer controlling pipeamp and

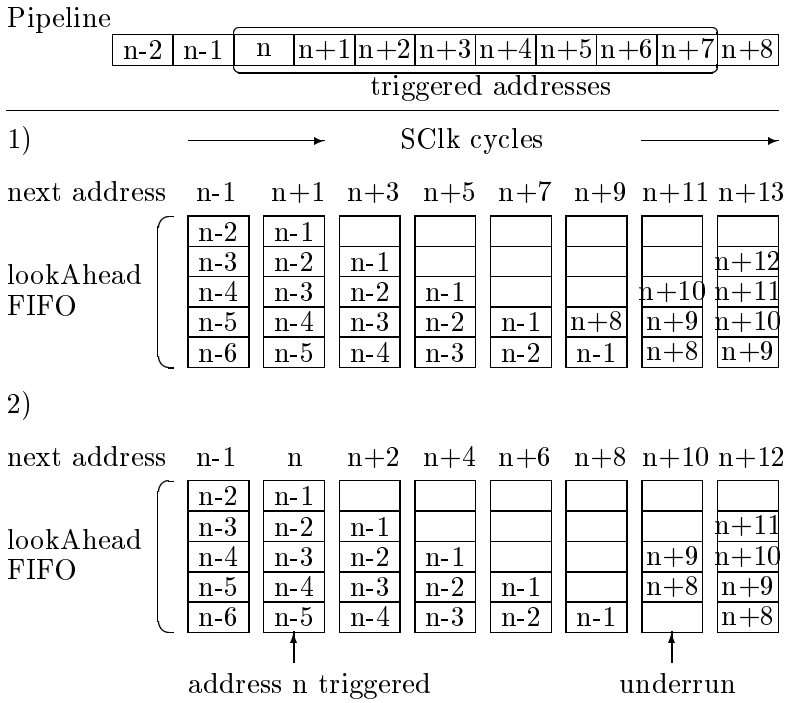


Figure 3.36: Contents of the "write" *Incrementer's* lookAhead FIFO when traversing 8 subsequent triggered addresses: 1) normal 2) bug on HELIX128-2.2 (and earlier) when the address n is triggered immediately before its calculation by the 'next address' counter. The underrun occurs since the address $n + 8$ is calculated in the same `SClk` cycle in which it is already needed for the write operation (cf. appendix E).

readout multiplexer is started. Upon arrival of the `ReturnToken`, the *inhWrite* bit is cleared and the pointer is incremented.

- *Discard:* An entry is discarded from the buffer, when its *inhTrig* flag is cleared. This is done, when its address is written to the "write" *Incrementer*'s FIFO. It ensures, besides the conservation of latency, that analogue data has been written to the address, before it can be added to the "trigger" *Incrementers* FIFO. The discarding of entries does not necessarily happen in the order in which they have been added to the buffer.

The *inhTrig* bit referenced by the derandomiser's write pointer is the `FifoFull` signal[15], indicating the outside world that the HELIX128 is temporarily unable to accept further triggers. Fig. 3.37 illustrates the function of the *Multi-Event Buffer*.

[15] On HELIX128-3.1, cf. appendix E.

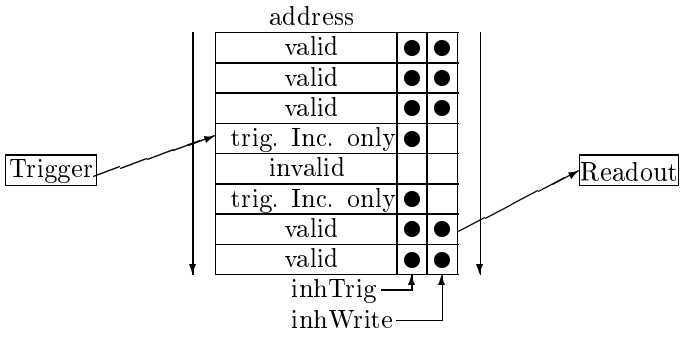


Figure 3.37: Principle of the HELIX128's *Multi-Event Buffer*: The pointers propagate from top to bottom with the acceptance of a trigger or the arrival of the `returnToken` respectively. The *inhTrig* bit of the entry referenced by the trigger pointer (left) determines the value of the HELIX128's `FifoFull` signal, i.e. if the chip will accept a trigger or not.

3.10 The Interface-, Control- and Bias Generator Circuit (*SUFIX*)

The first HELIX128[16] readout chip [HX96], [Fal96], [Sex97] (cf. appendix B) required six control voltages and 7 bias currents. Furthermore its latency was adjusted with two individual reset signals – one for the sampling process and the other for the trigger and readout operation. To adjust these parameters and accomplish a remote control of the chips e.g. in the HERA-*B* silicon vertex detectorfor which it was intended, a "SUpport and control chip For the HELIX readout chip" (*SUFIX*) [Tru96] was developed. The basic functionality of this chip was much inspired by the APV5-RH bias generator chip [Øde95]. It implemented the same programming method using the trigger line. In addition to the features of that chip, the *SUFIX* included circuits to detect SEU failures (cf. sect 4.6.1) and an alternative serial interface, independent from the trigger line. Figure 3.38 shows the block schematic of the *SUFIX* chip, which is still valid for the implementation of these circuits on the HELIX128. On HELIX128-2.0 "*SUFIX*" was integrated on the readout chip itself, the name for that part of the chip, however, remained.

The following sections describe the different parts of the HELIX128-2's interface, bias generator and control circuit, which was developed in this work. The circuits are:

- Six DACs to adjust control voltages, e.g. for pulse shape, discriminator threshold and the DC offset of different amplifier stages.
- Seven DACs to adjust the bias currents of the chip's analogue stages.
- A reference current source, from which all bias currents can be derived.

[16]This chip will be referred to as HELIX128-1 in the following, since HELIX128 designates the HELIX128–2 in this document.

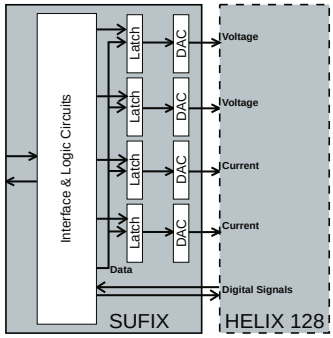


Figure 3.38: Block schematic of the *SUFIX* chip. It also represents the implementation of the interface, bias generator and control circuits on the HELIX128–2.

- A serial interface to program the chip.
- A circuit to adjust the latency (*Starter*).
- A circuit to generate a programable pause between two readout bursts (*TokenDelay*).
- Switches for the routing of the readout token.
- A programable clock divider to derive the sampling clock `SClk` from the readout clock `RClk` (*ClkDiv*).
- A Circuit to detect SEU failures by monitoring the synchronous operation of two or more HELIX128 chips (*SyncMon*).

3.10.1 The Bias Generator Circuit

One of the dominant effects of ionising radiation on CMOS devices is the change of the threshold voltage V_{th}, which alters the operating point of transistors with a fixed gate source voltage V_{GS} (cf. sect. 4.3.2). While the current of an n-MOS FET with fixed gate voltage increases with irradiation, it decreases for a p-MOS transistor, in the worst case cutting off the bias (drain) current completely. This undesirable behaviour can be circumvented by forcing the bias current of an amplifier stage via current mirrors. While the current of such a circuit is still controlled by the different gate voltages, these voltages are derived from the diode-connected part of current mirrors and therefore are subject to the same change of the threshold voltage as the amplifier stage itself – the gate voltage changes with irradiation, but the bias current remains constant. However, an initial bias has to be provided to circuits with this topology. And since the internal resistance and the noise of an amplifier changes with the bias current, it has to be adjustable.

In other parts of the HELIX128 adjustable voltages are required. The most obvious one is the threshold voltage of the trigger discriminators, but also the compensation of offset voltage shifts caused by the current biasing described

above and the use of transistors as tunable resistors require adjustable control voltages.

The required remote control of the system calls for digital-to-analogue converters (*DAC*s) to adjust these voltages and currents: DACs transform binary numbers to a physical quantity, usually a voltage or a current. The four characteristic properties usually quoted for such devices are the resolution (in bits), the transfer characteristic (linear or logarithmic), the (differential) nonlinearity and the maximum frequency at which the output can be changed.

For the DACs on the HELIX128 other properties are more relevant: The DACs are operated statically and thus the maximum sampling frequency is irrelevant. Most important for the DACs on the HELIX128 is that their output is extremely "quiet", especially those which feed the chip's frontend. They must not show any noise or clock feedthrough, which excludes dynamic DAC concepts like $\delta\Sigma$-converters[17] or successive approximation converters. Consequently only static converters were implemented on HELIX128.

DACs for Control Voltages

The most demanding requirements on the DACs for the HELIX128's control voltages surprisingly originate from only two parts of the chip:

- A slope of $\lesssim$ 3mV/LSB for the comparator threshold level.
- A dynamic range of $\geq$ 80mV (i.e. a resolution $\geq$ 6bit) for the trigger discriminator.
- A dynamic range of $-1 \ldots 2$V for all other control voltages.
- Reproducibility of the absolute voltages, esp. no change with irradiation.
- Very low internal resistance ($\leq 200\Omega$) for `Vdcl` (the source voltage of the pipeamp's input transistor).
- Very low noise for `Vdcl` and the frontend's feedback control voltages V_{fp} and V_{fs}.

To achieve a good reproducibility of the absolute values without employing additional references, it was decided to use the power supply rails V_{dd} and V_{ss} ($\pm$2V) to limit the dynamic range. This, together with a solution based on the matching of passive components (i.e. polysilicon resistors) ensures excellent reproducibility and radiation hardness. To achieve the required slope for the trigger threshold, a 10:1 voltage divider, using polysilicon resistors and *Gnd* (0V) as a reference, was installed. The resolution of 8bit or 15.5mV/LSB[18] was chosen since it is compatible with the internal 8bit data bus connecting the circuits in the *SUFIX* part of HELIX128. Voltage buffers between the DACs and the control voltage nodes with a finite resistance like `Vd` and `VcompRef`'s

[17] The digital data is converted to a bit stream representing pulse width modulated data, which is then simply integrated.

[18] 7bit or 31mV/LSB on HELIX128-2.0 and 2.1.

voltage divider decouple the DAC from the load and, together with external blocking capacitors, provide the required low internal resistance.

The original *SUFIX* chip and HELIX128-2.0 used a single resistor chain connecting from V_{dd} to V_{ss} as a reference, from which each DAC selected its output voltage via a demultiplexer. As expected the circuit showed an excellent linearity, which was severely deteriorated under irradiation, due to parasitic currents in the (minimum sized) n-MOS transistors of the demultiplexer (cf. sect. 4.3.1). The device was halved on HELIX128-2.0, reducing the resolution to 7bits (ignoring the LSB of the 8bit data bus) and shrinking the chip area occupied to about 1/2 of the original circuit. However, due to the poor performance under irradiation it was replaced by an 8bit $R-2R$-ladder type DAC on HELIX128-2.2.

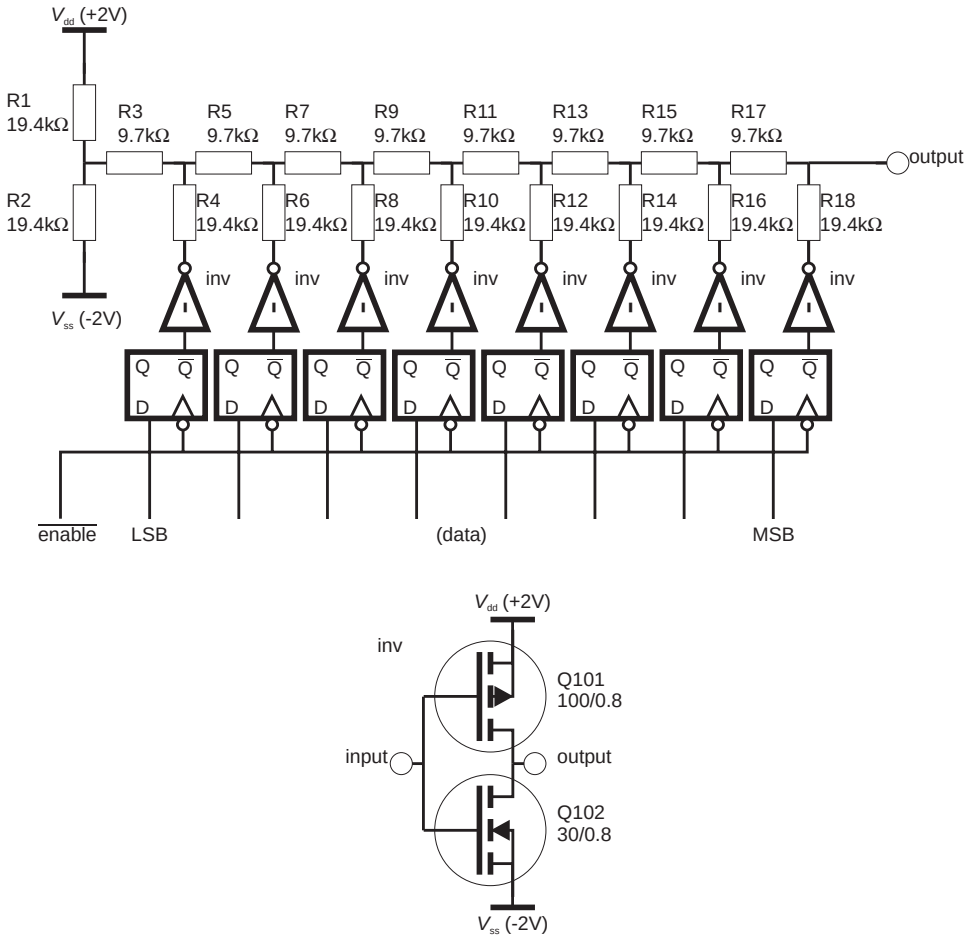


Figure 3.39: $R-2R$ ladder voltage DAC of the HELIX128-2.2's bias generator circuit. The resistors are implemented as compounds of resistors in both polysilicon layers with a constant ratio $\frac{R_{\mathrm{poly1}}}{R_{\mathrm{poly2}}}$ to reduce the space required.

Figure 3.39 shows the schematic of the $R-2R$-ladder DAC implemented on HELIX128-2.2. Only considering the LSB and neglecting the remaining part of the circuit, the output voltage of this "bit" is given by $V_{\text{out}} = \frac{V_{\text{dd}}-v_{\text{ss}}}{2} + \frac{V_1}{4}$, with V_1 being the output voltage of the inverter (i.e. V_{dd} or V_{ss}). Since the internal resistance of this part (and of the complete chain) is R, we end up with:

$$V_{\text{out}} = \frac{V_{\text{dd}} - V_{\text{ss}}}{2} + \sum_{i=1}^{n} \frac{V_i}{2^{i+1}} \tag{3.45}$$

n = resolution in bits.

$i = 1$ = MSB

$i = n$ = LSB

V_i = output voltage of the inverter associated with the i^{th} bit (i.e. V_{dd} or V_{ss}).

To obtain an estimation for the circuit's linearity, we neglect the internal resistance of the inverters (in the order of a few 10Ω) which adds to the "$2R$" resistors $R_4, R_6, \ldots R_{18}$ and conclude that it is mainly determined by the $\frac{R_{18}}{R_{17}}$ ratio. To achieve a strictly monotonous behaviour, i.e. a nonlinearity better than 1LSB, we find:

$$\frac{R_{2i+2}}{R_{2i+1}} - 2 \leq 2^{-i+1} \tag{3.46}$$

$i = 1$ = LSB.

$i = 8$ = MSB in fig. 3.39.

R_x = Resistor in fig. 3.39.

From that it is obvious that the linearity of the circuit is dominated by the matching of the MSB's resistors (i.e. $\frac{R_{18}}{R_{17}}$), which finally is limited by the manufacturing process. However, sophisticated layout techniques have to be applied to fully exploit the matching offered by the manufacturing process:

- Matched devices must have similar shapes.
- The most critical device should be placed in the geometrical centre of its counterparts ("*common centroid*" arrangement).
- Matched devices should be placed as close together as possible to minimise the impact of gradual changes of process parameters or the circuit's temperature.

Unfortunately the last two items are somewhat contradicting: Placing the devices in a "*common centroid*" arrangement implies a more complicated wiring, which in turn causes a wider spacing of the devices. As shown in fig. 3.40, a tight spacing of the devices, also resulting in compact over all dimensions of the circuit was chosen.

A disadvantage of the $R-2R$-ladder DAC should not be unmentioned: Its power dissipation strongly varies with the binary number (i.e. the output

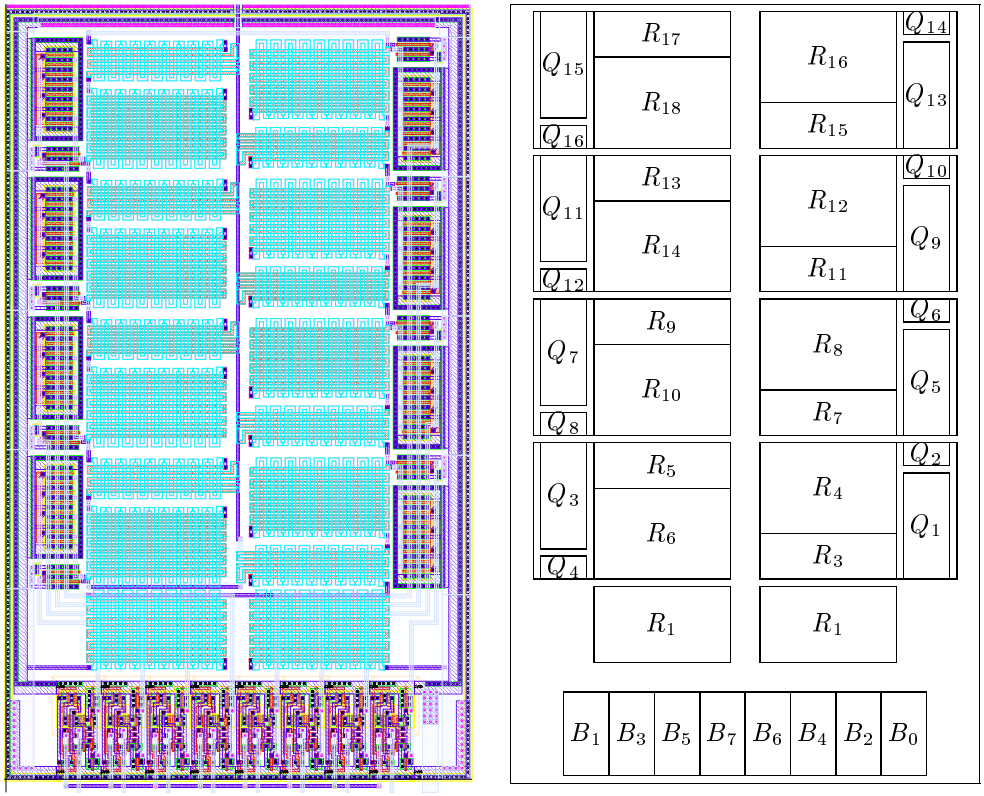


Figure 3.40: $R-2R$ ladder voltage DAC of the HELIX128-2.2's bias generator circuit. The layout is depicted on the left-hand side. The sketch on the right-hand side identifies the devices with the designators in fig. 3.39. B_i designates the latch and Q_{2i+1}, Q_{2i+2} the transistors of the inverter of the i^{th} bit. The area of the circuit is 218.0µm×361.5µm. The colour scheme of the layers is explained in fig. 4.1.

voltage). At minimum (*0x00* and *0xFF*) about 550µW are consumed, while the maximum power consumption occurs for "checkerboard patterned" numbers (*0x55* and *0xAA*) and reaches 1.8mW.

The Control Voltage Buffer Every (ohmic) load connected to the voltage DAC's output will, since in parallel with the MSB's "$2R$" resistor, deteriorate the linearity (cf. eq. 3.46). The DAC's internal resistance of about 9.7kΩ also limits its capability to drive loads and a voltage buffer has to be used to decouple the DAC from them.

each `SClk` cycle each `SClk` cycle The schematic of the voltage buffer is depicted in fig. 3.41. It is based on a design by A. Stellberger [Ste] and modified to meet the requirements of the HELIX128 chip. The buffer consists of a differential amplifier for each transistor of its push-pull output stage. The complementary differential amplifiers of the driver stage are fed by the input and the output of the amplifier and thus fix its gain to unity.

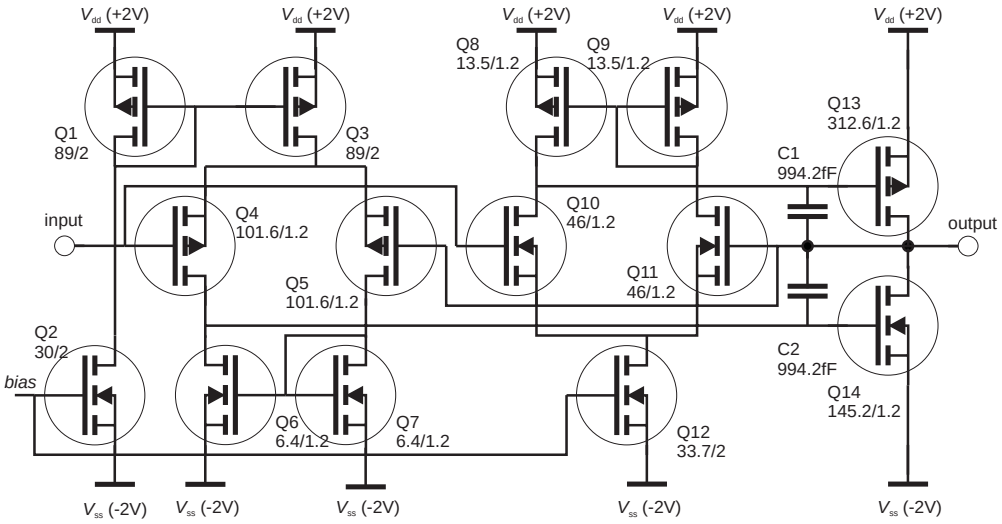


Figure 3.41: Buffer for the control voltages of the HELIX128-2.2.

The common source push-pull class A/B output stage has several advantages:

- The common source topology allows the voltage drop across the transistors to be $V_{\mathrm{DS}} < V_{\mathrm{th}}$ (for a source follower it has to be $V_{\mathrm{DS}} \geq V_{\mathrm{th}}$). This ensures a minimum impact on the dynamic range of the DACs as shown in fig. 3.43.
- Due to the class A/B operation an internal resistance of $R_{\mathrm{out}} \leq 58\Omega$ is achieved.

The layout of the voltage buffer is depicted in fig. 3.42.

Some of HELIX128's buffered control voltages connect to pads, which allow the attachment of blocking capacitors to further decrease the internal resistance. These connections also allowed the measurement of the buffered voltage DACs as shown in fig. 3.43. The dynamic range is decreased by $200 \ldots 300\mathrm{mV}$ at the power supply rails, while the nonlinearity in the usable range is $\Delta V_{\mathrm{out}} \leq 10\mathrm{mV}_{\mathrm{peak}}$ or $\leq 0.65\mathrm{LSB}$.

DACs for Bias Currents

The DACs providing bias currents for the different amplifier stages on HELIX128 are parallel converters using again the principle of a current mirror. Compared to the voltage DACs, the requirements are more relaxed:

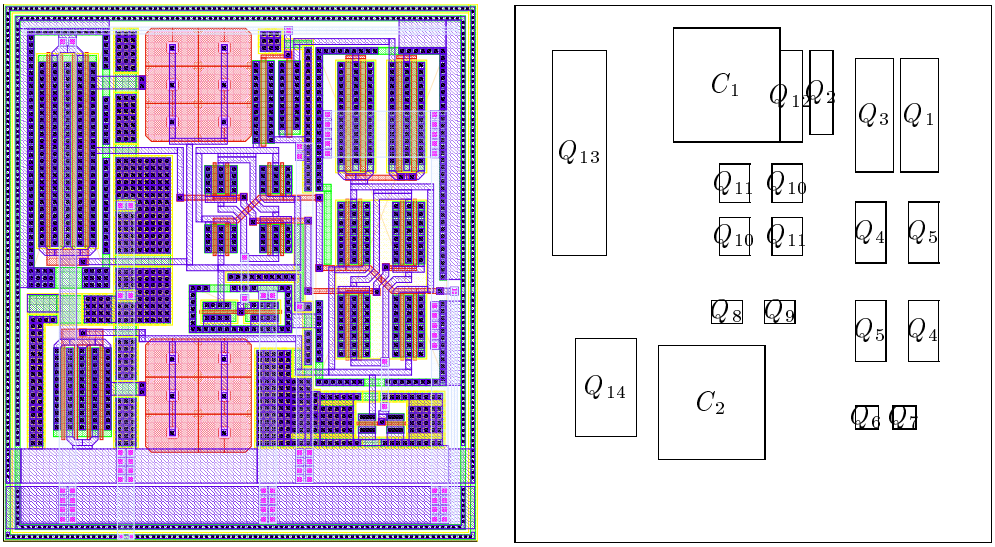


Figure 3.42: Layout of the buffer for the HELIX128-2's control voltages. The sketch on the right-hand side identifies the layout with the devices in fig. 3.41. The dimensions are 218.0µm×218.2µm. The colour scheme of the layers is explained in fig. 4.1.

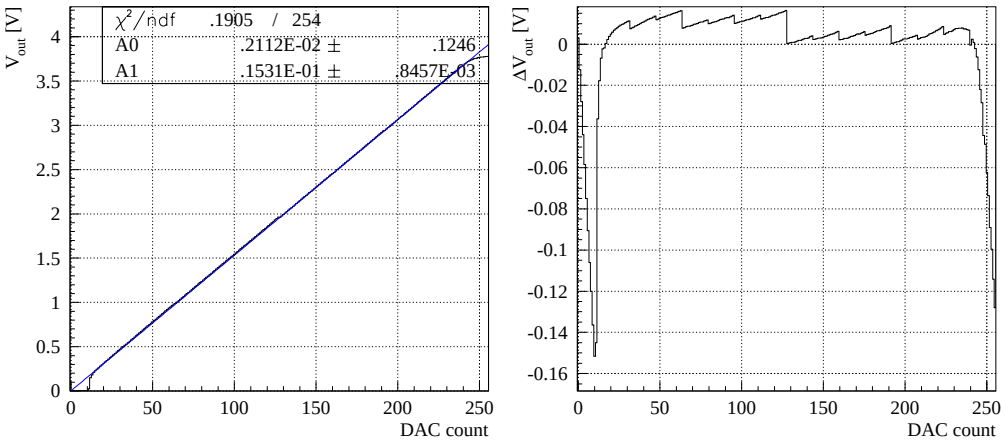


Figure 3.43: Linearity of the HELIX128-2.2's buffered $R-2R$ ladder voltage DACs. Left: Characteristic showing the restriction of the dynamic range by the buffer. Right: Nonlinearity. In the usable range the deviation is less than 10mV.

- A maximum current of about 400µA is required to exploit the capabilities of the preamplifier.
- A resolution $\leq$ 5µA is sufficient to adjust the low bias currents e.g. of the pipeline readout amplifier.
- No noise or clock feedtrough to prevent impairing effects on the amplifier stages, especially in the frontend.

At this point it should be mentioned that the amplifiers' transconductance g_m and their internal resistance only changes $\propto \sqrt{I_\mathrm{D}}$, which prevents exaggerated demands on the linearity.

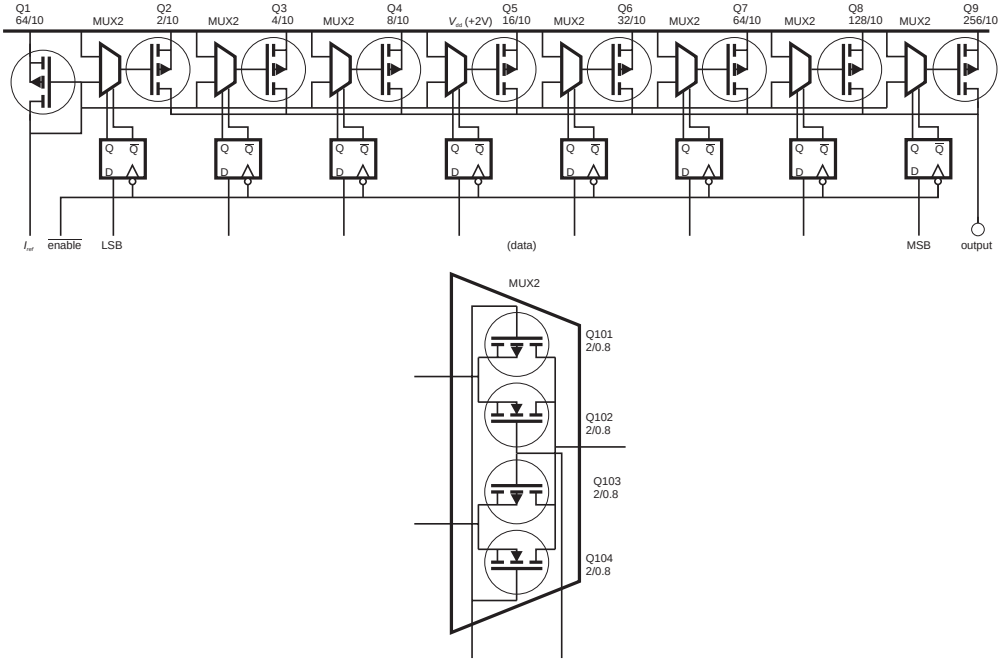


Figure 3.44: Current DAC of the HELIX128-2.2's bias generator circuit.

A DAC for one of the HELIX128's bias currents is depicted in fig. 3.44. It has to have a high internal resistance R_out to work as a current source, independent from the attached load, and therefore must also have a very low *Early Effect*[19]. The $\frac{W}{L} = \frac{10\mu\mathrm{m}}{2\mu\mathrm{m}}$ p-MOS transistor of the LSB delivers 2.5µA and fulfills this requirement in an excellent way as shown in fig. 3.45. This slope together with the implemented resolution of 8bits results in a dynamic range of 640µA.

The linearity of the circuit is again limited by the manufacturing process, and like for the voltage DACs, the accuracy of the MSB is the limiting factor. The dominating effects are the (effective) width W and the threshold voltage V_th of the transistor representing the LSB. Since the MSB consists of 2^{n-1} of these transistors, the condition for a strictly monotonous characteristic is $\sqrt{2^{n-1}}\Delta I_\mathrm{LSB} \leq I_\mathrm{LSB}$ and from eq. 4.5 we obtain:

$$\left|\frac{\Delta I_\mathrm{LSB}}{I_\mathrm{LSB}}\right| \approx \sqrt{\left(\frac{\Delta W_\mathrm{LSB}}{W_\mathrm{LSB}}\right)^2 + \left(\frac{2^{-n}\Delta V_\mathrm{th}}{V_\mathrm{GS} - V\mathrm{th}}\right)^2} \leq \sqrt{2^{1-n}} \qquad (3.47)$$

ΔW_LSB = variation in the width of a LSB transistor.

ΔV_th = variation of a LSB transistor's threshold voltage.

[19]Increase of $I_\mathrm{D} \propto V_\mathrm{DS}$ in the saturation region ($V_\mathrm{DS} > V_\mathrm{GS} > V_\mathrm{th}$, cf. eq. 4.4).

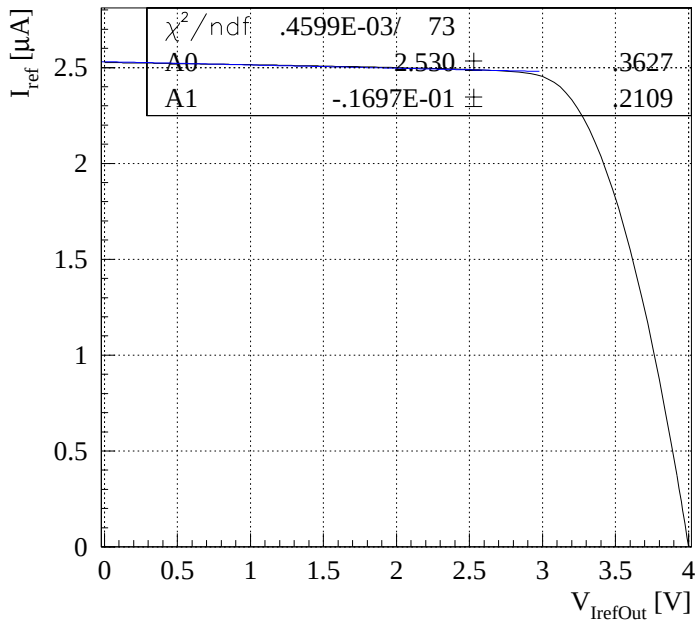


Figure 3.45: Output current of HELIX128-2's current DACs versus the voltage of the output node. The internal resistance of the DAC's LSB is 59MΩ (from the slope of the fit).

For the HELIX128's manufacturing process it is $\Delta V_{\mathrm{th}} \left(\frac{2\mu\mathrm{m}}{10\mu\mathrm{m}}\right) \leq 20\mathrm{mV}$, which can be neglected wrt. $\Delta W(W = 2\mu\mathrm{m}) = 0.05\mu\mathrm{m}$ [AMS95/1]. From this a strictly monotonous characteristic can be expected for resolutions of up to 11bits. However, since the LSB is only important when adjusting small currents (i.e. when the highest bit(s) are turned off), implementations with even higher resolutions are useful. The characteristics and nonlinearity of the circuit is shown in fig. 3.46.

In the layout of the circuit, which is depicted in fig. 3.47, it was attempted to obtain a (at least a sort of) "*common centroid*" arrangement of the transistors with the tightest spacing of the components permitted by the design rules [AMS97/1]. The higher bits are composed of the same transistor representing the LSB for best matching and linearity, which results in the "exotic" partitioning of the transistor array shown on the right-hand side of fig. 3.47.

Regarding radiation tolerance it should be mentioned that the transistors of the bits turned off during irradiation will show a threshold voltage shift slightly different from that of the bits turned on. This will result in a deterioration of the linearity, which has no impact on chip operation.

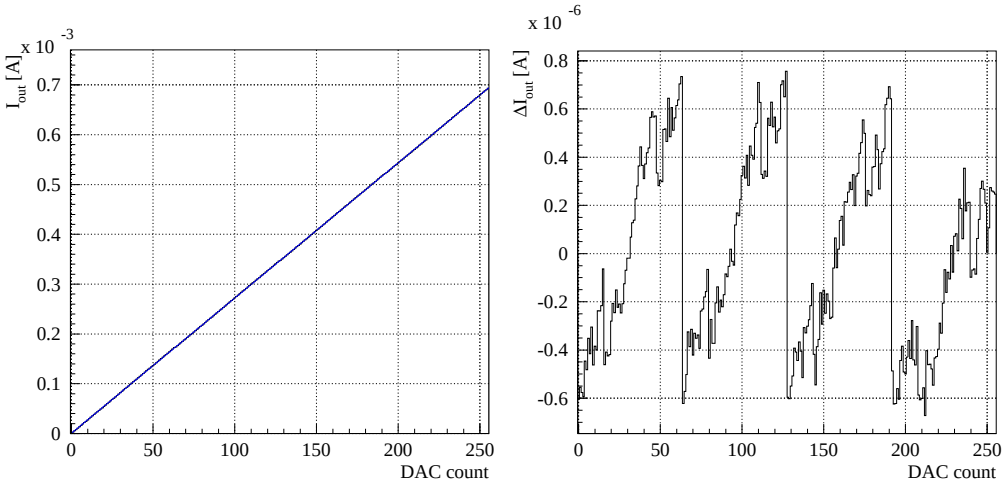


Figure 3.46: Linearity oft the HELIX128-2.2's current DACs. Left: Characteristics showing the dynamic range. Right: Nonlinearity, which is less than 0.75µA (0.3LSB) and obviously dominated by MSB-1 in this case.

The On-Chip Reference Current Source

On HELIX128-2 all bias currents are derived from a single reference current `IrefIn`. This current has to be independent from temperature and accumulated dose. Thus a radiation hard reference current source in a "radiation soft" process had to be developed and integrated on the HELIX128 chip.

The concept of the circuit was inspired by the textbook solution for a discrete precision current source [Tie93]: The voltage drop of the current across a resistor is compared to a reference voltage. However, due to the low power supply voltage and the dynamic range required, the resistor cannot be in the source path of the output transistor. To overcome this restriction, the circuit depicted in fig. 3.48 actually uses three current sources: Q_{11} generates the current through the reference resistor connected to `Rref`, Q_8 provides the bias current for the error amplifier and Q_{12} delivers the output current `IrefOut`.

The reference resistor on the original SUFIX chip was a polysilicon one, integrated on the chip. Despite the measured inaccuracy of the SUFIX' reference current of $\frac{\Delta I_{\mathrm{refOut}}}{I_{\mathrm{refOut}}} \leq 5\%$, it was replaced with an external resistor on HELIX128-2 since the process parameters [AMS97/2] guaranteed its absolute value only within a 60% tolerance.

The reference for the error amplifier consists of a simple voltage divider made of polysilicon resistors and is thus accurate within 0.4% [AMS91]. The voltage divider was chosen instead of a bandgap reference, which would be sensitive to (non-ionising) radiation damage (cf. chapt. 4). The disadvantage of this solution is the non-existent *PSSR*[20], which can be overcome by blocking the current output `IrefOut` (cf. appendix C).

The error amplifier is based on an operational amplifier designed by A. Stellberger [Ste], but was heavily modified for this application: The differential

[20] Power Supply Supression Ratio

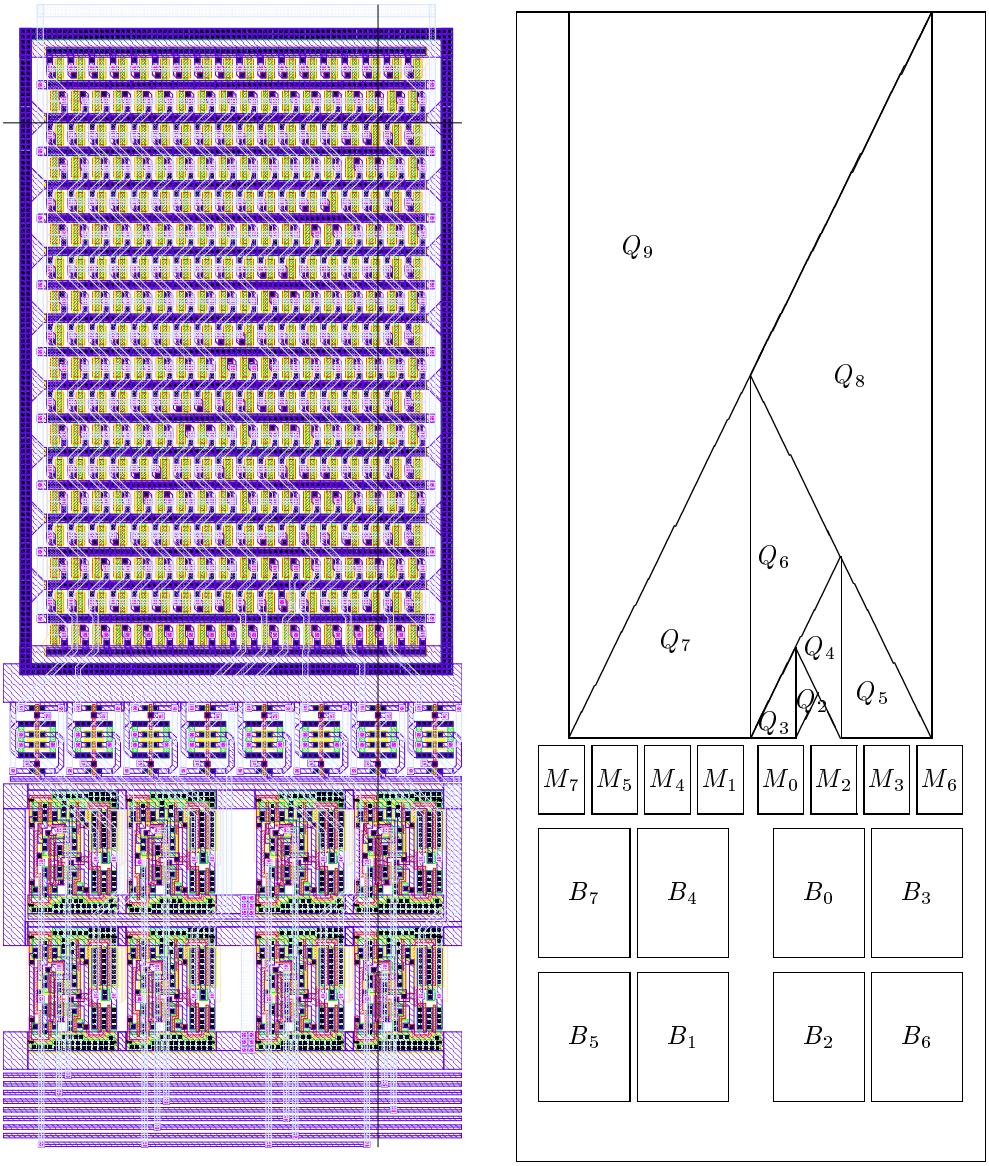


Figure 3.47: Layout of the current DACs in the HELIX128-2.2's bias generator circuit. The sketch on the right associates it with the device designations given in fig. 3.44 . M_i is the MUX2 and B_i the latch of the i^{th} bit in the layout. The size of the circuit is 243.6µm×609.5µm. The colour scheme of the layers is explained in fig. 4.1.

amplifier stage (Q_1, Q_2) and the low pass filter R_3C_1 had to be adapted to achieve stability at unity gain.

While the implementations of the current source on the SUFIX and the HELIX128-2.0 chips worked as expected, improvements in the manufacturing process caused problems on HELIX128-2.1, 2.2, 3.0 and 3.1, which could not be reproduced in the simulation of the circuit. These problems are described in detail in appendix E and were finally eliminated on the HELIX128-3.1a from

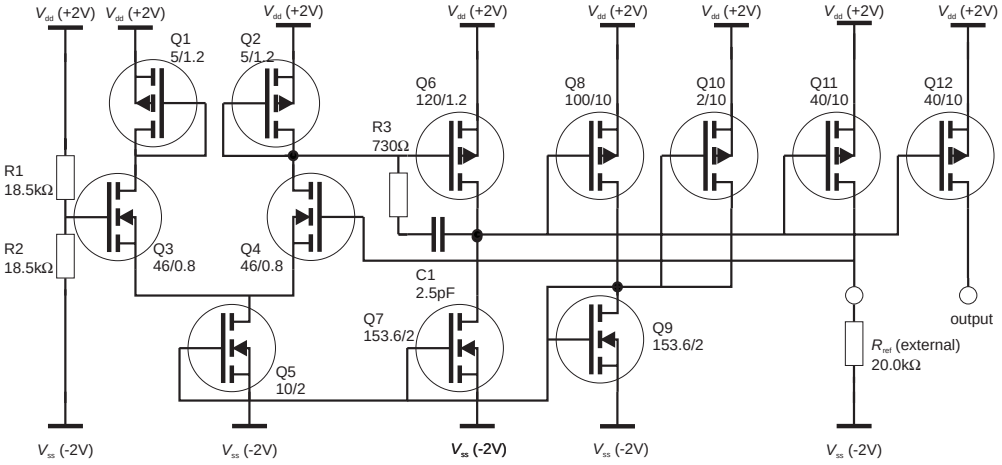


Figure 3.48: Schematic of the reference current source on HELIX128-3.1a.

which the schematic in fig. 3.48 was taken. Fig. 3.49 shows the layout of this circuit.

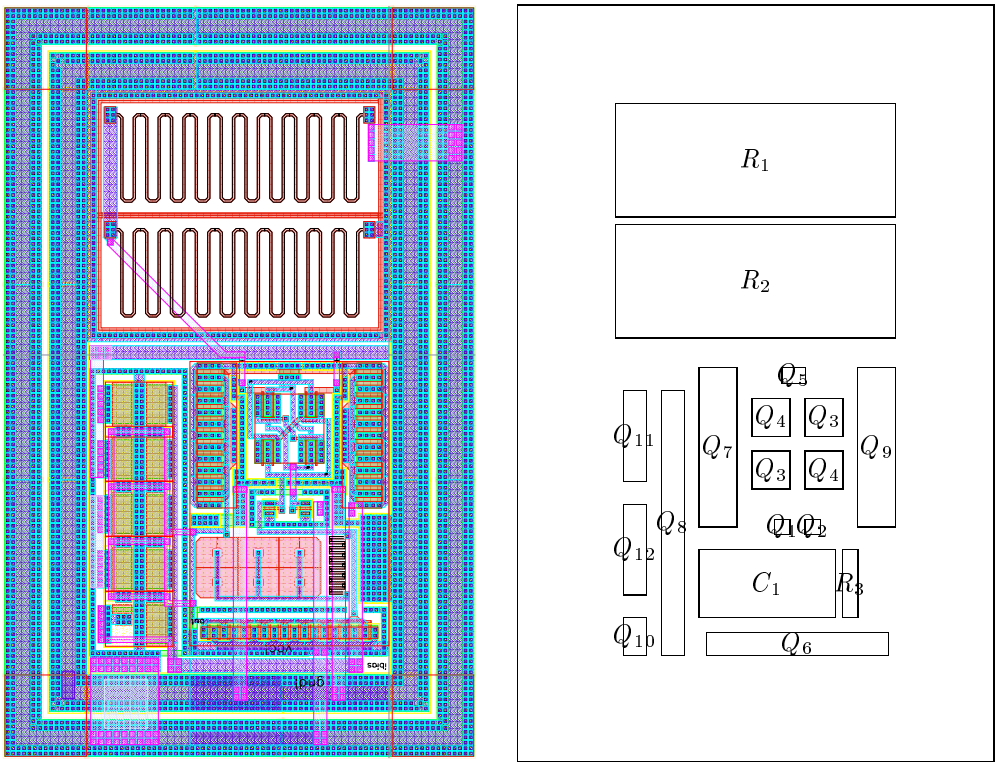


Figure 3.49: Layout of HELIX128-3.1a's reference current source (left). The sketch on the right identifies the devices with fig. 3.48. The size of the circuit is 241.5µm×386.5µm. The colour scheme of the layers is explained in fig. 4.1.

3.10.2 The Digital Control Circuits

The task of the digital control circuits is to provide HELIX128 with an interface to conveniently program the chips operational parameters. This is implemented as a serial interface, controlling the register based setup of the chip. Furthermore, the circuits to adjust or generate some digital control or monitoring signals were included. As for the pipeline control circuit, the schematic of this circuit was obtained by synthesising its functional description written in the *Verilog* HDL[21] (and explicitly listed in appendix F) with the digital standard cell library of the process used [AMS95/2]. The layout was automatically generated with *Cadence DFW II*'s *CellEnsemble* place-and-route tool. A schematic illustrating the different blocks of this circuit is depicted in fig. 3.50.

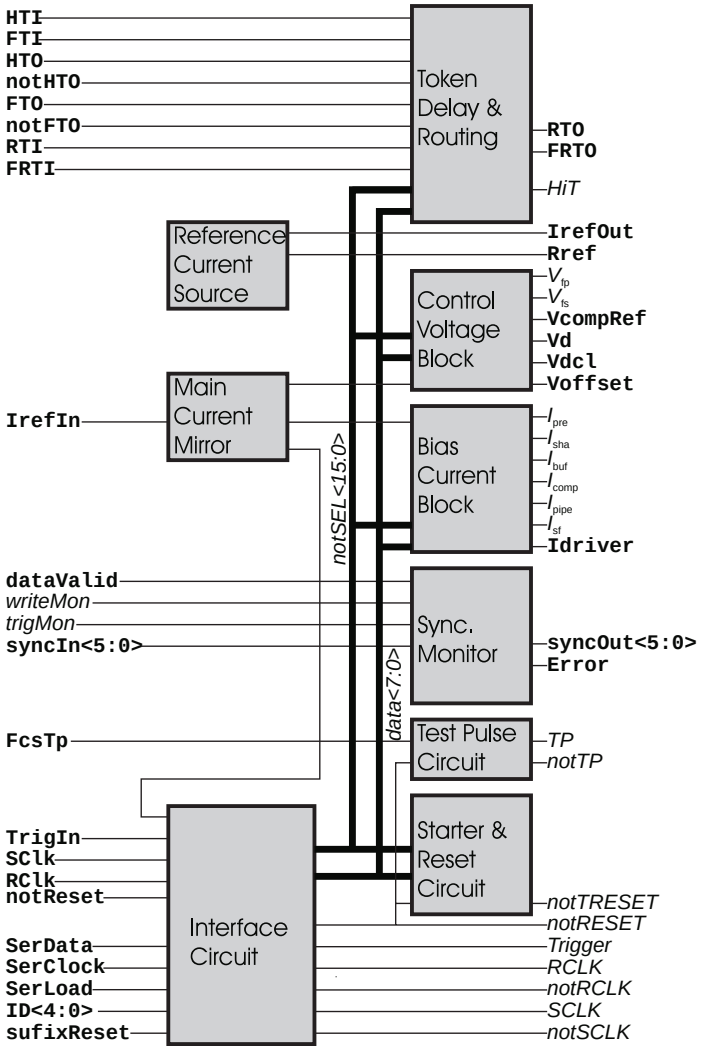


Figure 3.50: Block schematic of HELIX128-3's circuits in the bias generator, control and interface (*SUFIX*) part of the chip.

[21] Hardware Description Language

The Interface

The setup and operation mode of HELIX128-2 is defined by the contents of the 17 registers in the bias generator, control and interface (i.e. *SUFIX*) part of the chip, which are listed in tab. 3.3.

The programming of these registers is accomplished via a serial interface. The programing via a special trigger sequence adopted from the AP5-RH bias generator [Øde95] was dropped in favour of the capability to trigger subsequent events. On HELIX128-2.2 two of the interface lines were again merged: `SerClk` with `RClk` and `SerData` with `TrigIn`, i.e the trigger line is again used for programming, but this time without restricting the trigger functionality.

Based on a shift register, the interface uses 20 bit data frames. A frame consists of 8 data bits, a 5bit register address, a 6bit chip address and the *broadcast* (or *common set*) bit. The data is clocked into the interface in MSB-first order at the rising edge of `SerClk` and interpreted as programing data by pulling "high" `SerLoad` for one `SerClk` cycle. The chip address is determined by the levels of the six pads `ID<0>`...`ID<5>` and compared to the corresponding part of the data frame. If the chip address matches this part or the broadcast bit is set, the register address is decoded and the selected register latches the data. A programming sequence, including the structure of a data frame is shown in fig. 3.51.

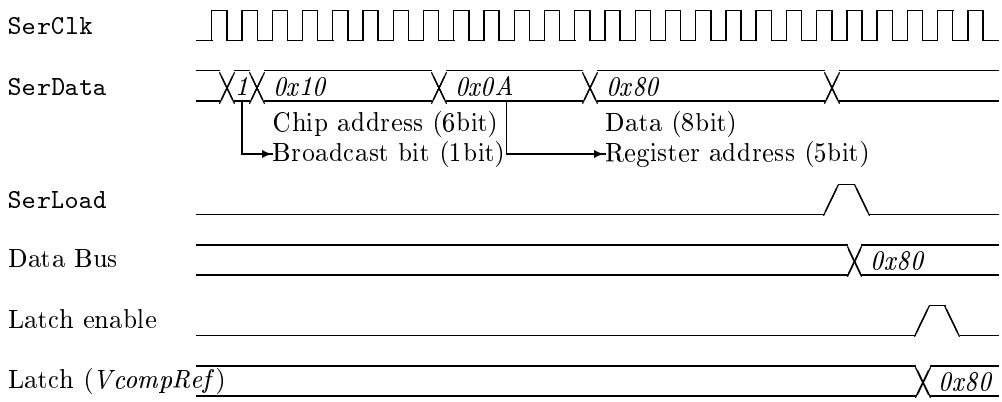


Figure 3.51: Interface and programming sequence of HELIX128–2. Data are clocked in MSB first. `SerClk` has to be replaced with `RClk` and `SerData` with `TrigIn` on HELIX128-2.2 and subsequent versions of the chip. If the chip or register addresses do not match, none of the "Latch enable" lines is activated.

The Initialisation and Reset Circuit (*Starter*)

The initialisation and reset circuit is in principle a simple counter: When the HELIX128's active low reset signal `notReset` is released, not only the "write" *incrementer* starts sampling data into the pipeline (cf. sect. 3.9.1), but also the starter counter, which is preset with the contents of the *latency* register, is counting down synchronously with the sampling clock `SClk`. Reaching zero,

the counter starts the "trigger" *incrementer* and the chip will accept triggers. The falling edge of `notReset` immediately stops both *incrementers*.

The *Token Delay* Circuit

The token delay circuit is another counter, which delays the return token before it is again fed to the readout sequencer of the first HELIX128 chip in a daisy chain. The maximum delay is 255 `RClk` cycles. Fig. 3.52 visualises the effect of the token delay circuit on the readout. It also generates an initial readout token, when `notReset` is pulled low. Also the switches for the fail safe token routing (cf. sect. 3.7.1), which are controlled by the upper 4 bits of the *ClkDiv* register, are included in this circuit. Their function is described in tab. 3.10.2.

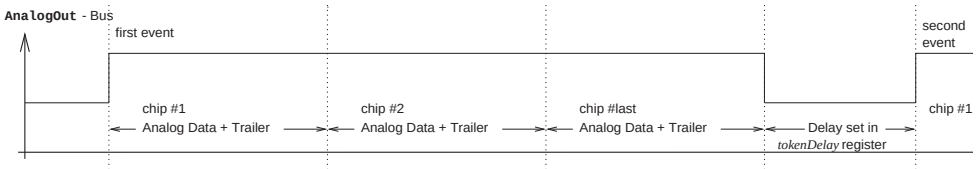


Figure 3.52: Pause between two subsequent readout bursts of HELIX128–2, which is inserted by the token delay circuit.

The *Internal SClk* Circuit (*ClkDiv*)

In many applications of the HELIX128 it is desirable to operate the chip with a minimum of clock signals and control lines. Reasons for that might be crosstalk or the number of vacuum feedtroughs. Since the readout frequency `RClk` should be an integer multiple of the sampling clock *SClk*, it was decided to implement a programmable clock divider to derive *SClk* from the readout clock. This avoids the noise and phase problems, sometimes associated with clock multiplying circuits.

Since a simple counter does not provide the required 50% duty cycle for odd clock ratios, a different concept was realised: The output signals of two counters, dividing RClk by $2 \cdot ClkDiv$ are XORed. The first counter starts three `RClk` cycles after `notReset` has been pulled low, since the sampling clock has to be running when `notReset` is released. The second counter, which is operated by the inverted `RClk` in case of odd clock dividers, starts with an additional delay of $\frac{ClkDiv}{2}$ `RClk` cycles. It should be mentioned that $\frac{ClkDiv}{2}$ is calculated by a bit shift operation, i.e. the result is truncated. The usage of the inverted `RClk` in case of odd divider numbers recovers the half clock cycle, which is lost in that case due to integer arithmetics. The operation of the clock divider circuit is visualised in fig. 3.53.

The Synchronicity Monitor (*SyncMon*)

The purpose of this circuit is to detect SEU failures (cf. sect. 4.6.1) within a group of HELIX128 chips in hardware. The circuit was already implemented

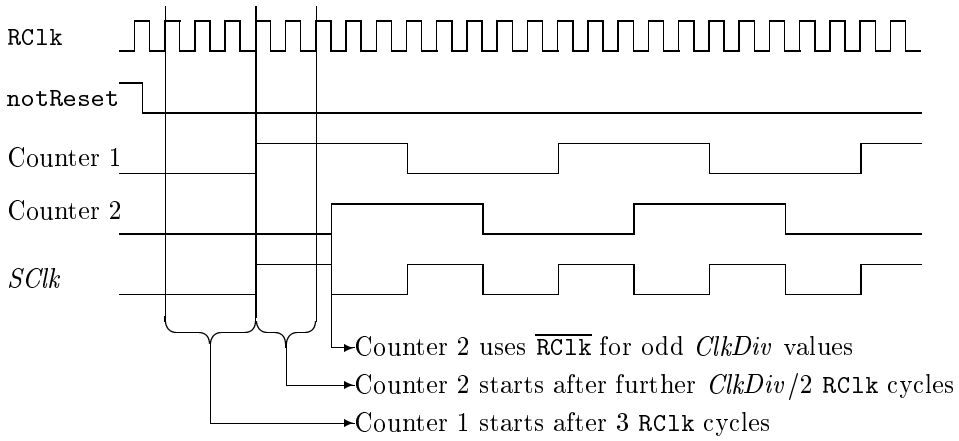


Figure 3.53: Principle of the HELIX128's internal *SClk* circuit.To divide `RClk` by *ClkDiv*, two counters are used. Both count up to *ClkDiv*, thus dividing `RClk` by 2· *ClkDiv*. To achieve a 50% duty cycle, the 2nd counter is delayed by *ClkDiv*/2 cycles and uses the inverted `RClk` (equalising the half cycle missing due to the integer division) for odd *ClkDiv* values.

on the original *SUFIX* chip, since the HELIX128-1 did not encode the pipeline address into the analogue readout. On HELIX128-2 the pipeline address is read out with the analogue data and similar checks can be performed in software.

The pipeline control circuit has three signals, which allow the monitoring of its operation: *TrigMon* and *WriteMon* are signals generated when the output of the corresponding *incrementer* is *0x00*. The third signal is `DataValid`, which is high whenever the chip sends analogue data. To detect SEU failures, the coincidence of these signals among a group of HELIX128 chips can be checked. To detect not only missing, but also excess signals, a logic *AND* as well as an (active low) *OR* of the signals is monitored. The connection to adjacent chips is established via the six `SyncIn<`*i*`>` and `SyncOut<`*i*`>` pads. The dependency of the signals, which is listed in tab. 3.5, is such that normal operation causes them to behave like differential signals, which reduces crosstalk and other disturbances. Fig. 3.54 shows the circuit to monitor one of the three signals.

The detection of the same logic level on both lines associated with the same monitor signal is flagged by the HELIX128's `Error` signal. However, only the `Error` signal of the last chip in a synchronicity chain has to be observed, since it recognises the errors of all "preceeding" ones. To facilitate debugging and gain usage of the synchronicity monitor and daisy-chained readout, which causes asynchronous occurrences of `DataValid`, the signals can be masked. The masking is set in the SyncReg register, whose contents are explained in tab. 3.6.

A nice side effect of the masking capabilities of the synchronicity monitor is the generation of a "*notDataValid*" signal for the length of the complete readout of all chips in a readout daisy-chain. It is available on the `SyncOut<4>` pad of the last chip in the corresponding synchronicity chain.

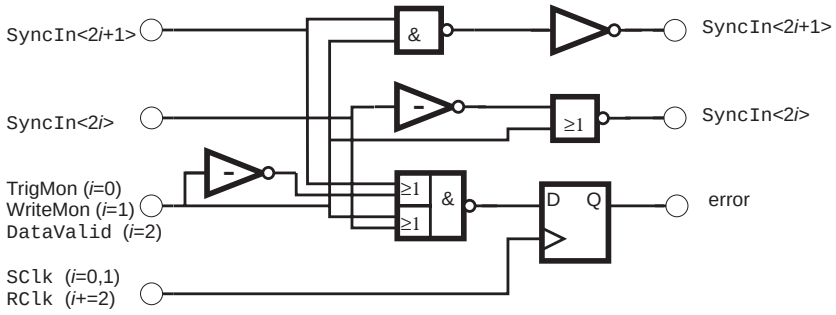


Figure 3.54: Synchronicity monitor module for one of the signals `DataValid`, *WriteMon* or *TrigMon*.

3.11 Other Circuits

3.11.1 The Test Pulse Circuit

To detect dead channels, either in the complete detector system, or during the wafer testing of the chips, it is mandatory to apply a defined stimulus to all channels. Unfortunately injecting of the same charge to all preamplifier channels is not feasible:

- The readout figure will, except for the offset, look the same with and without stimulus.
- The load on the power supply lines due to 129 simultaneously pulsed channels will cause a huge common mode signal.

To overcome this, an easily recognisable readout pattern, resulting from symmetrical charge injection of both polarities was chosen for the test pulse signal. The circuit that generates it is depicted in fig. 3.55. The capacitors C_1 together with $C_3, C_4, C_7, C_8 \ldots C_{131}$ and C_2 together with $C_5, C_6, C_9, C_{10} \ldots C_{130}$ form capacitive voltage dividers (ratio $= \frac{1}{1.03 \cdot 10^3}$), since the amplifier inputs are on a virtual ground potential. The charges injected on each transition of the FlipFlop therefore are $\approx 48 \cdot 10^3 \mathrm{e}^-$ (200fF) and $\approx 24 \cdot 10^3 \mathrm{e}^-$ (99.7fF), while the sequence of the capacitors results in a staircase-like readout pattern depicted in fig. 3.56. Due to the FlipFlop, the polarity of the pattern toggles every time a test pulse is applied by a signal on the `fcsTP` pad.

It should be denoted that, despite the symmetric charge injection, the quadratic characteristic of the preamp's input transistor still results in a major change in the power supplies' load. Thus it is not advised to use the test pulse for calibration purposes.

3.11.2 The LVDS Receiver Circuit

HELIX128-2.0 and 2.1 used differential CMOS-level signals for the readout clock `RClk`, the sampling frequency `SClk`, the trigger comparator clock `CompClk` and the trigger signal `TrigIn`. These signals caused crosstalk to the analogue signals via coupling paths outside the chip. Especially the impact of `CompClk` on

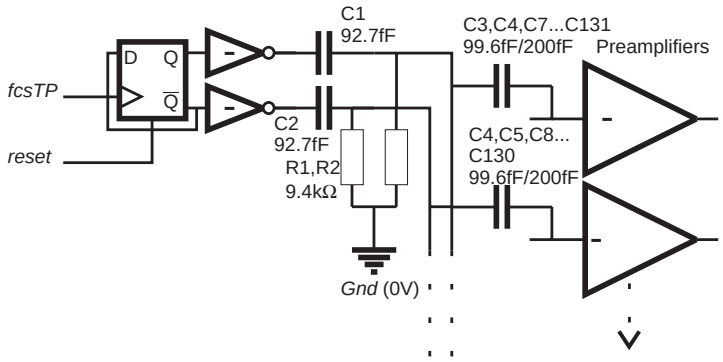


Figure 3.55: Test pulse circuit of HELIX128-3.0.

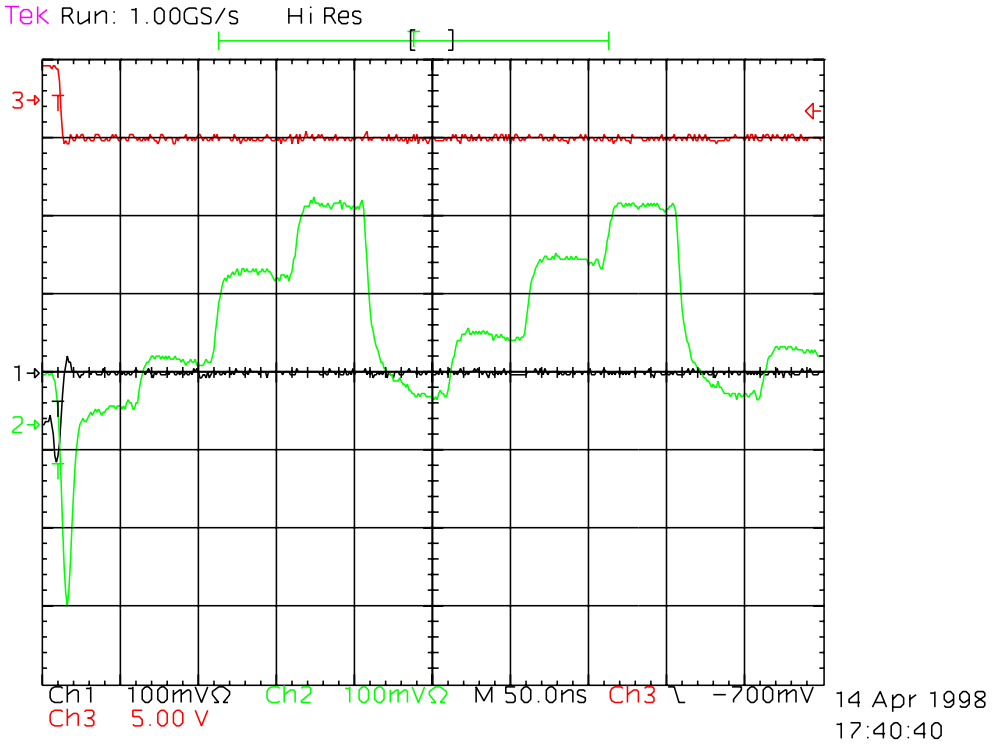


Figure 3.56: Section of HELIX128-2's readout figure with a test pulse applied.

the frontend and of `RClk` on the `AnalogOut` and `AnalogOutDummy` lines (cf. appendix B.1, E) had to be removed. Therefore HELIX128-2.2 uses LVDS[22] levels for these signals. The necessary receivers are based on a design by NIKHEF [Slu97] and were modified for current mirror biasing by R. Kluit [Klu]. This modification was necessary for radiation tolerance reasons, since the input stage in the schematic depicted in fig. 3.57, is actually an analogue circuit. Fig. 3.58 shows the layout of the circuit.

[22] Low Voltage Differential Signaling [LVD97].

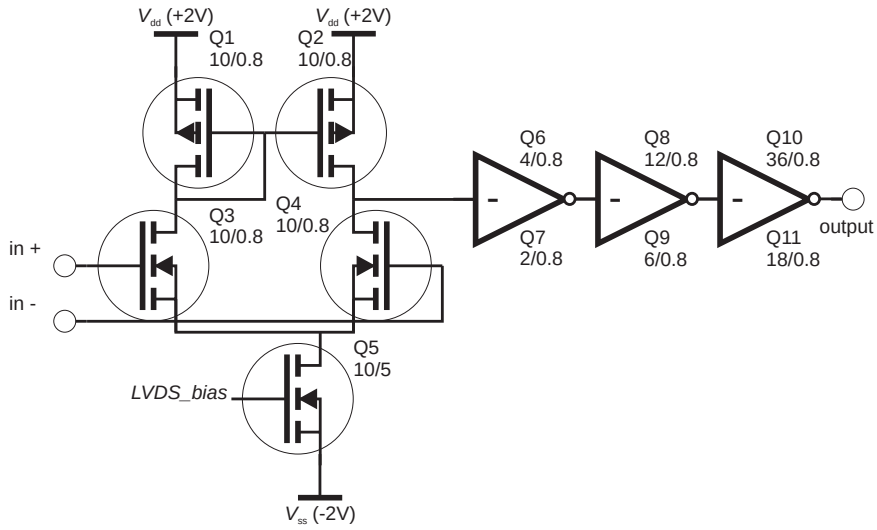


Figure 3.57: LVDS receiver for the digital signals of HELIX128-2.2.

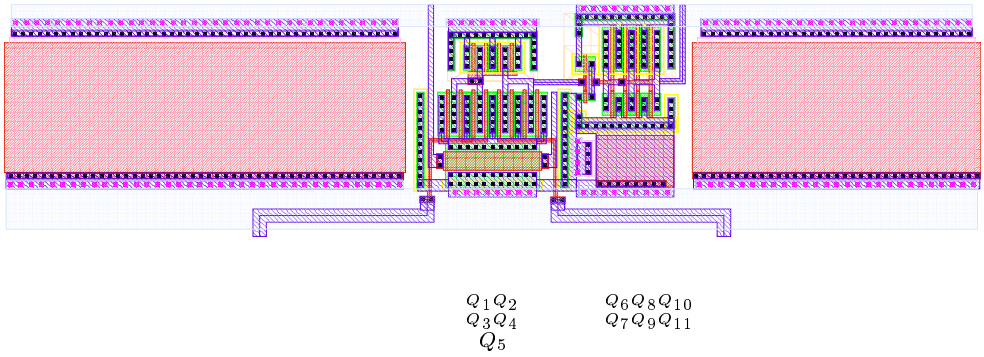


Figure 3.58: Layout of an LVDS receiver for the digital signals of HELIX128-2.2 [Klu]. The capacitors right and left of the circuit decouple the power supply of the differential amplifier from other digital circuits. The designators identify the devices with fig. 3.57. The area of the circuit is 260µ×63µm. The colour scheme of the layers is explained in fig. 4.1.

Register address (*HEX*)	(*BIN*)	(*DEC*)	Register name	Function	Range and step size
01	00001	01	*Ipre*	Charge amplifier bias current	0...640µA, 2.5µA/LSB
02	00010	02	*Isha*	Shaper bias current	0...640µA, 2.5µA/LSB
03	00011	03	*Ibuf*	Frontend buffer bias current	0...640µA, 2.5µA/LSB
04	00100	04	*Icomp*	Discriminator bias current	0...640µA, 2.5µA/LSB
05	00101	05	*Ipipe*	Pipeline readout amplifier bias current	0...640µA, 2.5µA/LSB
06	00110	06	*Isf*	Multiplexer source follower bias current	0...640µA, 2.5µA/LSB
07	00111	07	*Idriver*	Output current driver bias current	0...640µA, 2.5µA/LSB
08	01000	08	*Vfp*	Charge amplifier feedback control voltage	−2...2V, 15.6mV/LSB
09	01001	09	*Vfs*	Shaper feedback control voltage	−2...2V, 15.6mV/LSB
0A	01010	10	*VcompRef*	Comparator threshold voltage	−200...200mV, 1.56mV/LSB
0B	01011	11	*Vd*	Pipeline readout line reset voltage	−2...2V, 15.6mV/LSB
0C	01100	12	*Vdcl*	Pipeline readout amplifier source node voltage	−2...2V, 15.6mV/LSB
0D	01101	13	*Voffset*	Output current driver offset control voltage	−2...2V, 15.6mV/LSB
11	10001	17	*Latency*	L1 trigger latency (used storage depth of the pipeline)	(0...255 + 1) `SClk` cycles
12	10010	18	*SyncReg*	Synchronicity monitor operation mode	n.a.
13	10011	19	*ClkDiv*	Internal *SClk* divider and token routing	0...15 `RClk` cycles (0 = ext. `SClk` signal), upper 4 bits for token routing
14	10100	20	*TokenDelay*	Pause between subsequent readout bursts	0...255 `RClk` cycles

Table 3.3: Helix128-2's internal register map. The addresses *0x00* and *0x1F* are not used since they are prone to being overwritten by spurious `SerLoad` signals.

Bitname	Explanation	Number
BypassHelixToken	If 0 then `HelixTokenIn` is activated, if 1 then `FailsafeHelixTokenIn` is activated	4
BypassReturnToken	If 0 then `ReturnTokenIn` is activated, if 1 then `FailsafeReturnTokenIn` is activated	5
LastInChain	Connects `HelixTokenOut` to the return token path. If this chip is the last in the chain, this bit must be set to 1	6
FirstInChain	Connects the return token path to the token delay circuit. If this chip is the first in the chain, this bit must be set to 1	7

Table 3.4: Definition of fail safe token control bits, the upper 4 bits in the *ClkDiv* register.

signal name	logic dependency	comment
`SyncOut<0>`	!*TrigMon* & `SyncIn<0>`	*active low or* of all *TrigMon* signals
`SyncOut<1>`	*TrigMon* & `SyncIn<1>`	*and* of all *TrigMon* signals
`SyncOut<2>`	!*writeMon* & `SyncIn<2>`	*active low or* of all *TrigMon* signals
`SyncOut<3>`	*writeMon* & `SyncIn<3>`	*and* of all *writeMon* signals
`SyncOut<4>`	!`DataValid` & `SyncIn<4>`	*active low or* of all `DataValid` signals
`SyncOut<5>`	`DataValid` & `SyncIn<5>`	*and* of all `DataValid` signals

Table 3.5: Dependencies of the `SyncIn<5:0>` and `SyncOut<5:0>` signals

bit number	function if cleared (*0*)	function if set (*1*)
7 (MSB)	`Error` pin in latch mode (i.e. signal remains high after occurrence of an error	`Error` pin in transient mode (i.e. it becomes active only during the existence of an error condition)
6	`Error` signal is generated from `Sync<0:1>` (i.e. *TrigMon*) signals	`Sync<0:1>` (i.e. *TrigMon*) is ignored for the `Error` signal
5	`Error` signal is generated from `Sync<2:3>` (i.e. *WriteMon*) signals	`Sync<2:3>` (i.e. *WriteMon*) is ignored for the `Error` signal
4	`Error` signal is generated from `Sync<4:5>` (i.e. `DataValid`) signals	`Sync<4:5>` (i.e. `DataValid`) is ignored for the `Error` signal
3	`SyncOut<0:1>` signal is generated from `SyncIn<0:1>` and *TrigMon* signals	`SyncOut<0:1>` = `SyncIn<0:1>` (i.e. *TrigMon* of this Helix128-2 does not contribute to `SyncOut<0:1>`)
2	`SyncOut<2:3>` signal is generated from `SyncIn<2:3>` and *WriteMon* signals	`SyncOut<2:3>` = `SyncIn<2:3>` (i.e. *WriteMon* of this Helix128-2 does not contribute to `SyncOut<2:3>`)
1	`SyncOut<4:5>` signal is generated from `SyncIn<4:5>` and `DataValid` signals	`SyncOut<4:5>` = `SyncIn<4:5>` (i.e. `DataValid` of this Helix128-2 does not contribute to `SyncOut<2:3>`)
0 (LSB)	`Error` = *0* (i.e. reset `Error`, only useful if bit #7 = *0*)	`Error` = *1* (i.e. set `Error`, only useful if bit #7 = *0*)

Table 3.6: Flags of the *SyncReg* register

Chapter 4

Radiation Damage in CMOS Structures

In 1962 the *TelstarI* communications satellite failed due to the damage its circuits took from the radiation in the Van Allen Belt. This unpleasant experience promoted radiation effects in semiconductor devices to an active field of research. Besides for aerospace applications, radiation hardened electronics are mainly required for advanced weaponry, since the radiation pulse of a thermonuclear explosion causes similar effects, and thus research was mainly driven (as well as hampered) by military interests.

The increasing density of VLSI[1] circuits, causing a higher sensitivity for transient radiation effects and the integration of electronics on radiation sensors, especially for medical and high energy physics applications, resulted in a civil, i.e. aerospatial, automotive, medical and physics, demand for radiation hardened electronics.

In CMOS integrated circuits, the active devices are located on the wafer surface and thus will experience effects similar to radiation damage already within their manufacturing process.

4.1 CMOS Manufacturing Process

The most common principle for nowadays VLSI integrated circuits is Complementary Metal-Oxide-Semiconductor (CMOS) technology, sometimes also called twin-well MOS processes. The term "MOS" originates from the order of layers forming an active device (field effect transistor): A metal gate[2] is isolated by a silicon oxide layer from the channel on the surface of the semiconductor material.

As the name CMOS implies, the available active devices are n-channel and p-channel field effect transistors (FETs). Passive components are limited to diffusion and polysilicon resistors as well as (nonlinear) gate capacitors. Additional devices can be implemented with further process steps. The AMS CYE

[1] Very Large Scale Integration.

[2] present silicon processes use polysilicon gates instead of metal. Metal gates are still used e.g. in GaAs technology

0.8µm CMOS process used for the HELIX128 chip e.g. offers two metal layers and a second polysilicon layer, the latter to implement linear capacitors composed of the two polysilicon layers [AMS97/1][3].

4.1.1 Process Steps

There are several techniques to implant or deposit the various layers of a CMOS circuit, which are combinations from some of the following five basic processing steps [Ale87]:

Oxidation: The wafer is exposed to an atmosphere of pure oxygen or water vapor at $\approx 1000°C$. A SiO_2 layer will grow on top and into the silicon in equal shares. SiO_2 is used as an insulator or dielectric between all conductive layers and as a mask to apply other (esp. implanted) layers.

Doping: n- or p-doped implants can be placed in the bulk material with different techniques:

Diffusion: The wafer is exposed to the vapor of the donor or acceptor material. A thin layer of this material will deposit on the wafer surface. In the subsequent *Drive In* step the impurities will diffuse into the bulk material.

Ion Implantation: Ions of the doping material are accelerated towards the wafer by an electric field. The wafer acts as a cathode and the impurities become embedded underneath its surface. The doping profile depends on the ion's velocity and can be further modified in a subsequent *Drive In* step. The ions also cause crystal damage, which has to be annealed at temperatures around 800°C.

The so-called *Drive In* process is the last step in the doping process: The wafer is heated following a well-defined temperature curve and the final doping profile is established by diffusion of the impurities.

Deposition is used to create layers on top of the wafer's surface. The technologies available are:

Chemical Vapor Deposition (CVD): The wafer is exposed to an atmosphere of Silane (SiH_4, creating a Polysilicon layer), ammonium (NH_3, creating silicon nitride Si_3N_4) or a mixture of Silane and oxygen (creating SiO_2). The layers grown on the wafer surface have an amorphous structure.

Epitaxy is used to grow monocrystallic layers. The process is similar to CVD, except that the wafer is heated to $\approx 1000°C$ during deposition, which allows a reorientation of the deposited material.

Vacuum Deposition is mainly used for metal layers. The layer's material is evaporated in a vacuum chamber and precipitates on the

[3] In some processes, it is even possible to include mechanical structures on top of a wafer. E.g. acceleration sensors for automotive applications use this technology.

wafer surface. An electric field can be used to increase the efficiency of the deposition.

Sputtering is a very special form of electrostatic deposition: Negative ions are knocked off a cathode made of the deposition material by means of an (positive) ion beam. The wafer surface acts as an anode that collects the material.

Etching: To remove unwanted material, like masks no longer needed, from the wafer surface, etching is used.

Wet Etching uses fluid inorganic acids like HF or H_3PO_4.

Plasma Etching uses an ionised gas instead. A big advantage of this technique is the absence of residual acid on the wafer's surface.

Photolithography: The masks for subsequent process steps are generated by photolithography, using either positive or negative lacquer. The exposure of the photosensitive layer with UV light is done with *stepper devices*. These work in principle like a slide projector, except that the layout image on the *reticle* (i.e. the slide) is shrunk instead of magnified. The exposed area is usually that of a single die, and thus the exposure of the wafer is performed in several steps.

The cross section of a wafer manufactured in a CMOS process is shown in fig. 4.1.

The manufacturing process starts with the oxidation of the complete wafer. In this oxide layer the windows for the well diffusion are etched, the corresponding material is deposited and driven in.

In the next step the *active area* mask is applied and, after etching away all unwanted layers, the gate oxide is grown. This step has to take place in an early stage of the process to achieve a good quality of the gate oxide–silicon interface. This is crucial for device matching and noise performance.

The first polysilicon layer is usually deposited immediately after the gate oxide. This again improves matching and noise performance by a smooth interface between gate oxide and the polysilicon gate. In some processes the polysilicon gate serves as a self aligned mask for the subsequent n- and p-implantation steps, which further improves transistor matching.

If the subsequent implantation of the drain and source area is done by ion implantation, charges are trapped in the gate oxide – an effect also known from radiation. Some manufacturers even use dedicated doping steps for gates and gate oxides. Thus it is possible to implement transistors with almost arbitrary threshold voltage levels.

In the following steps the 2^{nd} polysilicon layer, the two metal layers and the vias in-between them (if applicable) are deposited.

The last layer is the passivation, which covers the complete wafer, except for the bonding pads. It protects the chip from mechanical damages and corrosion.

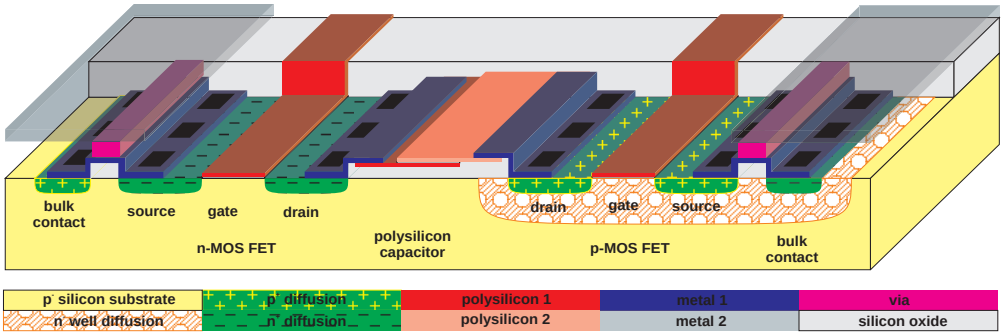


Figure 4.1: Wafer cross section of a CMOS double metal double poly process with tungsten vias. The colours of n^+, p^+, n-tub, poly-1, poly-2, metal-1, via, metal-2 and the contacts match the colours in the circuit layouts. The silicon oxide is partly removed to reveal the devices.

4.2 MOS transistor characteristics

A MOS field effect transistor[4] consists of two heavily doped regions called *drain* and *source*, separated by an area lightly doped with the opposite charge carriers. Above this *channel* area the isolated *gate* electrode is located, as it is shown in fig. 4.1.

Connecting all three electrodes to the potential of the substrate (or n-well in case of the p-MOS FET), a depletion region is formed between the heavily doped drain and source areas and the oppositely doped surrounding material.

Applying a positive voltage to the gate electrode of the n-MOS transistor[5] collects negative charges in the surface layer underneath the gate oxide. To compensate all charges in this surface layer, a voltage of

$$V_{\mathrm{th}} = -\frac{\rho_{\mathrm{CC}} q_{\mathrm{CC}}}{C_{\mathrm{Gox}}}. \tag{4.1}$$

ρ_{CC} = (majority) charge carrier concentration in the surface layer due to the doping [m^{-2}]

q_{CC} = charge of the carriers [C]

$C_{\mathrm{Gox}} = \frac{\varepsilon_{\mathrm{ox}}}{d_{\mathrm{ox}}}$ = specific capacitance of the gate oxide [$\mathrm{F/m}^2$]

is required, i.e. with V_{GS} reaching V_{th} the collected electrons compensate the charge of the holes in a layer of infinitesimal thickness underneath the gate oxide.

A further increase of V_{GS} results in the build-up of an n-conductive *channel* in that area. This state is also called strong inversion.

Since the sheet resistance of a majority charge carrier layer is defined as $r_{\mathrm{A}} = \frac{1}{\mu_Q \rho_Q q_Q}$ (with μ_{Q} the mobility and ρ_Q the effective surface density of the charge carriers of charge q_Q), we end up with:

[4]We will restrict this discussion to enhancement transistors only. The drain current of enhancement FETs is cut of for $V_{\mathrm{GS}} = 0$, while depletion FETs are conducting for $V_{\mathrm{GS}} = 0$.

[5]We will restrict this discussion to n-MOS transistors. For p-MOS FETs n- and p-diffusion have to be reversed as well as the signs (directions) of voltages and currents.

$$R_{\mathrm{DS}}|_{V_{\mathrm{DS}}=0} = \frac{L_{\mathrm{eff}}}{W_{\mathrm{eff}}} \frac{1}{\mu C_{\mathrm{Gox}} (V_{\mathrm{GS}} - V_{\mathrm{th}})} \tag{4.2}$$

W_{eff} = effective width of the transistor [µm]

L_{eff} = effective length of the transistor [µm]

R_{DS} = Drain resistance [Ω]

$\overline{\mu}$ = effective mobility of the charge carriers [$\mathrm{m}^2/(\mathrm{Vs})$]

Assuming a linear voltage drop across the channel for $0 < V_{\mathrm{DS}} < (V_{\mathrm{GS}} - V_{\mathrm{th}})$, the $(V_{\mathrm{GS}} - V_{\mathrm{th}})$ term in eq. 4.2 has to be replaced with $\frac{V_{\mathrm{GS}}-V_{\mathrm{th}}}{2} + \frac{V_{\mathrm{GS}}-V_{\mathrm{th}}-V_{\mathrm{GS}}}{2} = \frac{2(V_{\mathrm{GS}}-V_{\mathrm{th}})-V_{\mathrm{DS}}}{2}$.

With V_{DS} exceeding $(V_{\mathrm{GS}} - V_{\mathrm{th}})$, the channel vanishes at $x = L\frac{V_{\mathrm{GS}}-V_{\mathrm{th}}}{V_{\mathrm{DS}}}$, i.e. usually near the drain area. The voltage at the channel's end therefore is $(V_{\mathrm{GS}} - V_{\mathrm{th}})$, while the effective gate voltage is $\frac{V_{\mathrm{GS}}-V_{\mathrm{th}}}{2}$. Substituting this into eq. 4.2, we end up with

$$I_{\mathrm{DS}} = \frac{W_{\mathrm{eff}}}{L_{\mathrm{eff}}} \frac{\mu C_{\mathrm{ox}}}{2} (V_{\mathrm{GS}} - V_{\mathrm{th}})^2 , \tag{4.3}$$

i.e. the drain current becomes independent from V_{DS} and the FET operates in the *saturation region.*

At second sight, one notices that the inverted channel region still has a finite resistance and thus the electric field between drain and source will affect the charge carrier distribution in the channel. This gives rise to a small contribution to I_{DS}, linearly increasing with $\frac{V_{\mathrm{DS}}}{L_{\mathrm{eff}}^2}$. The phenomenon is called *Early Effect* and is in most respects similar to the grid emission transparency found in electron valves.

Putting eqs. 4.2 and 4.3 together and including the Early Effect, we arrive at the large signal model of a FET:

$$I_D = \begin{cases} 0 & V_{\mathrm{GS}} < V_{\mathrm{th}} \\ \frac{W_{\mathrm{eff}}}{L_{\mathrm{eff}}} \frac{\overline{\mu} C_{\mathrm{Gox}}}{2} \left[2 \left(V_{\mathrm{GS}} - V_{\mathrm{th}} \right) V_{\mathrm{DS}} - V_{\mathrm{DS}}^2 \right] & V_{\mathrm{GS}} > V_{\mathrm{th}}, V_{\mathrm{DS}} < \left(V_{\mathrm{GS}} - V_{\mathrm{th}} \right) \\ \frac{W_{\mathrm{eff}}}{L_{\mathrm{eff}}} \frac{\overline{\mu} C_{\mathrm{Gox}}}{2} \left(V_{\mathrm{GS}} - V_{\mathrm{th}} \right)^2 \left(1 + \lambda V_{\mathrm{DS}} \right) & V_{\mathrm{GS}} > V_{\mathrm{th}}, V_{\mathrm{DS}} > \left(V_{\mathrm{GS}} - V_{\mathrm{th}} \right) \end{cases} \quad (4.4)$$

W_{eff} = effective width of the transistor [µm]

L_{eff} = effective length of the transistor [µm]

I_{D} = Drain current [A]

$\overline{\mu}$ = effective mobility of the charge carriers ($\overline{\mu}_{\mathrm{n}} \approx 450\mathrm{cm}^2/(\mathrm{Vs})$ $\overline{\mu}\mathrm{p} \approx 150\mathrm{cm}^2/(\mathrm{Vs})$)

C_{Gox} = specific capacitance of the gate oxide ($C_{\mathrm{Gox}} \approx 2\mathrm{fF}/\mu\mathrm{m}^2$)

V_{GS} = gate–source voltage [V]

V_{DS} = drain–source voltage [V]

V_{th} = threshold voltage [V]

$\lambda = \frac{1}{L_{\mathrm{eff}} \sqrt{(V_{\mathrm{DG}} - V_{\mathrm{T}}) N_{\mathrm{imp}}}}$ = slope of the *Early Effect* [1/V]

For small signal calculations (i.e. using linear approximation of the devices' characteristics), the transconductance $g_{\mathrm{m}} = \frac{d\ I_{\mathrm{DS}}}{d\ V_{\mathrm{GS}}}$ is a more convenient quantity:

$$g_{\mathrm{m}} = \frac{W_{\mathrm{eff}}}{L_{\mathrm{eff}}} \overline{\mu} C_{\mathrm{Gox}} \left(V_{\mathrm{GS}} - V_{\mathrm{th}} \right) \quad (4.5)$$

$$g_{\mathrm{m}} = \sqrt{2 \frac{W_{\mathrm{eff}}}{L_{\mathrm{eff}}} \overline{\mu} C_{\mathrm{Gox}}} \sqrt{I_{\mathrm{D}}} \quad (4.6)$$

4.3 Ionising Damage

The predominant cause for radiation induced degradation of MOS devices is ionisation, resulting in broken bonds and atom relaxation in the surface layer and trapped charges in the silicon oxide. Fig. 4.2 gives an overview of the processes caused by ionising radiation, while tab. 4.1 (at the end of this chapter) summarises all radiation induced effects in semiconductors. To some extent, CMOS devices will experience defects of this kind already during their manufacturing process.

Ionising radiation passing through silicon generates electron/hole pairs ($\approx$ 110 per µm path length for a *MIP*, as pointed out in sect. 2.2). But the charge carriers generated this way usually recombine again, e.g. when they leave the depleted area of a silicon detector. However, a few of the charge carriers generated near the surface of the silicon or in the silicon oxide on top of it will be trapped and in turn deteriorate the properties of MOS devices located there.

It should be denoted, that wrt. ionisation the effects of electromagnetic radiation and charged particles are more or less equivalent. In principle it is

$$3 \times 10^{12}\, MIP/\mathrm{cm}^2 \hat{=} 1\mathrm{kGy}. \quad (4.7)$$

wrt. to the inflicted ionising radiation damage[Spi96].

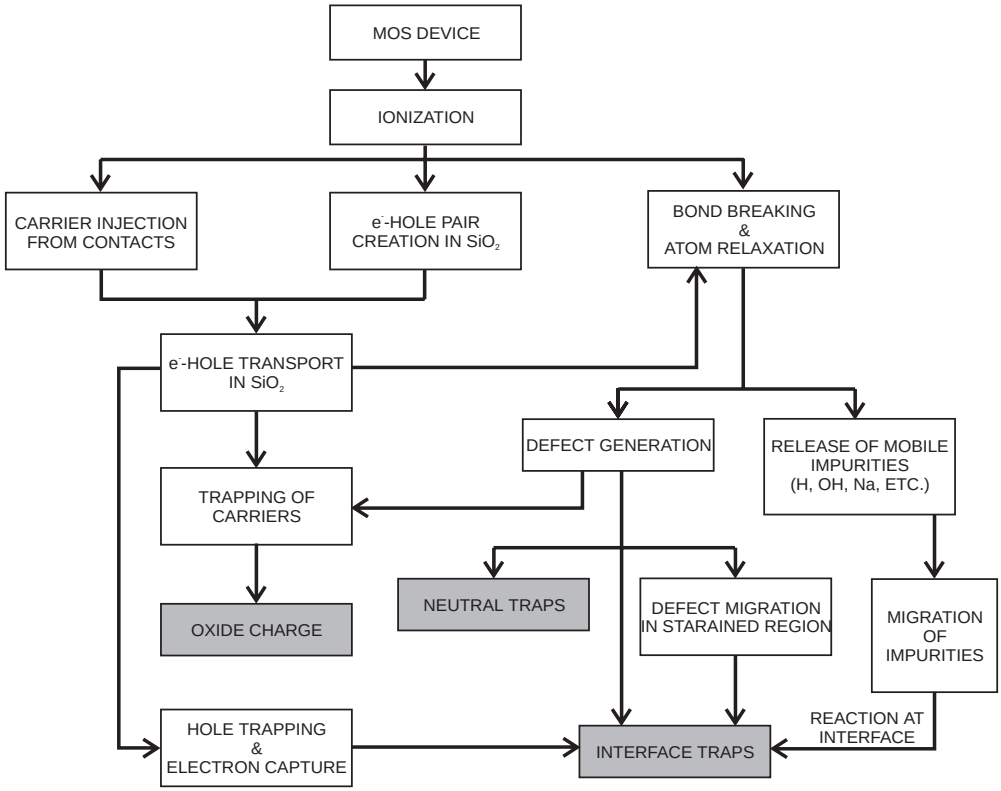


Figure 4.2: Processes caused by ionising radiation in MOS devices (taken from [Dre89]).

4.3.1 Trapped Charges in Silicon Oxide

Ionising radiation not only generates electron/hole pairs in silicon, but also in the silicon oxide on top of a chip. The electron mobility in silicon oxide is by a factor of 10^{11} larger than that of the holes. Therefore the electrons can leave the oxide within a very short time scale (few ps), which greatly reduces the chance of recombination. The presence of an electric field (i.e. $V_{\mathrm{GS}} \neq 0$) and higher energies of the incident radiation increase this effect. The remaining holes will slowly drift in the direction of the applied field, until they are captured in traps or leave the oxide layer. This is visualised in fig. 4.3. Oxide (or hole) traps are preferably located near the surface of the oxide layer, since they originate from the transition between two lattice structures.

Despite the transition from Si to SiO_2 within a very few atomic layers, the incompatibility of the two materials' lattice constants causes a thin ($1 \ldots 4$nm [Dre89]) region with irregularities, like strained bonds, in the lattice structure. Examples for strained bonds are e.g. the reduction of the 144° angle in the SiO_2 network (sp^3 orbitals) to just 120° near the surface. Another example are the $O_3 \equiv Si - Si \equiv O_3$ "*Oxygen Vacancies*": The two silicon atoms are directly bonded together, lacking the oxygen usually in-between them. Before

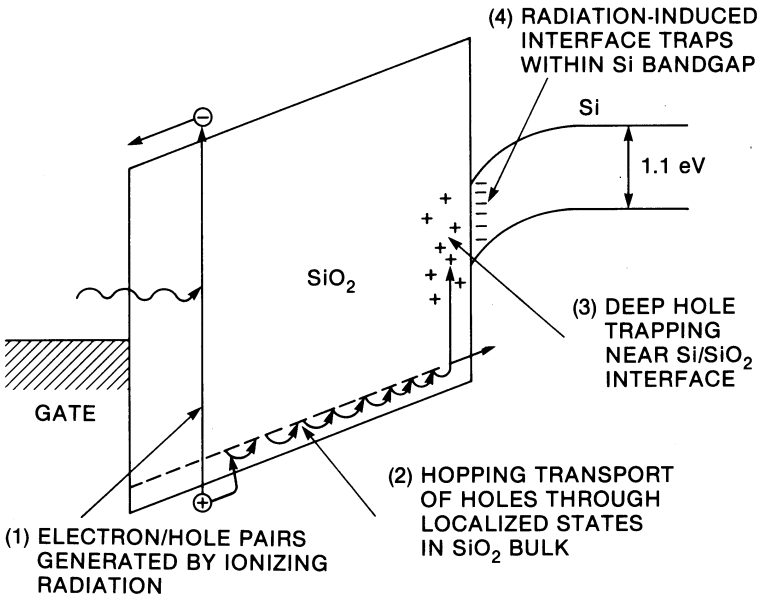


Figure 4.3: Mechanism of the charge trapping in the gate oxide of a MOS FET (taken from [Dre89]).

irradiation, its silicon atoms are stretched out of the plane of their three oxygen ligands, as fig. 4.4 shows. Trapping a hole results in the breaking of the $\equiv \mathrm{Si} - \mathrm{Si} \equiv$ bond by recombination with one of the electrons. The positively charged silicon relaxes back into the plane of its three oxygen atoms (due to now three sp^2 orbitals), while the other silicon atom is even further stretched out of the plane of its oxygen ligands. This is due to the unpaired electron being attracted by the positive charge of the other silicon atom. The resulting structure is the positively charged E_1' centre [Fei74], which is also shown in fig. 4.4. Other variants of the E' centre include trivalent silicon with a non-bridging oxygen [Rev71][Gru82] or displaced oxygen [Gri82]. However, due to their larger cross section for electron capture, these defects usually annihilate in a radiative environment.

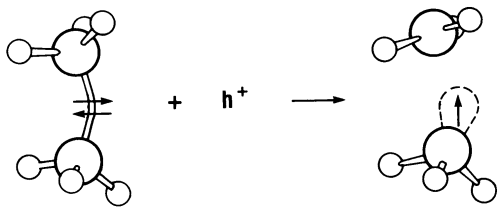


Figure 4.4: Conversion of an Oxygen Vacancy to an E_1' centre (taken from [Dre89]).

Shift of the Threshold Voltage V_{th}

The electric field of the trapped positive charges in the silicon oxide causes the accumulation of the corresponding *mirror charge* in the channel region. This charge adds to ρ_{CC} in eq. 4.1, i.e. we obtain $\Delta V_{\mathrm{th}} \approx \frac{\rho_{Q\,\mathrm{ox}} q_e}{C_{\mathrm{Gox}}}$, which is negative for n- and p-channel FETs due to the sign of q_e. As a result, n-channel FETs can be turned on easier (i.e. by a lower V_{GS}), while p-MOS FETs become harder to turn on.

It should be mentioned that the build-up of oxide charges governs the change of V_{th} only for low accumulated doses. Furthermore, ions brought into the gate oxide during the manufacturing process (e.g. in ion implantation, sputtering or plasma etching steps) have the same effect as oxide charges and contribute to the initial V_{th}. Processes providing FETs with $V_{\mathrm{th}} = 0$ usually use a dedicated process step to dope the gate oxide and achieve this characteristic.

With decreasing thickness of the gate oxide, the probability for electrons to tunnel (either from the channel or the gate surface) into the gate oxide increases. The trapped holes in the gate oxide will annihilate with these electrons, removing the threshold voltage shift. This effect results in an increased radiation hardness of processes with a gate oxide thickness below 10nm, as shown in fig. 4.5. Thus deep submicron processes are intrinsically radiation hard, while HELIX128 ($d_{\mathrm{Gox}} \approx 15$nm) does not profit from this effect.

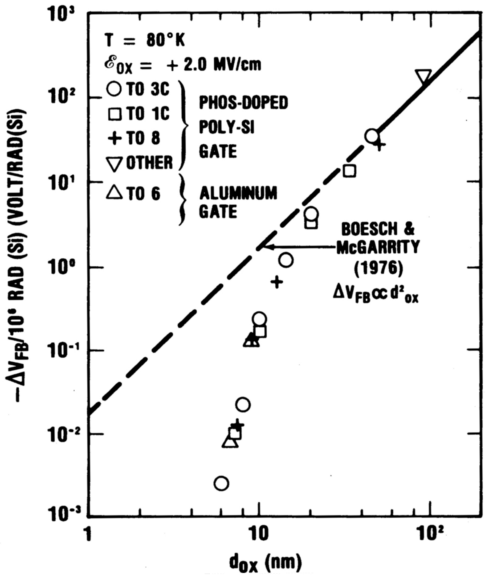


Figure 4.5: ΔV_{fb} (i.e. ΔV_{th}) per unit dose for different thicknesses of the gate oxide d_{Gox}. The line represents the d^2_{Gox} dependency valid for thick oxides (taken from [Sak82]).

Leakage Currents and the *Birds Beak*

Ionising radiation also generates electron/hole pairs in the much thicker field oxide on top of a MOS circuit. However, the probability for them to recombine is much larger than for the holes in the gate oxide:

- There is no electric field, sweeping the electrons out of the oxide layer.
- Due to its thickness, the electrons remain longer inside the oxide.
- The holes are not moved towards the hole traps near the surface by an electric field.

Therefore, charges trapped in the field oxide do not contribute to radiation damage, with one exception:

Growing the field oxide on top of a wafer results in a continuous transition of the oxide thickness at the edges of the gate area. In LOCOS[6] processes, this region is called "*birds beak*", due to it's profile, which is depicted in fig. 4.6.b. For n-MOS transistors, the electric field caused by the (positive) gate voltage will accumulate trapped holes on the boundary of the channel region. Since these charges are collected from a larger volume than those in the gate oxide, their density is higher and thus their field can build up a conducting channel on both sides of the gate at higher doses.

This "*End Around*" [Dre89] leakage currents due to these parasitic transistors will especially affect minimum sized transistors, like they are used in digital circuits.

As a result, the power consumption of statically operated digital circuits will increase with irradiation, and the circuit will fail, when a single transistor can no longer be turned off.

For analogue circuits with constant current biasing, the effects are by far less drastic, since the contribution of the parasitic current is suppressed with increasing transistor width (i.e. $\frac{I_{\text{leak}}}{I_{\text{D}}} \propto \frac{W_{\text{min}}}{W}$). Furthermore, constant current biasing compensates (!) for the leakage currents, since they are present in both branches of a current mirror, as fig. 4.7 shows.

In general these leakage currents can be avoided by using enclosed gate structures[7], especially in digital circuits. However, since the area required to implement a certain digital standard cell (e.g. an inverter), increases by about a factor of 8 [Sex], this approach is only viable in quarter micron processes and below.

It should also be mentioned, that for geometrical reasons it is impossible to build enclosed transistors with $\frac{W}{L} \lesssim 4$ as a single device.

4.3.2 Interface States

The build-up of interface states at the $Si - SiO_2$ interface is in many aspects very similar to the generation of oxide traps, though its mechanisms are not as

[6] Local Oxidation of Silicon
[7] Waffle transistors partly consist of enclosed gate structures.

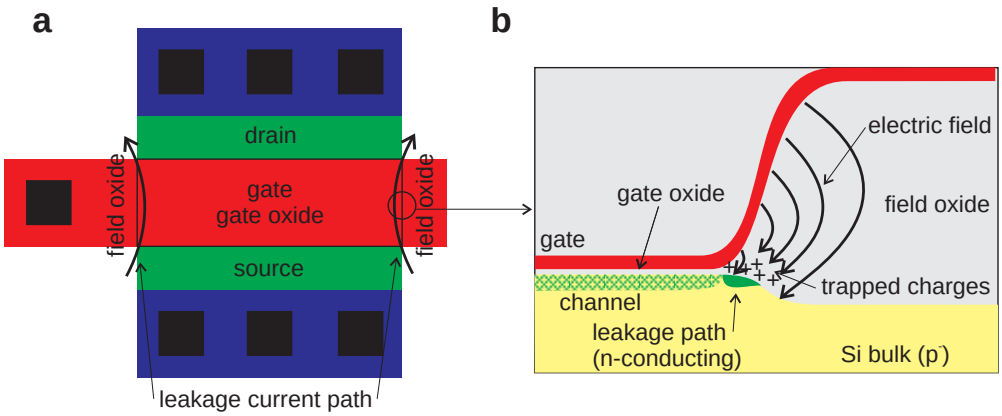


Figure 4.6: (a) "*End Around*" leakage current paths in an n-MOS FET. (b) Cross section of (a) at the gate's end (small circle in (a)). It shows the "*birds beak*" oxide profile found in LOCOS processes and indicates the mechanisms generating a leakage path.

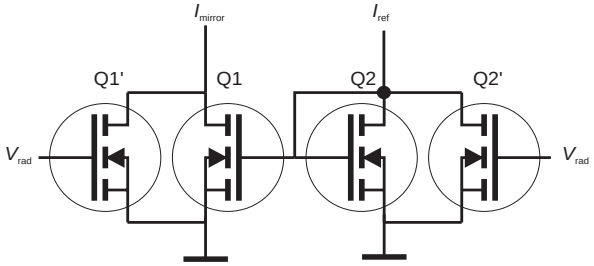


Figure 4.7: Effects of "*End Around*" leakage currents on a current mirror. Q_1' and Q_2' are the parasitic transistors of the leakage path. It is compensated in well-matching devices (i.e. $L(Q_1) = L(Q_2)$ and an equal number of gate ends per transistor width).

well known as those in the oxide layer. Also the responsible structures are very similar to the E_1' centre, forming a hole trap in the silicon oxide:

- P_{b0} centre, a silicon bonded to three others as $\dot{\mathrm{S}}\mathrm{i} \equiv \mathrm{Si}_3$ (i.e. a E_1' centre with all three oxygen atoms replaced by silicon)[Con98]. It is shown in fig. 4.8.

- P_{b1} centre,which is presumed to be a $\dot{\mathrm{S}}\mathrm{i} \equiv \mathrm{Si}_2\mathrm{O}$ structure (i.e. a E_1' with only two oxygen atoms replaced by silicon)[Poi89]. It is shown in fig. 4.9.

For the creation of P_b centres, two time constants have been observed [Dre89]: *Fast build-up* is the generation of interface traps directly from strained $\mathrm{Si}-\mathrm{Si}$ bonds during and immediately after irradiation.

Slow build-up is a proposed reaction of *Radiolytic Hydrogen* with $\mathrm{Si}-\mathrm{H}$ bonds. The Hydrogen can become embedded in the crystal lattice e.g. during oxidation or CVD deposition process steps.

Important precursors in the creation of the P_b centres by slow build-up are the 74G centre ($H - Si = O_2$) and the 10.4G centre ($O_2 = Si - OH$), which both were experimentally verified. Their creation dissociates the *Radiolytic Hydrogen* H_2, leaving over $\dot{H}$ radicals. These radicals can react with P_bH centres to P_b+H_2 or break strained $Si - Si$ bonds, resulting in further P_b and P_bH centres.

Fig. 4.9 shows a section of the silicon – silicon oxide interface with some defects.

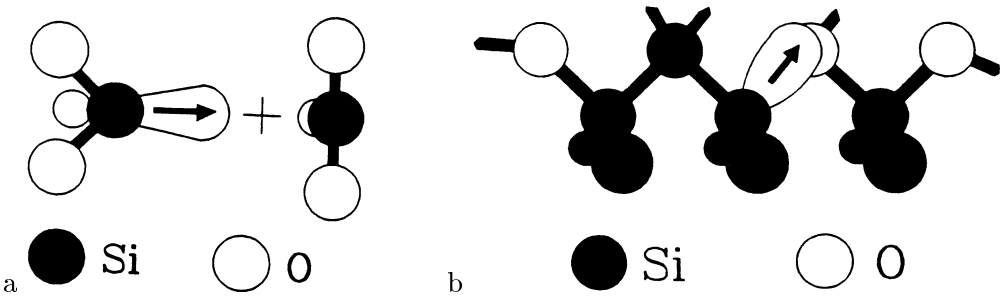


Figure 4.8: a) E_1' centre and b) P_{b0} centre (taken from [Con98]).

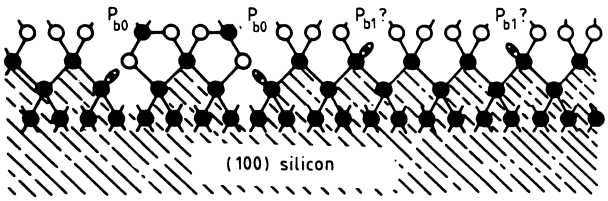


Figure 4.9: Si/SiO_2 interface with P_{b0} and P_{b1} centres ($\bullet$ = Si, $\circ$ = O, taken from [Poi89]).

V_{th}-Shift

The P_b centres have two broad bands of energy levels located above and below the middle of the band gap. Thus they show an amphoteric behaviour: For ϵ_{f} above midgap, the defects act as acceptors, while for ϵ_{f} below midgap they act as donors. Since ϵ_{f} changes with V_{GS}, the defects have to be filled with minority carriers, before inversion can be achieved in the channel region. This additional charge gives rise to a further shift in the threshold voltage V_{th} (cf. eq. 4.1): Towards negative values for p-MOS FETs and towards positive ones for n-MOS devices.

The *rebound* observed for n-channel FETs is caused by this behaviour, i.e. V_{th} increases again when exceeding a certain dose, eventually even rising above the value of the unirradiated device. An explanation for this are the different saturation levels imposed by the space charge density for oxide charges and interface states.

Degradation of the Transconductance g_m

The localised charges of the interface traps put some obstacles in the path of the majority carriers in a conducting transistor channel. The Coulomb Scattering of the carriers at these defects causes a reduction of the carriers' mean free path length and in turn of their mobility:

$$\mu = \frac{\mu_0}{1 + \alpha \cdot (\Delta\rho_{\mathrm{it}})} \tag{4.8}$$

μ = mobility of the charge carriers [$\mathrm{cm}^2/\mathrm{Vs}$]

ρ_{it} = density of the interface traps [cm^{-2}]

This is shown in fig. 4.10. Since it is $\rho_{\mathrm{it}} \propto D^{2/3}$ ([Dre89]), we end up with

$$\mu = \frac{\mu_0}{1 + \alpha' \cdot (D^{2/3})} \tag{4.9}$$

D = accumulated dose [Gy]

For the degradation of the transconductance g_{m}, one has to consider two cases: For a fixed gate voltage, we obtain from eq. 4.5

$$g_{\mathrm{m}}|_{V_{\mathrm{GS}}=const.} = \frac{g_{\mathrm{m0}}}{1 + \alpha \cdot \Delta\rho_{\mathrm{it}}}, \tag{4.10}$$

while the degradation is less for constant current biasing (from eq. 4.5):

$$g_{\mathrm{m}}|_{ID=const.} = g_{\mathrm{m0}} \sqrt{\frac{1}{1 + \alpha \cdot \Delta\rho_{\mathrm{it}}}}, \tag{4.11}$$

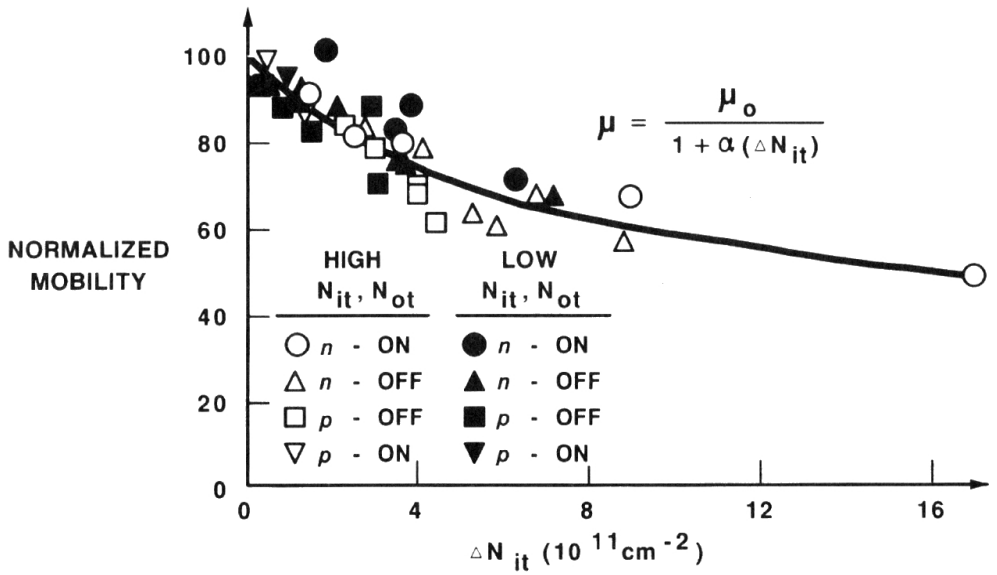


Figure 4.10: Degradation of the normalised effective channel mobility with the density of interface states (taken from [Sex85]).

4.4 Non-Ionising Damage

Incident corpuscular radiation, e.g. baryons or mesons, can inflict non-ionising damage to a semiconductor by three different mechanisms [Lut99]:

- Displacement of lattice atoms, leading to interstitials (atoms between regular lattice sites) and vacancies (empty lattice sites).
- Nuclear interactions (e.g. neutron capture or nucleus transmutation).
- Secondary processes from energetic displaced lattice atoms, forming so-called *defect clusters*.

We restrict further discussions to the displacement of lattice atoms (i.e. the first and the last item), since an incident charged particle will almost exclusively cause damage by Coulomb Interaction with the lattice atoms.

To displace a silicon atom from its lattice site, a recoil energy of at least 15eV is required. The displaced atom can in turn create further (isolated) defects, if its recoil energy is in the 1 ... 2keV region. Atoms with recoil energies within 2 and 12keV will create defect clusters, dense agglomerations of typical 100 point defects inside a 5nm diameter [Lut99]. As pointed out in sect. 2.2, this is due to incident particles as well as the recoil atoms losing most of their energy at the very end of their trajectory.

The interstitials can move within the lattice and are usually trapped by donor impurities. This neutralises the latter and is therefore called *Donor Removal*. The vacancies form localised acceptor like defects. Both phenomena result in the type inversion observed in silicon detectors at high accumulated doses. CMOS circuits usually use p-doped wafers and higher doping concentrations, and thus are immune against this phenomenon.

The created defects have some impact on the electrical properties of (primarily bipolar) devices:

- Due to additional energy levels in the band gap, the leakage current in reverse biased pn-junctions is increased [Lut99]:

$$I_{\text{leak}} = I_{\text{leak}_0} + \alpha \cdot \Phi \cdot A \cdot d_{\text{junction}} \tag{4.12}$$

  I_{leak_0} = pre-radiation leakage current [µA]
  α = specific damage rate, dependent on particle type and energy $[\frac{\mu A}{\mu m^3}]$
  Φ = integrated particle fluence
  A = area of the pn-junction [µm^2] d_{junction} = depletion depth of the pn-junction [µm]

  This is the only effect of non-ionising radiation damage affecting CMOS circuits.

- Like for interface states, the majority carriers will scatter at the interstitial and vacancy defects, resulting in a degradation of bipolar transistors amplification factor β.
- The defects can also act as generation–recombination centres, further reducing the bipolar transistors' amplification factor β and also decreasing their transit frequency f_{T}.

4.5 Total Dose Effect and Annealing

In first order the damage inflicted by a certain dose does not depend on the dose rate. However, some radiation damage like the slow build-up of interface states establishes with some delay, as fig 4.11 shows. The final damage observed depends upon the bias conditions during irradiation, i.e. on the electric fields collecting or repelling mobile charged damages. The effect of some damages can be even altered after irradiation: To some extent the trapped charges in the silicon oxide can be moved from the gate-oxide interface to the channel-oxide interface and vice versa by changing V_{GS}, resulting in a slight change in V_{th}. The time constant for these changes is in the order of several hours and depends on the temperature.

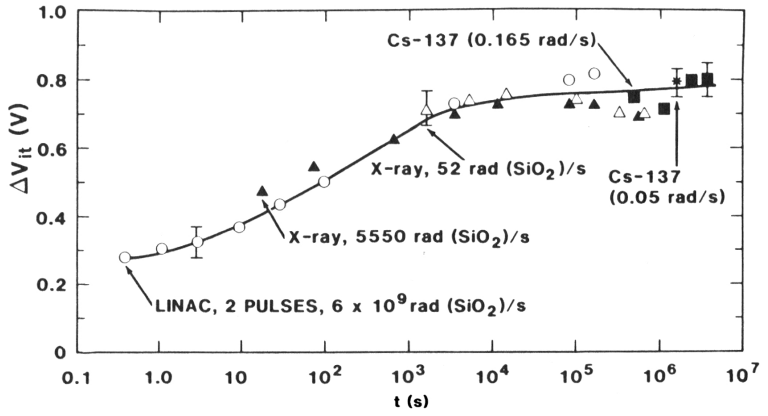


Figure 4.11: Threshold voltage shift due to interface traps ΔV_{it}. Obviously the final change does not depend on the dose rate (taken from [Fle88]).

On a long time scale, electrons tunneling into the oxide can recombine with the trapped charges and increase the threshold voltage. This process shows a $\Delta V_{\mathrm{th}} \propto \log t$ behaviour. At $T \gtrsim 150°\mathrm{C}$ oxide charges are thermally released from their traps [Dre89].

Also interface states can anneal due to thermal effects. The temperatures required for these processes are reported to be as low as $\approx 100°\mathrm{C}$ [Sno67]. "Artifacts" of the radiation damage (e.g. dangling bonds) are however not removed by this treatment and thus annealed circuits show an increased sensitivity for further irradiation damage.

4.6 Single-Event effects caused by Radiation

Localised ionisation caused by e.g. nuclear fragments or heavy ions, can inflict besides the ionising damage already described, a transient malfunction of integrated circuits:

4.6.1 Single-Event Upset (*SEU*)

Irradiation induced charge, collected on a circuit's node can cause spurious signals at its output. Looking e.g. at the simplified schematic of a latch (fig. 4.12) the voltage of its storage node has to be raised above the threshold level V_s of the hold amplifier A_1 for at least A_1's delay time t_d. Thus the collected charge Q_{rad} has to be

$$Q_{rad} \geq C_{node} V_s e^{\frac{t_d}{R_i C_{node}}} \tag{4.13}$$

C_{node} = node capacitance [F]

V_s = threshold level of the feedback amp [V]

R_i = resistance in parallel with C_{node}, i.e. the internal resistance of the feedback amp [Ω]

t_d = delay time of the feedback amp [s]

to flip this bit. Assuming $V_s = 2V$, $C_{node} = 10fF$, $R_i = 100k\Omega$ and $t_d = 2ns$, about 15fC are required to change the status of the latch. Unlike in a silicon detector, the charge has to be deposited in the very close vicinity (very few µm) of the nodes' diffusion contacts, which is very unlikely.

However, the probability for SEU increases with decreasing V_s (i.e. power supply voltage), C_{node} and t_d, as well as increasing R_i. Thus CMOS processes with smaller feature sizes (e.g. deep submicron technologies) are more prone to single event upset. The most critical devices are DRAMs (with $R_i = \infty$ and a very small C_{node}), which for that reason can't be used in a radiation environment.

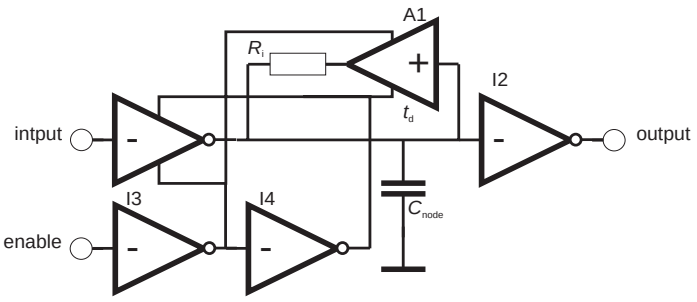


Figure 4.12: Simplified schematic of a latch, including the passive components related to SEU. Further explanation can be found in the text.

4.6.2 Single-Event Latchup (*SEL*)

Single-event latchup is a radiation induced short between the power supply nodes of an integrated circuit. If no protective measures, like current limitation, are taken, the circuit will be destroyed by the SEL.

The possibility to shorten the power supply arises from the sequence of pn-junctions found in CMOS circuits. Fig. 4.13 shows the cross section of an inverter, also including two parasitic bipolar transistors. Unfortunately collec-

tors and bases of the transistors are connected together, forming a pnpn-SCR[8] (thyristor) structure. The device becomes conductive, if either of the "*base*" areas is subjected to (radiation induced) charge carrier inversion. To bring this thyristor back into its cut off state, the power supply voltage has to be removed.

In the chip layout, substrate and well contacts are used, to "drain" radiation induced charges from the sensitive areas to prevent charge carrier inversion.

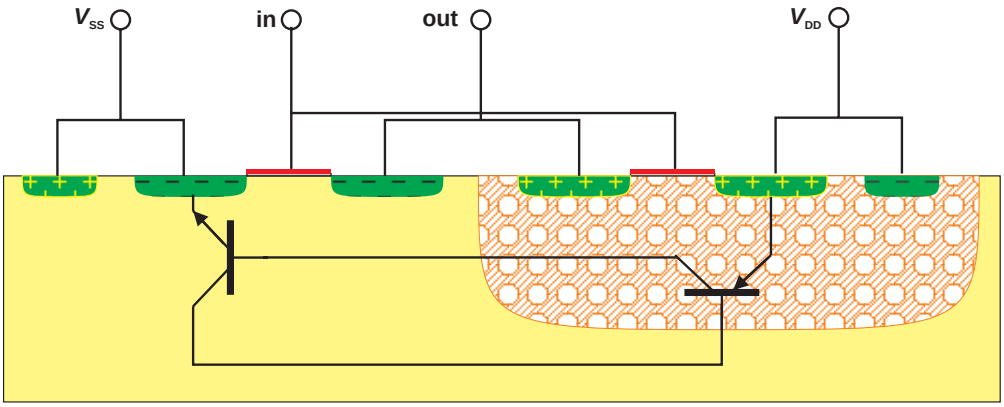


Figure 4.13: Parasitic SCR (thyristor) structure caused by the sequence of pn-junctions in a CMOS circuit and responsible for SEL.

[8] Silicon Controlled Rectifier

Location	Effect	Consequences for		
		n-MOS	p-MOS	other
Ionising Energy Loss				
Gate Oxide	Trapped Charges	Decrease of V_{th}	Decrease of V_{th}	—
Field Oxide	Trapped Charges	"*End Around*" Leakage Current	—	—
Silicon	Interface States	Increase of V_{th}	Decrease of V_{th}	—
		Decrease of μ (and K', g_{m})	Decrease of μ (and K', g_{m})	
	Charge Carrier Injection	SEU, SEL		
Non Ionising Energy Loss				
Silicon	Interstitials and Vacancies	—	—	"*Donor Removal*" and "*Acceptor Generation*" ($\rightarrow$ Type Inversion)
				Decrease of μ (and β) in Bipolar Transistors
				pn-Junction Leakage Current

Table 4.1: Effects and consequences of radiation damage in semiconductor devices.

Chapter 5

Characterisation and Irradiation Results

The readout electronics of the HERA-B silicon vertex detector and inner tracking system have to survive a rather hostile environment: They are subjected to considerable doses of radioactive radiation.

For that reason it was not sufficient to perform an electrical characterisation of the unirradiated chip (like it was done for the HELIX128-1 [Sex97]). It also had to be proven that the chip can withstand the radiation dose it will accumulate during the lifetime of the detectors. To obtain a strategy to compensate or minimise the effects of radiation damage it was decided to repeat the characterisation after every irradiation step.

The main component of the radiation encountered in HERA-B are hadrons with energies $\geq$ 1GeV, i.e. minimum ionising particles (*MIP*s), of which about 75% are pions. But also nuclear fragments and γ-rays are present.

The expected particle flux in HERA-B is approximately given by $\phi(R) = \phi_1 \cdot (r_1/R_\perp)^2$ with $\phi_1 = 3 \cdot 10^7 \mathrm{cm}^{-2}\mathrm{s}^{-1}$ and $r_1 = 1\mathrm{cm}$, i.e. it only depends on the distance from the beam axis and is independent of the polar angle Θ for $\Theta \geq 10\mathrm{mrad}$ [HB93] [HB95] . Therefore the VDS' silicon detectors have to be replaced every year due to radiation damage – together with the readout chips bonded to them. The original design [HB93] assumed the VDS readout electronics mounted at $R_\perp = 7\mathrm{cm}$. Applying eq. 4.7 leads to a total dose of $\leq$ 2kGy (by defining '1 year' as 10^7s of HERA operation), which was a requirement for the development of the HELIX128 chip. However, in the actual design [Bau00] the VDS readout electronics are mounted at $R_\perp = 10\mathrm{cm}$ from the beam axis, which reduces the dose to about 1kGy/a (100krad/a)[1]. The inner tracking system's readout electronics are placed about 25cm from the beam axis. Applying the above formula, the expected doses are less then 160Gy/a, but do not include showers of secondary particles. A safety margin of 100% was included to cover for that additional dose. The chips do not have to be replaced during the lifetime of the experiment.

[1] Recent measurements using glass dosimeters resulted in an extrapolated dose of 1.2kGy/a at $R_\perp = 10\mathrm{cm}$ [Knö].

To demonstrate the radiation tolerance an irradiation of 10 HELIX128 chips, mounted on daughtercards *A* through *E* with two chips each, was performed. A total dose of ≈4kGy was anticipated to provide a safety margin of two times the expected dose in the silicon vertex detector. As pointed out in Chapter 4, the deteriorating effects in MOS devices are oxide charges and interface traps at the Si-SiO_2 interface, both originating mainly from ionising energy loss of the incident radiation. Non-ionising energy loss on the other hand causes bulk damage giving rise to leakage currents in pn-junctions. Since the HELIX128 does not use any bipolar transistors, bulk damage is less important and a γ-source can be employed for the irradiation. A further advantage of using a γ-source is the homogeneity of the irradiation resulting in a precise and easy determination of the accumulated dose for a given calibration.

The irradiation was performed with the ^{137}Cs source installed at the blood repository of the University of Heidelberg's Institute for Immunology and Serology. It is a Buchler OB29/4 [Buc] intended to irradiate blood plasma for GVHD[2]-prophylaxis at a dose rate of about 150Gy/h. As depicted in fig. 5.1 the apparatus consists of a 82TBq ^{137}Cs source oscillating up and down the side wall of the bucket-like rotating can forming the irradiated volume. The rather homogeneous distribution of dose inside the irradiated volume depicted in fig. 5.2 is due to the unique arrangement of the source wrt. the irradiated volume.

To obtain results comparable with the deterioration of the chips in the HERA-*B* ITR and VDS, the chips had to be operated during irradiation. This was accomplished by the battery-powered irradiation setup depicted in fig. 5.3, which uses a 10MHz TTL oscillator for `SClk`, `RClk` and a 74LS593 counter creating the `TrigIn` signals. A Tektronix DG2020A pattern generator was used to initialise the chips' bias and latency control registers before irradiation. Two HELIX128-2.2 chips originating from adjacent locations on the wafer were mounted on a daughter card depicted in fig. 5.4, which was plugged into the irradiation or measurement setup, respectively. Six channels per chip were bonded to test pulse injection circuitry and load capacitances of 5 different values. The two chips form a readout daisy-chain like in the HERA-*B* experiment.

The measurement setup is depicted in fig. 5.5. It contains two *transconductance amplifier* circuits (depicted in fig. 5.6) based on National Semiconductor's (Comlinear) CLC400 current feedback operational amplifiers. The circuit is based on the one proposed in apx. C. The CLC400 was also employed in the difference amplifier stage due to its (wrt. the CLC401) much lower phase difference between inverting and non-inverting inputs, which greatly reduces overshoots, ringing and distortion. The complete circuit has a bandwidth of ≥180MHz (-3db) to exploit the full performance of the HELIX128-2.2's output driver. The HELIX128's control and clock lines as well as the testpulse inputs were driven by a Tektronix DG2020A pattern generator. A Tektronix TDS784A digitising oscilloscope was used for analogue readout and a HP 34401A digital multimeter to monitor various node voltages. Pattern generator, oscilloscope

[2] Graft Versus Host Disease

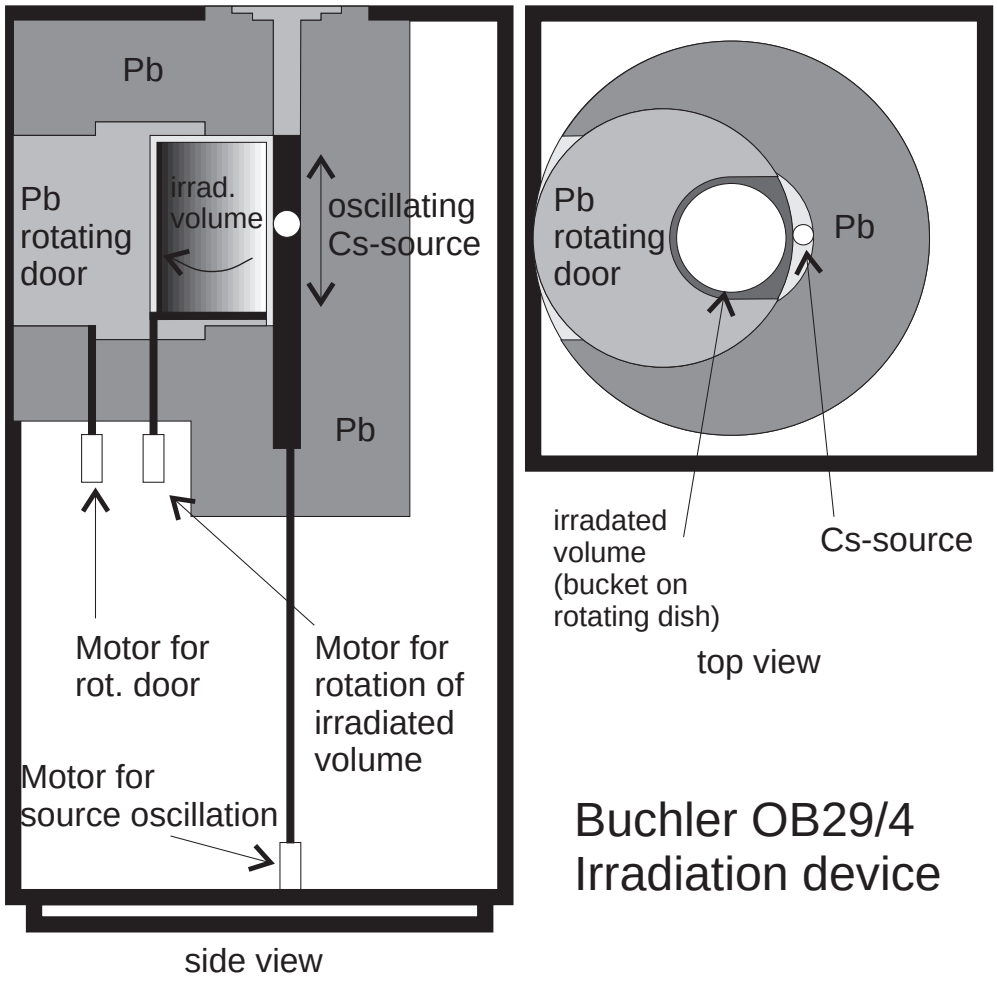


Figure 5.1: OB29/4 irradiation device: Schematic showing the arrangement of the oscillating 82TBq ^{137}Cs source wrt. the rotating irradiated volume. The lead shielding weights approximately 2700kg [Buc].

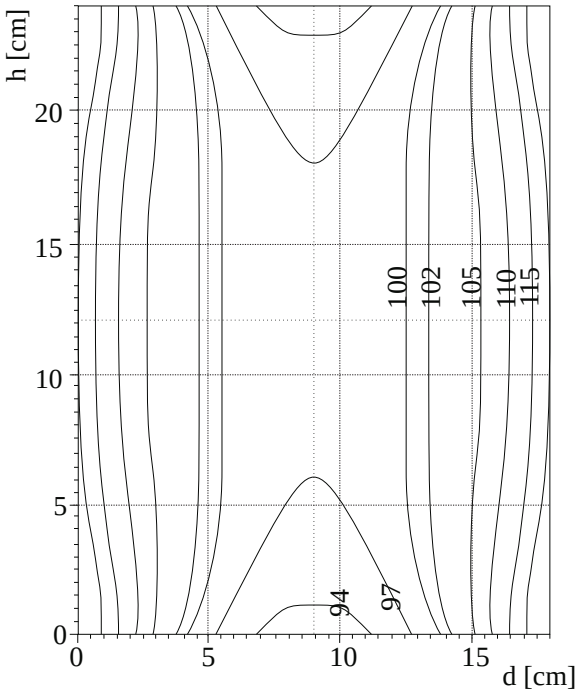


Figure 5.2: OB29/4 irradiation device: Isodose profile of the irradiated volume (18cm⌀×24cm). The numbers give the percentage of the dose wrt. the centre of the volume [Buc].

and multimeter were controlled via HP-VEE™ software and connected to an IEEE488 (GPIB) bus interface.

The irradiation itself was performed in steps as given in tab. 5.1[3]. A rather large discrepancy between the doses measured with alanine dosimeters [Reg] and the calibration of the irradiation device was observed, which is similar to that reported in [Tip99]. It turned out that the calibration data includes a rather large safety margin, since the blood plasma has to accumulate at least a dose of 30Gy. Therefore this calibration was performed under worst case conditions: The complete irradiated volume was filled with a water phantom and the activity of the ^{137}Cs source was extrapolated until the expiration of the calibration. Thus the values from the alanine dosimeters have to be used.

5.1 CMOS-Process Parameters

The simplified model given in chapter 4.2 characterises a FET implemented in a CMOS process by 4 quantities (process parameters): the gain factor $K' = \mu C_{\mathrm{Gox}}$, the threshold voltage $V_{\mathrm{th_0}}$ and the effective geometry (i.e. L_{eff}

[3]The last irradiation step was only performed to evaluate the limit of radiation tolerance. Previous radiation tests with 4 HELIX128-2.2 chips from an out-of-spec production run resulted in a limit of 5.2kGy for the total dose.

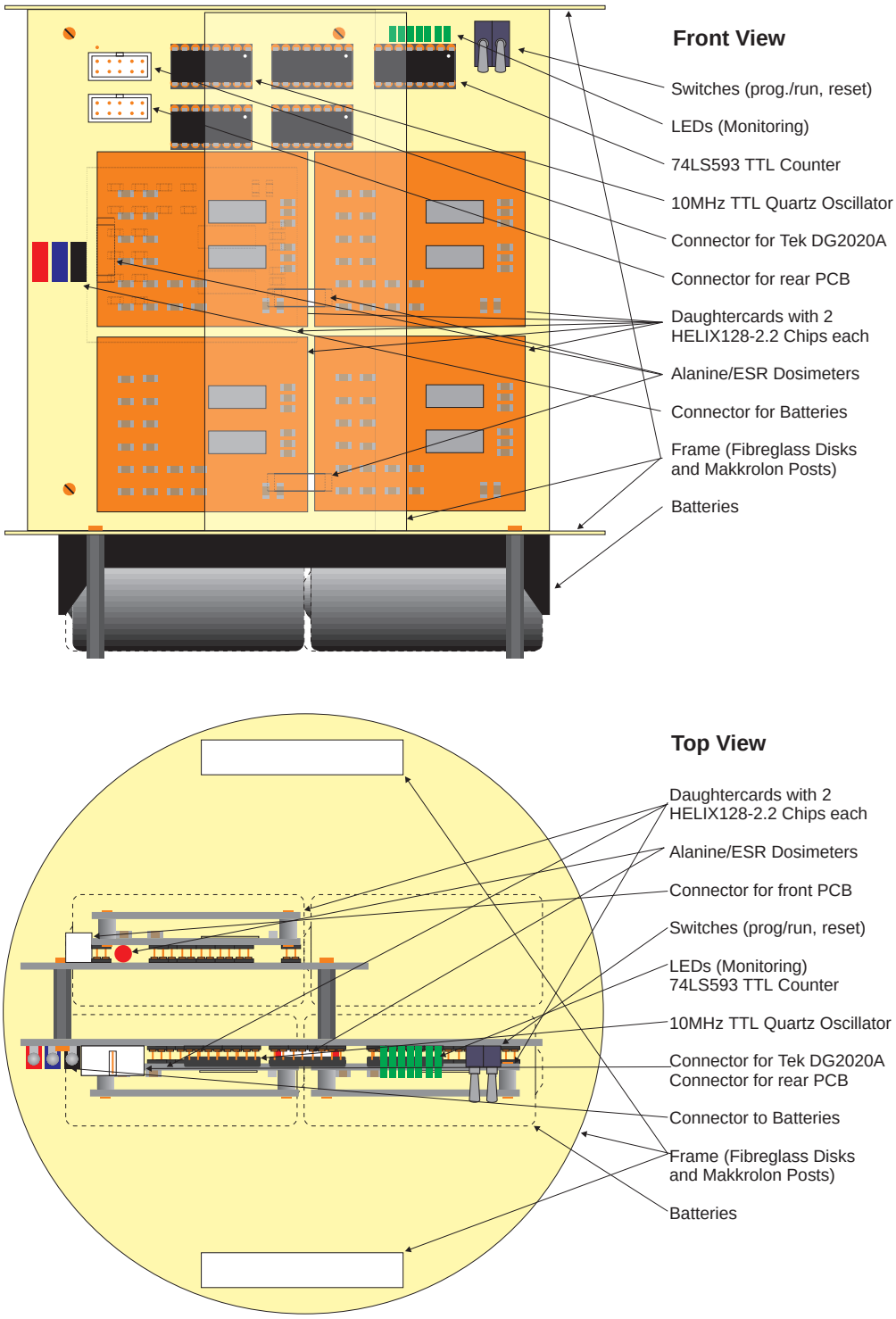


Figure 5.3: Battery powered setup to operate the HELIX128 chips during irradiation.

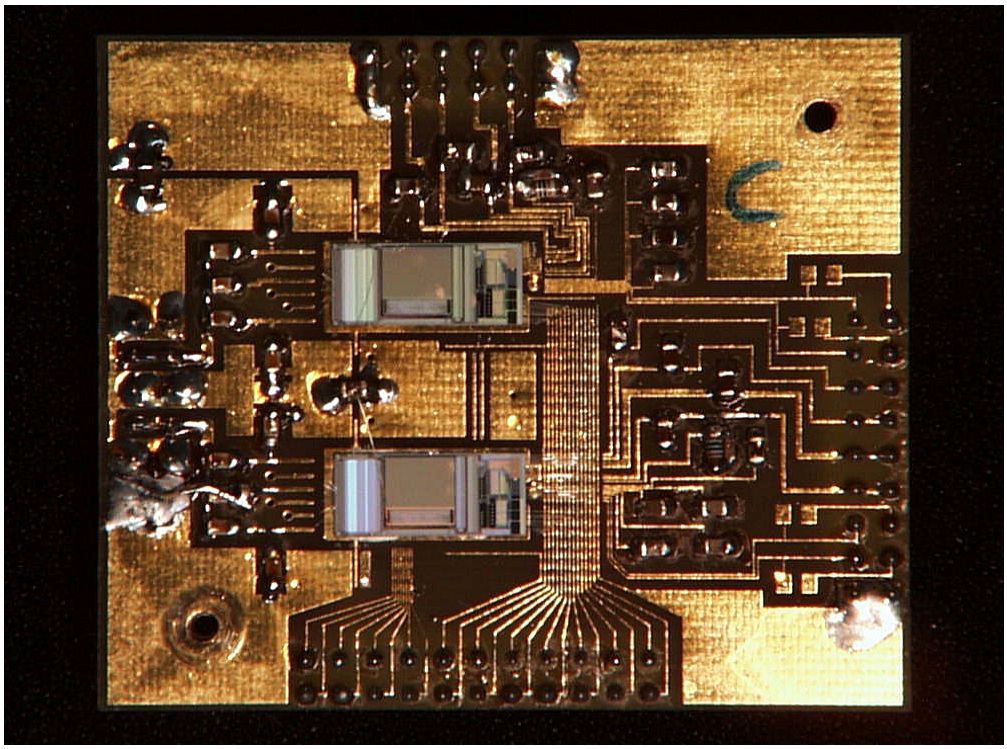


Figure 5.4: Photograph of a daughter card with 2 HELIX128-2.2 chips. On the left-hand side six load/coupling capacitors for test pulse injection are visible. The remaining six are located on the bottom side of the board. Two long bonds give access to the output of each chip's test channel. On the right-hand side, blocking capacitors, control lines (bus structure) and the token path (between chips) are visible. For the photograph the top shielding made of PCB-material was removed.

and W_{eff}). However, only K' and V_{th} are affected by radiation damage. Knowing the degradation of these quantities will allow the prediction of the chip's characteristics under irradiation.

To monitor these and other process parameters, semiconductor manufacturers usually include test structures on their wafers. These structures consist in principle of reference designs for all devices available in the particular process. Usually located within the channels between the chips on the wafer, they are destroyed when the dice are cut. To overcome this and to provide a possibility to monitor the changes in V_{th} and especially K', four gaps in the HELIX128-2.2's pad frame were filled with a test structure consisting of four transistors. The structure chosen was the *TEST* cell from AMS' *SFCLIB_CYE* library [AMS_HK], for which measurement instructions as well as process parameters are available [AMS97/2]. As shown in fig. 5.7 it consists of n- and p-MOS transistors with W/L=2µm/0.8µm (the *minimum size* for a transistor in this process) and W/L=20µm/0.8µm.

For measurements the structures were contacted by the needles of a probecard, using a manual wafer prober station. Assuming K' being constant for one

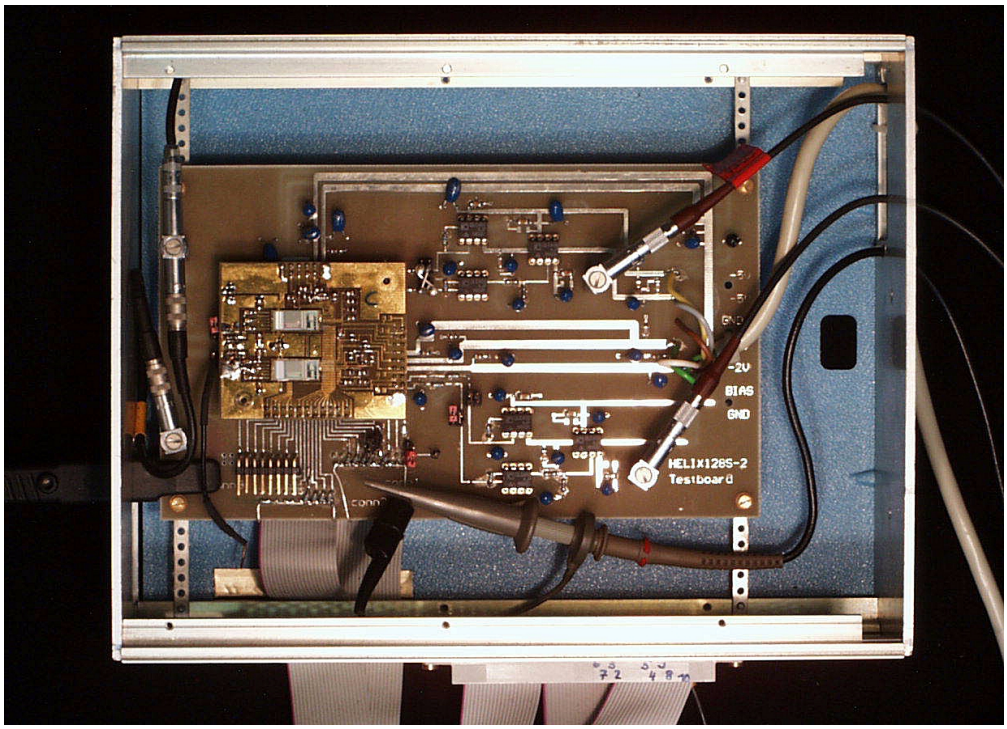


Figure 5.5: Measurement setup mounted inside the enclosure of a NIM module. The LEMO connectors on the left-hand side are the test pulse inputs, while the ones on the right-hand side are the analogue outputs. Right of the daughtercard with two HELIX128-2.2 chips the two receiver circuits are visible. The digital control signals are fed to the setup via the flat ribbon cable from the bottom.

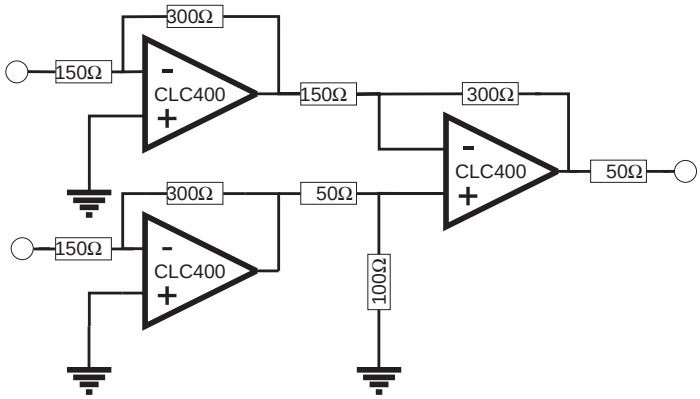


Figure 5.6: Receiver circuit for the HELIX' analogue readout.

single wafer and $W = W_{\text{eff}}$ for the W=20µm transistors (which according to [AMS97/2] is both valid), L_{eff} was calculated with

$$\beta = \frac{K'}{2} \cdot \frac{W_{\text{eff}}}{L_{\text{eff}}} \tag{5.1}$$

Step	Dose from OB29/4 "calibration"	Dose from alanine/ESR dosimeters	Date	Number of irrad. chips (failed chips)	Daughter-cards
1	125Gy	161Gy	02.11.98	10 (0)	*A,B,C,D,E*
2	250Gy	322Gy	16.11.98	10 (0)	*A,B,C,D,E*
3	500Gy	644Gy	25.11.98	10 (0)	*A,B,C,D,E*
4	1000Gy	1288Gy	03.12.98	10 (0)	*A,B,C,D,E*
5	1500Gy	1932Gy	17.12.98	10 (0)	*A,B,C,D,E*
6	2000Gy	2576Gy	30.12.98	10 (0)	*A,B,C,D,E*
7	3000Gy	3864Gy	14.01.99	$6^{1)}$ ($0^{2)}$)	*A,D*
8	4000Gy	5152Gy	27.04.99	$2^{3)}$ (0)	*A,B*

[1] Daughtercards *A* and *D*, daughtercard *B* was irradiated to 3864Gy at 27.04.99

[2] A dose rate dependent temporary failure of the chips' digital circuits was observed. Chips had to be operated for 8 days at $\approx 55°$C to regain full functionality.

[3] Daughtercard *A*

Table 5.1: Doses and dates of the radiation steps performed. The OB29/4 "calibration" values include a safety margin for the 30Gy minimum dose delivered to blood plasma, while the values from the alanine dosimeters are exact.

from the measured β and the K' value from the wafers' production data. For the minimum size transistors it is $W \neq W_{\text{eff}}$ and therefore only the 20µm×0.8µm transistors were used to measure V_{th} and K'. These measurements were performed according to AMS' specifications [AMS97/2]:

- **Threshold Voltage:** Gate and drain are connected together and V_{DS} is swept. $\sqrt{I_{\text{D}}}$ is plotted versus V_{DS}. A tangent is put to the curve at the point of maximum slope. The intersection of the tangent with the abscissa yields V_{th}.
- **Gain Factor:** V_{DS} =0.2V (-0.2V for p-MOS), V_{GS} is swept, i.e. the measurement is done in the linear region of the transistor characteristics. $\frac{\partial I_{\text{D}}}{\partial V_{\text{GS}}}$ is numerically calculated and K' is extracted at the maximum of the curve. i.e.

$$\max \frac{\partial I_{\text{D}}}{\partial V_{\text{GS}}} = K' \cdot \frac{W_{\text{eff}}}{L_{\text{eff}}} \cdot V_{\text{DS}}. \tag{5.2}$$

Besides a manual wafer probe station (SUSS PM200) and a custom made probecard, a HP 4155A semiconductor parameter analyzer was used for measurement and (online) data analysis.

Unfortunately it was not possible to shield the wafer probe station against light, which prevented a measurement of the transistors' leakage currents under cut-off conditions (cf. sect 4.3.1). It turned out, that indeed these leakage currents are the dominating effect deteriorating the chip's performance with irradiation (cf. sect. 5.3).

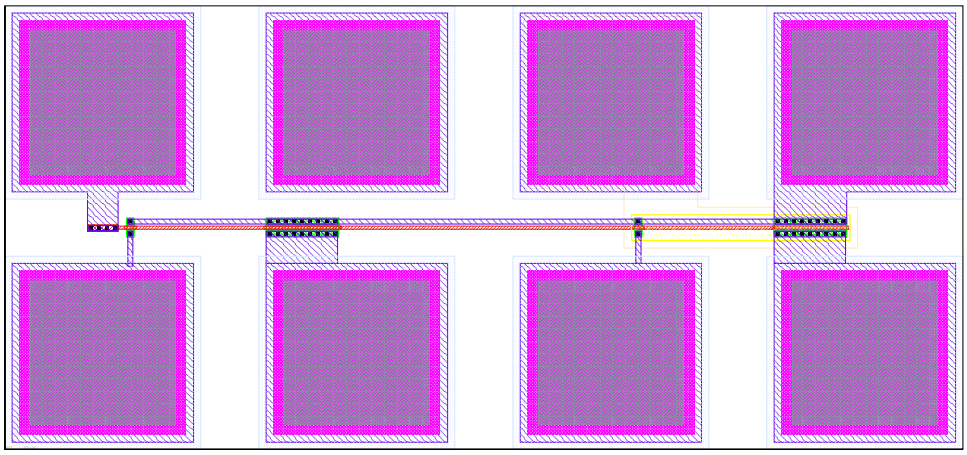


Figure 5.7: Layout of the *TEST* structure from AMS' *SFCLIB_CYE* library. It consists of n-MOS transistors with W/L=2µm/0.8µm, n-MOS W/L=20µm/0.8µm, p-MOS W/L=2µm/0.8µm and p-MOS W/L=20µm/0.8µm (left to right). The pads in the top row connect gate (common), bulk, n-well, source (common), while the bottom pads connect the drains of the individual transistors.

The results of the measurements are shown in figs. 5.8 and 5.9 and tab. 5.2.

As shown in eq. 4.9 the dependence of the gain factor K' on the accumulated dose D is given by

$$K' = \frac{K'_0}{1 + \alpha \cdot (D^{2/3})} \tag{5.3}$$

since the oxide capacitance C_{ox} does not change with irradiation. Therefore eq. 5.3 was fitted to fig. 5.9. The results are given in tab. 5.3 and exhibit almost no difference in α between n-channel and p-channel transistors.

Dose	n-MOS		p-MOS	
	V_{th} [V]	K' [µA/V^2]	V_{th} [V]	K' [µA/V^2]
0Gy	0.669	99.53	-0.822	35.61
161Gy	0.663	97.59	-0.839	35.15
322Gy	0.661	98.26	-0.858	34.95
644Gy	0.645	96.71	-0.904	34.55
1288Gy	0.621	91.32	-0.980	32.57
1932Gy	0.592	87.93	-1.054	31.07
2576Gy	0.589	83.95	-1.119	29.41
3864Gy	0.630	77.09	-1.223	27.22

Table 5.2: Measured process parameters for different accumulated doses.

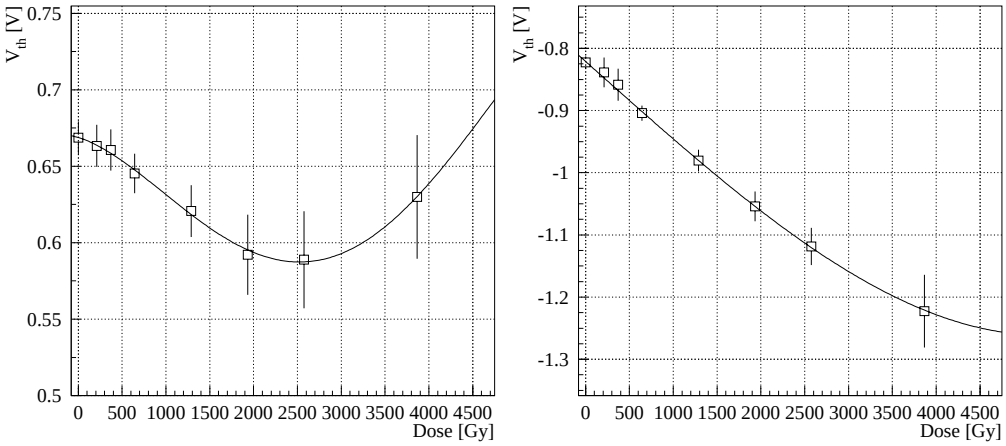


Figure 5.8: Threshold voltage V_{th} of the 20µm × 0.8µm test structures implemented on the HELIX128-2 chips vs. total accumulated dose. Left: n-MOS FET. Right: p-MOS FET.

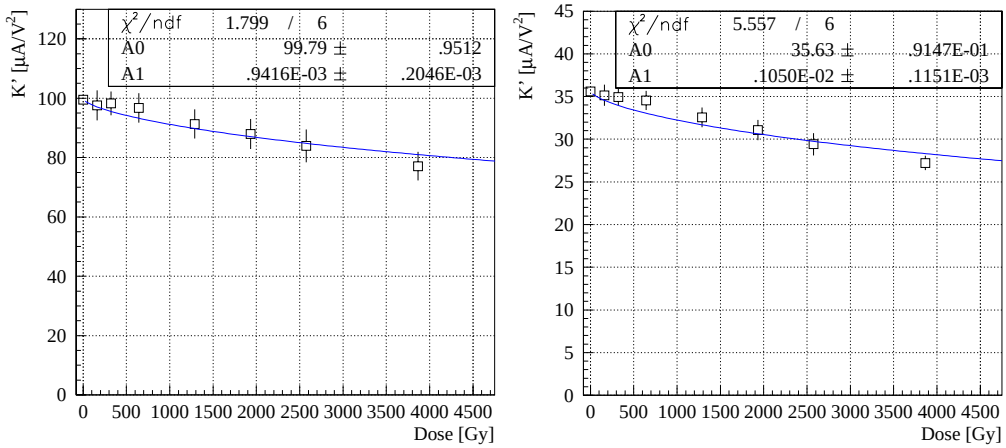


Figure 5.9: Gain Factor K'_{n} (for n-MOS transistors, left) and K'_{p} (for p-MOS transistors, right) vs. accumulated dose, extracted from the test structures on the HELIX128-2 chip. Also the results from the fit of eq. 5.3 (with P1 = K'_0 and P2 = α) to the data are shown.

n-MOS	Fit to measurement	AMS wafer data
K'_0	$(99.79 \pm 0.95)\mu\mathrm{A/V}^2$	$(99.53 \pm 0.72)\mu\mathrm{A/V}^2$
α	$(9.416 \pm 2.046) \cdot 10^{-4}\mathrm{Gy}^{-2/3}$	

p-MOS	Fit to measurement	AMS wafer data
K'_0	$(35.63 \pm 0.91)\mu\mathrm{A/V}^2$	$(35.61 \pm 0.40)\mu\mathrm{A/V}^2$
α	$(1.050 \pm 0.115) \cdot 10^{-3}\mathrm{Gy}^{-2/3}$	

Table 5.3: Results from the fit of eq. 5.3 to fig. 5.9.

5.2 Characteristics of the unirradiated Chip

To provide a solid data base for the irradiation measurements, HELIX128-2.2 was characterised wrt. pulse shape and noise. Like for the characterisation of HELIX128-1 [Sex97] the measurements were performed in dependence of preamplifier bias current I_{pre}, shaper feedback control voltage V_{fs} and the parallel capacitance C_{p} on the amplifier input. These measurements were repeated after each irradiation step. The parameter set tested was:

- C_{p} = 1.6pF, 6.8pF, 16.3pF, 29.4pF, 58.0pF
- I_{pre} = 100µA, 200µA, 300µA, 400µA, 500µA and 600µA (Daughtercard *A*) or 100µA, 350µA and 300µA (Daughtercards *B, C, D, E*).
- V_{fs} = 0.0V, 0.5V, 1.0V, 1.5V, 2.0V.

The measurements were always performed in alphabetical order of the daughtercards (except for *B* at 3.9kGy). Since they are more detailed, the results reported are from daughtercard *A* unless otherwise denoted.

5.2.1 Pulse Shapes and Sensitivity

To obtain the rise and fall times of the frontend's signal as well as the sensitivity, a pulse shape scan was performed for each $I_{\mathrm{pre}} - V_{\mathrm{fs}}$ combination. Therefore a test charge of $\approx 24 \cdot 10^3 \mathrm{e}^-$ was injected. The time of the charge injection was swept over 410ns in steps of 2.5ns. 1000 measurements were accumulated with the average function of the Tek TDS784A DSO[4] used and the baseline (i.e. the amplitude at t = 0ns) was subtracted. The complete measurement procedure was automated with a VEE program and the results are shown in figs. A.1 to A.5.

Obviously the undershoot or tail of a pulse is independent from V_{fs} and depends only on the parallel capacitance C_{p} and the preamplifier bias current I_{pre}. It was found that a pulse without remainder or undershoot is obtained for $I_{\mathrm{pre}} \propto \sqrt{C_{\mathrm{p}}}$. The absolute I_{pre} values for this condition are given in apx. D.1.

Sensitivity The sensitivity of the preamplifier is given by the peak value of the pulse shape. The results are depicted in fig. A.6. As a function of the three parameters C_{p}, I_{pre} and V_{fs} one finds:

$$A_Q = \frac{\alpha\sqrt{I_{\mathrm{pre}}}}{\sqrt{I_{\mathrm{pre}}} + (\beta + \gamma V_{\mathrm{fs}}) \cdot C_{\mathrm{p}}} \cdot \frac{\sqrt{I_{\mathrm{pre}}}}{\sqrt{I_{\mathrm{pre}}} + \delta V_{\mathrm{fs}}} \tag{5.4}$$

$\alpha, \beta, \gamma, \delta$ = Fit parameters.

The first term in eq. 5.4 represents the sensitivity of the charge sensitive am-

[4] Digital Storage Oscilloscope

plifier which depends on the charge sharing $\frac{A_V C_{\mathrm{fb}}}{A_V C_{\mathrm{fb}} + C_{Q_1} + C_{\mathrm{p}}}$. The second term represents the shaper gain $A_V \propto \frac{1}{R_{\mathrm{fb}}}$. From the measured data we find:

$$\begin{aligned} A_Q &= \frac{(0.160 \pm 0.016)\frac{\mathrm{V}}{24 \cdot 10^3\,\mathrm{e^-}} \cdot \sqrt{I_{\mathrm{pre}}}}{\sqrt{I_{\mathrm{pre}}} + C_{\mathrm{p}} \cdot \left((0.196 \pm 0.041)\,\frac{\sqrt{\mu\mathrm{A}}}{\mathrm{pf}} + (0,239 \pm 0.020)\,\frac{\sqrt{\mu\mathrm{A}}}{\mathrm{pf\ V}} V_{\mathrm{fs}} \right)} \cdot \\ &\cdot \frac{\sqrt{I_{\mathrm{pre}}}}{\sqrt{I_{\mathrm{pre}}} + (7.72 \pm 0.41)\frac{\sqrt{\mu\mathrm{A}}}{\mathrm{V}} V_{\mathrm{fs}}} \end{aligned}$$

Pulse Length The pulse length was defined as for eq. 3.23, i.e. the time between the beginning of the pulse and the signal reaching (or crossing) the baseline again. The pulse length increases linearly with C_{p}, with a slope independent from V_{fs}, as shown in fig. A.7. Therefore

$$t_{\mathrm{pulse}} = \frac{1}{\sqrt{I_{\mathrm{pre}}}} \left(\frac{\alpha}{V_{\mathrm{fs}} + \beta} + \frac{\gamma}{\sqrt{I_{\mathrm{pre}}}} C_{\mathrm{p}} \right) \tag{5.5}$$

α, β, γ = Fit parameters.

was fitted to the data, resulting in:

$$t_{\mathrm{pulse}} = \frac{1}{\sqrt{I_{\mathrm{pre}}}} \left(\frac{(3611 \pm 4)\mathrm{ns\ V}\ \sqrt{\mu\mathrm{A}}}{V_{\mathrm{fs}} + (0.933 \pm 0.002)\mathrm{V}} + \frac{(773 \pm 13)\frac{\mathrm{ns}\ \mu\mathrm{A}}{\mathrm{pF}}}{\sqrt{I_{\mathrm{pre}}}} C_{\mathrm{p}} \right).$$

Peak Time The peak time is also defined as for eq. 3.23, i.e. the time between the beginning of the pulse and its maximum. The measurement results are shown in fig. A.8. Again a linear increase with C_{p} is expected. From [Fal98] we know

$$t_{\mathrm{peak}} = \frac{\alpha + \beta C_{\mathrm{p}}}{\sqrt{I_{\mathrm{pre}}}\,(V_{\mathrm{fs}} + \gamma)}. \tag{5.6}$$

α, β, γ = Fit parameters.

The result of the fit is:

$$t_{\mathrm{peak}} = \frac{(1285 \pm 1)\mathrm{ns}\ \sqrt{\mu\mathrm{A}}\ \mathrm{V} + (24.7 \pm 1)\frac{\mathrm{ns}\ \sqrt{\mu\mathrm{A}}\ \mathrm{V}}{\mathrm{pF}} C_{\mathrm{p}}}{\sqrt{I_{\mathrm{pre}}}\,(V_{\mathrm{fs}} + (0.789 \pm 0.002)\mathrm{V})}$$

5.2.2 Noise

As already pointed out in sect. 3.3.1, noise are signals not caused by any external input to the device under test. Thus for noise measurements all disturbances caused by external signals have to be avoided. The standard approach to accomplish this is a thorough filtering of all power supplies, grounding and shielding the device inside a closed conductive box ([Ott81]). In case of the HELIX128's charge sensitive amplifier frontend this approach fails: The different load capacitances C_{p} cause different feedtrough from power supply lines,

which prevents common mode subtraction as a method to compensate for it. To overcome this, pairs of channels were equipped with the same parallel capacitor values C_p and the difference of their signals divided by $\sqrt{2}$ was used. This eliminates all problems with correlated disturbances, besides power supply feedtrough also including the loops caused by the screens of the IEEE488 cords and protective ground lines, leaving only uncorrelated signals. Like for the pulse shape measurements, 1000 measurements for each $I_\mathrm{pre} - V_\mathrm{fs}$ combination, yielding a statistical error of 3.1%, were performed by a VEE program. The equivalent input noise charge $\overline{ENC}$ is the measured noise divided by the measured sensitivity.

From eqs. 3.31 and 3.32 a linear increase of the $\overline{ENC}$ with C_p is expected and very well reproduced by the measurement results in fig. A.9 and tab. 5.4. The function

$$\overline{ENC} \quad = \quad \alpha \cdot C_\mathrm{p} \cdot \frac{V_\mathrm{fs} + \beta}{\sqrt[4]{I_\mathrm{pre}}} + \gamma \cdot \frac{V_\mathrm{fs} + \delta}{\sqrt[4]{I_\mathrm{pre}}} \tag{5.7}$$

$\alpha, \beta, \gamma, \delta =$ Fit parameters.

fitted to the measurement result can also be deduced from eqs. 3.31 and 3.32. The result is

$$\begin{aligned} \overline{ENC} \quad = \quad & (36.75 \pm 0.41)\, \frac{\mathrm{e}^- \sqrt[4]{\mu\mathrm{A}}}{\mathrm{pF\ V}} \cdot C_\mathrm{p} \cdot \frac{V_\mathrm{fs} + (3.33 \pm 0.41)\,\mathrm{V}}{\sqrt[4]{I_\mathrm{pre}}} + \\ & (299.8 \pm 0.4)\, \frac{\mathrm{e}^- \sqrt[4]{\mu\mathrm{A}}}{\mathrm{V}} \cdot \frac{V_\mathrm{fs} + (4.30 \pm 0.41)\,\mathrm{V}}{\sqrt[4]{I_\mathrm{pre}}} \end{aligned}$$

5.3 Characteristics of the irradiated Chip

5.3.1 Sensitivity

Figures A.10 to A.14 show the behaviour of the chips' sensitivity under irradiation. For very long pulses (i.e. $V_\mathrm{fs} = 0\mathrm{V}$) an essentially linear decrease was found. For doses $D \lesssim 2.5\mathrm{kGy}$ this behaviour is consistent with the decrease of the pulse length observed (cf. figs. A.15 to A.19). Dependent on the time between irradiation and measurement, a mostly linear decrease in sensitivity for doses $D \gtrsim 2\mathrm{kGy}$ was observed. It was most significant on daughtercard A, which was measured only a few hours after irradiation and almost imperceptible on daughtercard D, always measured a few days later (cf. fig. 5.10).

Since the respective pulse shapes do not show the corresponding changes, leakage currents in the pipeline, pipeline readout amplifier or the multiplexer's S&H stage have to account for this change. The decrease of this effect towards lower sensitivities (amplitudes) also supports this assumption.

5.3.2 Pulse Shapes

Pulse Length

The results of the measurement of the pulse length are shown in figs. A.15 to A.19. Except for very long pulses (i.e. $V_{\mathrm{fs}} = 0\mathrm{V}$, for which a minimum of the pulse length around 2.5kGy was found), the chips on daughtercard *A*, show a slight linear increase of the pulse length with the dose. The effect becomes stronger with increasing parallel capacitances and anneals after a few days, as the data from daughtercard D show (cf. fig. 5.10).

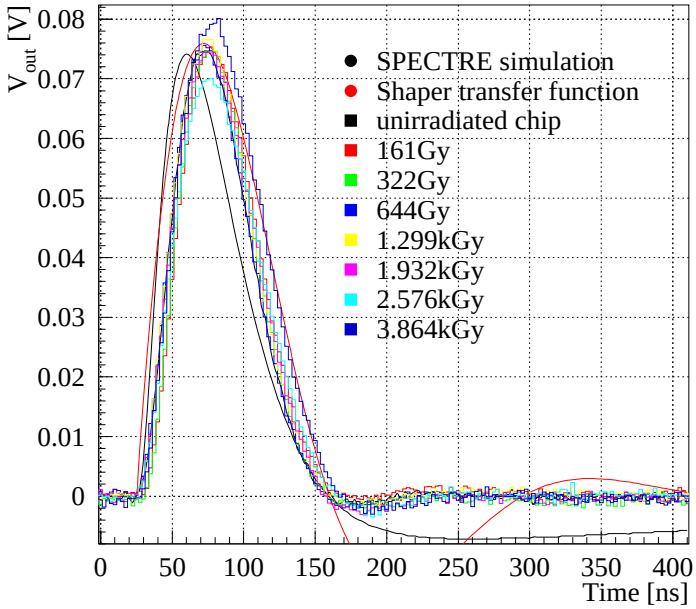


Figure 5.10: HELIX128-2's frontend response to a charge of $24 \cdot 10^3 e^-$ for the accumulated doses given. The parallel capacitance at the amplifier input is $C_{\mathrm{p}} = 16.3\mathrm{pF}$ and the bias current $I_{\mathrm{pre}} = 350\mu\mathrm{A}$. The data is from daughtercard *D*. The first two curves show the normalised results of a *Spectre* simulation and eq. 3.21 with α and β taken from the measured data for comparison.

A look at the schematic of the shaper (fig. 3.11) shows, that the source voltage of the n-MOS feedback transistor changes with the threshold voltage shift $\Delta V_{\mathrm{th_p}}$ of the p-MOS input transistor. Thus the effective gate voltage $V_{\mathrm{GSeff}} = V_{\mathrm{GS}} - V_{\mathrm{th_0}}$ of the feedback transistor changes by $-\Delta V_{\mathrm{th_p}} - \Delta V_{\mathrm{th_n}}$, i.e. the transistor is turned "on" and a decrease of the pulse length is expected instead of the slight increase observed. The degradation of the transconductance g_m on the other hand causes an increase of the pulse length, since the amplifier core becomes slower and the internal resistance R_{out} increases. But it is extremely unlikely that by accident both effects compensate each other, however, it would help to explain the results of the measurement.

Peak Time

Like for the pulse length, the peak time of the long pulses with $V_{\mathrm{fs}} = 0\mathrm{V}$ exhibits a weak minimum around 2.5kGy as the results depicted in figs. A.20 to A.24 show. For $V_{\mathrm{fs}} \gtrsim 0.5\mathrm{V}$ and low parallel capacitances $C_{\mathrm{p}} \lesssim 20\mathrm{pF}$ no significant change was found. For higher values of C_{p} a slight linear increase, always smaller than 5%/kGy, was observed. This is the behaviour expected from the radiation induced decrease of the transconductance g_{m} ($\approx 3.7\%/\mathrm{kGy}$).

5.3.3 Noise

The results of the noise measurement are shown in tab. 5.4 and figs A.25 and A.26. From the measurements of K'_{p} and eq. 3.17 we expect for the noise:

$$\begin{aligned} \overline{ENC}(D) &\approx \overline{ENC}_0 \cdot \sqrt{\frac{g_{\mathrm{m}_0}}{g_{\mathrm{m}}(D)}} \leq \overline{ENC}_0 \cdot \sqrt{\frac{K'}{K'(D)}} \\ &\approx (1 + (D \cdot 0.037/\mathrm{kGy})) \cdot \overline{ENC}_0 \end{aligned} \tag{5.8}$$

The measurement results for $C_{\mathrm{p}} = 0\mathrm{pF}$ (noise offset), which are shown in fig. A.25, show a much higher increase of about $67\mathrm{e}^-/\mathrm{kGy}$, independent from $\overline{ENC}_0$ (i.e. I_{pre} and V_{fs}). On the daughtercard A further excess noise was observed at 3.9kGy. It is caused by the "*End Around*" leakage path (cf. sect. 4.3.1) in the preamp's feedback transistor, which prevents V_{fp} to be adjusted to the cut off point (proven by fig. D.3). The resulting low parallel resistance in eqs. 3.15 and 3.16 causes the additional increase in noise.

The slope of the noise (i.e. $\frac{d\,\overline{ENC}}{d\,C_{\mathrm{p}}}$) shown in fig. A.26 also increases with the dose. From eq. 3.33 it is expected to be independent from R_{fb} and thus from the "*End Around*" leakage path found there. Indeed no excess noise was found at 3.9kGy.

Like for the offset, the increase exceeds the $0.037 \cdot \frac{\overline{ENC}_0}{C_{\mathrm{p}}}/\mathrm{kGy}$ expected from the degradation of g_{m}. Furthermore, the increase is less for short pulses (i.e. higher values of V_{fs}) than for long ones, as shown by fig. A.26.

Both slope and offset of the noise degrade more than expected from the change of g_{m} and by about the same factor. Thus additional noise sources or degradation mechanisms (e.g. resistances deteriorating g_{m} in eq. 3.17) have to be considered. Similar descrepancies are reported e.g. in [Fal93].

5.3.4 Power Consumption

The results from total power consumption measurements depicted in fig. 5.12 clearly show the effects of annealing: The increase is much steeper for the short (≈ 1 week) irradiation intervals than for the longer ones (cf. tab. 5.1). The current mirror biased analogue stages show no increase of the power consumption. For the digital ones an increase due to leakage currents is observed, which can be annealed, as the curve of the daughtercard B in fig. 5.13b shows. The lack of annealing also accounts for the upward bent of the $V_{\mathrm{ss}}A$ and $V_{\mathrm{ss}}D$ curves at 3.8kGy in fig. 5.12.

V_{fs}	0.0V		0.5V		1.0V		1.5V		2.0V	
I_{pre}	$\overline{ENC} = a[e^-] + b[e^-/\mathrm{pF}] \cdot C_{\mathrm{p}}[\mathrm{pF}]$									
µA	a	b	a	b	a	b	a	b	a	b
0Gy										
100	350.1	30.75	456.2	43.72	531.3	51.71	571.2	56.58	615.2	58.70
200	294.4	26.74	388.6	34.62	415.8	42.83	454.1	45.50	499.7	52.03
300	284.7	16.92	356.4	33.72	406.9	38.91	452.2	37.59	473.2	43.87
400	298.1	14.84	337.7	30.70	376.9	36.31	410.1	40.32	419.0	41.71
500	262.2	23.81	310.5	31.97	365.9	34.25	392.0	36.63	436.6	38.75
600	248.5	23.63	320.3	29.64	350.9	34.27	393.7	35.86	384.5	39.98
1288Gy										
100	460.3	43.50	574.0	50.34	622.3	57.13	648.6	65.17	766.2	63.87
200	414.7	38.39	476.1	44.50	530.0	48.47	583.2	51.88	614.0	61.16
300	373.6	35.12	462.5	38.77	472.7	44.08	522.0	47.69	556.3	46.53
400	357.6	34.55	410.9	40.37	443.7	43.71	476.2	44.49	517.2	46.22
500	361.8	30.89	404.7	36.57	409.2	43.67	477.0	42.00	483.8	44.10
600	353.4	30.90	400.3	36.44	428.6	37.67	463.4	41.51	485.6	41.89
2576Gy										
100	584.7	52.84	614.5	61.56	700.7	62.35	693.8	73.07	796.7	71.31
200	504.6	49.98	564.8	53.16	628.8	54.82	629.5	58.42	675.4	66.10
300	519.7	44.45	549.6	48.53	578.2	51.49	604.0	54.15	620.9	53.60
400	461.2	40.30	509.1	46.74	507.9	51.67	558.8	49.50	591.4	49.97
500	428.6	40.87	487.1	45.14	538.4	45.24	563.0	46.62	601.3	48.51
600	433.9	40.12	492.1	44.01	520.7	47.07	558.8	46.18	570.1	51.85
3864Gy										
100	767.0	60.99	832.8	63.56	911.3	66.99	856.6	80.46	1005	72.79
200	740.0	49.95	797.4	56.27	867.4	56.24	878.2	62.79	958.6	68.85
300	719.8	51.06	758.2	57.54	809.8	59.01	890.5	59.10	881.4	60.46
400	739.4	50.66	827.1	53.34	903.3	54.41	917.4	56.40	938.6	58.24
500	781.1	46.19	819.7	52.63	845.3	58.65	937.0	53.25	871.9	59.91
600	816.0	49.19	886.6	51.30	898.1	57.12	970.9	53.27	952.5	56.17

Table 5.4: $\overline{ENC}$ of HELIX128-2.2 (cf. figs. A.25 and A.26).

5.3.5 Node Voltages

To understand the radiation induced changes on HELIX128 one would like to know about the voltage changes on its internal nodes. Unfortunately, only a very few of them are accessible. Their voltages were monitored.

The HELIX128's test channel is identical to the chip's 128 input channels, except that its output connects to a pad instead of the pipeline. Its output voltage drops with the accumulated dose almost like the threshold voltage of a p-MOS FET, as fig. 5.14 shows. Indeed, the shaper's input transistor is a p-MOS and can account for the over-all behavior, which has to be compared to the results in section 5.3.2. The threshold voltages of Q_5 in fig. 3.11 and Q_1 in fig. 3.13 are in parallel and are expected to compensate. The curve can be used as a reference for the `Vd` adjustment (cf. appendix D.7).

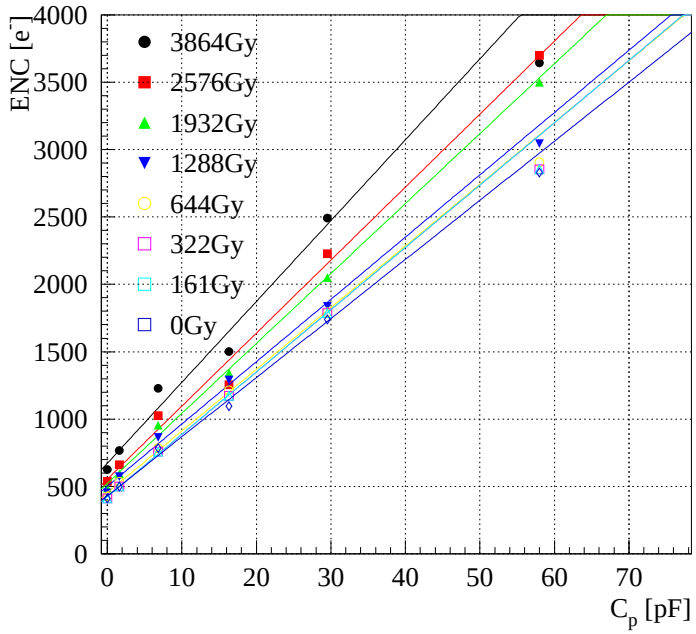


Figure 5.11: HELIX128-2.2 noise for the doses indecated, bias settings are $I_{\text{pre}} = 350\mu\text{A}$ and $V_{\text{fs}} = 1.5\text{V}$ (daughtercard D).

The `IrefIn` pad is the drain node of a diode connected n-MOS FET. Since it was bonded to the `IrefOut` pad, the fixed current prevented the extraction of transistor characteristics. Thus, its voltage shown in fig. 5.15 follows the threshold voltage shift of an n-MOS. Except for the highest dose, the curve nicely follows the same shifts as the n-MOS test structures' threshold voltage given in tab. 5.2 and fig. 5.8.

The voltage drop across the reference resistor of the HELIX128's current source should by design not change with irradiation, since the current has to be constant. This is shown in fig. 5.16.

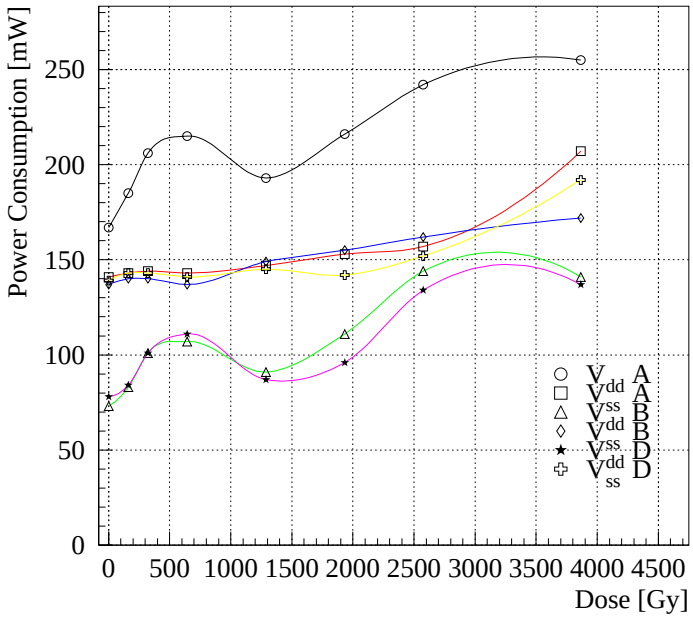


Figure 5.12: Power consumption of HELIX128-2. The curves are from daughtercards *A*, *B* and *D*. The offset of ≈ 90mW of $V_{\mathrm{dd}}D$ (which has to be lower than $V_{\mathrm{ss}}D$) is due to a bad blocking capacitor.

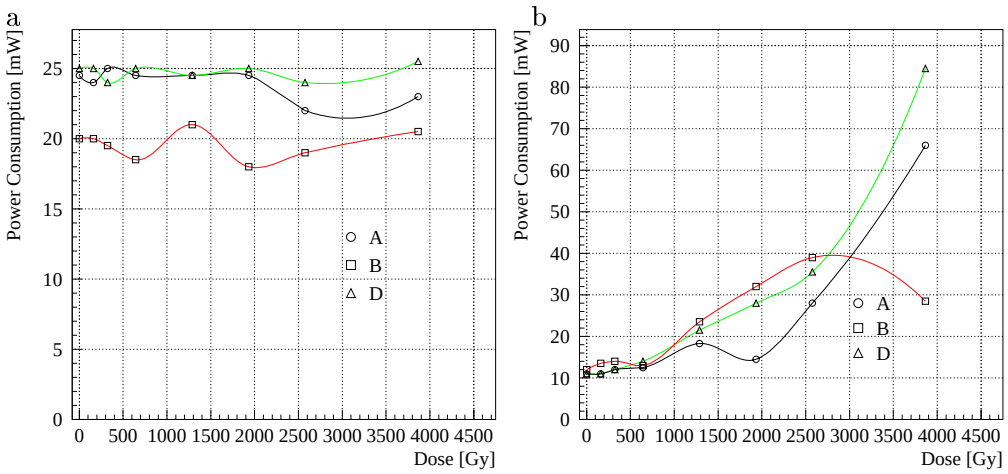


Figure 5.13: Power consumption of HELIX128-2: Data form daughtercards *A*, *B* and *D*. Left graph shows some analogue stages in the rear part of the chip, right graph shows the digital circuits. It clearly shows the annealing of the "*End Around*" leakage current on daughtercard *B* (cf. sect. 4.3.1).

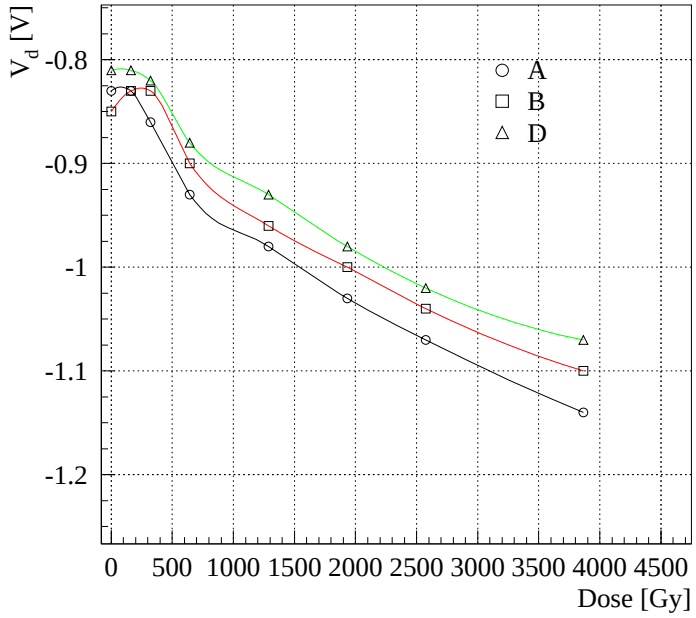


Figure 5.14: Offset voltage of the HELIX128's test channel.

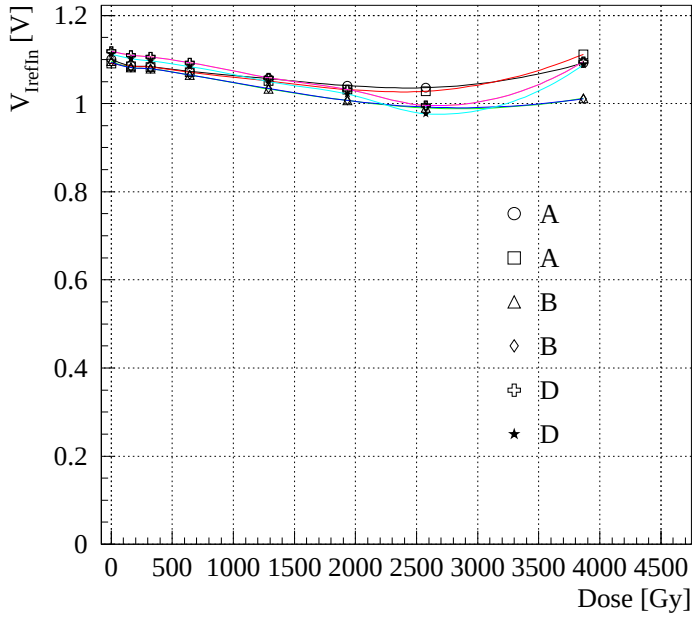


Figure 5.15: Voltage of the HELIX128's reference current input `IrefIn`. Data from the chip pairs on daughtercards *A*, *B* and *D*

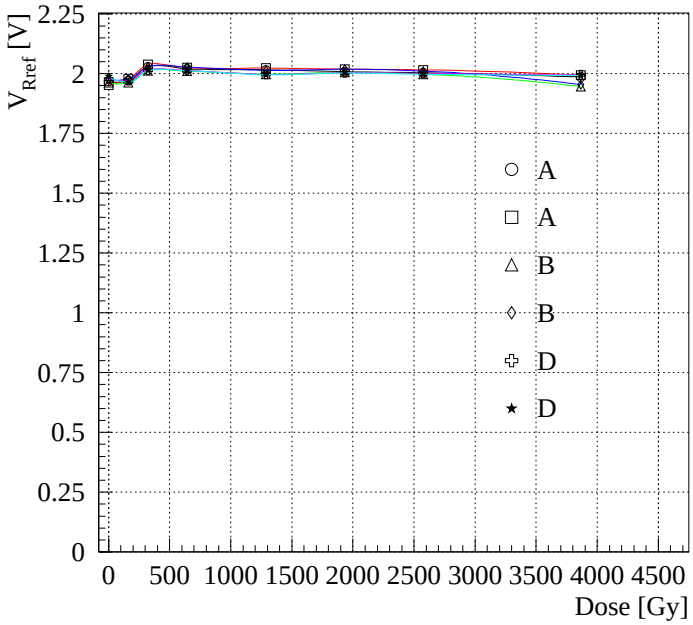


Figure 5.16: Voltage drop over the reference resistor of HELIX128's reference current source. Data from the chip pairs on daughtercards *A*, *B* and *D*.

5.4 Conclusions

The behaviour of HELIX128-2.2 before irradiation is well understood and in good agreement with theoretical calculations. The noise, which was found $462e^- + 35.4e^-/pF$[5] and the pulse shapes are well reproduced by eqs. 5.4...5.7.

Noise Measurements of the irradiated chip show an increase larger than expected from degradation of $\overline{\mu}$. From the mobility an increase of $\overline{ENC}$ to about $1.14 \cdot \overline{ENC_0}$ at 3.9kGy is expected.

Instead a much higher increase to about $1.4 \ldots 1.8 \cdot \overline{ENC_0}$ (i.e. to $571e^- + 52.0e^-/pF$) at 3.9kGy was found. This is only half of the degradation measuered for chips produced in technologies with a larger feature size like e.g. VIKING 2 (1.5µm Mietec process) [Fal93].

The excess noise for the $\overline{ENC}$-offset at 3.9kGy was found to be due to the "*End Around*" leakage path in the preamplifier's feedback, which decreases R_p. Annealing removes this problem.

However, such leakage currents are also expected in the n-MOS transistors of the preamplifier's load branch (cf. fig 3.8), where they can also contribute to the increase of the noise slope.

Table 5.5 permits an extrapolation of the expected noise for arbitrary doses.

V_{fs}	0.0V		0.5V		1.0V		1.5V		2.0V	
I_{pre}	$\overline{ENC}(D) = \overline{ENC_0} + (a \cdot 10^{-2}[\frac{e^-}{Gy}] + b \cdot 10^{-3}[\frac{e^-}{pF\,Gy}] \cdot C_p[pF]) \cdot D[Gy]$									
µA	a	b	a	b	a	b	a	b	a	b
100	7.86	7.65	5.21	5.06	5.72	3.54	3.10	5.38	3.74	3.86
200	7.66	6.36	5.95	5.05	6.38	3.66	5.49	4.37	4.78	4.24
300	6.36	6.20	4.86	5.85	4.29	4.76	4.00	4.47	4.11	4.06
400	5.37	6.75	5.98	5.23	3.93	4.82	4.25	4.47	4.84	3.98
500	5.94	6.10	6.17	5.53	5.61	6.04	5.07	4.34	5.89	4.51
600	5.39	6.61	5.32	5.06	5.15	6.34	4.46	4.22	5.35	4.93

Table 5.5: Increase of $\overline{ENC}$ with dose for HELIX128-2.2 from fits to figs. A.25 and A.26. $\overline{ENC_0}$ is the noise of the unirradiated chip.

The observed change of the pulse shape with irradiation is small and vanishes after annealing of "*End Around*" leakage currents assumed in the shaper's feedback transistor.

The pipeline n-MOS read and write switches are also candidates for "*End Around*" leakage currents. A discharge of the storage capacitors for times $\geq$ 4.8ms could not be observed. These switches are open almost all the time. The gate–source voltage in that case is $V_{GS} \ll 0V$, which prevents the detrimental charge accumulation at the channel ends.

The pipeline readout amplifier of HELIX128-2.2 did not exhibit the radiation tolerance problems of its predecessors. The pipeamp causes only a small contribution to the noise offset, which can not be seperated from that of the preamplifier.

[5] under HERA-B conditions (i.e. $t_{fall} \approx 100$ns at $C_p = 16.3$pF and $I_{pre} = 350$µA)

For the multiplexer and the current output buffer no degradation with radiation could be found.

An impact of V_{th}-shifts on the chips performance could not be found. This is due to the fixed bias current concept used for all analogue stages.

A detailed strategy to minimize the impact of radiation effects on the chip's performance are given in appendices C and D.

A second effect of the irradiation is the increase of the power consumption. The measurements clearly indicate that the increase is mainly due to "*End Around*" leakage currents in digital circuits. This effect also puts up the limit for the radiation tolerance of the chip, which is > 5.1kGy. The power consumption of constant current biased analogue stages remained unchanged.

Chapter 6

Summary

During the work for this thesis, major parts of the HELIX128-2.2 readout chip were developed and the complete chip was improved throughout various revisions. It resulted in a up to $\approx$ 4kGy radiation tolerant chip manufactured in a commercial non-radiation hard technology.

Due to the moderate cost, it is especially suited for applications requiring a periodic replacement of detectors and their readout electronics, like in the HERA-B VDS.

It fulfills all requirements of the HERA-B silicon vertex detector and inner tracking system, especially

- Radiation tolerance up to $\approx$ 4kGy
- Noise (increasing from $462e^- + 35.4e^-/\mathrm{pF}$[1] for a new chip to $571\mathrm{e}^- + 52.0\mathrm{e}^-/\mathrm{pF}$[1] at 3.9kGy).
- Latency of 128 clock cycles.
- Dead-time free operation due to a derandomiser buffer for 8 triggered events.
- Sufficiently sensitive comparators to derive trigger signals.
- Daisy chained analogue readout at up to 40MHz speed.
- Convenient programming of operational parameters for remote control.
- Seamless integration into the HERA-B DAQ system.

The noise increases linear with dose, which is also reported for other readout chips [Fal93]. Though meeting the specs, this increase turned out to be higher than expected from the degradation of transistor's transconductance g_m. The latter was assumed to be the dominating contribution at the beginning of the development. As a reason for the remaining increase additional noise sources or mechanisms deteriorating g_m in the input transistors' series noise density have to be assumed.

[1] for $C_\mathrm{p} < 58\mathrm{pF}$ under HERA-B conditions (i.e. $t_\mathrm{fall} \approx 100\mathrm{ns}$ at $C_\mathrm{p} = 16.3\mathrm{pF}$ and $I_\mathrm{pre} = 350\mu\mathrm{A}$)

All radiation tolerance related problems in analogue stages have been solved, either by design (e.g. in the pipeamp) or a sufficient safety margin (in the front end).

The digital circuits are even stronger affected by radiation damage. These circuits suffer from "*End Around*" leakage currents, which increase power consumption and deteriorate the functionality especially of the minimum size transistors used there. There are no viable solutions to increase the radiation tolerance of those components, which limits the radiation tolerance of the complete chip.

To facilitate the constant current biasing required for radiation tolerant analogue circuits, and to establish a convenient operation of the chip, a bias generator block, delivering bias currents and control voltages was developed and integrated on HELIX128 as a part of this thesis. As a component of this block, also a radiation hard current source in radiation-soft technology was developed and implemented. Furthermore, digital circuits to monitor SEU failures and to set up the chips operation mode, as well as a serial interface to control them have been developed and implemented.

The subsequent characterisation and irradiation tests led to various improvements, resulting in the versions HELIX128-2.2, 2.3, 3.0, 3.1 and 3.1a. Within that context not only the insufficient radiation tolerance of the 2.1's pipeamp was detected, but also many hidden bugs in the pipeline read/write control circuit were discovered and fixed.

Furthermore, recommendations for bias currents and control voltages have been extracted from irradiation results (see appendix D).

About 350 wafers (or 21,000 chips) have been manufactured and tested since April 1998. The yield for perfect (i.e. no dead channels or pipeline cells) chips was found to be about 57% [Dep]. About 1,056 HELIX128-2.2 chips have been successfully operated in the HERA-*B* silicon vertex detector for almost two years now, while the complete VDS will contain 1,152 HELIX128 chips in 2001.

Outlook

Since the pulse shape of its frontend matches the *bunch crossing* frequency of the HERA storage ring and the ease of operation, the chip was also chosen for the ZEUS micro vertex detector and an upgrade of the HERMES experiment. Furthermore, a binary readout chip for H1's central inner proportional chamber upgrade was derived from it by removing the analogue readout [Bau99][Löc98].

In the long term, commercially available deep sub-µm processes, which are intrinsically radiation hard will become the technology of choice for applications in radiative environments. These technologies provide enough space for edgeless transistors in digital circuits to eliminate the detrimental "*End Around*" leakage currents there.

In turn the ongoing development of a readout chip for the LHC*b* vertex locator and inner tracking detectors uses a deep sub-micron technology together with the pipeline r/w control algorithm and the schematic of the bias generator circuits developed for the HELIX128.

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Ulrich Trunk

Appendix A

Measurement Data

A.1 Data of the unirradiated Chip

Pulse shapes figs. A.1 to A.5

Sensitivity fig. A.6

Pulse length fig. A.7

Peak time fig. A.8

Noise fig. A.9

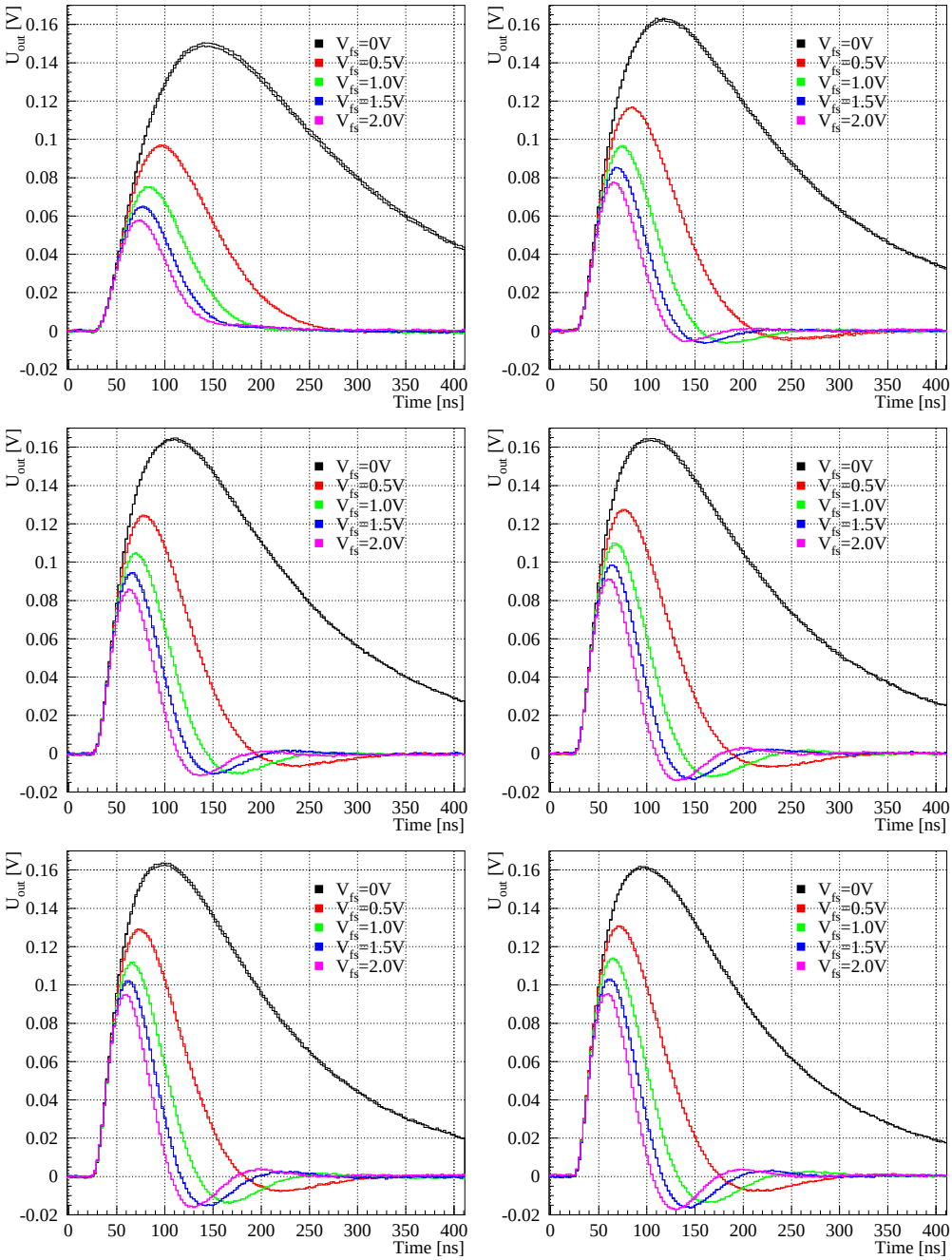

Figure A.1: HELIX128-2.2 pulse shape scan for different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). The parallel capacitance attached to the amplifier input is caused by the coupling capacitor (i.e. $C_{\mathrm{p}} = 1.6\mathrm{pF}$).

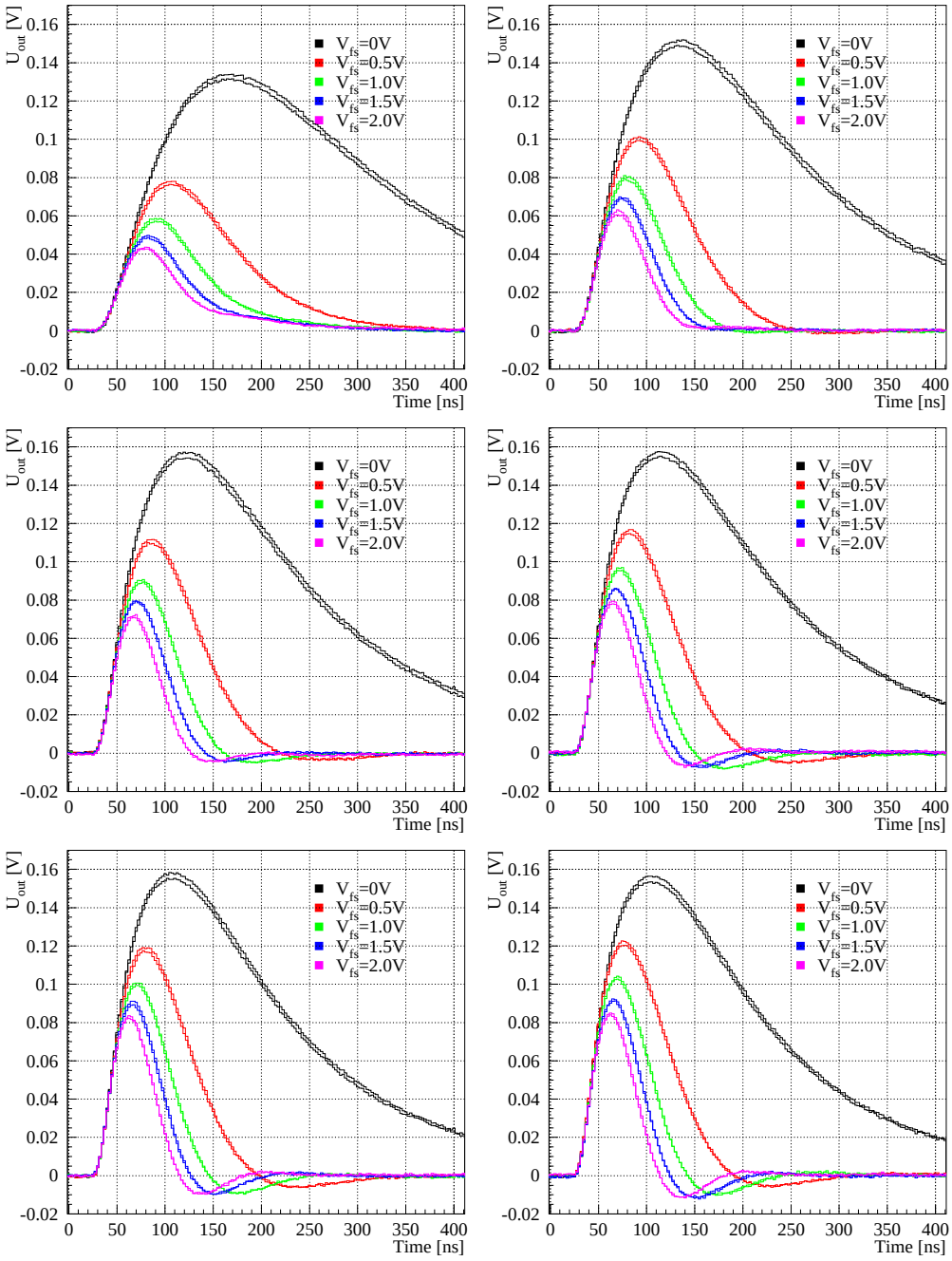

Figure A.2: HELIX128-2.2 pulse shape scan for different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 6.8\mathrm{pF}$.

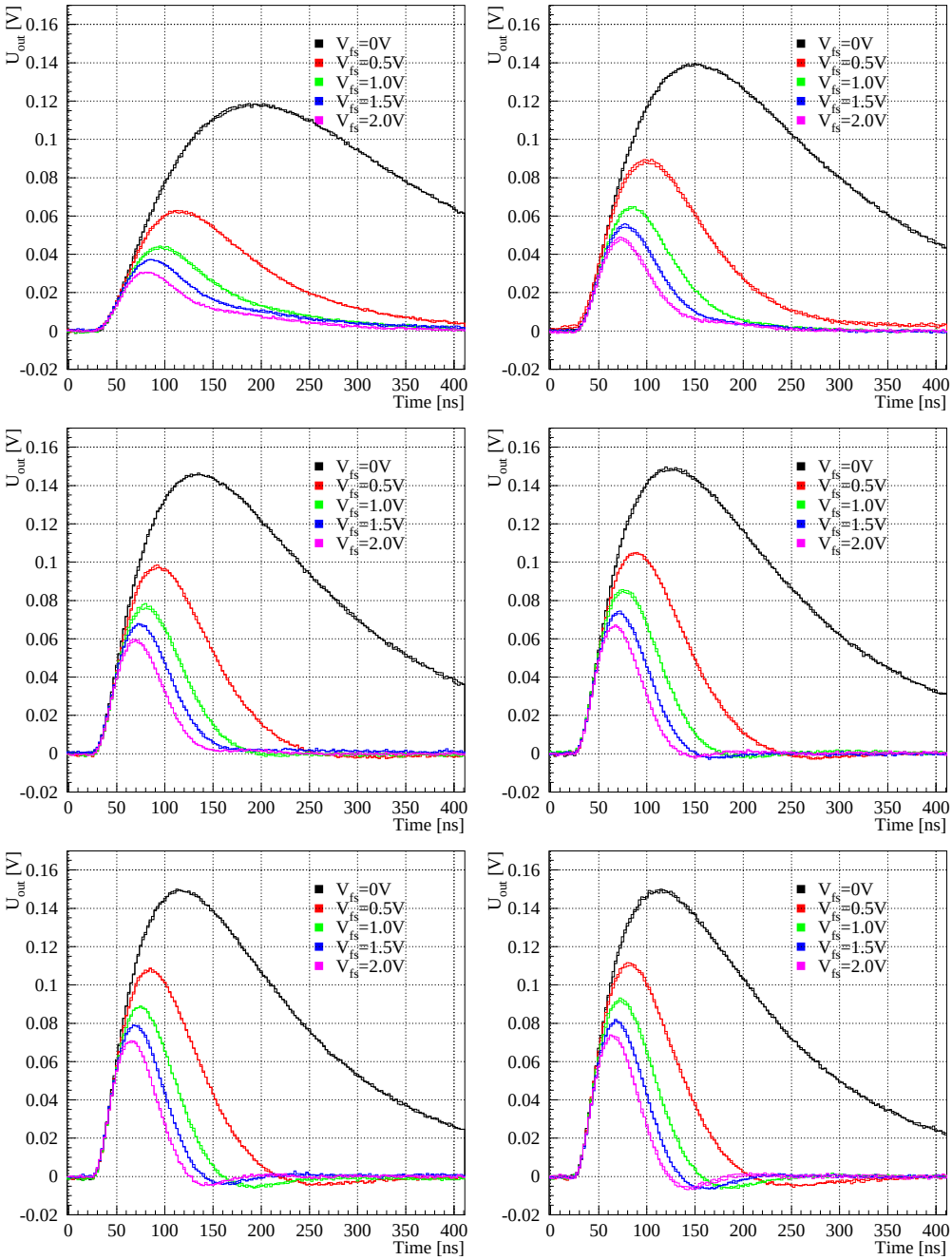

Figure A.3: HELIX128-2.2 pulse shape scan for different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 16.3\mathrm{pF}$.

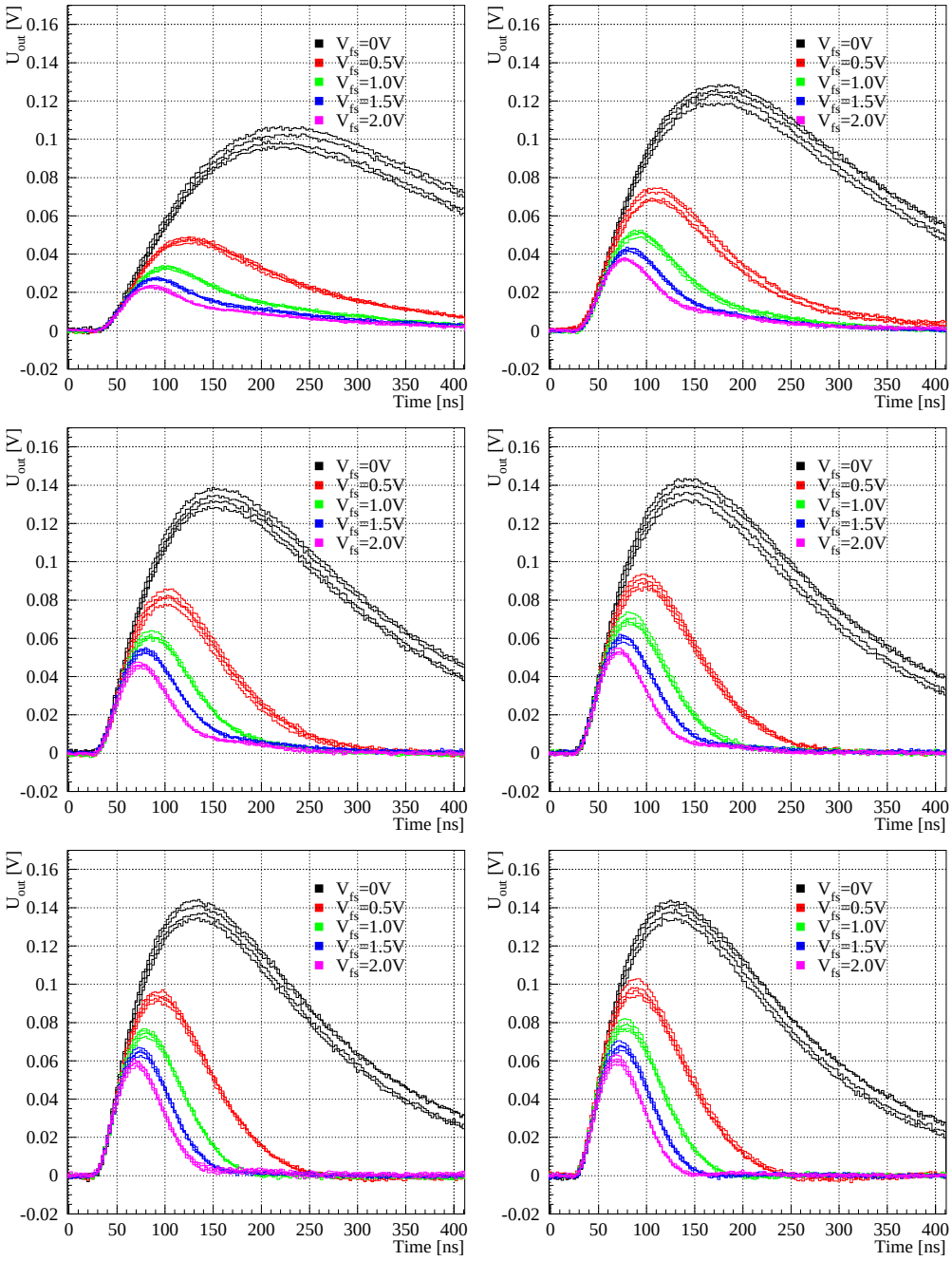

Figure A.4: HELIX128-2.2 pulse shape scan for different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 29.4\mathrm{pF}$.

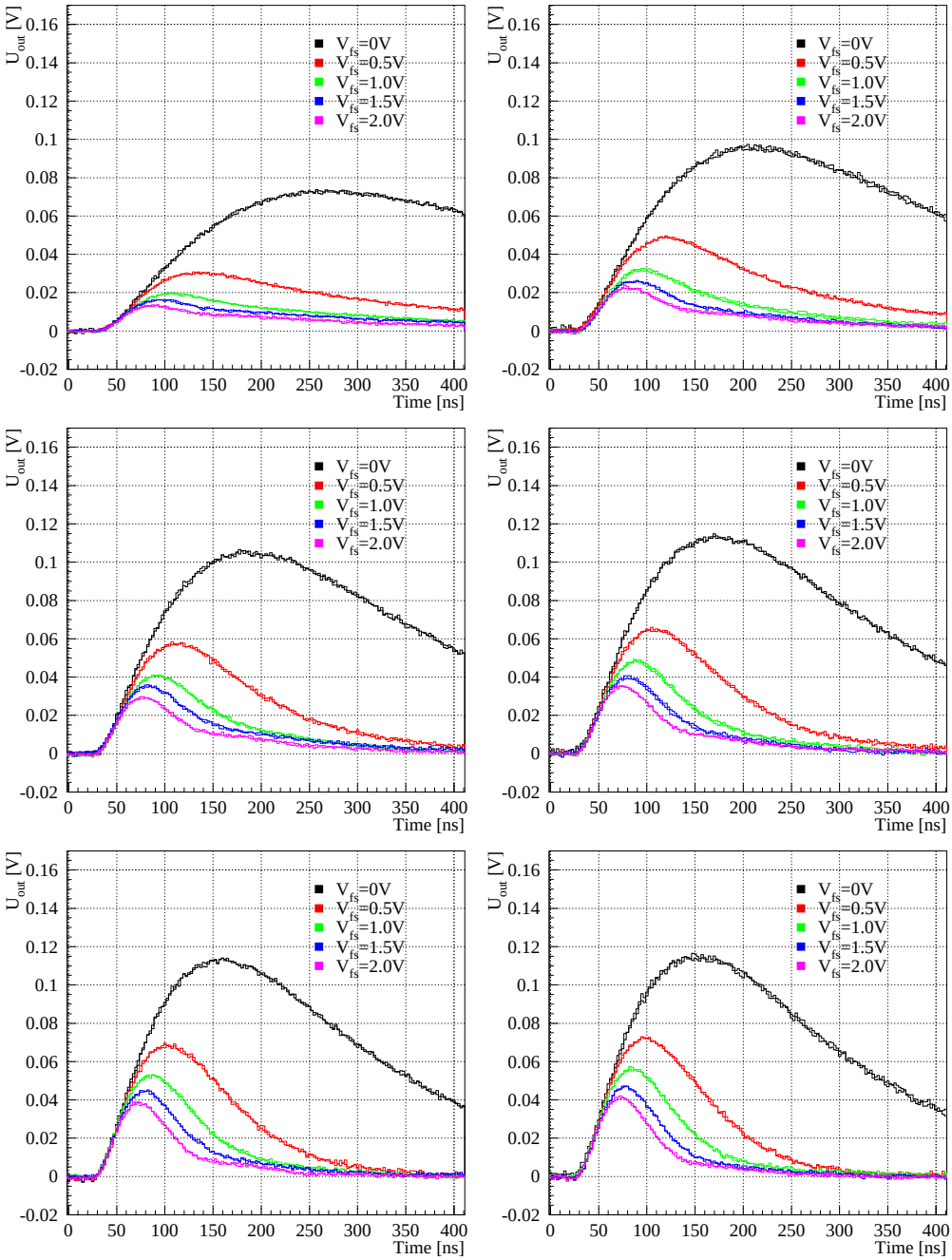

Figure A.5: HELIX128-2.2 pulse shape scan for different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 58\mathrm{pF}$.

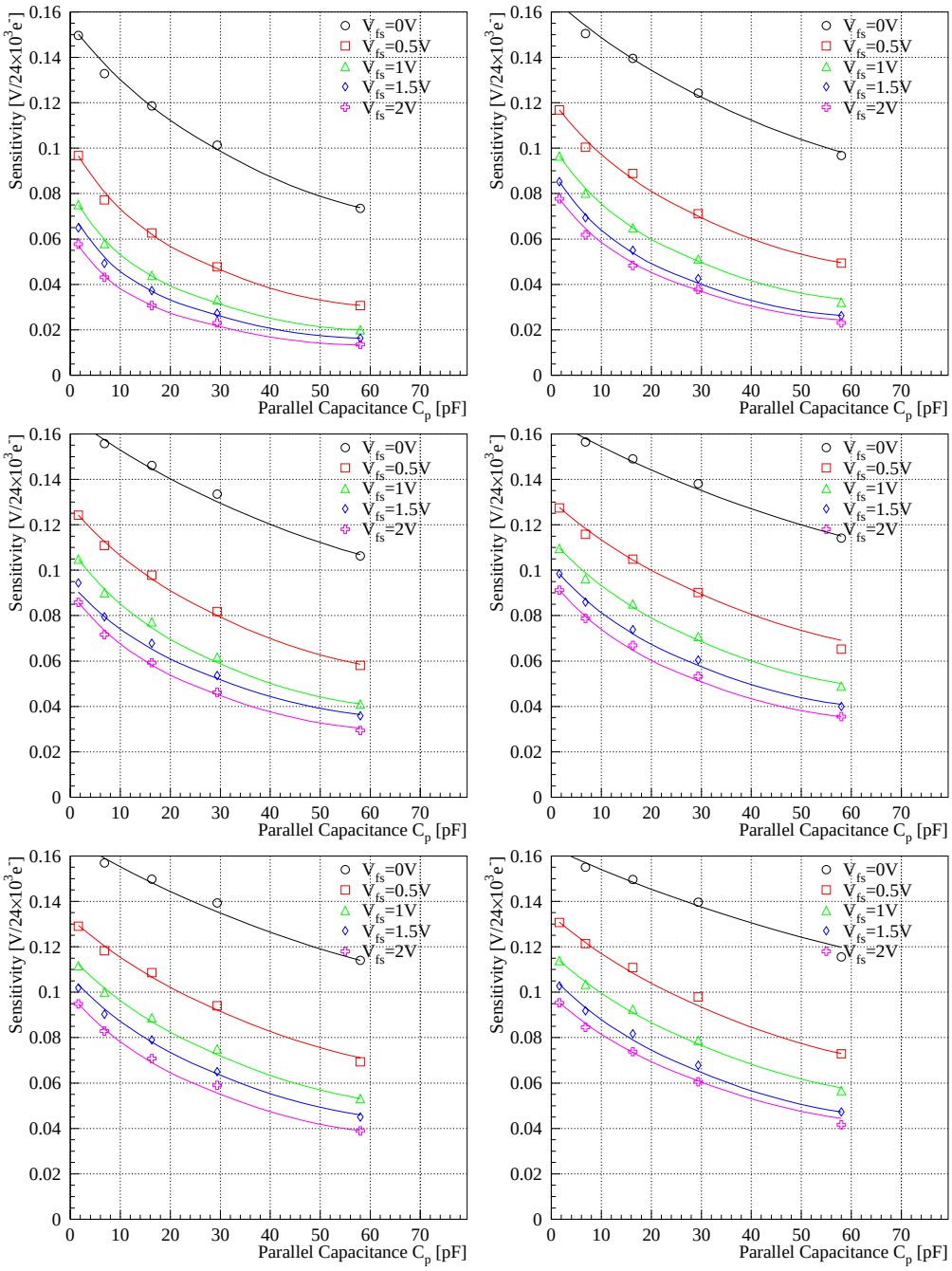

Figure A.6: Sensitivity of the HELIX128-2.2 as a function of the parallel capacitance. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, 200µA, 300µA, 400µA, 500µA and 600µA (from top left to bottom right). The curves are fits showing the $1/C_{\mathrm{p}}$ behaviour of the data.

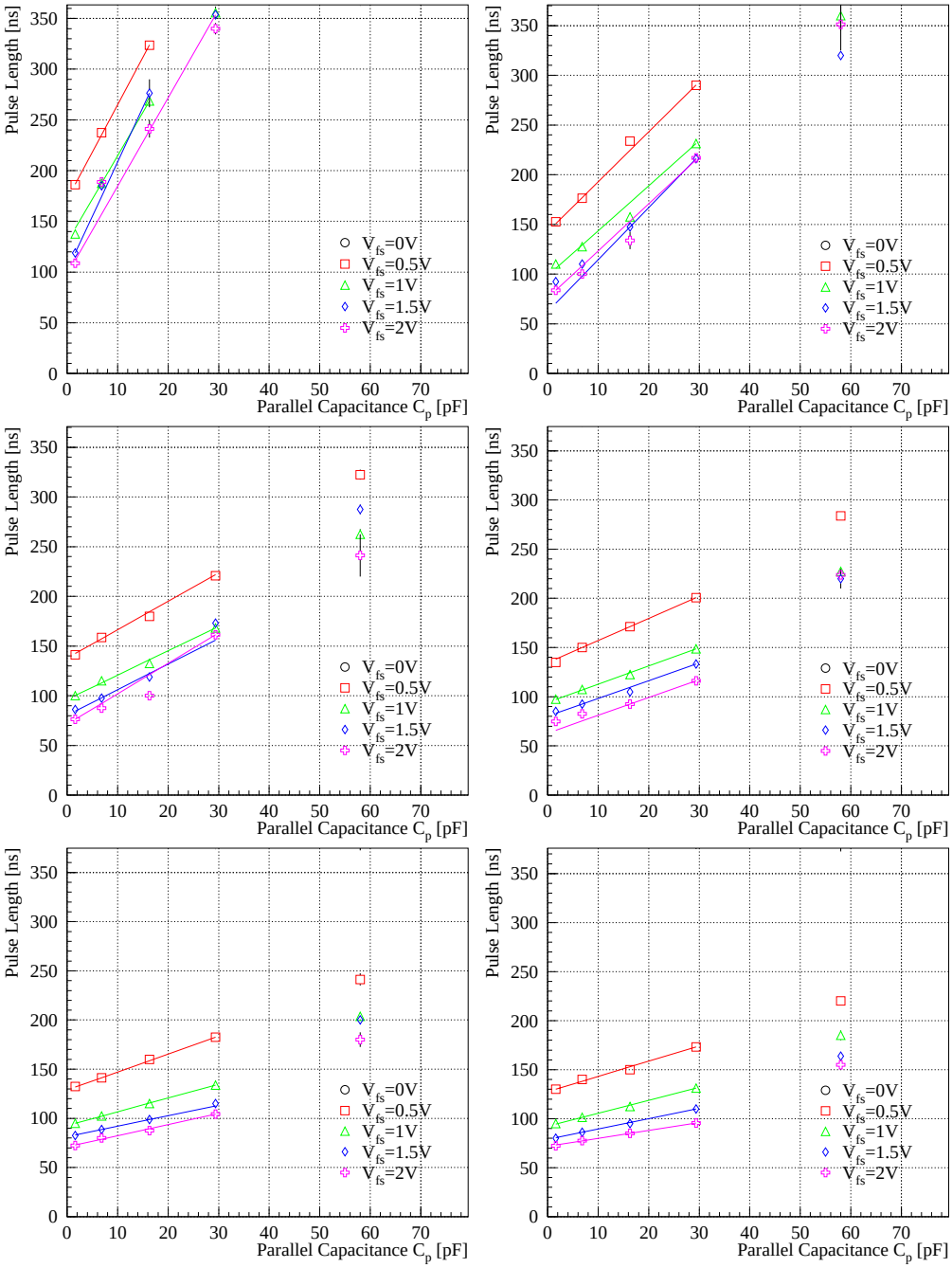

Figure A.7: Pulse Length (as defined in eq. 3.23) of the HELIX128-2.2 as a function of the parallel capacitance. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). Pulse lengths $t_{\mathrm{pulse}} \gg 350\mathrm{ns}$ could not be determined due to the measurement window of 410ns. The curves are linear fits to the data.

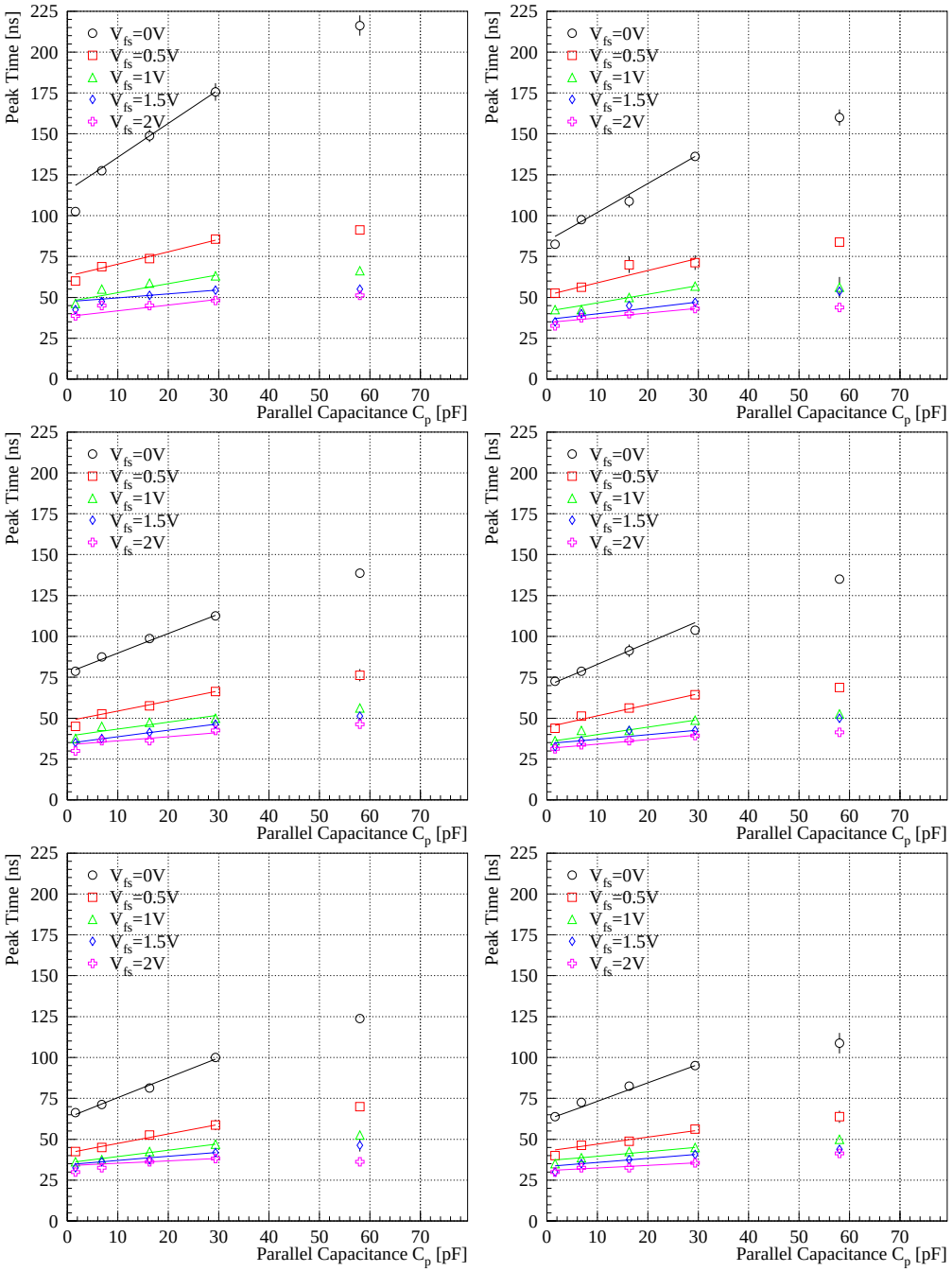

Figure A.8: Peak time (as defined in eq. 3.22) of the HELIX128-2.2 as a function of the parallel capacitance. The graphs represent different preamplifier bias currents: I_{pre} = 100µA, 200µA, 300µA, 400µA, 500µA and 600µA (from top left to bottom right). The curves are linear fits to the data.

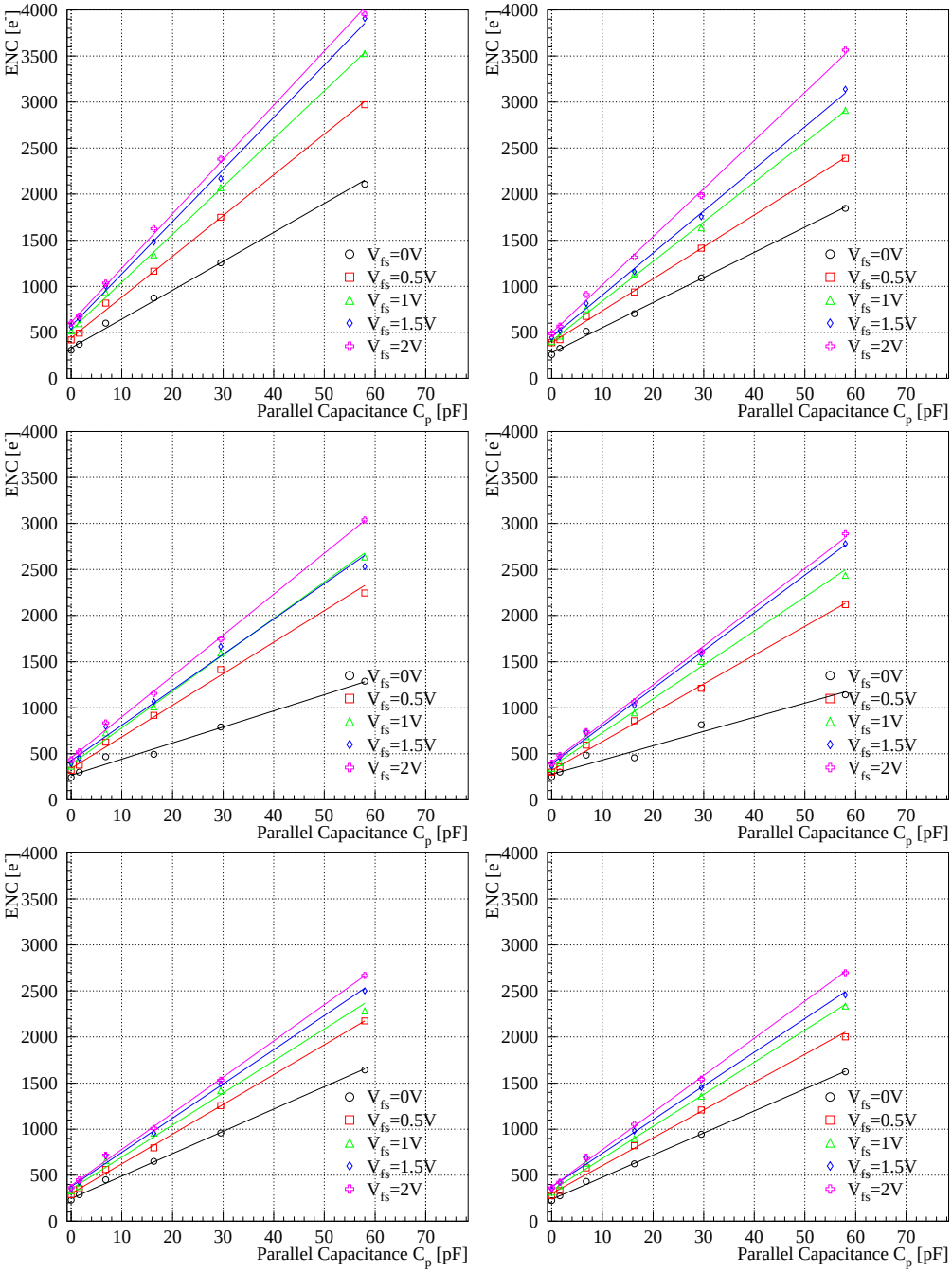

Figure A.9: Equivalent noise charge ($\overline{ENC}$) of the HELIX128-2.2 as a function of the parallel capacitance. The graphs represent different preamplifier bias currents: I_{pre} = 100µA, 200µA, 300µA, 400µA, 500µA and 600µA (from top left to bottom right). The curves are linear fits to the data.

A.2 Data of the irradiated Chip

Sensitivity figs. A.10 to A.14

Pulse length figs. A.15 to A.19

Peak time figs. A.20 to A.24

Noise figs. A.25 and A.26

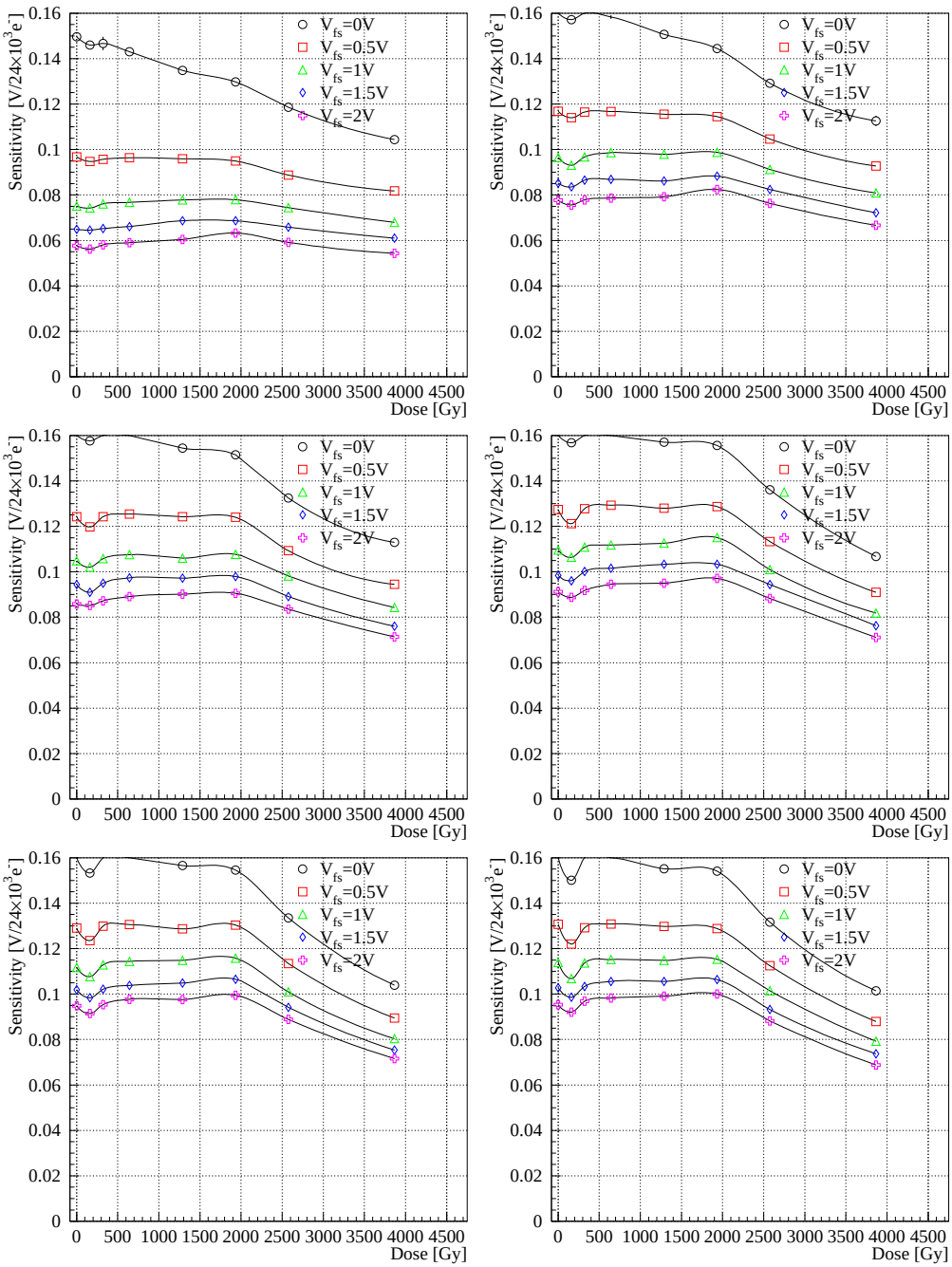

Figure A.10: Sensitivity of the HELIX128-2.2 as a function of the accumulated dose. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu A$, $200\mu A$, $300\mu A$, $400\mu A$, $500\mu A$ and $600\mu A$ (from top left to bottom right). The coupling capacitor for charge injection causes a parallel capacitance of $C_{\mathrm{p}} = 1.6pF$.

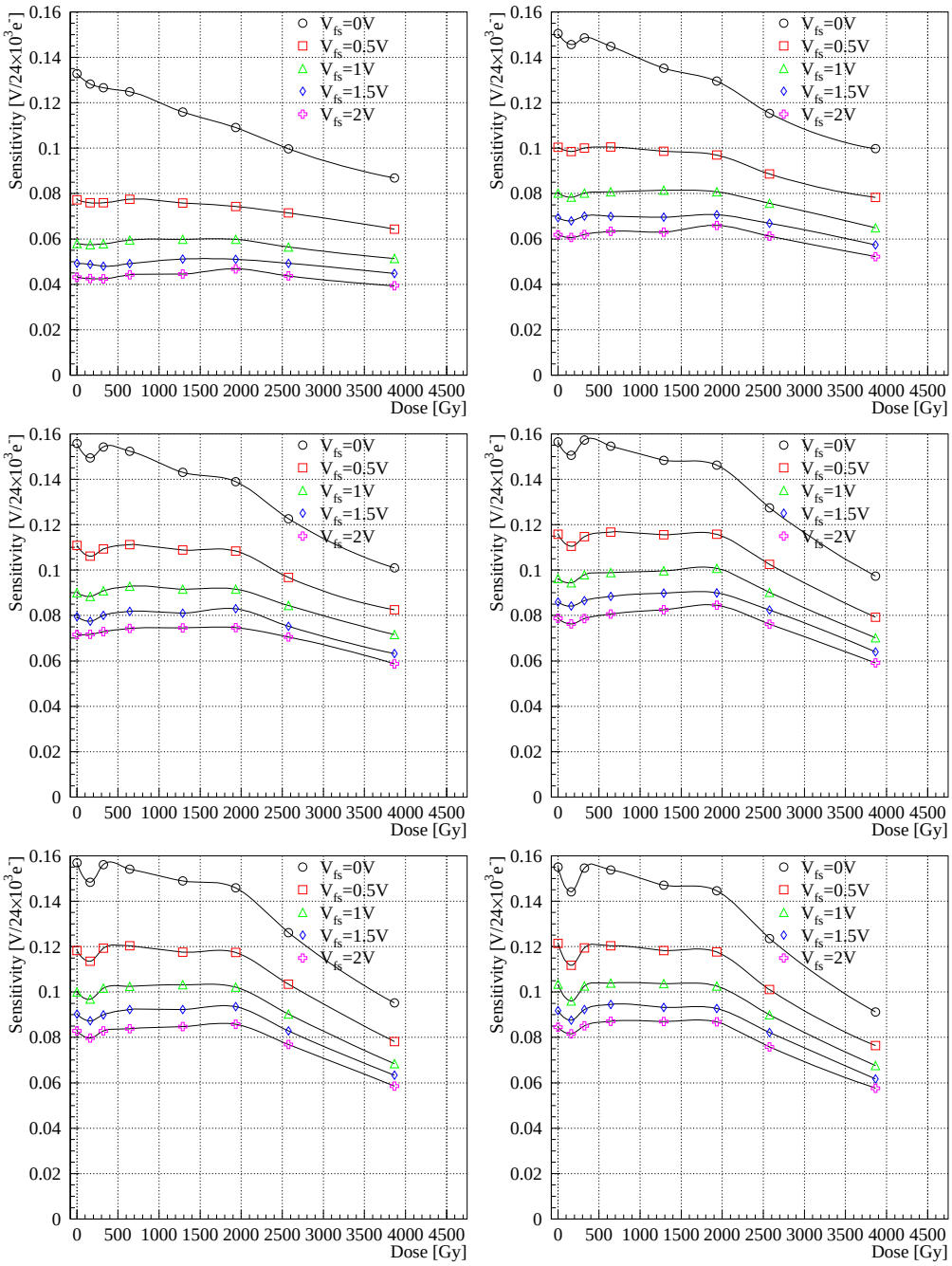

Figure A.11: Sensitivity of the HELIX128-2.2 as a function of the accumulated dose. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, 200µA, 300µA, 400µA, 500µA and 600µA (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 6.8\mathrm{pF}$.

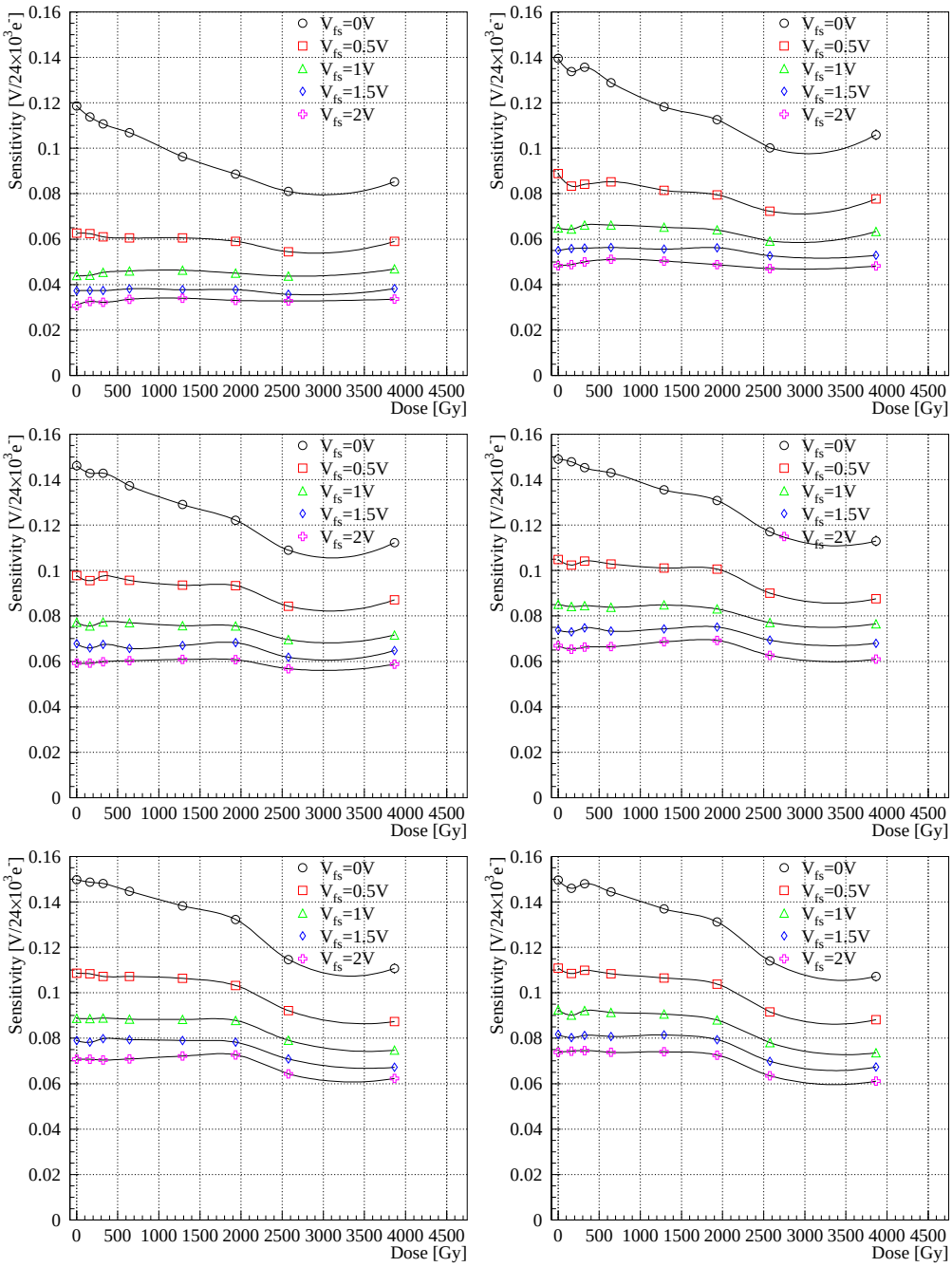

Figure A.12: Sensitivity of the HELIX128-2.2 as a function of the accumulated dose. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, 200µA, 300µA, 400µA, 500µA and 600µA (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 16.3\mathrm{pF}$.

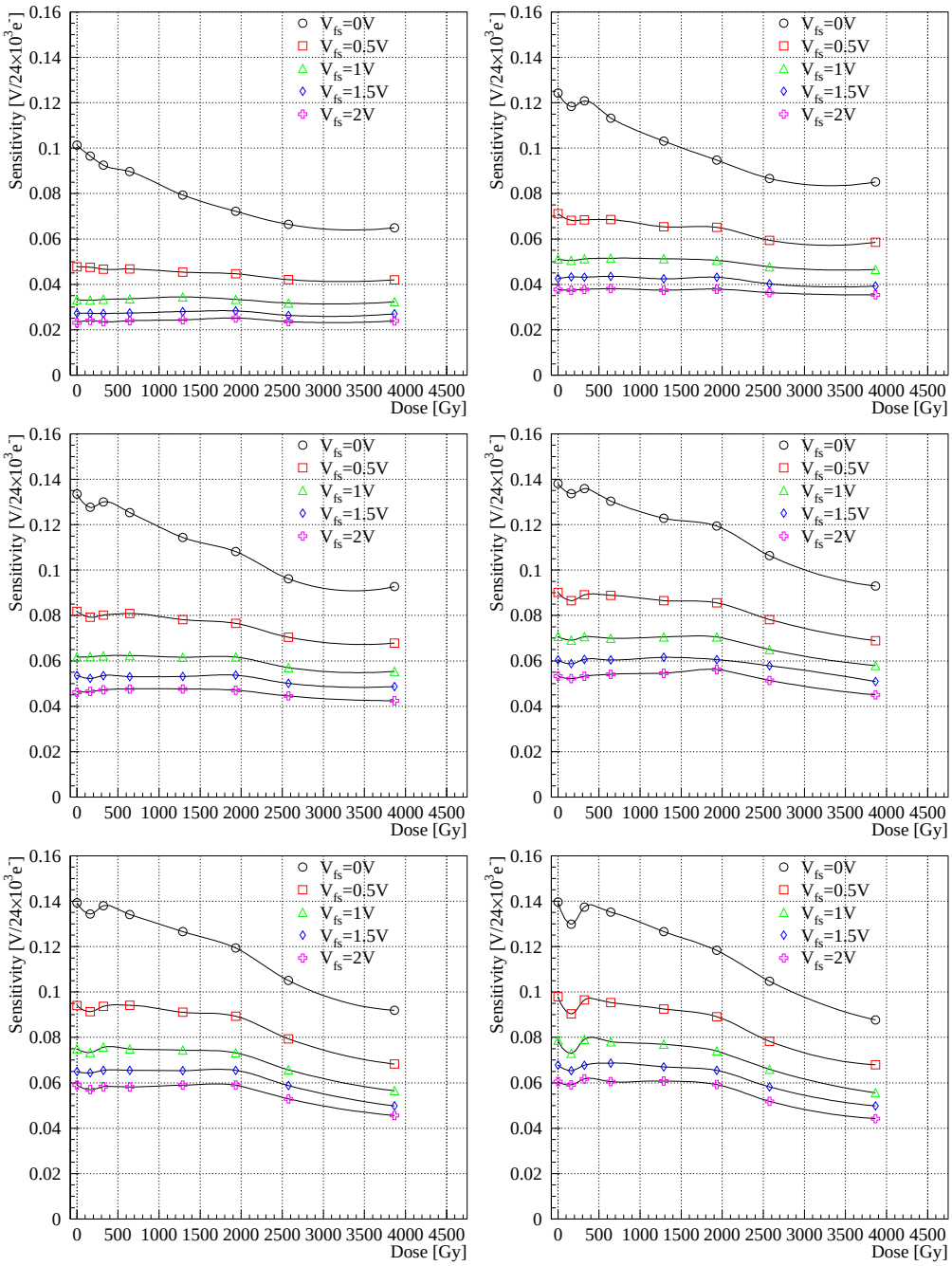

Figure A.13: Sensitivity of the HELIX128-2.2 as a function of the accumulated dose. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, 200µA, 300µA, 400µA, 500µA and 600µA (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 29.4\mathrm{pF}$.

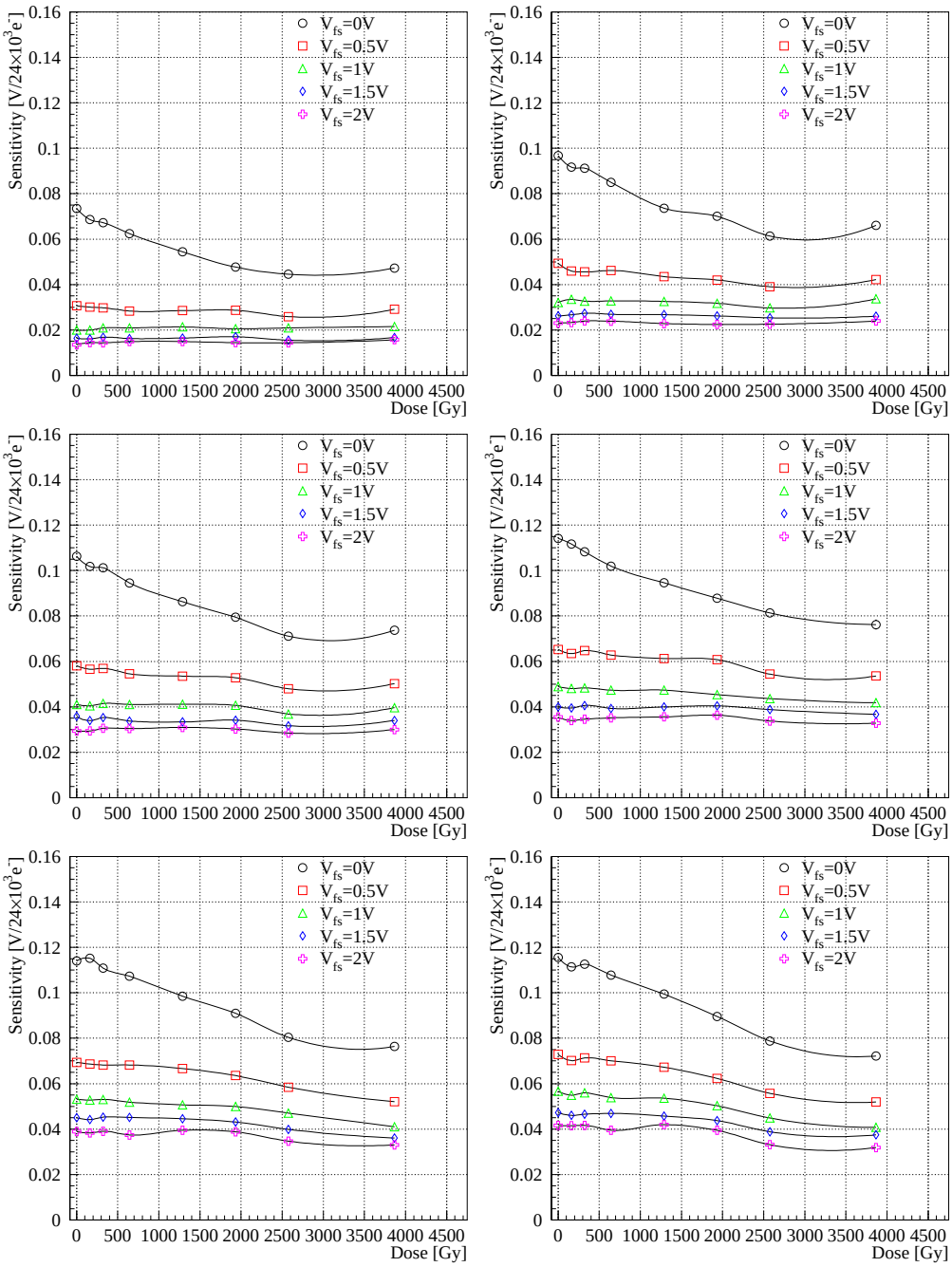

Figure A.14: Sensitivity of the HELIX128-2.2 as a function of the accumulated dose. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, 200µA, 300µA, 400µA, 500µA and 600µA (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 58\mathrm{pF}$.

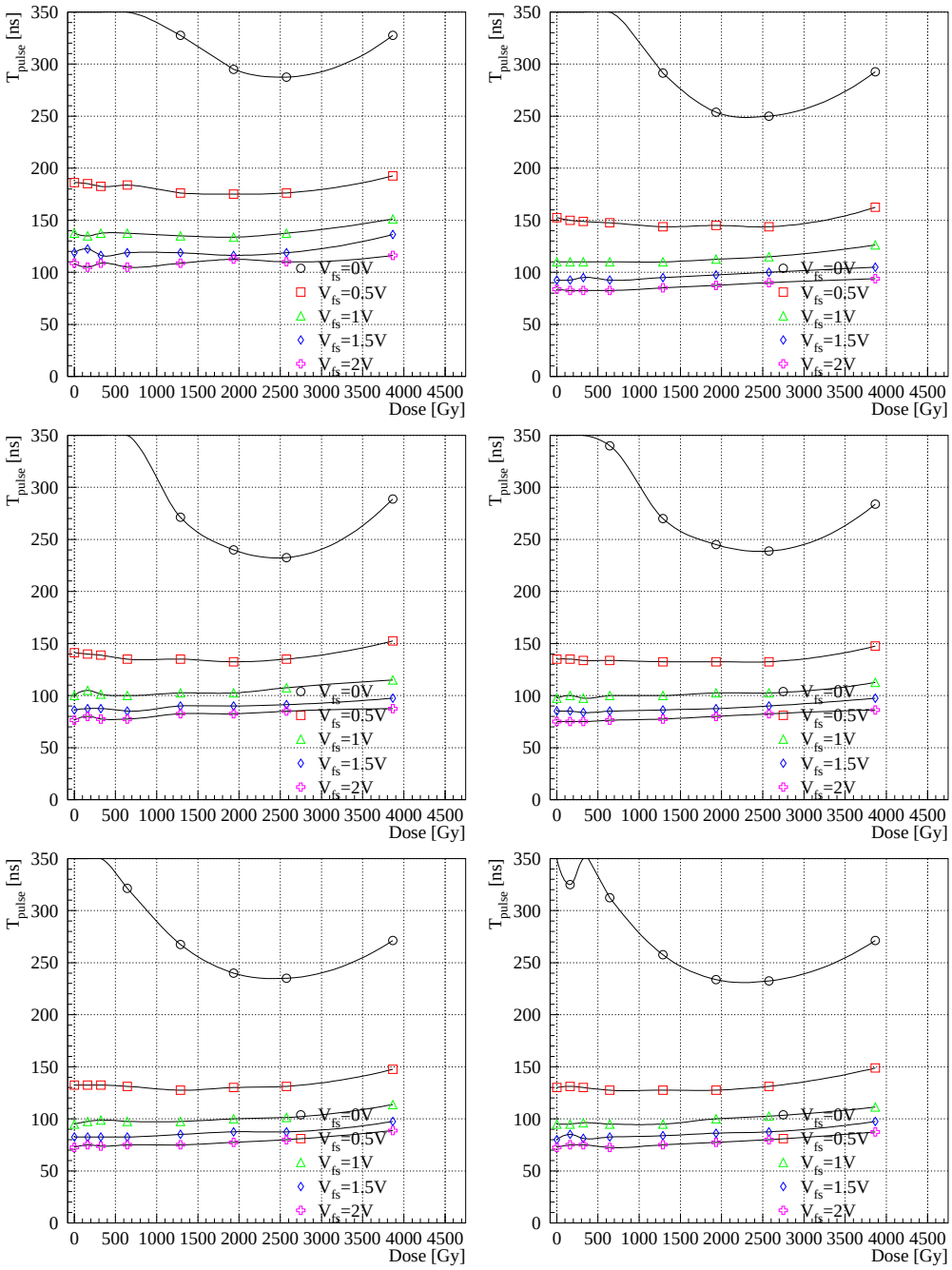

Figure A.15: Pulse Length (as defined in eq. 3.23) of the HELIX128-2.2 as a function of the accumulated dose. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). The coupling capacitor for charge injection causes a parallel capacitance of $C_{\mathrm{p}} = 1.6\mathrm{pF}$.

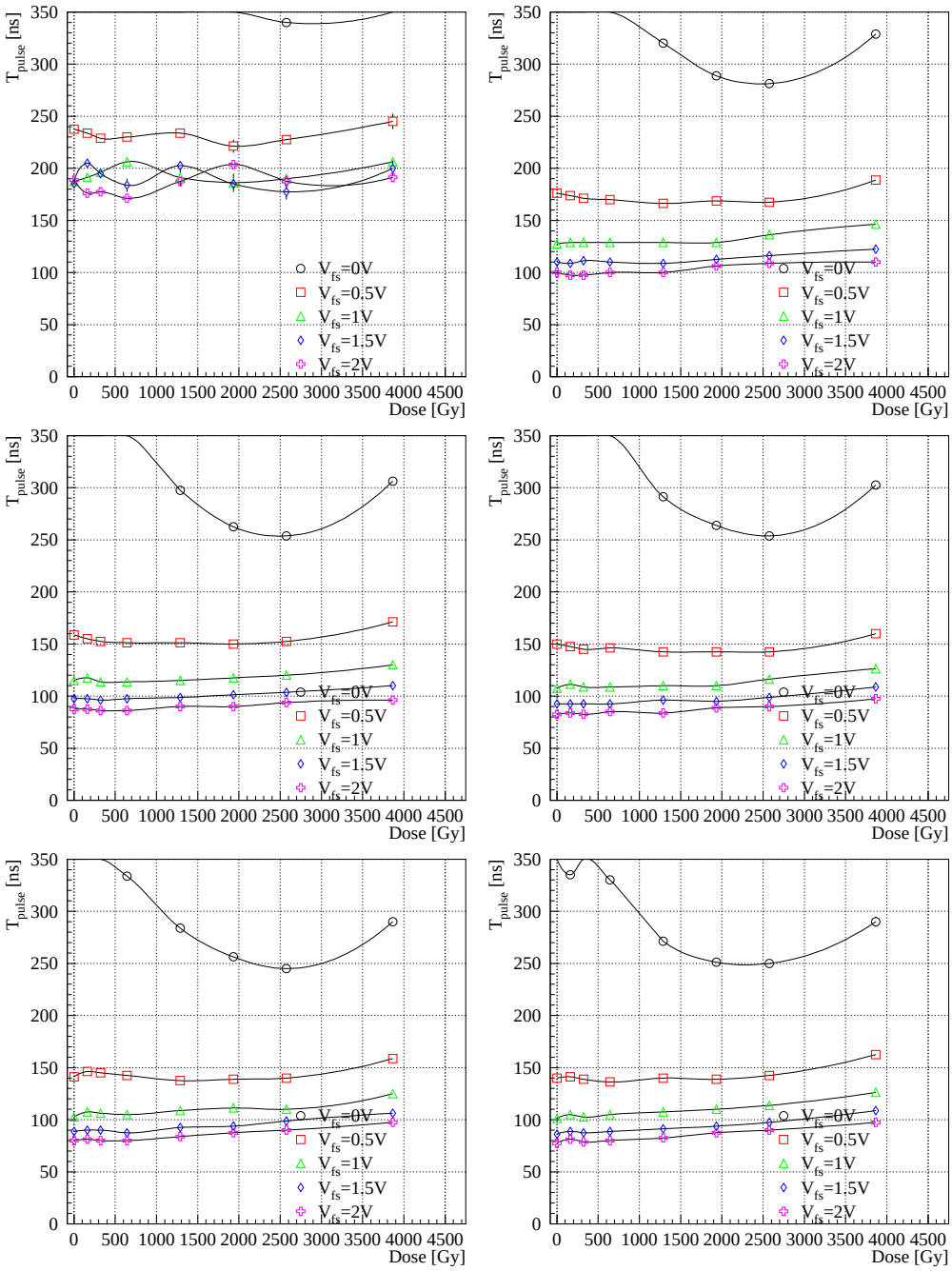

Figure A.16: Pulse Length (as defined in eq. 3.23) of the HELIX128-2.2 as a function of the accumulated dose. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 6.8\mathrm{pF}$.

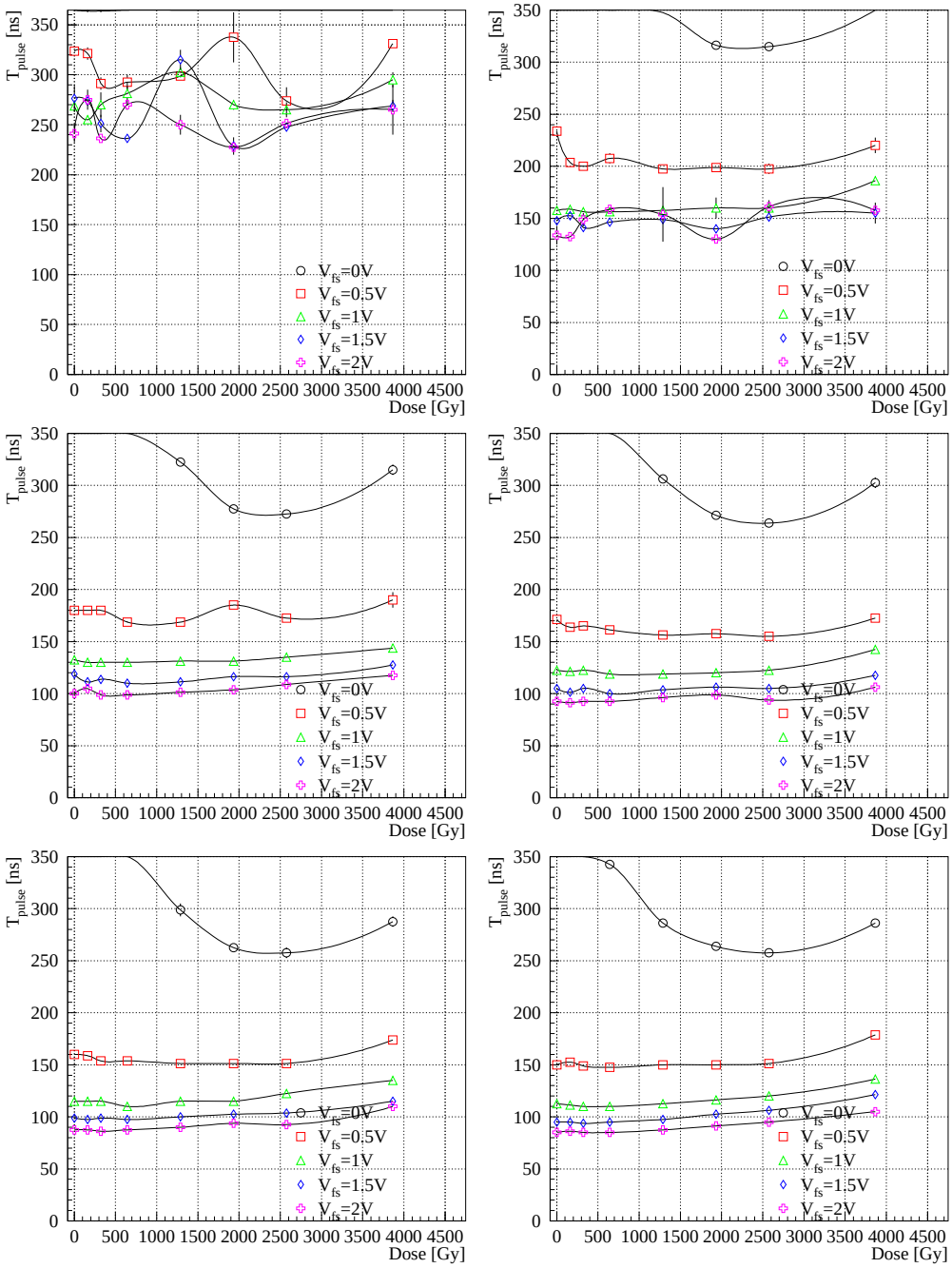

Figure A.17: Pulse Length (as defined in eq. 3.23) of the HELIX128-2.2 as a function of the accumulated dose. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 16.3\mathrm{pF}$.

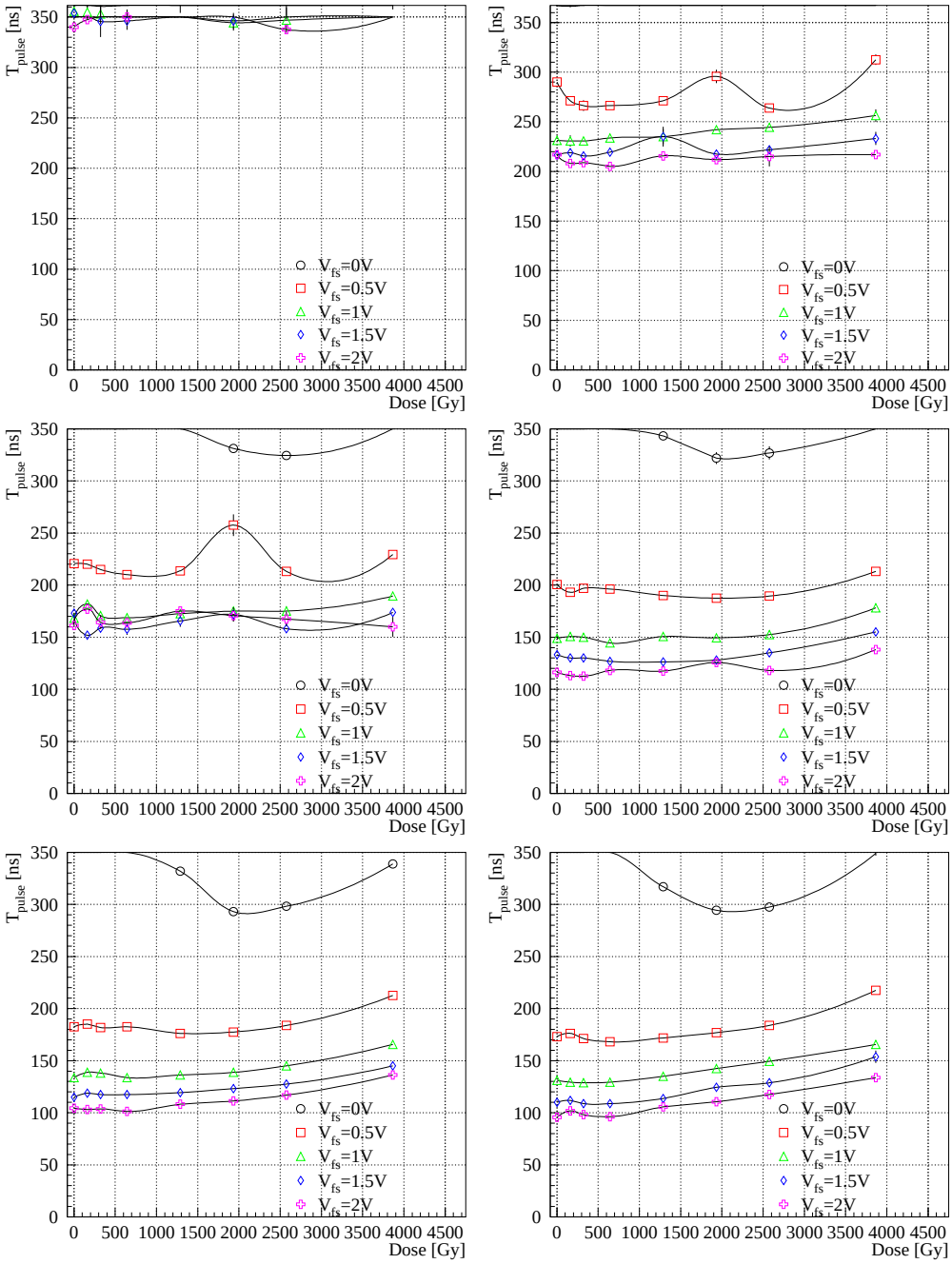

Figure A.18: Pulse Length (as defined in eq. 3.23) of the HELIX128-2.2 as a function of the accumulated dose. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 29.4\mathrm{pF}$.

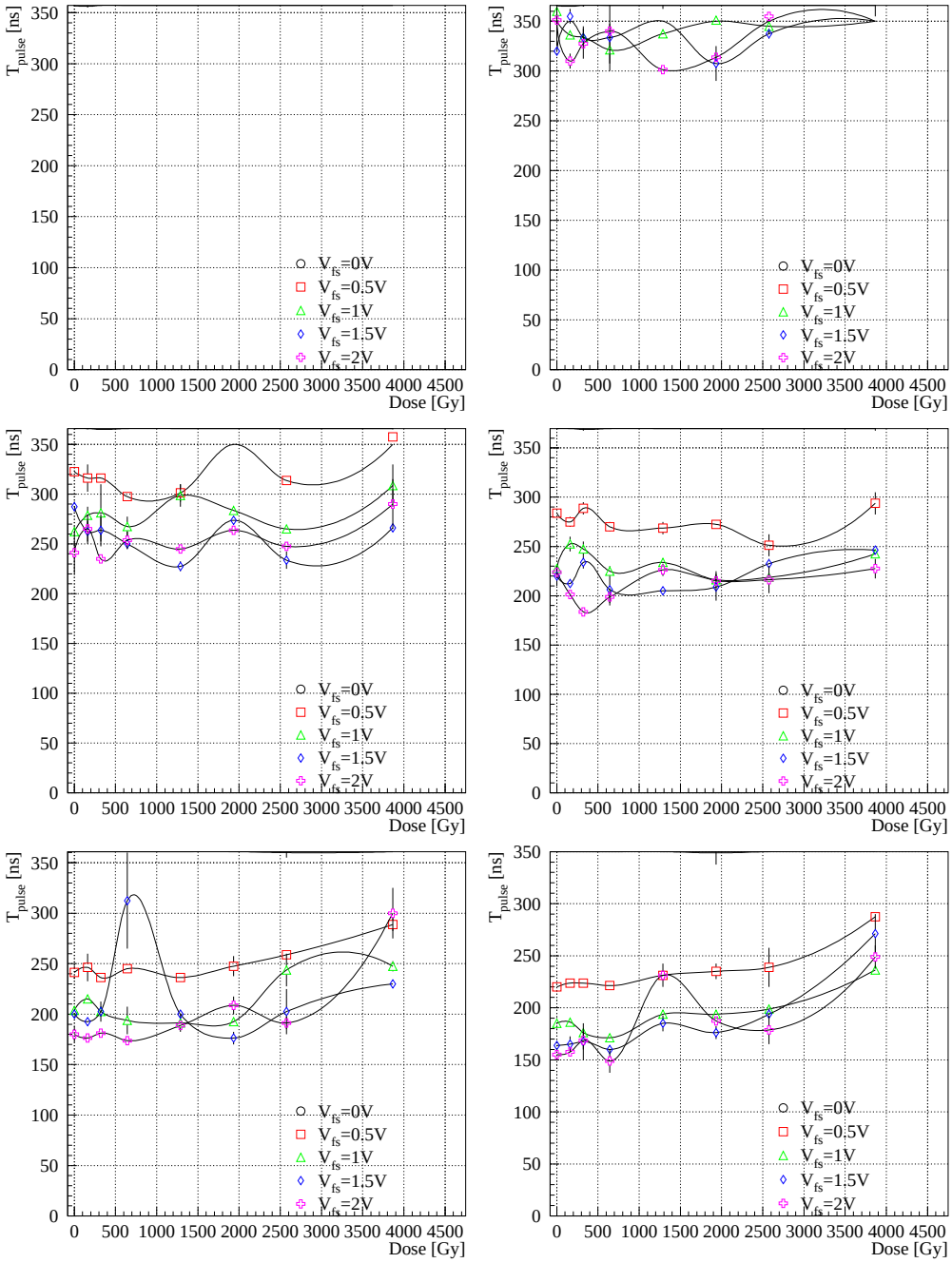

Figure A.19: Pulse Length (as defined in eq. 3.23) of the HELIX128-2.2 as a function of the accumulated dose. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 58\mathrm{pF}$.

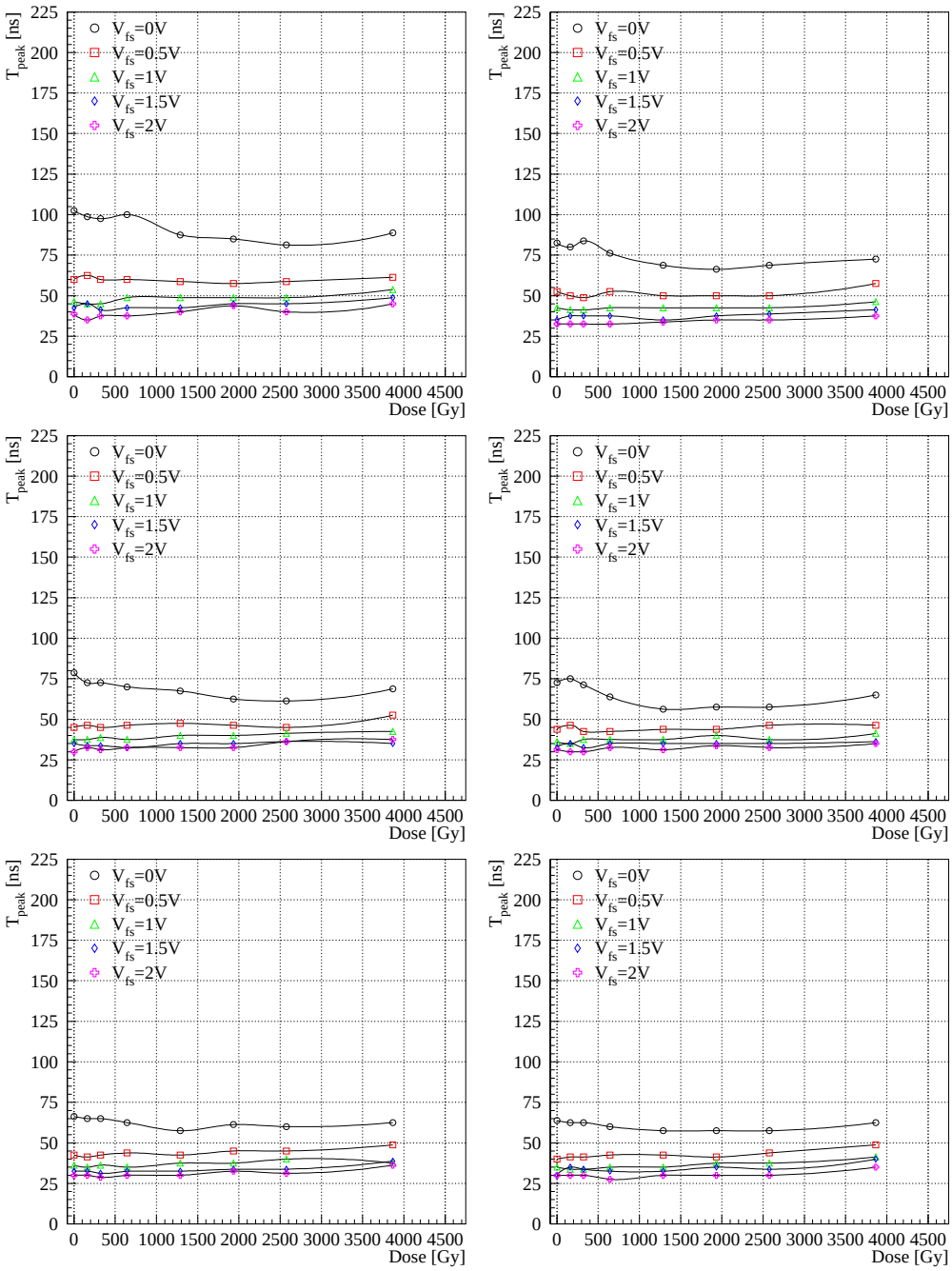

Figure A.20: Peak time (as defined in eq. 3.22) of the HELIX128-2.2 as a function of the accumulated dose. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). The coupling capacitor for charge injection causes a parallel capacitance of $C_{\mathrm{p}} = 1.6\mathrm{pF}$.

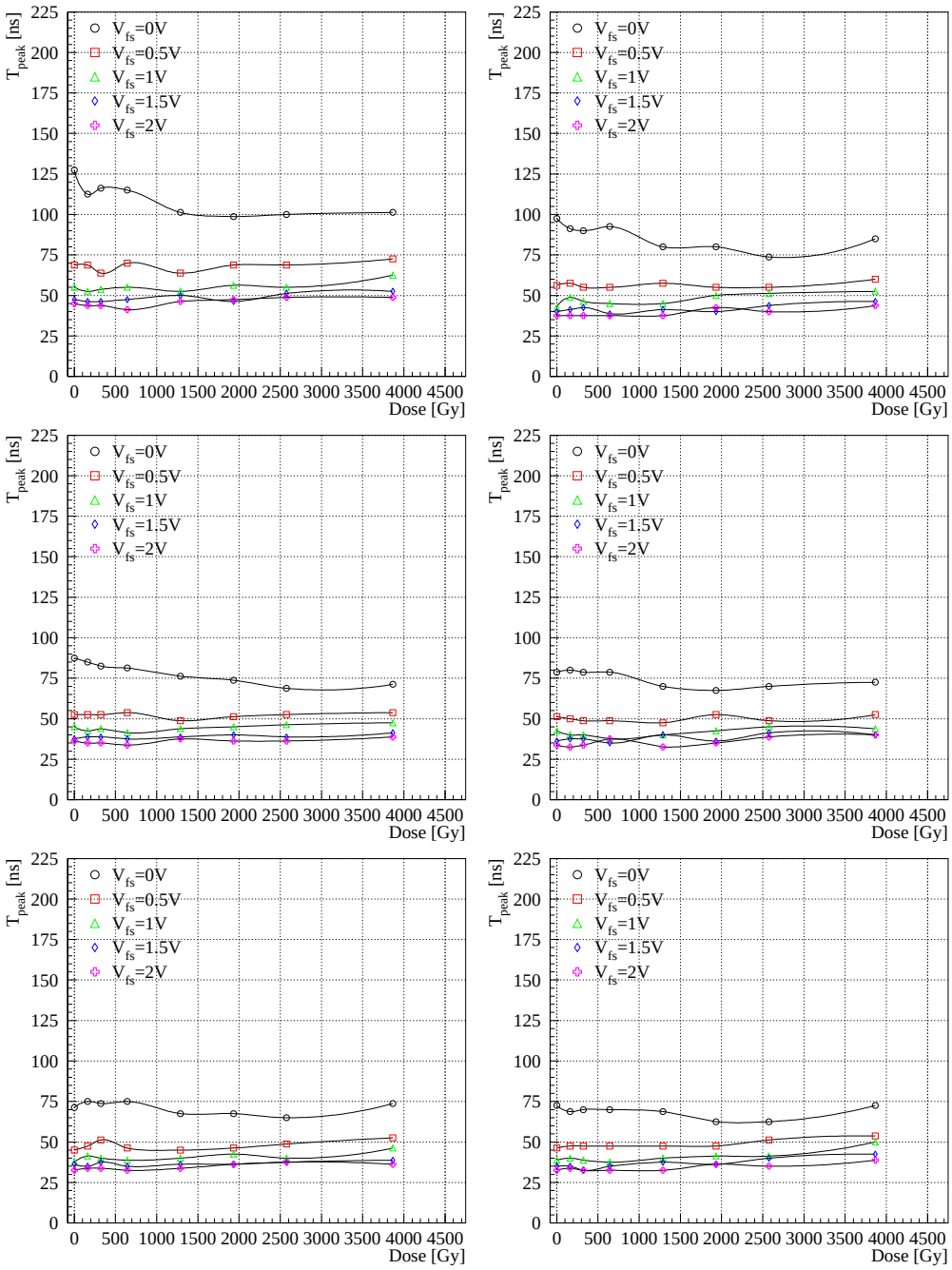

Figure A.21: Peak time (as defined in eq. 3.22) of the HELIX128-2.2 as a function of the accumulated dose. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 6.8\mathrm{pF}$.

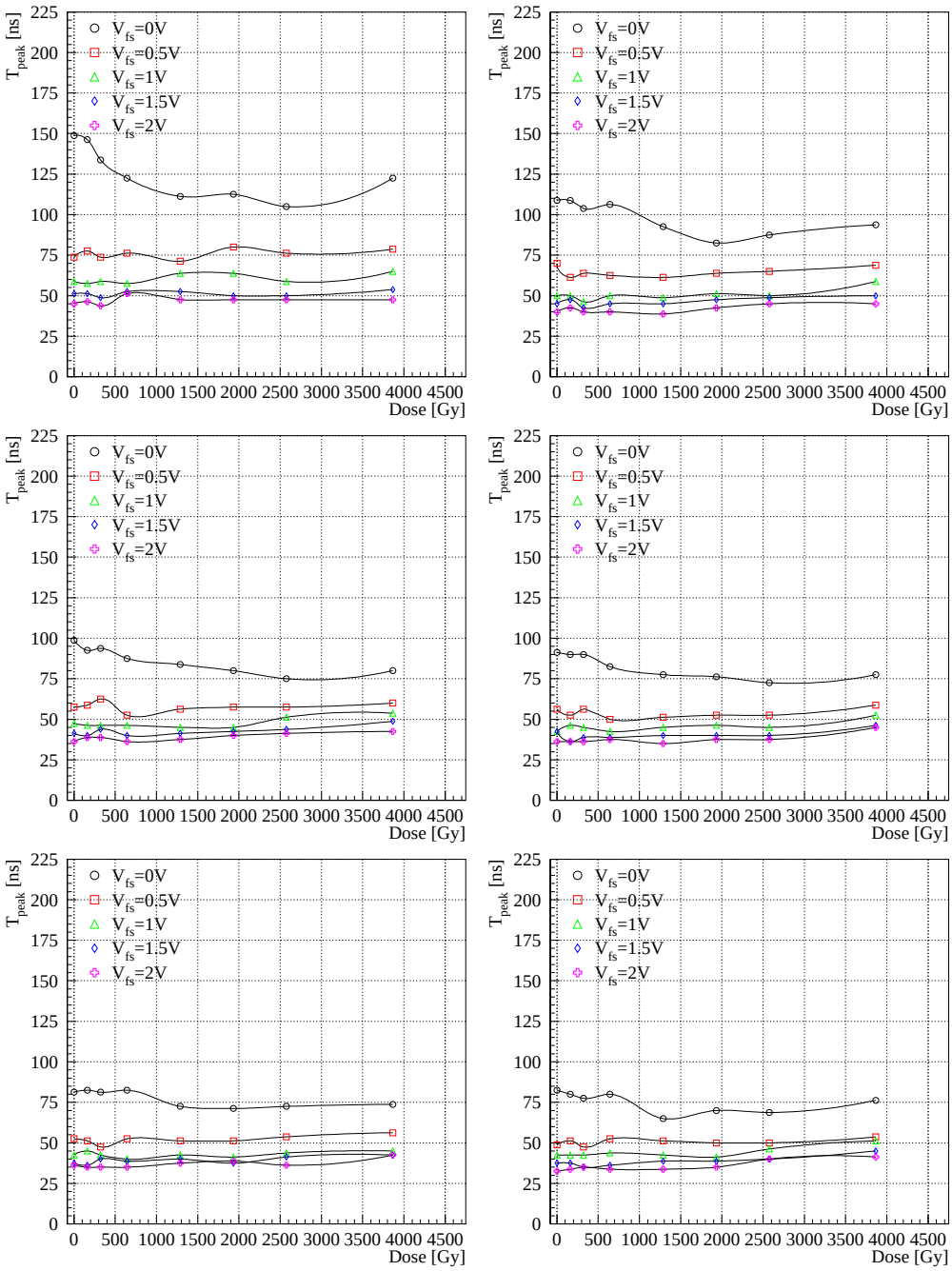

Figure A.22: Peak time (as defined in eq. 3.22) of the HELIX128-2.2 as a function of the accumulated dose. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 16.3\mathrm{pF}$.

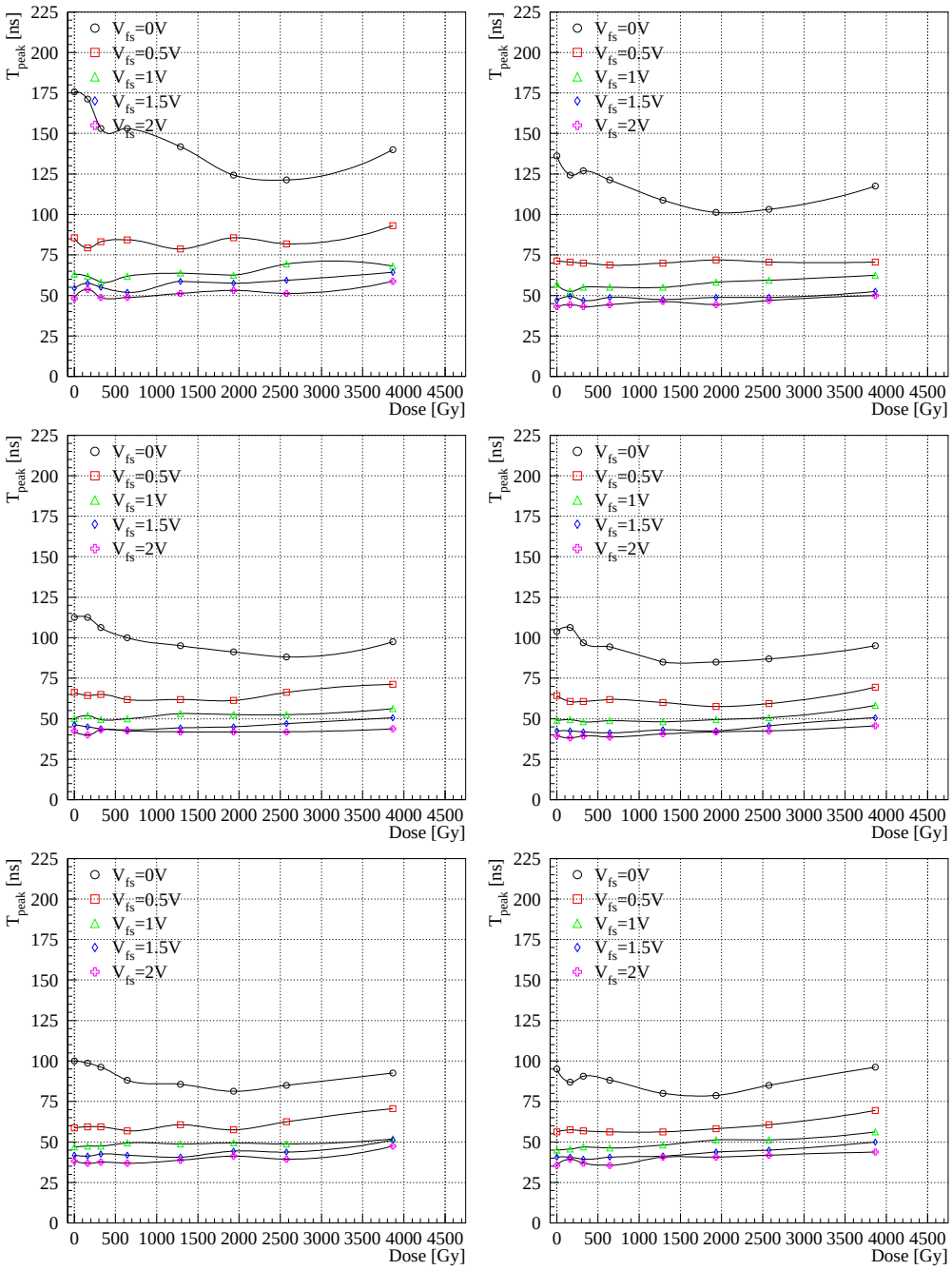

Figure A.23: Peak time (as defined in eq. 3.22) of the HELIX128-2.2 as a function of the accumulated dose. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 29.4\mathrm{pF}$.

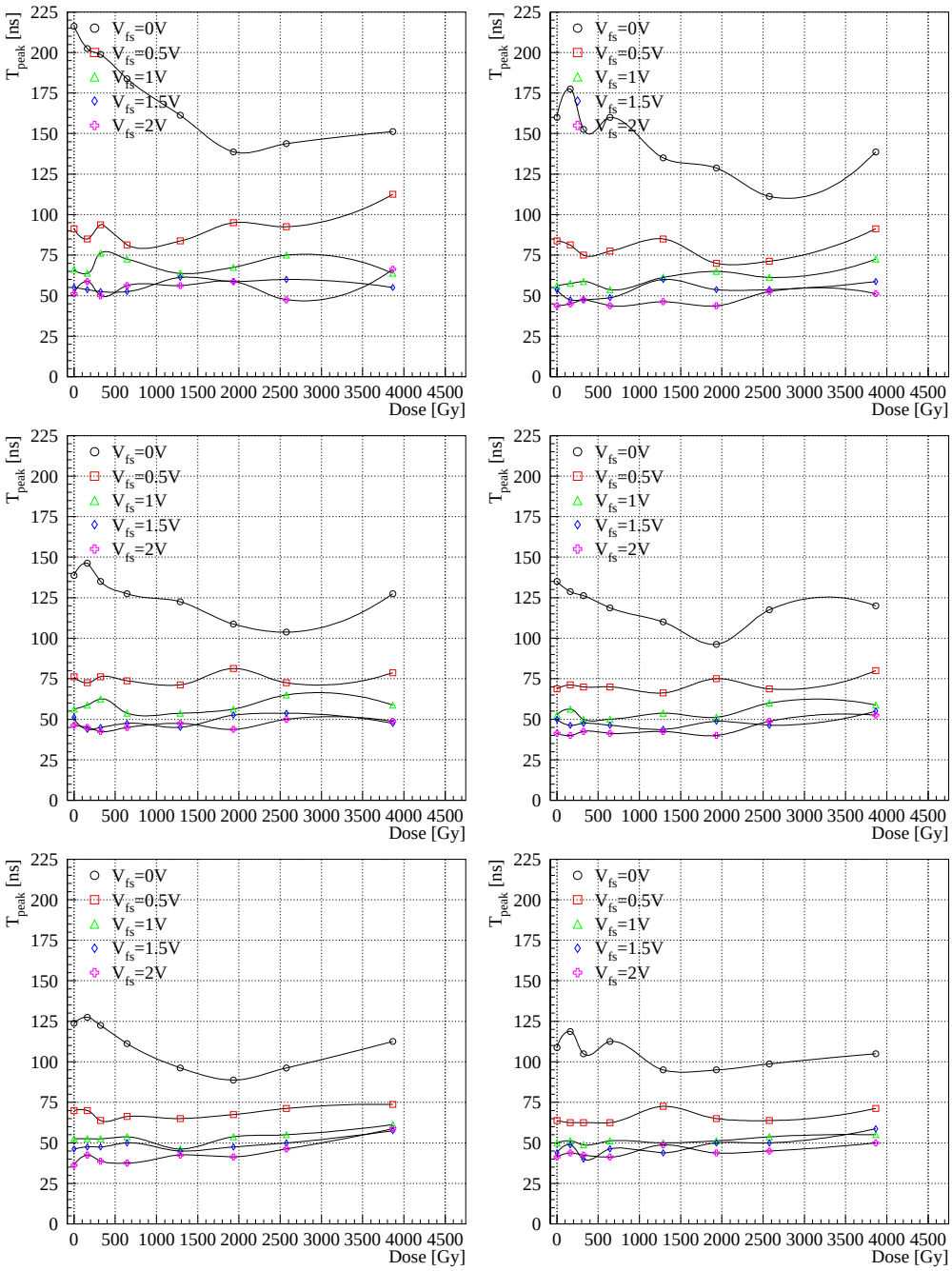

Figure A.24: Peak time (as defined in eq. 3.22) of the HELIX128-2.2 as a function of the accumulated dose. The graphs represent different preamplifier bias currents: $I_{\mathrm{pre}} = 100\mu\mathrm{A}$, $200\mu\mathrm{A}$, $300\mu\mathrm{A}$, $400\mu\mathrm{A}$, $500\mu\mathrm{A}$ and $600\mu\mathrm{A}$ (from top left to bottom right). The parallel capacitance attached to the amplifier input is $C_{\mathrm{p}} = 58\mathrm{pF}$.

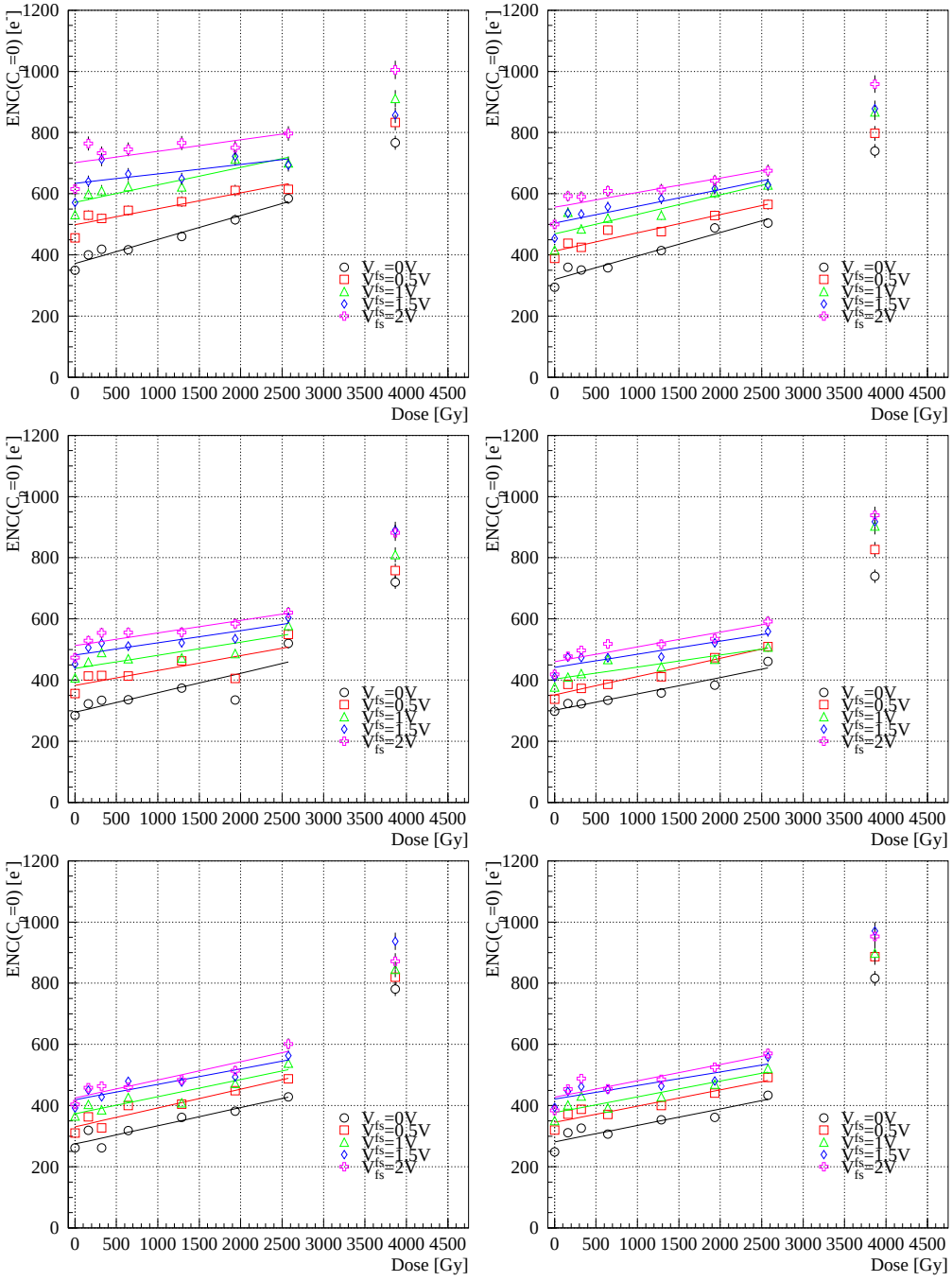

Figure A.25: $\overline{ENC}$ of the HELIX128-2.2 for a parallel capacitance of C_p = 0pF as a function of the accumulated dose. The graphs represent different preamplifier bias currents: I_pre = 100µA, 200µA, 300µA, 400µA, 500µA and 600µA (from top left to bottom right). The curves are linear fits to the data.

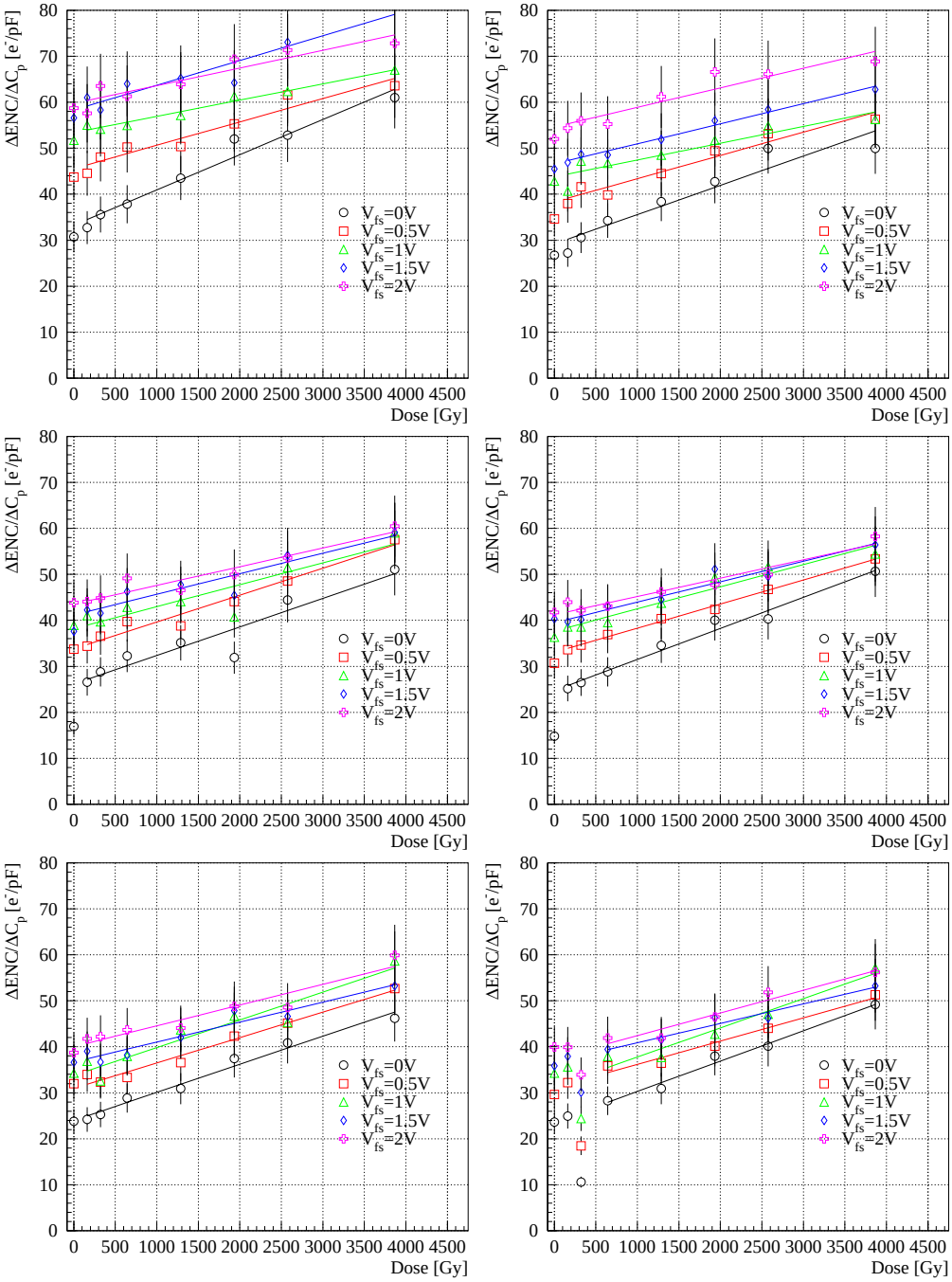

Figure A.26: Increase of HELIX128-2.2's $\overline{ENC}$ per unit of parallel capacitance as a function of the accumulated dose. The graphs represent different preamplifier bias currents: I_{pre} = 100µA, 200µA, 300µA, 400µA, 500µA and 600µA (from top left to bottom right). The curves are linear fits to the data.

Appendix B

History: The Family Tree of the HELIX Chip

When the HERA-B experiment was finally approved in 1994, it soon became obvious, that for the inner tracking system's readout there was no purchasable solution available.

For the silicon vertex detector the situation was only slightly better: The original RD20/FElix chip was no longer available and it was for several reasons not possible to modify it according to HERA-B specs for a dedicated production run. However, Rutherford Lab's APV series of chips was available (in samples) and nearly met all the requirements of the HERA-B VDS. But due to the high cost, arising from the rad-hard manufacturing process and the annual replacement of the electronics in the HERA-B VDS, it was only considered a backup solution.

The situation was cleared in Okt. '94: The Heidelberg ASIC lab was founded by Max-Planck Institut für Kernphysik (in charge of the HERA-B VDS), the Physikalisches Institut der Universität Heidelberg (responsible for the HERA-B ITR) and the former Institut für Hochenergiephysik der Universität Heidelberg. In turn it was decided to build a dedicated readout chip suitable for the HERA-B inner tracking system and silicon vertex detector. The evolution of this venture is shown in fig. B.1

HELIX1 contained various implementations of the FElix' frontend schematics (thus the name HELIX = Heidelberg FElix) in AMS' CAE 1.2µm process. It was submitted by W. Fallot-Burghardt in May '95, together with a chip containing a 128 channel multiplexer provided by J. Kaplon.

This chip did not meet the specifications, especially wrt. its pulse shape. Therefore an improved version was submitted in August '95: Together with a comparator (by M. Keller from IHEP) on **HELIX1.1K** and with a 4×16 pipeline on **HELIX1.1P**.

The results of the latter permitted the submission of **HELIX32**, a complete 32 channel readout chip (without discriminators) in November '95, which for the first time implemented the FiFo/pointer based pipeline r/w circuit by M. Feuerstack-Raible.

In January '96 **HELIX2**, a chip containing a frontend with a different architecture and far better noise performance was submitted by W. Fallot-Burghardt.

At the same time the first bias generator and control chip was submitted by U. Trunk. **SUFIX1.0** was already intended for a 128 channel readout chip still under development at that time.

This **HELIX128**(-1) chip followed in April '96. It now included the comparators and required a transition to AMS' CYE 0.8µm process due to the area required for the pipeline r/w control circuit.

The good results from HELIX2.1 resulted in an adaption of the chip to the 0.8µm technology. **HELIX2.1** was submitted in October '96.

The failing of the trigger comparators on HELIX128-1 lead to the submission of **IDEFIX** (the watchdog in Uderzo's Asterix comics) by B. Glass in March '97. It contained a new differential amplifier type comparator.

At the same time HELIX128-1 and SUFIX were merged to a single chip. Therefore SUFIX was modified resulting in **SUFIX2.0**. The IDEFIX's comparators, the HELIX2.1 frontend and a 2-stage multiplexer were included on **HELIX128-2.0**.

The pipeline r/w control of this chip failed and required a patch of the metal mask to become functional. The resulting **HELIX128-2.1** was submitted in September '97.

Problems with HELIX128-2.1 wrt. clock feedthrough and radiation tolerance resulted in the submission of **HELIX128-2.2** and **2.3**. These chips included LVDS receivers for clock and trigger signals, new "$R-2R$" DACs in the bias generator and two different implementations of the pipeline readout amplifier. Unfortunately only that on HELIX128-2.2 worked.

HELIX128-3.0 was submitted in December '98. It included the fail safe token schema required by the ZEUS experiment and a revised reference current source to overcome startup problems. The maximum latency of this chip was crippled to 123 samples by a bug when porting the library to a newer release of the *Cadence Synergy* tool used for the synthesis of the pipeline r/w control circuit. A scribeline cut on this chip was a major breakthrough in supressing crosstalk from the comparator outputs.

At about the same time **CIPIX**, a 64 channel digital readout only chip for H1's CIP upgrade was deduced from HELIX128-2.2 by D. Baumeister and S. Löchner.

TRIX was submitted by U. Trunk in summer '99. It converted the HELIX' open drain outputs to LVDS signals. A reduction of the open drain outputs' voltage on the HELIX resulted in the same improvements wrt. to crosstalk as the usage of the TRIX. Thus the chip was not used in the HERA-B ITR.

An improved pipeline r/w control circuit resulted in **HELIX128-3.1**, which was submitted in April '00, while a metal mask patch fixed an increasing oscillation problem of the current source and resulted in **HELIX128-3.1a** submitted in July '00. HELIX128-3.1a is expected to be the last version of HELIX128.

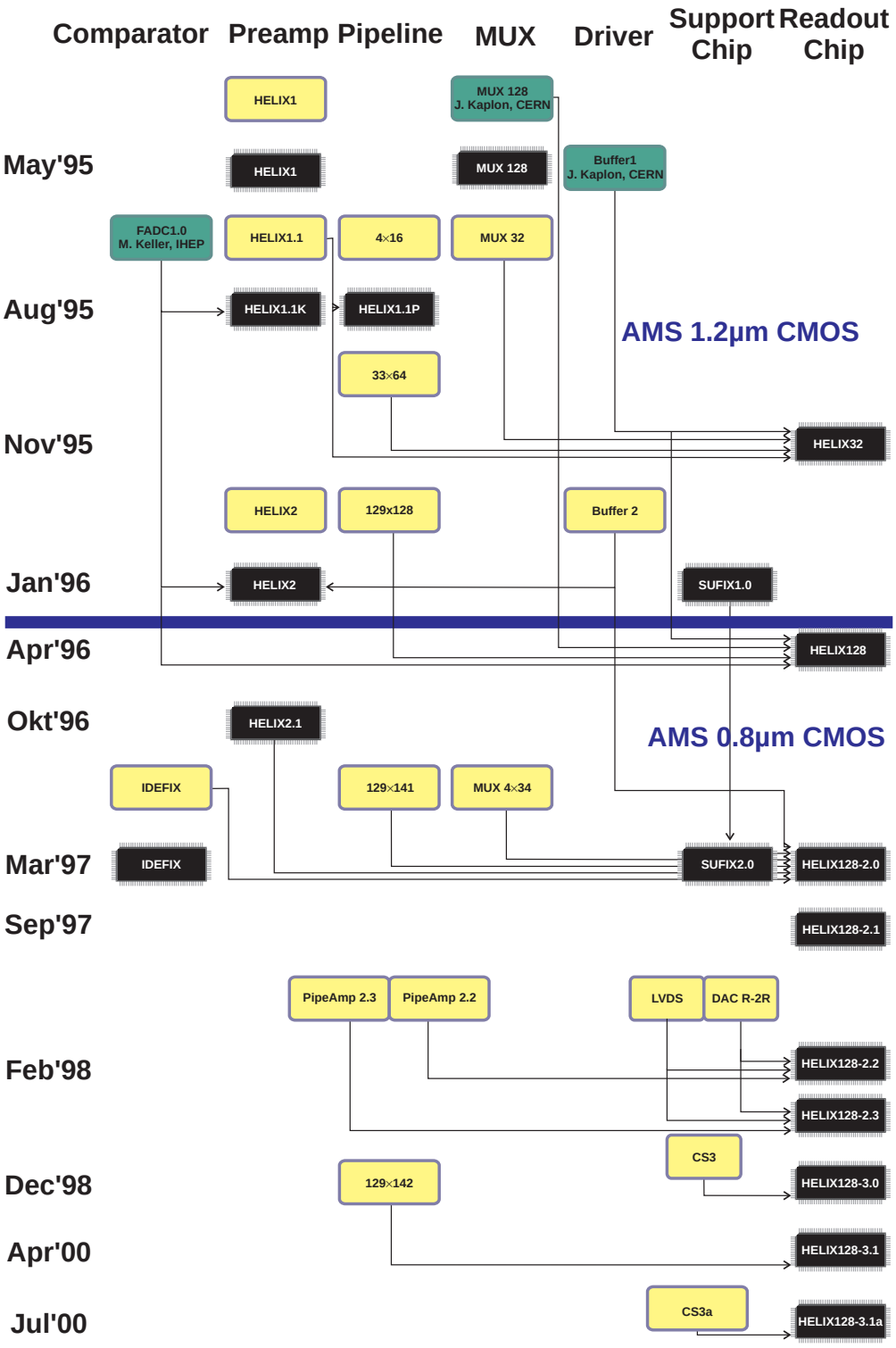

Figure B.1: Family Tree of the HELIX chip.

Appendix C

HELIX128-x Users Manual

HD-ASIC-33-0697

Helix128-x[1] User Manual

V2.2, 25.10.2000

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[1] includes Helix128-2.x and Helix128-3.x

Abstract

Helix128-2 and its variants 2.1, 2.2, and 2.3 are analog readout chips for silicon microstrip detectors and microstrip gaseous chambers manufactured in the 0.8µm-CMOS process of AMS. The chips integrate 128 channels with low noise charge sensitive preamplifier/shapers whose outputs are sampled into an analog pipeline with a maximum latency of 128 sampling intervals. A pipeline readout amplifier, a fast 40MHz multiplexer and a 40MHz current buffer form the backend stages of the designs. Additionally, each channel is equipped with an AC-coupled comparator behind the preamplifier/shaper. All comparators share a common threshold, the output of four neighbouring comparators being ORed and brought offchip.

The bias settings and various other parameters are programmable via a serial line protocol. The chips also integrate some monitoring functionality and the ability to report error conditions.

On Helix128-3.0 remaining bugs were fixed. It is additionally equipped with a failsafe token scheme, which makes the chip useable in long daisy chains.

The newly introduced bugs on Helix128-3.0 were fixed on Helix128-3.1, which unfortunately also introduced a new one. A metal mask change fixed the current source's oscillation problem and resulted in the (hopefully) final version Helix128-3.1a.

Contents

List of Tables

C.1 Changes applied to this manual

Version	Date	Author	description
1.3	30.6.1997	MFR	Changed table C.1 on page 196 Changed table C.5 on page 210 `TrigIn` is sampled at the rising edge of `SClk` Changed description of serial interface on page Changed description of `MuxDisable`
1.4	16.10.1997	MFR	Noted two new bugs.
1.5	28.10.1997	MFR	Changed pad description of Helix128-2.0 and included pad description of Helix128-2.1
1.6	25.2.1998	MFR	Included pad description of Helix128-2.2
1.7	2.3.1998	MFR	Removed bug in analog receiver circuit description
1.8	17.4.1998	WFB, ES	Several bugs removed
1.9	12.5.1998	MFR	Introduced change bars, corrected pad layout for Helix128-2.2/2.3 (tables C.10, C.15)
2.0	17.12.98	MFR	Included Helix128-3.0 description and corrected Helix128-2.2 pad layout description
2.1	3.2.98	MFR	Corrected bugs in pad layout description and test pulse circuit description. Added description of failsafe token scheme control bits and corrected several smaller bugs.
2.2	16.10.00	UT	Included Helix128-3.0 bugs and added versions Helix128-3.1 and -3.1a. Updated recommendations to compensate radiation effects and added reference. Removed bugs in bias settings. Added Helix128-3.1 bugs.

C.2 Important note

This manual describes different versions of the second generation of the Helix readout-chip; the chips developed so far differ in some details, especially concerning pad layout and electrical specification of some control signals. The Helix128-2 (sometimes also called Helix128-2.0) chip is the first in this line; Helix128-2.1 emerged from it by a metal/poly mask redesign.

Helix128-2.2 is an improved version making use of a modified pipeline readout amplifier; it is equipped with LVDS line receivers for some control lines and with a pad layout that will make it compatible with a fail safe token scheme which will be implemented in future. Finally, Helix128-2.3 is a derivation of Helix128-2.2 with yet another pipeline readout amplifier.

The name Helix128-2 is used throughout this manual when describing features that are common for all versions of the chip.

The Helix128-3.0 includes some remaining bug fixes and in addition has implemented a failsafe token mechanism, which enhances reliability in systems with large daisy chains. Only changes applied to this chip with respect to its predecessors are discussed here.

The bugs introduced on Helix128-3.0, which restricted the latency, and a hidden problem to simultaneously exploit the full latency and buffer depth were fixed on Helix128-3.1, which unfortunately introduced a new bug. The remaining oscillation problem of the current source was solved by a metal mask change, resulting in Helix128-3.1a. The functionality and specs of the 3.0 version (with one explicitly denoted exception) also apply to Helix128-3.1 and 3.1a.

C.3 Analog Signal Processing Architecture

Helix128-2 is an analog readout chip for silicon microstrip detectors and microstrip gaseous chambers specially suited to the needs of the HERA-B experiment [1]. Major electrical specifications are a 10MHz sampling clock frequency (i.e. the *bunch crossing* frequency) implying a shaper peaking time in the 50 ns regime, a storage time depth of about 10µs to comply with the first level trigger latency, the ability to store up to eight events to equalize statistical trigger fluctuations and the complete deadtimeless readout of the detectors in 10µs due to the mean second level trigger rate of 100kHz. Further demands are lowest possible total system noise and a moderate radiation tolerance of $\leq$2kGy.

To cope with the tremendous amount of detector channels 128 channels are integrated per chip with 41.4µm pitch (which yields in a 50µm overall pitch) of input pads as imposed by the silicon strip detector pitch.

C.3.1 Overview

Helix128-2 contains 128 channels (see fig. C.1), each consisting of

- a low noise charge sensitive preamplifier for signals of both polarities. It is implemented as a folded cascode amplifier circuit with a 342fF feedback capacitor yielding a gain of 11.2 mV/MIP_{Si} (1 MIP_{Si}=24000 electrons).
- a CR-RC shaper forming a semigaussian pulse with a peak time of 50... 70ns.
- a buffer amplifier driving the internal pipeline write line and the pipeline cell.
- a comparator circuit indicating hit channels, the output of four neighbouring channels being ORed and brought offchip via open drain outputs.
- an analog pipeline consisting of 128+8+5 (128+8+6 on Helix128-3.1) capacitors resulting in a maximum latency of 128 events and a multievent buffer capable of storing up to eight triggered events (time slots)
- a switched charge sensitive pipeline readout amplifier.

A cascaded 128+8+1 channel multiplexer and a current output buffer are provided for the fast serial readout of the analog data and the 8 bit pipeline column number.

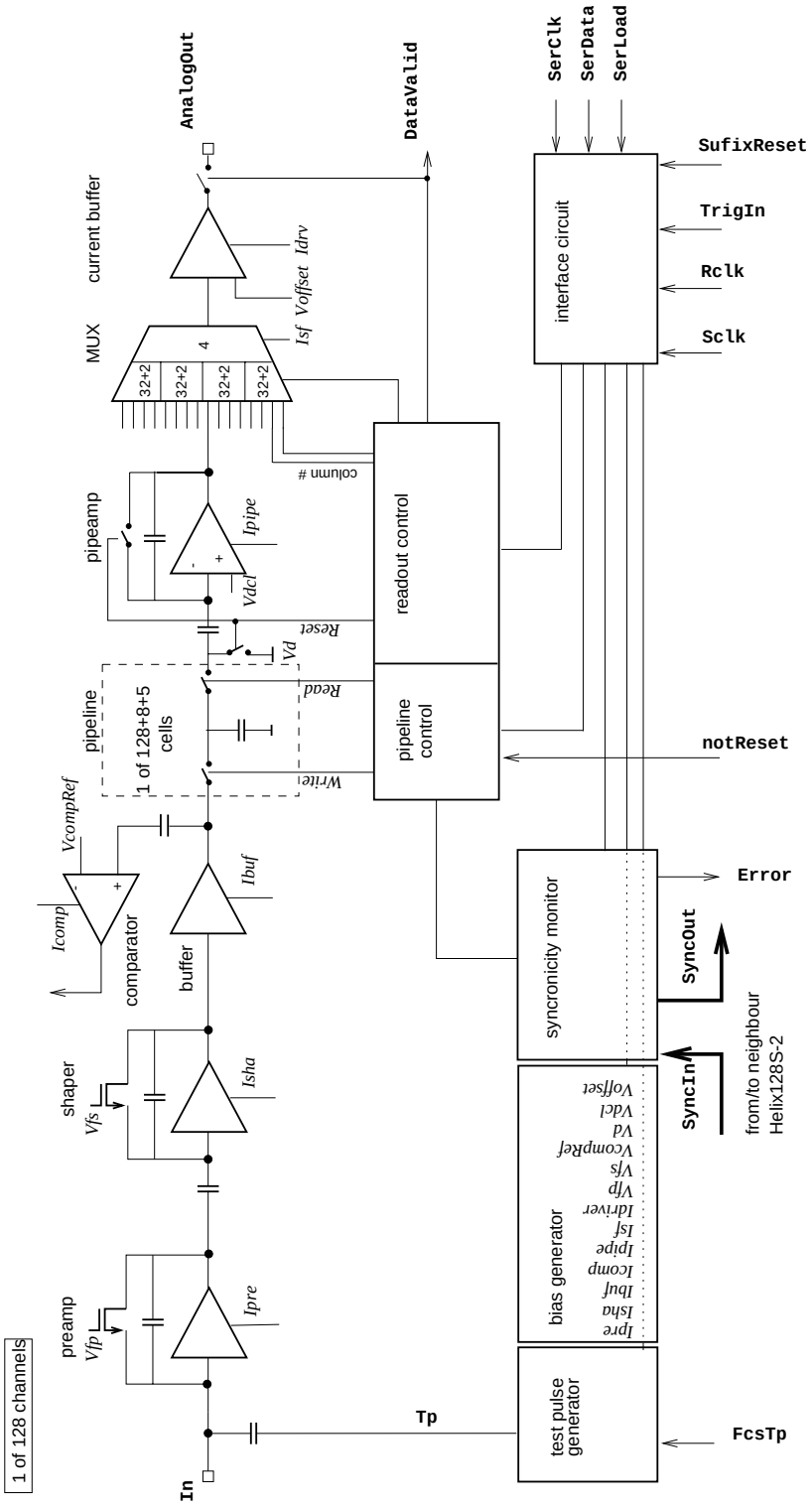

Figure C.1: Schematic diagram of Helix128-2

The operation points of all Helix128-2 amplifier stages can be adjusted via programming of corresponding DAC registers. We will outline radiation compensation strategies which ensure proper operation up to the demanded dose of HERA-B. Further explanation of the suggested strategies can be found in [6], [7] and especially concerning the Helix128 chip in [8].

C.3.2 The Frontend (Helix2.1)

Helix128-2 uses the Helix2.1 frontend (fig. C.2) which has been carefully optimized with respect to noise, pulse shape (peak time and undershoot), linearity, space and power consumption. More detailed descriptions can be found in [2], [3] and [4]. To set the frontend operation mode and to

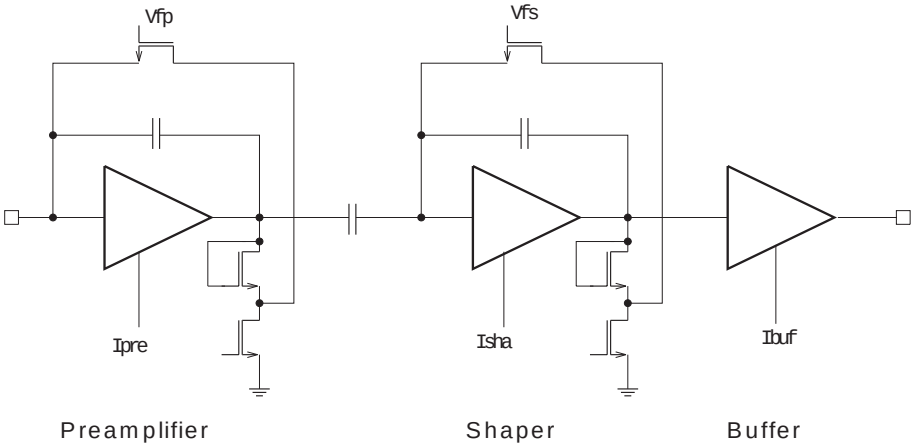

Figure C.2: Helix2.1 frontend

compensate for radiation damage the frontend bias voltages and currents (not to be confused with the power supplies +2V,0V,−2V) may be adjusted via programming of the corresponding DAC registers as explained in section C.4. The nominal values are listed in table C.1.

- *Ipre* sets the preamplifier bias current. *Ipre* , since it determines the preamplifier's internal resistance, controls, in conjunction with the parallel capacitance (i.e. the detector capacitance) on the input, the peak time and the undershoot or tail of the shaped pulse (fig. C.3). Large undershoots and high parallel capacitances require higher values of *Ipre*. A higher *Ipre* current also reduces noise, so that a noise degradation of the preamplifier due to decrease of the g_m of the input transistor can be cured by increasing this current (at the cost of power consumption). Depending on the requirements it is recommended to select *Ipre* to match either the desired undershoot ratio or the demanded S/N ratio.

- *Isha* sets the shaper bias current. In case of a finite parallel capacitance on the preamp's input, *Isha* has allmost no influence on the

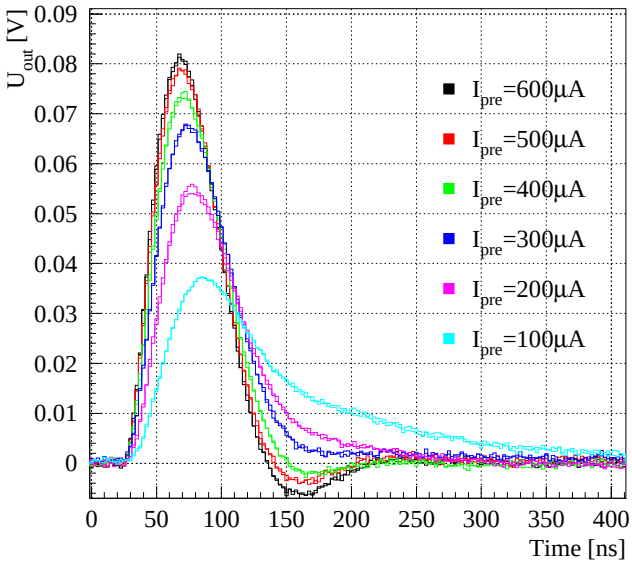

Figure C.3: Impact of *Ipre* on pulse shape: from slowest to fastest pulse: *Ipre*=100µA, 200µA, 300µA, 400µA, 500µA, and 600µA, the parallel capacitance is 16.3pF

pulse shape. Therefore *Isha* should be kept at its default value and unchanged under irradiation.

- *Ibuf* sets the buffer bias current. It should be kept constant. If the buffer becomes too slow by a decrease of g_m (this can be observed e. g. by changing pulse heights at different `SClk` frequencies), *Ibuf* can be increased.

- *Vfp* controls the value of the preamplifier feedback resistance. It should be as low as possible for optimum noise performance. *Vfp* has to be increased *continuously* at low doses, so that the preamplifier operates slightly above the *Vfp* cutoff edge (for DC coupled detectors this value can be quite large). At higher doses ($D \geq 500$Gy) it has to be *continuously* decreased.

- *Vfs* controls the value of the shaper feedback resistance and thus determines the discharge of the shaper feedback capacitor (see fig. C.4). The undershoot ratio of the shaped pulse is almost independent of *Vfs*. Therefore it is recommended to control peak time and pulse length by adjusting *Vfs*, while the undershoot ratio is adjusted by altering *Ipre*. Since the peak time only changes very slightly with irradiation, *Vfs* should be kept constant.

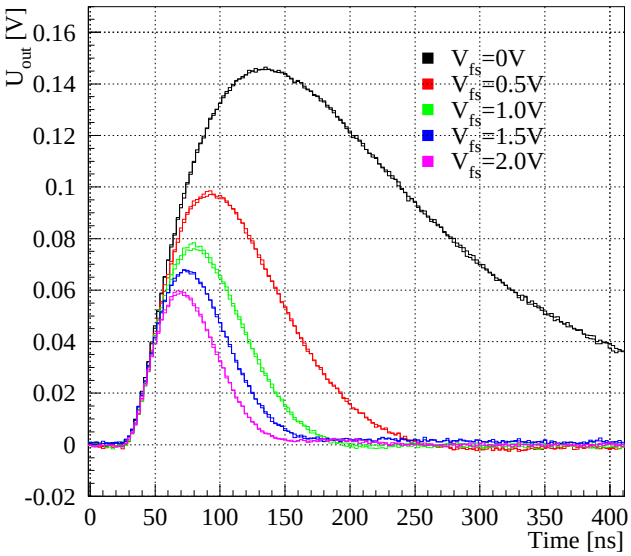

Figure C.4: Impact of *Vfs* on pulse shape. *Ipre*=300µA was chosen and a parallel capacitance of 16.3pF was attached to the input.

C.3.3 The Comparator

The comparator (fig. C.5) with programmable signal polarity is located behind the frontend to detect hit channels. To suppress frontend pedestal fluctuations the comparator has been AC-coupled with a large time constant. The output of four neighbouring channels is ORed, latched on the positive edge of `CompClk` and brought offchip as open drain signals `notCompOut`⟨31...0⟩ which can drive 4mA at maximum [2].

In case of radiation damage the following strategy is recommended:

- *VcompRef* controls the comparator threshold level (1 $MIP_{Si} \approx 50$mV peak height, so a value of 20mV is a good start to detect *MIP* signals[3]); due to the AC-coupling this level is independent from radiation induced frontend baseline shifts and so it should not be altered.
- *Icomp* sets the comparator bias current. It can be increased slightly under irradiation (however, no strong effects expected)

C.3.4 The Pipeline

The frontend outputs are stored in a sample&hold capacitor array of $129 \times (128 + 8 + 5)$ ($129 \times (128 + 8 + 6)$ on Helix128-3.1) cells.

[2] This enables logically "OR"ing several comparator outputs by connecting them to a common drain resistor.

[3] cf. also appendix C.6

Name	Nominal value and dec. reg. cont.	Irradiation compensation
Ipre	200µA=80	⇒⇵
Isha	100µA=40	⇒
Ibuf	100µA=40	⇒⇵
Icomp	50µA=20	⇒⇑
Ipipe (Helix128-2.0...2.1)	50...100µA=20..40	⇒
Ipipe (Helix128-2.2)	40µA=16	⇒
Ipipe (Helix128-2.3)	20µA=8	⇒
Isf	100µA=40	⇒⇵
Idriver	90µA=36	⇒
Vfp	0.2V=140	⇑($D \lesssim$ 500Gy), ⇓($D \gtrsim$ 500Gy)
Vfs	1.5V=224	⇵⇒
VcompRef	±20mV=140	⇒
Vdcl (Helix128-2.0...2.2)	1V=192	⇒
Vdcl (Helix128-2.3)	−1.1V=58	⇒
Vd (Helix128-2.0,2.1)	0V=128	⇓
Vd (Helix128-2.2,2.3)	−840mV=74	⇓
Voffset	−0.5V=96	⇒⇑

Table C.1: Nominal values of analog bias voltages and currents and suggested radiation compensation strategies; ⇒ indicates no change, ⇓/⇑ suggests negative/positive adjusting of the corresponding bias. ⇵ etc. indicates that the proposed change was found to be unnecessary. Since the LSB of the 8bit wide voltage value registers is ignored on Helix128-2.0 and 2.1, the corresponding values must *not* be corrected for that.

Each cell capacitor (850fF) is connected by a *read* switch to the *read line* (frontend output), and by a *write* switch to the *write line* leading to the pipeline readout amplifier ("pipeamp") (fig. C.1). The switches are controlled by the pipeline logic which is explained in more detail in section C.4.1. The charge stored per MIP_{Si} is $\approx$ 260.000 electrons implying a charge gain of 11, so that the noise requirements on the pipeamp are relatively relaxed.

C.3.5 The Pipeline Readout Amplifier ("Pipeamp")

The pipeline readout amplifier is a switched charge sensitive amplifier (fig. C.6). Before operation the internal reset signal is applied thus discharging the two capacitances (for clearness assume *Vdcl*=*Vd*). After the reset the pipeamp is sensitive to the pipeline capacitor charge; since the node at the inverting input stays on constant potential, the charge transfer between the two capacitors causes a related voltage on the output when coupling charge to the input. The following strategy is recommended in case of radiation damage:

- *Vd* controls the reset level; it should follow the frontend baseline shift, i. e. it should be continuously diminished.

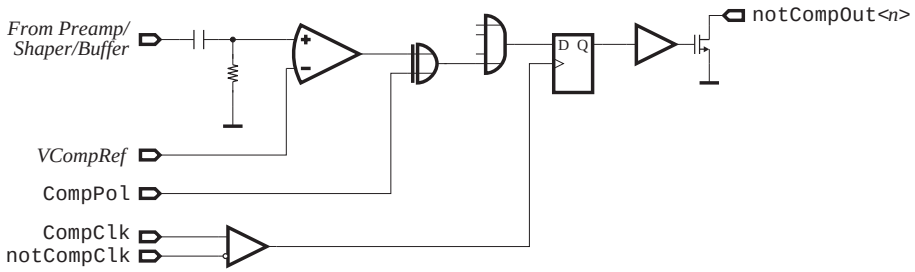

Figure C.5: AC-coupled comparator

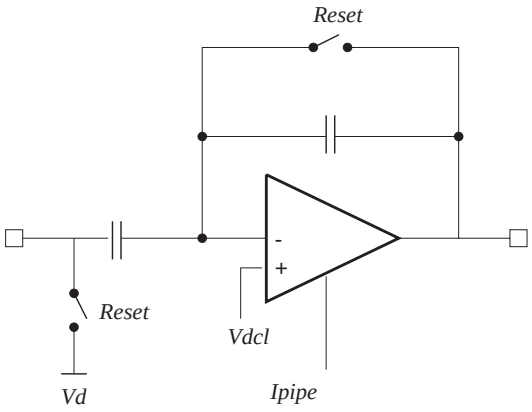

Figure C.6: Pipeline readout amplifier: a switched charge sensitive amplifier

- *Vdcl* controls the folded cascode "ground" level; it should be adjusted after the *Vd* adjustment such that the channel output offsets equal approximately the pipeline column number's mean value in the readout figure.

- *Ipipe* sets the pipeamp bias current. It should be kept constant.

C.3.6 The Multiplexer

The multiplexer (fig. C.7) has been implemented using a cascaded architecture, i. e. in the first stage four 34 channel multiplexers operate at a fourth of the `RClk` rate with a second stage at full `RClk` speed. This approach would lead to a reordering of the channel numbers. Thus, to equalize this effect a permutation fan through has been implemented so that the channels arrive at the output in their geometrical order. The multiplexer first stage consists of a buffered sample&hold circuit with the drive strength controlled by *Isf*. In case of radiation damage the following strategy is recommended:

- *Isf* should be kept constant; if the buffer becomes too slow by a decrease of g_m, (this can be observed e. g. by changing pulse heights at different `RClk` frequencies) *Isf* can be increased.

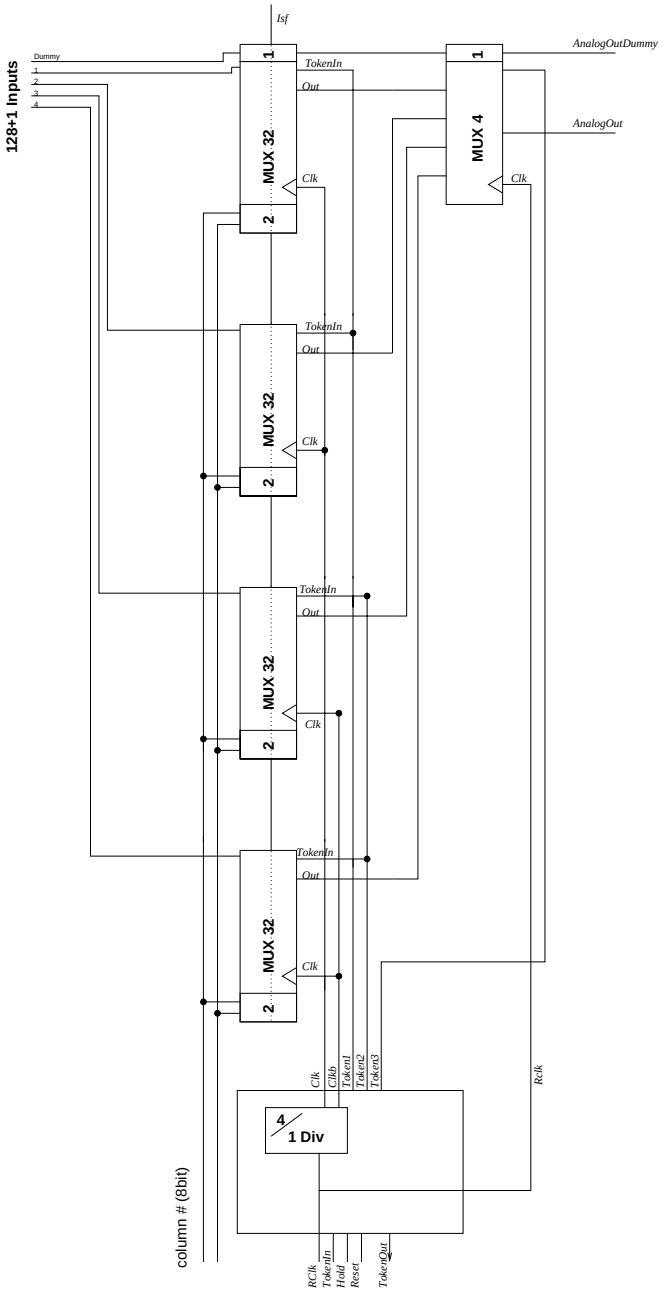

Figure C.7: Cascaded 128+8+1 channel multiplexer

As can be seen from fig. C.7 8 bits denominating the pipeline column the current event has been stored in are "woven" into the multiplexer, appearing as trailer in the analog output (fig. C.9).

C.3.7 The Current Buffer

The current buffer is a differential voltage input/single current output ("transconductance") amplifier (fig. C.8) that converts the voltage signals

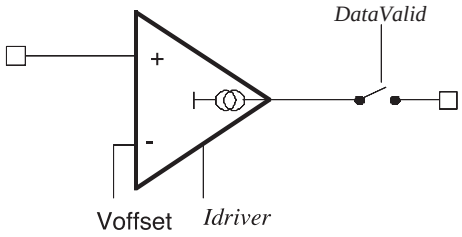

Figure C.8: Current buffer

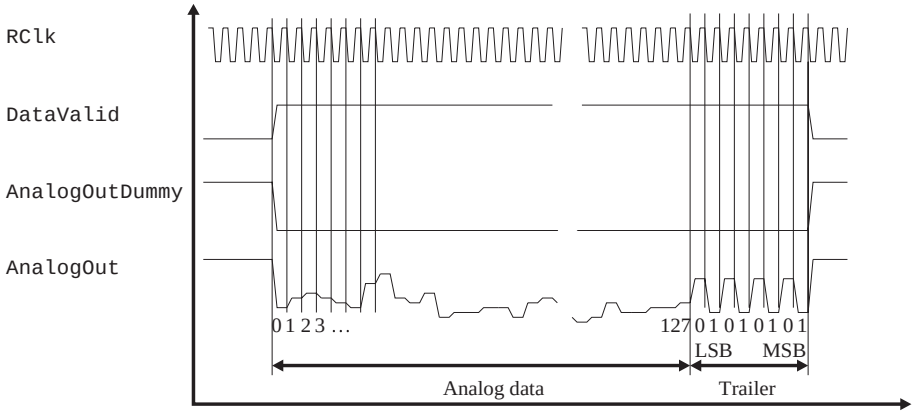

Figure C.9: Format of a readout burst

delivered by the multiplexer. Linearity is achieved by a current feedback topology. The two multiplexer output voltages *AnalogOut* and *AnalogOutDummy* are amplified by two separate buffers sharing the common reference voltage *Voffset*. In case of radiation damage

- *Idriver* should be kept constant.
- *Voffset* should be adjusted so that the output offset current stays constant (probably the level must be raised).

Figure C.9 shows how the chip outputs its data after receiving a trigger. Synchronously to the falling edge of `RClk` data are asserted, indicated by `DataValid` going high. The current output signals `AnalogOut` and `AnalogOutDummy` are plotted as they can be observed at the chip output shorted to ground. The 128 amplifier channels are output channel 0 first, followed by channel 1 etc. up to channel 127. Analog data are followed immediately by an 8 bit trailer showing the pipeline column number the event has been stored in. This number is coded LSB first, a "1" bit coded as $\approx$+2 MIP_{Si}, a "0" bit as $\approx$-2 MIP_{Si}. `AnalogOutDummy` should be subtracted from `AnalogOut` to cancel offset, common mode and clock feed through.

C.3.8 The Analog Receiver Circuit

The current signals delivered on `AnalogOut` and `AnalogOutDummy` should be received by a fast (bandwidth 100 MHz) transimpedance amplifier to make use of the full 40 MHz drive capability of the on-chip current buffer and subtracted from each other to reduce common mode interference. The schematic depicted in fig. C.10 shows the suggested receiver circuit. The gain delivered at 1.5kΩ transimpedance is $\approx$ 85mV/MIP_{Si} (Helix128S-2/2.1) resp. 425mV/MIP_{Si} (Helix128S-2.2/2.3). The 50 Ω resistors at the inputs were chosen to terminate properly a 50 Ω cable. The Comlinear CLC 401 opamp features a high bandwidth and the ability to handle large voltage gains (voltage gain = 30 in the suggested configuration).

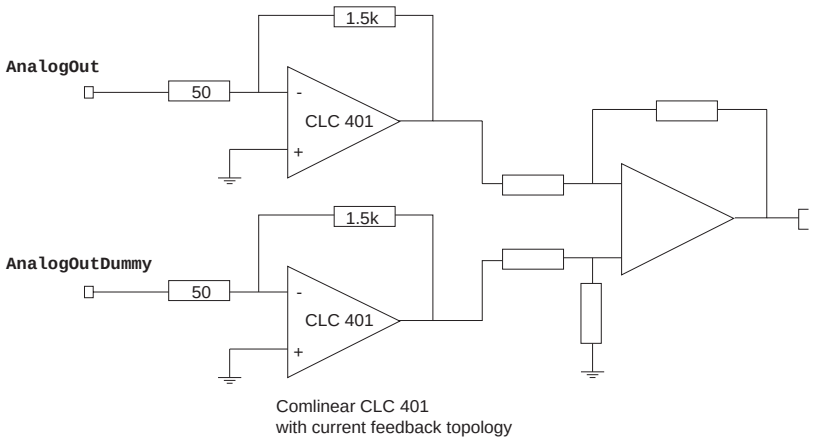

Figure C.10: Suggested receiver circuit for the analog signals `AnalogOut` and `AnalogOutDummy` of the Helix128-2.0. For the Helix versions 2.2 and 2.3, 300Ω should be used as feedback resistor together with a Comlinear CLC400 instead of the CLC401.

C.4 Digital Control Circuitry

In the predecessor version to the chip described, HELIX128 [10], the digital control circuitry necessary to operate according to the experimental requirements has been split between the HELIX128 itself and the support and control chip SUFIX [11]. In the present version, this separation was abandoned and all functions could be merged into Helix128-2.

C.4.1 The Pipeline and Readout Control Logic

The pipeline control logic (see fig. C.1) receives incoming triggers via the interface circuit and tags the corresponding columns of the capacitor storage array such that they are not overwritten by new data before they are read out. A write pointer scans over the pipeline columns incremented by the sampling clock *SClk* which can be either internally generated from the `RClk` or taken from the `SClk` pad (refer to section C.4.4). After `notReset` is set to +2 V, the pointer starts its walk at column 0, the one nearest to the frontend, wrapping around at column number 140 = 128 + 8 + 5 - 1 (141 for Helix128-3.1). Sampling the output of the preamplifier/shaper to the storage capacitor is enabled during the high period of `SClk`, the falling edge determining the held frontend output value.[4] With the latency specified by the content of the *Latency* register the trigger pointer follows the write pointer. When a trigger occurs (indicated by a high `TrigIn` signal at the rising edge of `SClk`, see fig. C.11), the column number which is currently pointed at by the trigger pointer is stored into a FIFO and marked to be read out. The FIFO has a storage capacity of eight numbers.

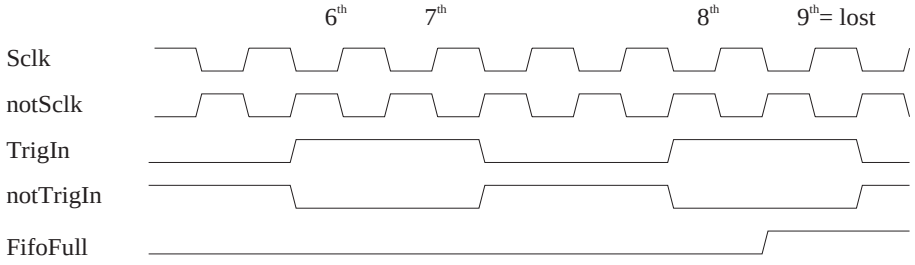

Figure C.11: Sampling of the `TrigIn`-signal occurs at the rising edge of `SClk`; if more than 8 triggers are given in fast sequence, the derandomizing buffer flows over signalling "`FifoFull`"

The "oldest" number within the FIFO is loaded into the read pointer which addresses the column of the storage capacitor array to be loaded into the readout multiplexer. Loading the multiplexer is a multi-stage process: it takes 2 *SClk* cycles to reset the readout line and the pipeamp, followed by 1 *SClk* cycle break and another 2 *SClk* cycles to read the data

[4] Since the risetime of the preamplifier/shaper is about 50ns, the high period of the external `SClk` should be of the same value.

with the pipeamp until its output is stored by the readout multiplexer. After this period the

multiplexer is ready to transmit data. The condition for the multiplexer to start transmission once it has loaded data is given by a high `TransmitEnable`, a high `MultiplexerEnable` and the presence of a token (as explained in section C.4.6). After transmission of data the chip immediately starts loading data from the next tagged column into the multiplexer. In parallel, the chip watches its `ReturnTokenIn` line. When this is high during a falling edge of `RClk`, the previous pipeline column is untagged thus being available for writing again. Thus, since all chips in a daisy chain share the *ReturnToken* line, the synchronicity of pipeline operation is maintained even in daisy chain operation.

C.4.2 The Bias Current Sources

The various bias currents of the analog stages described in section 1 are generated by 8 bit digital to analog converters which are controlled by registers of the same name. The conversion slope of the DACs is 2.5µA/LSB with a register value of 0 corresponding to zero output current. To achieve correct operation of the bias generator circuit, a reference current of 100 µA must be flowing into the `IrefIn` pad which can be generated either by an external source or by using the internal reference current generator. When using the latter, `IrefOut` has to be bonded directly to `IrefIn` and a resistor of $20k\Omega$ must be connected from `Rref` to `Vssa` (−2V).

Capacitance on the `Rref` node increases the problem No. 13 described in sect. C.6 and therefore the reference resistor *must not be blocked*. A capacitor $\geq$ 100nF from `IrefIn/IrefOut` to `Vssa` is recommended to stabilize the operation of the current source. This is not required, on Helix128-3.1a but still recommended to increase the PSSR of the circuit.

C.4.3 The Control Voltage Sources

The control voltage sources are generated by DACs with a resolution of 7 bits (Helix128-2/2.1) resp. 8 bits (Helix128-2.2/2.3/3.x), working from rail to rail (i.e. from $-2V$ to $+2V$); the slope provided is $\approx$ 31 mV/LSB (Helix128-2/2.1) resp. 15 mV/LSB (Helix128-2.2/2.3). The voltage DACs are controlled by the registers of the same name with the LSBs of the 8 bit wide registers ignored (Helix128-2/2.1). A register setting of 0 corresponds to an output voltage of -2V.

C.4.4 The Sampling Clock Generator

In the following we discuss the sampling clock *SClk* ruling the pipeline operation. This clock should not be confused with the comparator's `CompClk` clock described in sect. C.3.3 (both run at 10 MHz in the HERA-*B* experiment; both try to catch the maximum pulse height of the shaped

frontend pulse but, however, the sampling transitions of the two clock should be slightly detuned to avoid mutual interference). The falling edge of the sampling clock determines the sampling point of time, i. e. when the frontend outputs are sampled into the pipeline column "on duty". The sampling clock (nominally 10Mhz) *SClk* can be either applied to the `SClk` input pad or generated internally from `RClk`. Therefore the lower four bits of the *ClkDiv* register hold the ratio of the `RClk` (readout) and *SClk* (sampling) clocks. Valid values are 0-15. If the content of $ClkDiv = 0$, the signal applied to the `SClk` input pad is used for sampling. The internally generated *SClk* will have its first **rising edge** synchronously with the **fourth rising edge** of `RClk` following the **falling edge** of `notReset`, since *SClk* has to be running when `notReset` is released and the chip starts sampling. This behaviour is illustrated in Fig. C.12. The duty cycle of the internally generated *SClk* signal is 50%.

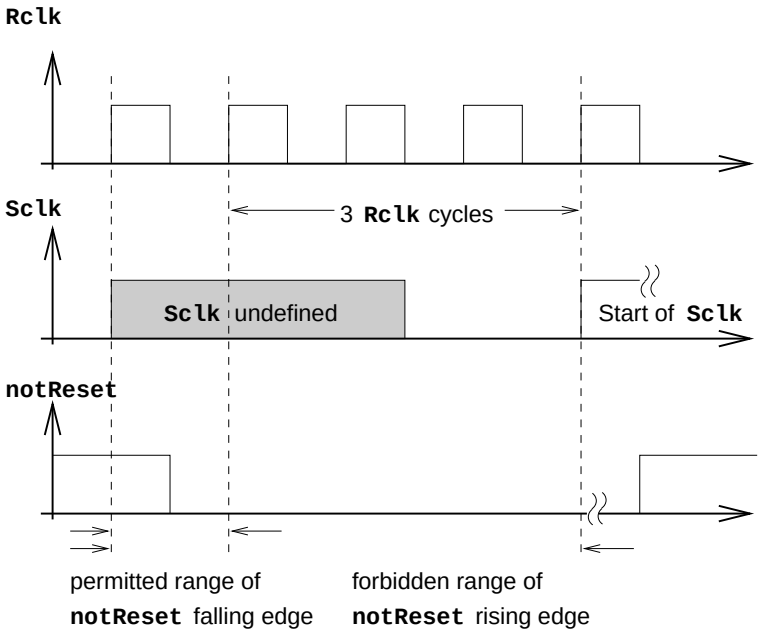

Figure C.12: `SClk` initialization for `Clockdiv` $\neq 0$

C.4.5 The Starter Circuit

Helix128-2 features two different resets: first, `SufixReset` resets all the registers as described in table C.5 but, however, leaves the pipeline and multiplexer operation unaffected. Applying a `SufixReset` signal after power up is not mandatory since the internal registers should wake up automatically in the 0 state. `notReset`, on the other hand, only resets the pipeline pointers (described in the following) and the readout multiplexer control circuitry. By activating `notReset`, which may be done asynchronously, an undefined state in the pipeline or in the multiplexer

can be corrected without the need of reprogramming all internal bias registers. For an initial reset we recommend to first perform `SufixReset` and `notReset`, then release the `SufixReset` and load the internal registers as described in section C.4.9, and finally release `notReset` by setting it to +2 V. The adjustment of the pipeline delay according to the desired trigger latency is done by programming the *Latency* register. To illustrate this feature, we repeat the pipeline operation for convenience (see section C.4.1 for a detailed discussion): immediately after releasing the active low `notReset` (synchronously to the rising edge of `SClk`) the write pointer starts walking over the pipeline incremented by `SClk`. The pipeline column the `write pointer` currently points at stores the frontend output voltage at the falling edge of `SClk`. The trigger pointer as the second pointer controlling the pipeline points to the pipeline column to be read out if a trigger on `TrigIn` was given. The start of the pipeline trigger pointer is delayed with respect to the start of the write pointer by the number of `SClk` cycles specified in the *Latency* register thus determining the latency of the pipeline.

C.4.6 The Readout

Daisy chain mode

Helix128-2 chips can be daisy-chained in order to save cost in following stages. A diagram of several Helix128-2.0/2.1 chips in a daisy chain is given in fig. C.13. The following discussion holds for Helix128-2.0/2.1; Helix128-2.2/2.3 makes use of an identical scheme but with reversed token direction (i. e. the chips in a daisy-chain are read out from top to bottom). Failsafe token pads as well as pads for a reversed-polarity token have been added for compatibility with the future Helix128-3.0. The first or leading Helix128-2 in the daisy chain generates the primary token at the output of `SufixTokenOut`. By bonding `SufixTokenOut` to `HelixTokenIn` on the first chip the token is transferred to the readout multiplexer which starts transmitting the analog values on the common analog busses (the outputs of chips not posessing the token are switched to high ohmic). After the final values of chip #1's analog data the token is output on `HelixTokenOut` of chip #1 to `HelixTokenIn` of chip #2. Upon receipt the second chip's multiplexer starts sending data since the `HelixTokenIn` and `SufixTokenIn` pads are internally connected (the `SufixTokenIn` pad has been added for ease of bonding). By bonding from `HelixTokenOut` to `ReturnTokenIn` on the daisy chain's last chip the *token* is fed into the token return path thus being directly transferred to the leading chip of the chain (since `ReturnTokenIn` and `ReturnTokenOut` are internally connected). By receipt of the returning token the leading chip is signaled the end of the transmission. The signal on the common output bus is illustrated in fig. C.14. If only a single chip is operated, `SufixTokenOut` must be bonded to `SufixTokenIn` and `HelixTokenOut` to `ReturnTokenIn`.

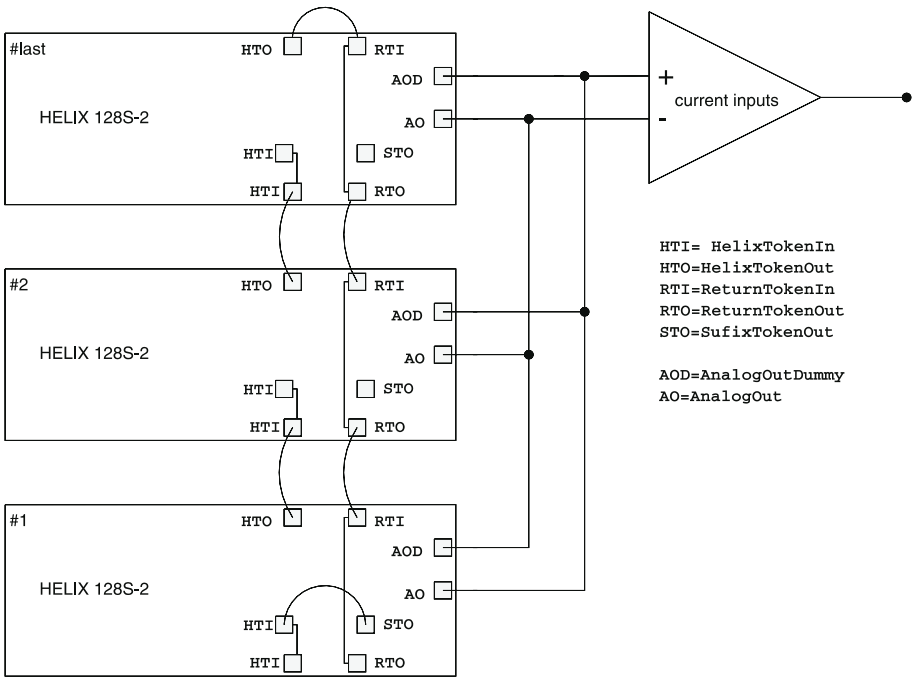

Figure C.13: Helix128-2.0/2.1 in daisy chain mode; with Helix128-2.2/2.3 the token circulates in opposite direction (i. e. from bottom to top)

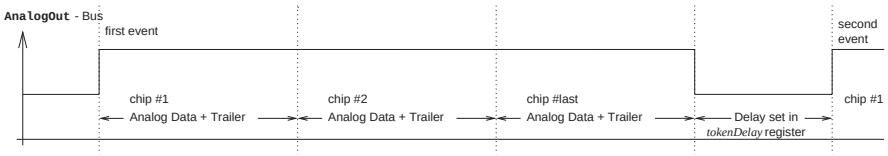

Figure C.14: Analog current signal on the `AnalogOut` bus for the daisy chain illustrated in fig. C.13

Failsafe daisy chaining with Helix128-3.0

With Helix128-2 daisy chaining, a single chip failure would cause the complete daisy chain of chips unaccessible. This is especially disastrous when the daisy chain is very long. To decrease the impact of a single chip failure on the whole daisy chain a failsafe daisy chain mechanism has been implemented in the Helix128-3.0, which ensures that no isolated defect chip in a daisy chain can block the complete chain. Every chip is not only connected to its predecessor and successor in the daisy chain, but also to the second predecessor and successor (fig. C.15). When a chip has sent its data it sends a token via the *HelixTokenOut* and *FailsafeHelixTokenOut* ports [5].

[5] *HelixTokenOut* port abbreviates `HelixTokenOut` and `notHelixTokenOut` pads and for all other differential token signals accordingly

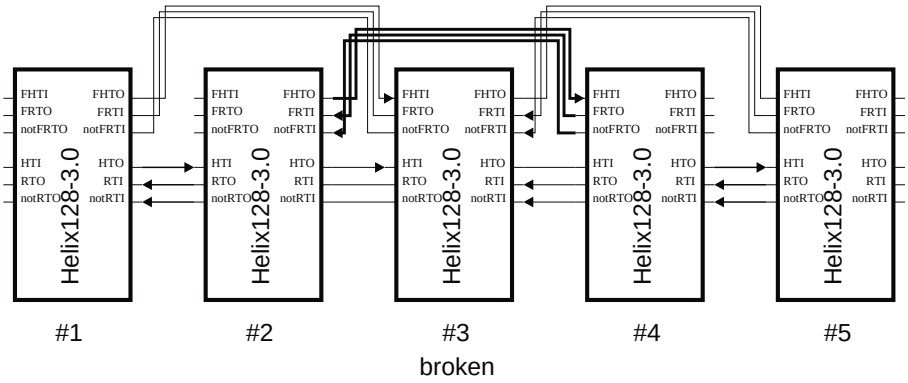

Figure C.15: Failsafe daisy chain mechanism. The arrows indicate where tokens are submitted. The thick lines indicate the active token path which is routed around the broken chip in the chain.

These tokens are routed to the chip's successor's *HelixTokenIn* port and to the second successor's *FailsafeHelixTokenIn* port. Normally, a chip starts transmission of data when the token arrives at the *HelixTokenIn* port. The successor of a broken chip can be programmed to start transmission of data upon reception of a token on its *FailsafeTokenIn* port. The same mechanism is implemented for the *ReturnToken* ports. The failsafe token mechanism is programmable via the bit 4 . . . 7 of the clock divider register. Table C.2 shows all bits necessary for controlling the mechanism.

Bitname	Explanation	Number
BypassHelixToken	If 0 then `HelixTokenIn` is activated, if 1 then `FailsafeHelixTokenIn` is activated	4
BypassReturnToken	If 0 then `ReturnTokenIn` is activated, if 1 then `FailsafereturnTokenIn` is activated	5
LastInChain	If this chip is the last in the chain, this bit must be set to 1	6
FirstInChain	If this chip is the first in the chain, this bit must be set to 1	7

Table C.2: Definition of failsafe token control bits and bit number in the *ClkDiv* register

TokenDelay

The content of the *TokenDelay* register determines the duration in `RClk` cycles the leading Helix128-2 waits before it starts sending the next event's analog data after having received the return token from the previous readout. Thus, a regular delay in processing of the sent data can be accounted for (see fig. C.14). The delay is achieved by holding back the `SufixTokenOut` token output of the leading Helix128-2. A value of 0 indicates immediate sending of the next event. In case of single chip operation

the delay as specified in the *TokenDelay* register is added to the time which is needed to load the multiplexer.

`TransmitEnable`

A sudden busy condition of the data receiving stage can be flagged to Helix128-2 by pulling low `TransmitEnable`; it then stops transmitting data and starts again when `TransmitEnable` is pulled up (this condition is checked at the falling `RClk` edge). `TransmitEnable` is internally pulled up to +2 V.

C.4.7 The Synchronicity Monitor

The synchronicity monitor circuit checks the signals of adjacent Helix128-2 chips to assure synchronous operation. For this purpose, internal signals *TrigMon* and *WriteMon* are generated when the write pointer resp. the trigger pointer passes by column 0 of the pipeline. The synchronicity monitor checks the simultaneous occurrence of these internal signals as well as of the `DataValid` signals with the ones received on `SyncIn<`*i*`>`. `SyncOut<`*i*`>` signals are generated depending on the comparison result according to table C.3. The `DataValid` check, naturally, has to be abandoned in daisy chain operation mode. Using a differential architecture both missing and wrong monitor pulses can be detected. If a deviation occurres, an error signal on `Error` is generated, which should be collected from the last chip in the synchronicity chain. The content of the *SyncCtrl* register determines the behaviour of the `SyncOut<0:5>` and `Error` signals. A description is given in Tab. C.4.

signal name	logic dependency	comment
`SyncOut<0>`	! *TrigMon* & `SyncIn<0>`	*active low wired or* of all *TrigMon* signals
`SyncOut<1>`	*TrigMon* & `SyncIn<1>`	*wired and* of all *TrigMon* signals
`SyncOut<2>`	!*writeMon* & `SyncIn<2>`	*active low wired or* of all *writeMon* signals
`SyncOut<3>`	*writeMon* & `SyncIn<3>`	*wired and* of all *writeMon* signals
`SyncOut<4>`	!`DataValid` & `SyncIn<4>`	*active low wired or* of all `DataValid` signals
`SyncOut<5>`	`DataValid` & `SyncIn<5>`	*wired and* of all `DataValid` signals

Table C.3: Dependencies of the `SyncIn<5:0>` and `SyncOut<5:0>` signals

bit number	function if cleared (*0*)	function if set (*1*)
7 (MSB)	`Error` pin in latch mode (i.e. signal remains high after occurrence of an error	`Error` pin in transient mode (i.e. it becomes active only during the existence of an error condition)
6	`Error` signal is generated from `Sync<0:1>` (i.e. *TrigMon*) signals	`Sync<0:1>` (i.e. *TrigMon*) is ignored for the `Error` signal
5	`Error` signal is generated from `Sync<2:3>` (i.e. *WriteMon*) signals	`Sync<2:3>` (i.e. *WriteMon*) is ignored for the `Error` signal
4	`Error` signal is generated from `Sync<4:5>` (i.e. `DataValid`) signals	`Sync<4:5>` (i.e. `DataValid`) is ignored for the `Error` signal
3	`SyncOut<0:1>` signal is generated from `SyncIn<0:1>` and *TrigMon* signals	`SyncOut<0:1>` = `SyncIn<0:1>` (i.e. *TrigMon* of this Helix128-2 does not contribute to `SyncOut<0:1>`)
2	`SyncOut<2:3>` signal is generated from `SyncIn<2:3>` and *WriteMon* signals	`SyncOut<2:3>` = `SyncIn<2:3>` (i.e. *WriteMon* of this Helix128-2 does not contribute to `SyncOut<2:3>`)
1	`SyncOut<4:5>` signal is generated from `SyncIn<4:5>` and `DataValid` signals	`SyncOut<4:5>` = `SyncIn<4:5>` (i.e. `DataValid` of this Helix128-2 does not contribute to `SyncOut<2:3>`)
0 (LSB)	`Error` = *0* (i.e. reset `Error`, only useful if bit #7 = *0*)	`Error` = *1* (i.e. set `Error`, only useful if bit #7 = *0*)

Table C.4: Flags of the *SyncReg* register

C.4.8 The Test Pulse Circuit

At the rising edge of a signal applied to the `FcsTp` pad, a charge equivalent to

- $\approx +2$ MIP_{Si} is injected into the inputs of the channels 1, 5, 9, 13 ...,
- $\approx +1$ MIP_{Si} into channels 2, 6, 10, 14 ...,
- ≈ -1 MIP_{Si} into channels 3, 7, 11, 15 ... and
- ≈ -2 MIP_{Si} into channels 4, 8, 12, 16 ....

with $+1MIP_{\mathrm{Si}}$ being equivalent to a charge of 24.000 electrons. Thus, with an appropriate trigger a stairway-like readout figure is generated . The polarity of the injected charge toggles after each application (i.e. -1 MIP_{Si} is injected into channels 1, 5, 9, 13 ... for an even number of test pulses).

C.4.9 The Serial Interface

The programming of the Helix128-2's internal registers is achieved via a simple serial interface of three lines. In Helix128-2.0/2.1 the three signals involved are `SeRClk`, `SerData`, and `SerLoad`, in Helix128-2.2/2.3 `SeRClk` has been merged with `RClk` and `SerData` with `TrigIn`. Thus, in the latter case, programming of the registers will give rise to multiple triggers; it is therefore recommended to keep `notReset` low during programming. The following explanation applies to Helix128-2.0/2.1, but is easily extended to the new scheme by making the above stated substitution. During programming of the chip `RClk` and `SeRClk` must run continuously. A 20 bit word is applied according to the Helix128-2 data frame (fig. C.16) on the `SerData` line synchronously to `SeRClk` (fig. C.17). The end of the word is signaled to Helix128-2 by activating `SerLoad`; note that `SeRClk` must continue running at least one more cycle. A Helix128-2 serial data frame consists of the following components:

- The *broadcast* or *common set bit*; if set, the chip address decoding is overridden and the register is set to the specified value.
- The *chip address*; the 6 bits of the chip address are compared to the signals of the `ID<5:0>` pads. If they do not match, the following bits are ignored (unless the *broadcast bit* has been set).
- The *register address*; the 5 bits specify the address of the register to be written to.
- The *data* word; the 8 bits contain the value the specified register is set to.

Data are written into the chip with the MSB first. Tab. C.5 shows the map of the register addresses.

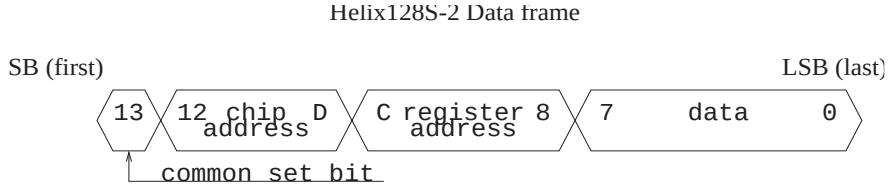

Figure C.16: Data format of the Helix128-2 chip

C.4.10 Last but not Least

`FifoFull`

The active high `FifoFull` flag is set when all eight slots in the event buffer are occupied; in this case Helix128-2 does not accept any further triggers and the corresponding events will be lost.

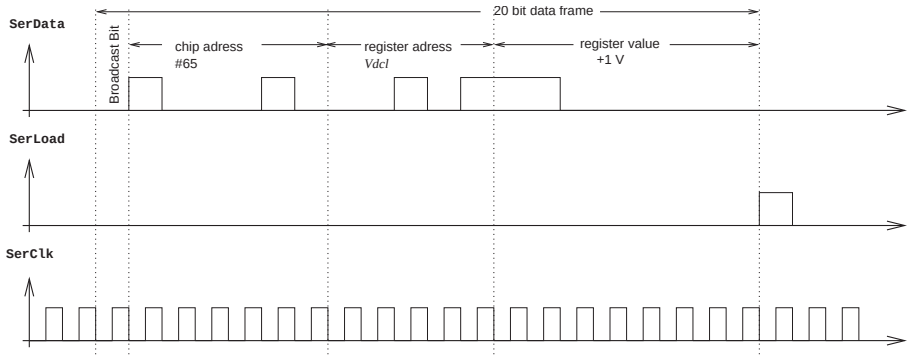

Figure C.17: Serial interface timing (Helix128S-2.0/2.1); substituting `SeRClk` by `RClk` and `SerData` by `TrigIn` gives the programming sequence of Helix128S-2.2/2.3. In the example plotted the *Vdcl* bias voltage is set to its nominal (Helix128-2.0/2.1/2.2) value of +1V

Register address (*HEX*)	(*BIN*)	(*DEC*)	Register name
01	00001	01	*Ipre*
02	00010	02	*Isha*
03	00011	03	*Ibuf*
04	00100	04	*Icomp*
05	00101	05	*Ipipe*
06	00110	06	*Isf*
07	00111	07	*Idriver*
08	01000	08	*Vfp*
09	01001	09	*Vfs*
0A	01010	10	*VcompRef*
0B	01011	11	*Vd*
0C	01100	12	*Vdcl*
0D	01101	13	*Voffset*
11	10001	17	*Latency*
12	10010	18	*SyncReg*
13	10011	19	*ClkDiv*
14	10100	20	*TokenDelay*

Table C.5: Helix128-2 register map

`MuxDisable`

`MuxDisable` is out of use.

C.5 Appendix: Pad Description

To match the pitch of 50µm silicon microstrip detectors an overall pitch of 50µm can be obtained by placing Helix128-2 chips side by side. The 128 analog input pads are located at the front of the chip w. r. t. the detector (see fig. C.18) while all pins necessary to operate the chip, i. e. power supply, digital control lines and analog output, are located at the rear side. The chip's trigger output pads are placed at the bottom side (with the input pads left) due to the relaxed space requirements of the HERA-*B* Inner Tracking Detector which makes use of the comparator information. Digital signals are categorized as outlined in table C.6. For a description of the analog pads refer to the text. All pads have been given reference numbers. Counting starts with the uppermost pad of the front (i. e. detector) side (with the input pads left) and continues with the peripheral pads counterclockwise around the chip. Finally, the probe pads in the chip's interior are counted from bottom to top. For the geometrical location refer to figure C.18 on page 227 (Helix128-2), fig. C.19 on page 228 (Helix128-2.1), and fig. C.20 on page 229 (Helix128-2.2/2.3).

C.5.1 Front Pads

The analog input pads and some analog supply pads are located at the front side of Helix128-2. The input pads are staggered fourfold with a pitch of 41.4µm. A description is given for Helix128-2.0 and Helix128-2.1 in table C.7 on page 212, a description for Helix128-2.2/2.3 can be found in table C.8 on page 212.

C.5.2 Bottom Pads

The bottom pads of Helix128-2.0/2.1 are explained in table C.9 on page 213. The bottom pads of Helix128-2.2/2.3 are explained in table C.10 and C.11 on page 214 and 215, respectively.

Type	Description
input	Digital CMOS input operating at -2V... +2V supply.
output	Digital CMOS output operating at -2V... +2V supply.
input (int. pulldown)	Digital CMOS input operating at -2V... +2V supply with internal pulldown resistor.
input (int. pullup)	Digital CMOS input operating at -2V... +2V supply with internal pullup resistor.
output (open drain)	Digital open drain output operating at -2V... +2V supply.
LVDS-input	Low voltage differential CMOS input ($\Delta V_{Sig,notSig} \geq 350$ mV)

Table C.6: Electrical specification of digital input and output pads

Ref. no.	Pin name	Type	Description
1	Vdda	supply	positive analog supply voltage (+2V)
2	Vssa	supply	negative analog supply voltage (−2V)
3	In⟨0⟩	analog input	input of channel 0
4	In⟨1⟩	analog input	input of channel 1
5	In⟨2⟩	analog input	input of channel 2
6-128	⋮	⋮	⋮
129	In⟨126⟩	analog input	input of channel 126
130	In⟨127⟩	analog input	input of channel 127
131,132	Gnda	supply	analog ground (0V)

Table C.7: Pads on the front side of Helix128-2.0/2.1. The first pad in the table corresponds to the uppermost pad of the front side (looking at the chip with the frontside left). The geometrical locations throughout the manual will always be referred to this orientation.

Ref. no.	Pin name	Type	Description
1	Vdda	supply	positive analog supply voltage (+2V)
2	Vssa	supply	negative analog supply voltage (−2V)
2a	InTest	input	analog input pad for test channel
3	In⟨0⟩	analog input	input of channel 0
4	In⟨1⟩	analog input	input of channel 1
5	In⟨2⟩	analog input	input of channel 2
6-128	⋮	⋮	⋮
129	In⟨126⟩	analog input	input of channel 126
130	In⟨127⟩	analog input	input of channel 127
131,132	Gnda	supply	analog ground (0V)

Table C.8: Pads on the front side of Helix128-2.2/2.3/3.x. The first pad in the table corresponds to the uppermost pad of the front side (looking at the chip having the frontside left). The geometrical locations throughout the manual will always be referred to this orientation.

Ref. no.	Pin name	Type	Description
133,134	Gnda	supply	analog ground (0V)
135,136	Vssa	supply	negative analog supply voltage (−2V)
137,138	Vdda	supply	positive analog supply voltage (+2V)
139	VssComp	supply	negative supply voltage for comparator (−2V)
140	VddComp	supply	positive supply voltage for comparator (+2V)
141	notCompClk	input	active low comparator dummy clock
142	CompClk	input	active high comparator clock
143	CompPol	input	polarity switch for comparator +2V⇒ detection of positive signals
144	notCompOut⟨31⟩	output (open drain)	ORed active low output of comparators on channels 127...124
145	notCompOut⟨30⟩	output (open drain)	ORed active low output of comparators on channels 123...120
146-173	⋮	⋮	⋮
174	notCompOut⟨1⟩	output (open drain)	ORed active low output of comparators on channels 7...4
175	notCompOut⟨0⟩	output (open drain)	ORed active low output of comparators on channels 3...0
176	MuxDisable	input (int. pulldown)	Out of use
177	TransmitEnable	input (int. pullup)	−2V disables analog data transmission
178	FifoFull	output	indicates readout fifo overflow.
179	HelixTokenIn	input	to be connected to pad no. 257 HelixTokenOut of predecessing Helix128-2.0/2.1 if the chip is non-leading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
180	ReturnTokenOut	output	to be connected to pad no. 256 ReturnToken-In of predecessing Helix128-2.0/2.1 if the chip is non-leading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
181	SyncIn⟨0⟩	input (int. pullup)	synchronicity monitoring input from neighbouring Helix128-2.0/2.1
182	SyncIn⟨1⟩	input (int. pullup)	“
183-185	⋮	⋮	⋮
186	SyncIn⟨5⟩	input (int. pullup)	“
187-197	n. c.		

Table C.9: Pads on the bottom side of Helix128-2.0/2.1. The first pad in the table corresponds to the very left hand pad of the bottom side (with the frontside left).

Ref. no.	Pin name	Type	Description
133,134	Gnda	supply	analog ground (0V)
135,136	Vssa	supply	negative analog supply voltage (−2V)
137,138	Vdda	supply	positive analog supply voltage (+2V)
138a	GndComp	supply	Reference voltage for comparators' AC coupling
139	VssComp	supply	negative supply voltage for comparator (−2V)
140	VddComp	supply	positive supply voltage for comparator (+2V)
141	notCompClk	LVDS-input	active high comparator dummy clock
142	CompClk	LVDS-input	active low comparator clock
143	CompPol	input	polarity switch for comparator +2V⇒ detection of positive signals
144	notCompOut⟨31⟩	output (open drain)	ORed active low output of comparators on channels 127...124
145	notCompOut⟨30⟩	output (open drain)	ORed active low output of comparators on channels 123...120
146-173	⋮	⋮	⋮
174	notCompOut⟨1⟩	output (open drain)	ORed active low output of comparators on channels 7...4
175	notCompOut⟨0⟩	output (open drain)	ORed active low output of comparators on channels 3...0
176	VssComp	supply	−2V supply for notCompOut⟨1⟩
177	TransmitEnable	input (int. pullup)	−2V disables analog data transmission
178	FifoFull	output	indicates readout fifo overflow.
178a	VssComp	supply	−2V supply for notCompOut⟨1⟩

Table C.10: Pads on the bottom side of Helix128-2.2/2.3. The first pad in the table corresponds to the very left hand pad of the bottom side (with the frontside left). See table C.11 for pads 179...197a.

Ref. no.	Pin name	Type	Description
179	notHelixTokenOut	output	Reserved for future use
180	notReturnTokenIn	input	Reserved for future use
180a	ReturnTokenIn	input	return path token input; must be bonded to pad no. 187 HelixTokenOut if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 257a ReturnTokenOut of following chip in the daisy chain)
181	SyncIn⟨0⟩	input (int. pullup)	synchronicity monitoring input from neighbouring Helix128-2.2/2.3
182	SyncIn⟨1⟩	input (int. pullup)	"
183-185	⋮	⋮	⋮
186	SyncIn⟨5⟩	input (int. pullup)	"
187	HelixTokenOut	output	must be bonded to pad no. 180a Return-TokenIn if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 251 HelixTokenIn of following chip in the daisy chain)
188	notFailsafe-HelixTokenOut	output	Reserved for future use
189	notFailsafe-ReturnTokenIn	input	Reserved for future use
190	Failsafe-ReturnTokenIn	input	Reserved for future use
191	Failsafe-HelixTokenOut	output	Reserved for future use
192	n. c.		
193-197a			Removed

Table C.11: Pads on the bottom side of Helix128-2.2/2.3 (continued). The first pad in the table corresponds to the very left hand pad of the bottom side (with the frontside left). See table C.10 for pads 133...178a.

Ref. no.	Pin name	Type	Description
179	n. c.		Reserved for future use
180	notReturn-TokenIn	input	Reserved for future use
180a	ReturnTokenIn	input	return path token input; must be bonded to pad no. 187 HelixTokenOut if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 257a ReturnTokenOut of following chip in the daisy chain)
181	SyncIn⟨0⟩	input (int. pullup)	synchronicity monitoring input from neighbouring Helix128-2.2/2.3
182	SyncIn⟨1⟩	input (int. pullup)	"
183-185	⋮	⋮	⋮
186	SyncIn⟨5⟩	input (int. pullup)	"
187	HelixTokenOut	output	must be bonded to pad no. 180a Return-TokenIn if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 251 HelixTokenIn of following chip in the daisy chain)
188	n. c.		Reserved for future use
189	notFailsafe-Return-TokenIn	input	To be connected to notFailsafe-ReturnTokenOut of the next but one chip in the chain.
190	Failsafe-Return-TokenIn	input	To be connected to FailsafeReturn-TokenOut of the next but one chip in the chain.
191	Failsafe-HelixTokenOut	output	To be connected to FailsafeHelix-TokenIn of the next but one chip in the chain.
192	n. c.		Reserved for future use
193-197a			Removed

Table C.12: Pads on the bottom side of Helix128-3.x (continued). The first pad in the table corresponds to the very left hand pad of the bottom side (with the frontside left). See table C.10 for pads 133...178a.

C.5.3 Rear Pads

The pads on the rear side of Helix128-2.x are placed in a 140µm pitch. A description of the pads of Helix128-2.0 is given in table C.13 on page 218, of Helix128-2.1 in table C.14 on page 219, and of Helix128-2.2 in table C.15 on page 220.

Ref. no.	Pin name	Type	Description
240	Vddg	supply	positive pad guard supply voltage (+2V)
239,238	Vddd	supply	positive digital supply voltage +2V)
237-234	Vdda	supply	positive analog supply voltage (+2V)
233-230	Vssa	supply	negative analog supply voltage (−2V)
229,228	Vssd	supply	negative digital supply voltage (−2V)
227	Vssg	supply	negative pad guard supply voltage (−2V)
226	Rref	output	to be connected to external resistor (20kΩ) if internal reference current source is used.
225	IrefOut	output	output of internal reference current source
224	IrefIn	input	reference current input for internal current DAC; may either be connected to an external reference current source or to the IrefOut pin, if internal reference current source is to be used
223	Voffset	blocking	should be connected to external blocking capacitor
222	Idriver	blocking	“
221	Vdcl	blocking	“ $> 1\mu F$
220	Vd	blocking	“ $> 1\mu F$
219	VcompRef	blocking	“
218	AnalogOut-Dummy	output	dummy serial analog output, should be subtracted from AnalogOut
217	AnalogOut	output	serial analog output
216,215	n. c.	n.c.	not connected
214	Id⟨0⟩	input (int. pulldown)	active high chip id address
213-209	⋮	⋮	⋮
209	Id⟨5⟩	input (int. pulldown	“
208	FcsTp	input	digital test pulse input; the rising edge signals moment of charge injection
207	SufixReset	input (int. pulldown	active high reset signal for bias generator and controller part
206	notReset	input	active low pipeline reset signal
205	DataValid	output	active high signal indicating valid data on analogOutDummy and analogOut
204	Error	output	active high signal indicating an error condition on the chip
203	SerLoad	input	active high load signal for serial line interface
202	SerData	input	active high data signal for serial line interface
201	TrigIn	input	active high readout trigger input
200	SeRClk	input	active high clock of serial line interface
199	RClk	input	active high readout clock for data multiplexer
198	SClk	input	active high sampling clock; the falling edge signals the sampling point of time

Table C.13: Pads on the rear side of Helix128-2.0. The first pad in the table corresponds to the uppermost pad on the rear side (with the frontside left).

Ref. no.	Pin name	Type	Description
240	Vddg	supply	positive pad guard supply voltage (+2V)
239,238	Vddd	supply	positive digital supply voltage (+2V)
237-234	Vdda	supply	positive analog supply voltage (+2V)
233-230	Vssa	supply	negative analog supply voltage (−2V)
229,228	Vssd	supply	negative digital supply voltage (−2V)
227	Vssg	supply	negative pad guard supply voltage (−2V)
226	Rref	output	to be connected to external resistor (20kΩ) if internal reference current source is used.
225	IrefOut	output	output of internal reference current source
224	IrefIn	input	reference current input for internal current DAC; may either be connected to an external reference current source or to the IrefOut pin, if internal reference current source is to be used
223	Voffset	blocking	should be connected to external blocking capacitor
222	Idriver	blocking	"
221	Vdcl	blocking	" $> 1\mu F$
220	Vd	blocking	" $> 1\mu F$
219	VcompRef	blocking	"
218	Analog-OutDummy	output	dummy serial analog output, should be subtracted from AnalogOut
217	AnalogOut	output	serial analog output
216	Id⟨0⟩	input (int. pulldown)	active high chip id address
215-211	⋮	⋮	⋮
211	Id⟨5⟩	input (int. pulldown)	"
210	FcsTp	input	digital test pulse input; the rising edge signals moment of charge injection
209	SufixReset	input (int. pulldown)	active high reset signal for bias generator and controller part
208	notReset	input	active low pipeline reset signal
207	DataValid	output	active high signal indicating valid data on AnalogOutDummy and AnalogOut
206	Error	output	active high signal indicating an error condition on the chip
205	SerLoad	input	active high load signal for serial line interface
204	SerData	input	active high data signal for serial line interface
203	TrigIn	input	active high readout trigger input
202	SeRClk	input	active high clock of serial line interface
201	notRClk	input	active low readout clock for data multiplexer
200	RClk	input	active high readout clock for data mux
199	notSClk	input	active low sampling clock; the rising edge signals the sampling point of time
198	SClk	input	active high sampling clock; the falling edge signals the sampling point of time

Table C.14: Pads on the rear side of Helix128-2.1. The first pad in the table corresponds to the uppermost pad of the chip's rear side (with the frontside left).

Ref. no.	Pin name	Type	Description
240	Vddg	supply	positive pad guard supply voltage (+2V)
239,238	Vddd	supply	positive digital supply voltage (+2V)
237-234	Vdda	supply	positive analog supply voltage (+2V)
233-230	Vssa	supply	negative analog supply voltage (−2V)
229,228	Vssd	supply	negative digital supply voltage (−2V)
227	Vssg	supply	negative pad guard supply voltage (−2V)
226	Rref	output	to be connected to external resistor (20kΩ) if internal reference current source is used.
225	IrefOut	output	output of internal reference current source
224	IrefIn	input	reference current input for internal current DAC; may either be connected to an external reference current source or to the IrefOut pin, if internal reference current source is to be used
223	Idriver	blocking	should be connected to external blocking capacitor
222	VcompRef	blocking	"
221	Vd	blocking	"
220	Vdcl	blocking	"
219	Voffset	blockin	"
218	Analog-OutDummy	output	dummy serial analog output, should be subtracted from AnalogOut
217	AnalogOut	output	serial analog output
216	Id⟨0⟩	input (int. pulldown)	active high chip id address
215-211	⋮	⋮	⋮
211	Id⟨5⟩	input (int. pulldown)	"
210	FcsTp	input	digital test pulse input; the rising edge signals moment of charge injection
209	SufixReset	input (int. pulldown)	active high reset signal for bias generator and controller part
208	notReset	input	active low pipeline reset signal
207	DataValid	output	active high signal indicating valid data on analogOutDummy and analogOut
206	Error	output	active high signal indicating an error condition on the chip
205	SerLoad	input	active high load signal for serial line interface
204	notTrigIn	LVDS-inp.	active low readout trigger input
203	TrigIn	LVDS-inp.	active high readout trigger input
202	n. c.	n.c.	Not connected
201	notRClk	LVDS-inp.	active low readout clock for data multiplexer
200	RClk	LVDS-inp.	active high readout clock for data mux
199	notSClk	LVDS-inp.	active low sampling clock; the rising edge signals the sampling point of time
198	SClk	LVDS-inp.	active high sampling clock; the falling edge signals the sampling point of time

Table C.15: Pads on the rear side of Helix128-2.2/2.3/3.x. The first pad in the table corresponds to the uppermost pad of the chip's rear side (with the frontside left).

C.5.4 Top Side Pads

A pad description for Helix128-2.0 and Helix128-2.1 is given in table C.16 on page 222, the description for Helix128-2.2 in table C.17 on page 223. The top side pads of Helix128-3.0 are described in table C.18 on page 224.

C.5.5 Core Pads

Some pads have been located in the chip's core. Most of them are for diagnostic purposes, but on Helix128-2.x pad no. 267 `SufixTokenOut` and no. 268 `HelixTokenIn` play an important role in the daisy chain token scheme; in Helix128-2.2/2.3 `SufixTokenOut` can also be obtained from the top side (pad no. 246). The pads for Helix128-2.0 and Helix128-2.1 are explained in table C.19 on page 225, the pads for Helix128-2.2/2.3 in table C.20 on page 226.

Ref. no.	Pin name	Type	Description
266,265	`Gnda`	supply	analog ground (0V)
264,263	`Vssa`	supply	negative analog supply voltage (−2V)
262,261	`Vdda`	supply	positive analog supply voltage (+2V)
260	`TestOut`	output	test channel preamplifier output
259	`HelixTokenOut`	output	token output; must be bonded to pad no. 256 `ReturnTokenIn` if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 179 `HelixTokenIn` of following chip in the daisy chain)
258	`ReturnTokenIn`	input	return path token input; must be bonded to pad no. 257 `HelixTokenOut` if the chip is the last in the daisy chain and for single chip operation (otherwise bonded to pad no. 180 `ReturnTokenOut` of following chip in the daisy chain)
257	`SyncOut`⟨0⟩	output	synchronicity monitoring output to neighbouring Helix128-2.0/2.1
256	`SyncOut`⟨1⟩	output	"
255-253	⋮	⋮	⋮
252	`SyncOut`⟨5⟩	output	"
251	`SufixBus`⟨7⟩	test outp.	bias generator data bus; used for verification of correct internal operation; no connection needed for normal operation
250	`SufixBus`⟨6⟩	test outp.	"
249-245	⋮	⋮	⋮
244	`SufixBus`⟨0⟩	test outp.	"
243	`notSel`⟨6⟩	test outp.	select bus in bias generator; strobes access to the *Idriver* DAC; used for verification of correct internal operation; no connection needed for normal operation
242	`notSel`⟨5⟩	test outp.	select bus in bias generator; strobes access to the *Isf* DAC; used for verification of correct internal operation; no connection needed for normal operation
241	`notSel`⟨4⟩	test outp.	select bus in bias generator; strobes access to the *Ipipe* DAC; used for verification of correct internal operation; no connection needed for normal operation

Table C.16: Pads on the top side of Helix128-2.0/2.1. The first pad in the table corresponds to the uppermost pad of the chip's top side (with the frontside left).

Ref. no.	Pin name	Type	Description
266,265	Gnda	supply	analog ground (0V)
264,263	Vssa	supply	negative analog supply voltage (−2V)
262,261	Vdda	supply	positive analog supply voltage (+2V)
260	TestOut	output	test channel preamplifier output
259c	GndComp	supply	Reference voltage for comparators' AC coupling (0V)
259b	VssComp	supply	Comparators' most negative supply (-2V)
259a	VddComp	supply	Comparators' most positive supply (+2V)
259	notHelixTokenIn	input	Reserved for future use
258	notReturnTokenOut	output	Reserved for future use
257a	ReturnTokenOut	output	to be connected to pad no. 180a ReturnTokenIn of predecessing Helix128-2.2/2.3 if the chip is non-leading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
257	SyncOut⟨0⟩	output	synchronicity monitoring output to neighbouring Helix128-2.2./2.3
256	SyncOut⟨1⟩	output	"
255-253	⋮	⋮	⋮
252	SyncOut⟨5⟩	output	"
251	HelixTokenIn	input	to be connected to pad no. 187 HelixTokenOut of predecessing Helix128-2.2/2.3 if the chip is non-leading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
250	notFailsafeReturn-TokenOut	output	Reserved for future use.
249	FailsafeReturn-TokenOut	output	Reserved for future use.
248	FailsafeHelix-TokenIn	input	Reserved for future use.
247	FailsafeHelix-TokenOut	output	Reserved for future use.
246	SufixTokenOut	output	Output of token generator (see pad no. 267)
245-240a	n. c.		Removed

Table C.17: Pads on the top side of Helix128-2.2/2.3. The first pad in the table corresponds to the uppermost pad of the chip's top side (with the frontside left).

Ref. no.	Pin name	Type	Description
266,265	Gnda	supply	analog ground (0V)
264,263	Vssa	supply	negative analog supply voltage (−2V)
262,261	Vdda	supply	positive analog supply voltage (+2V)
260	TestOut	output	test channel preamplifier output
259c	GndComp	supply	Reference voltage for comparators' AC coupling (0V)
259b	VssComp	supply	Comparators' most negative supply (-2V)
259a	VddComp	supply	Comparators' most positive supply (+2V)
259	n. c.	n. c.	Reserved for future use
258	notReturnTokenOut	output	Reserved for future use
257a	ReturnTokenOut	output	to be connected to pad no. 180a ReturnTokenIn of predecessing Helix128-2.2/2.3 if the chip is non-leading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
257	SyncOut⟨0⟩	output	synchronicity monitoring output to neighbouring Helix128-2.2./2.3
256	SyncOut⟨1⟩	output	"
255-253	⋮	⋮	⋮
252	SyncOut⟨5⟩	output	"
251	HelixTokenIn	input	to be connected to pad no. 187 HelixTokenOut of predecessing Helix128-2.2/2.3 if the chip is non-leading in a daisy chain (not to be connected for single chip operation and if the chip is the first in a daisy chain)
250	n. c.	n. c.	Reserved for future use
249	FailsafeReturn-TokenOut	output	To be connected to FailsafeReturn-TokenIn of the 2^{nd} previous chip.
248	FailsafeHelix-TokenIn	input	To be connected to FailsafeHelix-TokenOut of the 2^{nd} previous chip.
247	FailsafeHelix-TokenOut	output	To be connected to FailsafeHelix-TokenIn of the 2^{nd} previous chip.
246	n. c.	n. c.	Reserved for future use
245-240a		n. c.	Removed

Table C.18: Pads on the top side of Helix128-3.x. The first pad in the table corresponds to the uppermost pad of the chip's top side (with the frontside left).

Ref. no.	Pin name	Type	Description
267	`SufixTokenOut`	output	initial token out of first chip in daisy chain; to be bonded to pad no. 268 `HelixTokenIn` for the first chip in a daisy chain and for single chip operation (otherwise not to be connected)
268	`HelixTokenIn`	input	internally connected to the adjacent pad no. 182; to be bonded to pad no. 267 `SufixTokenOut` for the first chip in a daisy chain and for single chip operation (otherwise not to be connected)
269	`TrigMon`	test outp.	test pad to probe the `TrigMon` signal (no connection needed for normal operation)
270	`WriteMon`	test outp.	`WriteMon` signal
271	`Trigger`	test outp.	`Trigger` signal
272	`notTrigger`	test outp.	`notTrigger` signal
273	`notReset`	test outp.	`notReset` signal
274	`notTReset`	test outp.	`notTReset` signal
275	`Voffset`	test outp.	buffer *Voffset* voltage
276	`Vdcl`	test outp.	pipeamp *Vdcl* voltage
277	`Vd`	test outp.	pipeamp *Vd* voltage
278	`VcompRef`	test outp.	comparator *VcompRef* voltage
279	`Vfs`	test outp.	shaper *Vfs* voltage
280	`Vfp`	test outp.	preamplifier *Vfp* voltage

Table C.19: Description of the Helix128-2.0 and Helix128-2.1 core pads. The first pad in the table corresponds to the lowest right hand side core pad (with the frontside left).

Ref. no.	Pin name	Type	Description
267	`SufixTokenOut`	output	initial token out of first chip in daisy chain; to be bonded to pad no. 268 `HelixTokenIn` for the first chip in a daisy chain and for single chip operation (otherwise not to be connected)
268	`HelixTokenIn`	input	internally connected to the adjacent pad no. 182; to be bonded to pad no. 267 `SufixTokenOut` for the first chip in a daisy chain and for single chip operation (otherwise not to be connected)
269	`TrigMon`	test outp.	test pad to probe the `TrigMon` signal (no connection needed for normal operation)
270	`WriteMon`	test outp.	`WriteMon` signal
271	`Trigger`	test outp.	`Trigger` signal
272	`notTrigger`	test outp.	`notTrigger` signal
273	`notReset`	test outp.	`notReset` signal
274	`notTReset`	test outp.	`notTReset` signal
275	`Voffset`	test outp.	buffer *Voffset* voltage
276	`Vdcl`	test outp.	pipeamp *Vdcl* voltage
277	`Vd`	test outp.	pipeamp *Vd* voltage
278	`VcompRef`	test outp.	comparator *VcompRef* voltage
279	`Vfs`	test outp.	shaper *Vfs* voltage
280	`Vfp`	test outp.	preamplifier *Vfp* voltage

Table C.20: Description of the Helix128-2.2/2.3/3.x core pads. The first pad in the table corresponds to the lowest right hand side core pad (with the frontside left).

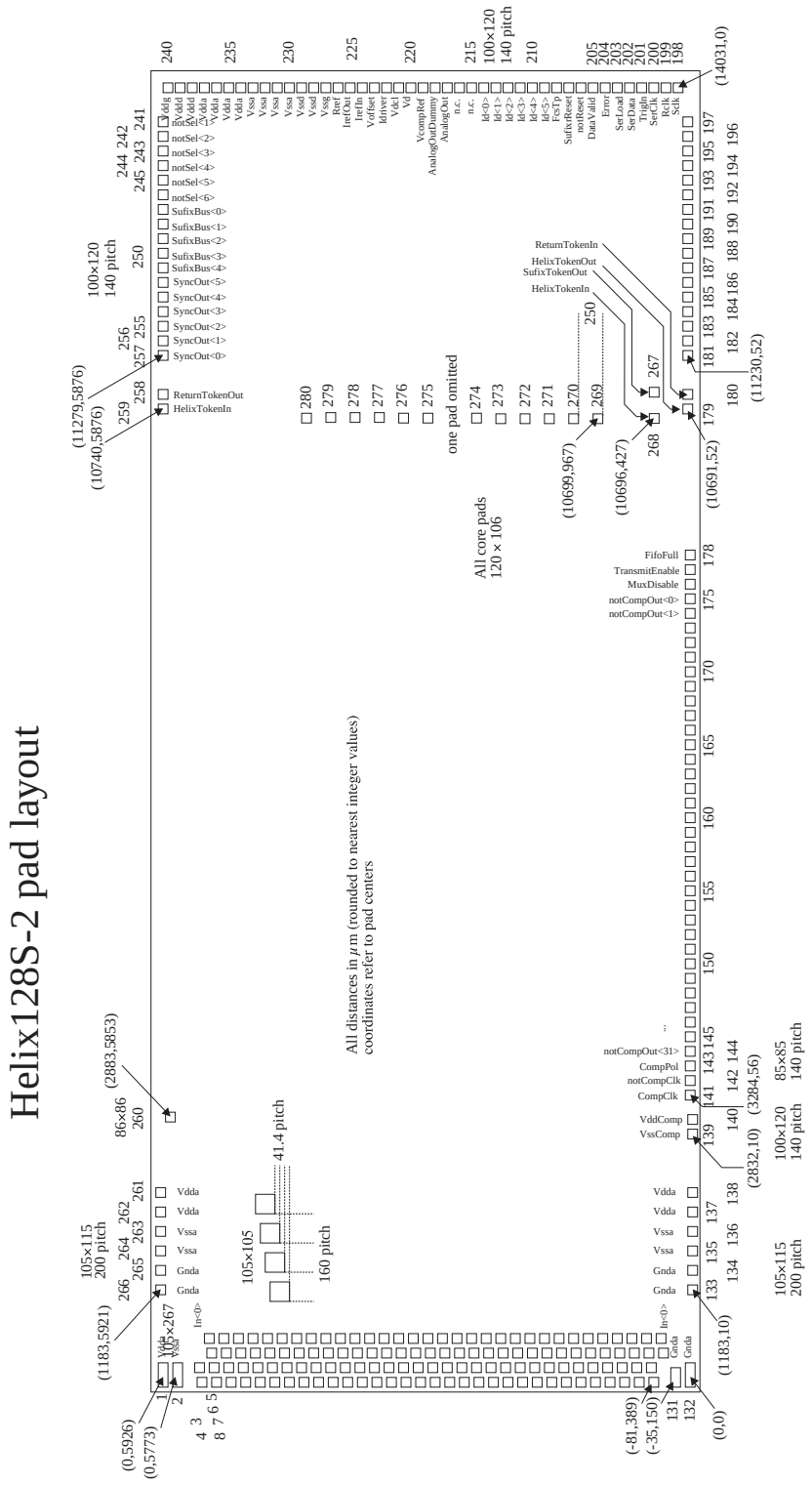

Figure C.18: Schematic drawing of the Helix128-2.0 pad locations. The overall chip dimension is 14,385µm x 6,146 µm; the frontside (facing the detector) is the bottom side in this view; in the descriptions we will refer to this side as the left side in regard of the "normal" signal flow from left to right

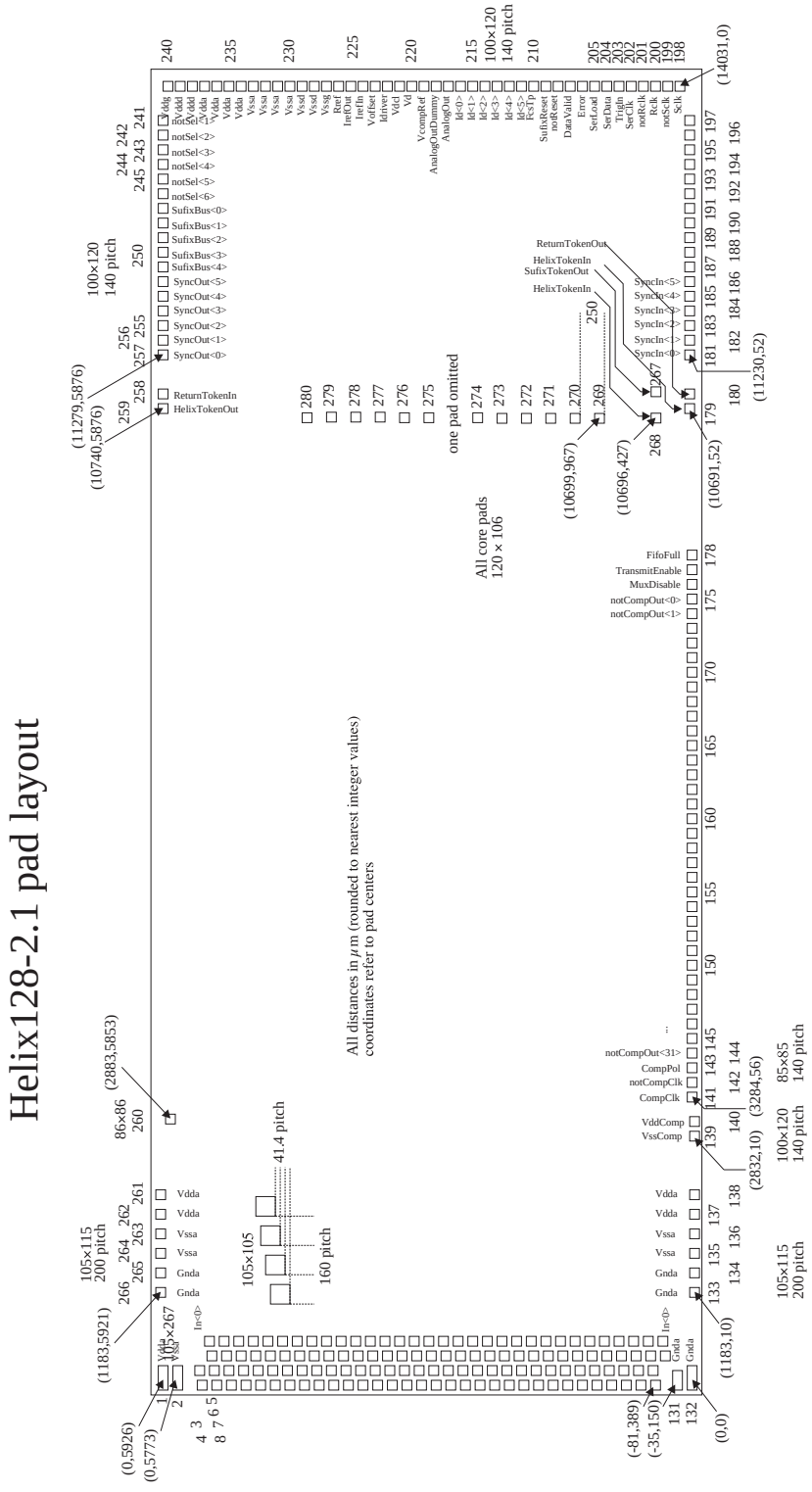

Figure C.19: Schematic drawing of the Helix128-2.1 pad locations. The `SClk` and `RClk` pads are now differential CMOS inputs.

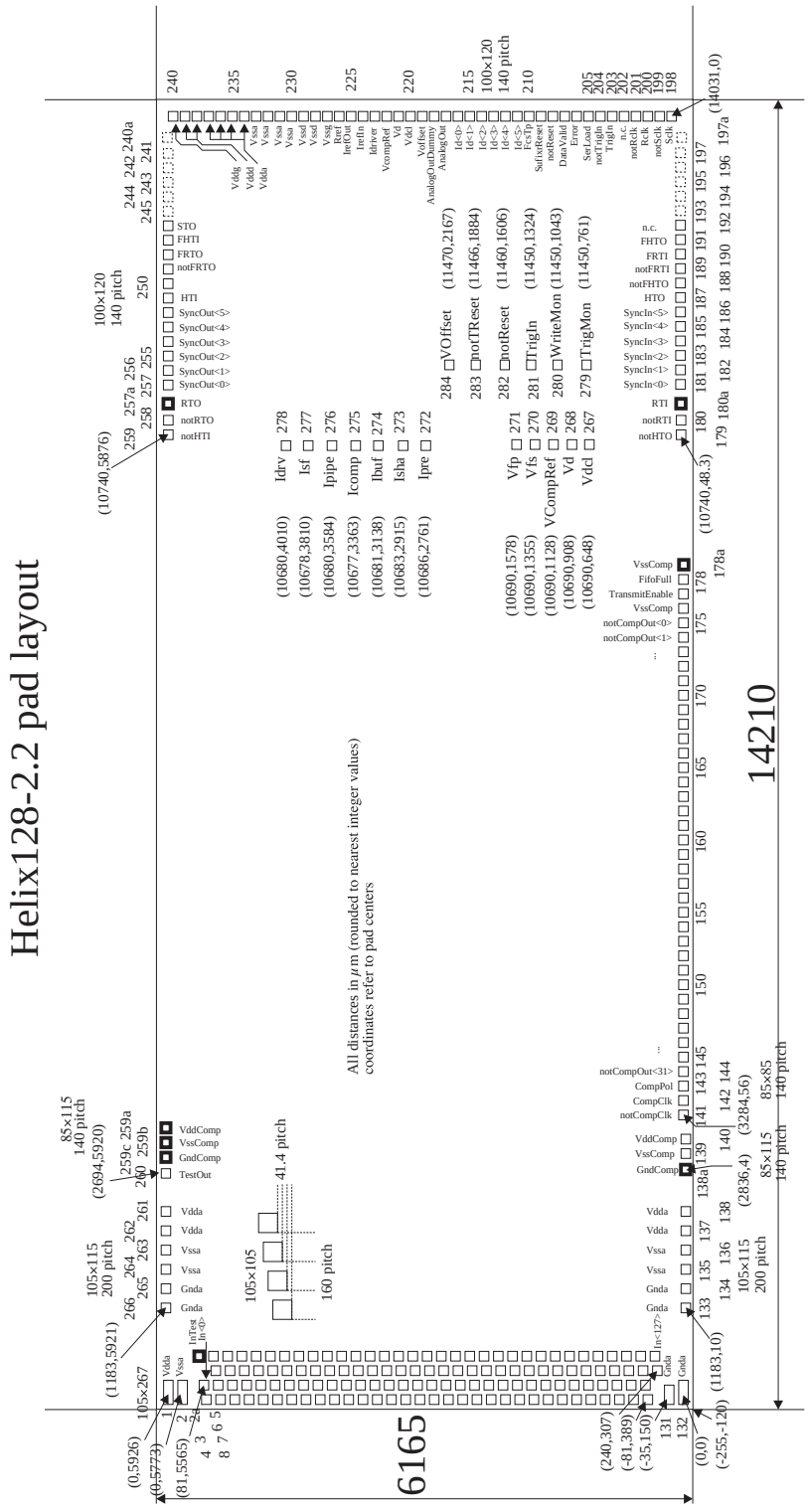

Figure C.20: Schematic drawing of the Helix128-2.2/2.3 pad locations. Token pads and power supply pads for the comparator outputs have been added.

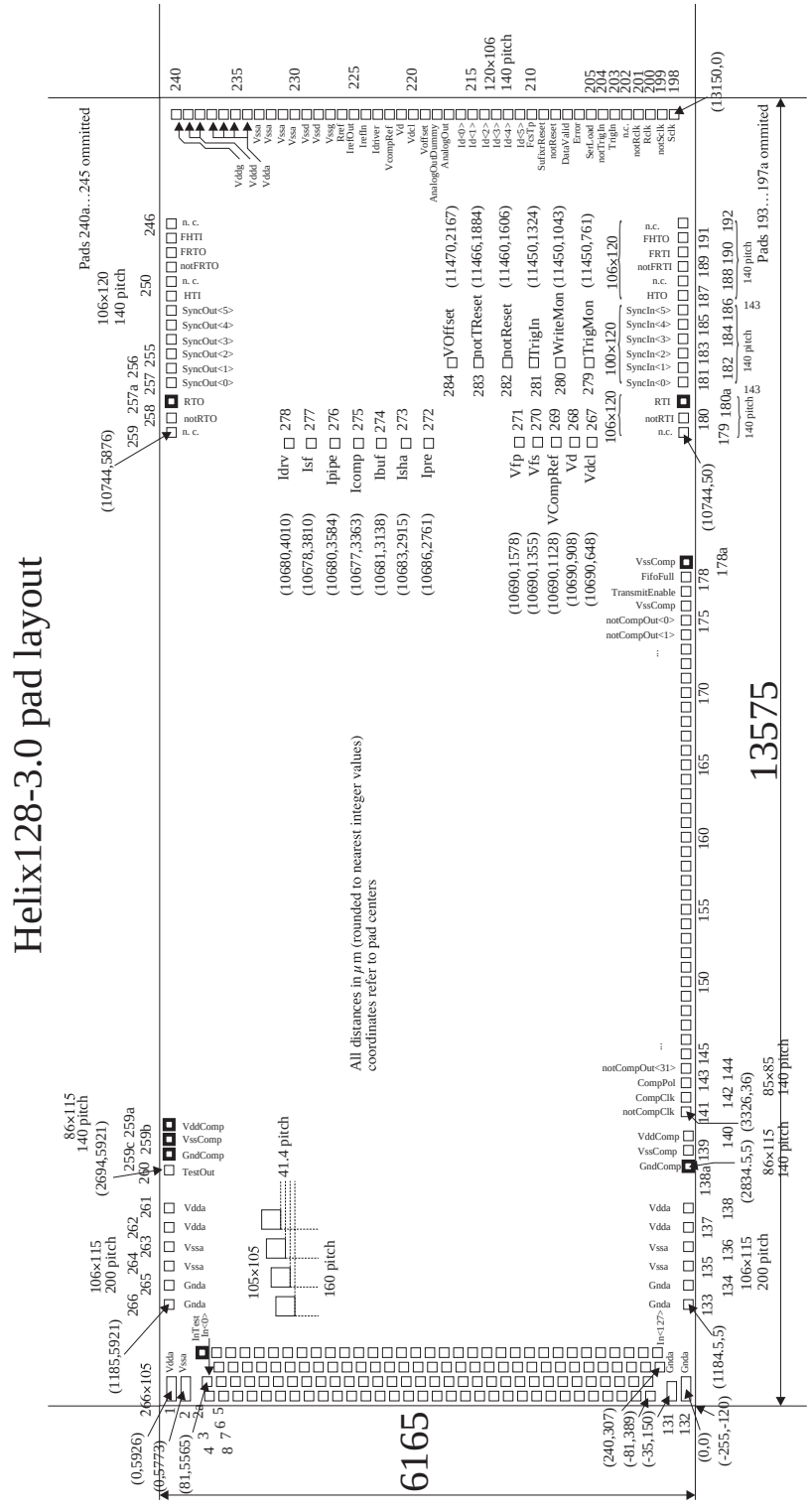

Figure C.21: Schematic drawing of the Helix128-3.0 and 3.1 pad locations.

C.6 Appendix: List of Known Problems

1. Multi-event buffer non functional (1);
   due to unfavorable routing of `SClk` the chip has to be reset after each trigger. The employment of Helix128-2.0 should be restricted to laboratory evaluation.

2. Multi-event buffer (2);
   at certain well defined conditions a trigger can halt the chip.

3. *VcompRef* adjustment;
   VcompRef is the dicriminator reference voltage of the comparators. It runs from -2V to +2V in 128 steps, giving a resolution of $\approx$ 31mV. Compared to the response to a signal of $1MIP_{\mathrm{Si}}$ (24.000 electrons) of $\approx$ 50mV, this is much to coarse.

4. `SClk` and `RClk`;
   `SClk` and `RClk` are unipolar (nondifferential) signals which may cause excess noise on the chip, especially at fast `RClk` timings.

5. `SeRClk` and `RClk`;
   `RClk` must run faster than `SeRClk` otherwise data might be lost.

6. `DataValid`, `AnalogOut` and `AnalogOutDummy`;
   `AnalogOut` and `AnalogOutDummy` jitter with respect to `DataValid`. The jitter can be up to 4 `RClk` cycles, but is the same for all chip that have their `notReset` released at the same time.

7. Offset of `AnalogOut` and `AnalogOutDummy`;
   due to unfavorable voltage level transitions in the pipeline readout amplifier, `AnalogOut` and `AnalogOutDummy` have a `SClk`-dependent offset, which limits the dynamic range.

8. Crosstalk of switching comparator to all channels;
   feedback via the open-collector discriminator outputs at the chip's bottom side to the amplifier inputs is suspected.

9. Pairwise crosstalk between channels (2n,2n+1) of approx. 8 %;
   even if the pattern follows an asymmetry in the pipeline, the origin is not yet clear.

10. Radiation softness of Pipeline amplifier; The functionality of the Pipeamp suffers from very low radiation doses. It is believed that this problem is related with problem 7.

11. Drift of the pipeline amplifier; The pipeline read out amplifier suffers from leakage currents. Charge up of the feedback capacitor due to them drives the amplifier into saturation when the chip is not read out. The reset period before each read out cycle is not long enough

to recover the amplifier from this state. This problem mainly occurs at low trigger rates (less than 100Hz). Higher trigger rates keep the amplifier operable. The effect can be increased by exposing the chip to light.

12. Startup of the internal bias current source; Some chips do not become operation because the internal current source does not start.

13. Oscillation of the internal current source; The internal current source shows oscillation, which increases common mode noise and limits the comparator threshold. The nearly sine-shaped oscillation of approx. 10MHz can be eliminated completely at most chips by blocking the reference current (i.e. the `IrefOut` pad).

14. Stall of operation; At maximum Latency, the chips internal operation can be stalled by a rare trigger sequence: Triggering the sample preceding 7 topologically consecutive triggered pipeline columns causes an underrun of a FIFO in the pipeline controll circuit.

15. Helix128-3.0 has reduced latency; The pipeline control circuit of Helix128-23.0 can only address $128+8=136$ pipeline columns. This reduces the usable latency to 123`SClk` cycles.

16. Helix128-3.0 has different readout timing; The time between the arrival of a trigger and the rising edge of `DataValid` is different from previous versions.

17. Helix128-3.1 has excess token; On power up every Helix128-3.1 has a readout token. It has to be removed by pulling low not reset during the chips' first readout in order to get a readout daisy chain working.

C.6.1 Solved Problems at Helix128-2.1

Problems 1, 3 have been solved, 4 has been improved.

C.6.2 Solved Problems at Helix128-2.2

Problems 6, 7, 10, 5, and 4 have been solved; problem 8 has been improved.

C.6.3 Solved Problems at Helix128-3.0

Problem 2, 8, 11 and 12 have been solved.

C.6.4 Solved Problems at Helix128-3.1

Problem 14and 15 have been solved. Problem 8 has been further improved, problem , 16 is currently under investigation.

C.6.5 Solved Problems at Helix128-3.1a

Problem 13 has been solved.

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Appendix D

Bias and Control Voltage Recommendations

To avoid a deterioration o the chip's performance by external crosstalk or feedthrough, a grounding schema as depicted in fig. D.1 is recommended. While it is not necessary to use different power supplies for the analogue and digital parts of the chip, their supply lines should be split and blocked independently. If possible, the front end's power supply pads should be contacted by more than one bond wire and if possible all available pads should be used. Blocking capacitors should be as large as possible (i.e. much bigger than calculated) and mounted as close as possible to the power supply pads.

Important

The `Gnd` power supply of the front end **has to connect** to the attached detector's signal ground return and **must not connect** to anything else. In particular stages subsequent to HELIX128 must not connect to it and power supplies other than those of the HELIX128 chip or the detector must not use it as a reference. Otherwise a severe deterioration of the chip's performance by crosstalk and common mode has to be expected.

Baseline fluctuations strongly depend on the parallel capacitance C_p on the amplifer input, since C_p is a path of power supply feedthrough. To enable common mode suppression from the shaper only `notAnalogOut` channel or a software baseline subtraction algorithm, all channels' C_p have to be identical.

For signal distribution and blocking the rear stages of HELIX128 the schema of fig. 5.4, i.e. distribution of common signals by lines in parallel to the chip's rear end and individual signals and blocking on the other side of this "street", have proven to be the optimal solution. A conductive shielding on top of the chips is strongly advised. It can be combined with the detector housing like e.g. the Roman Pots in the HERA-*B* VDS.

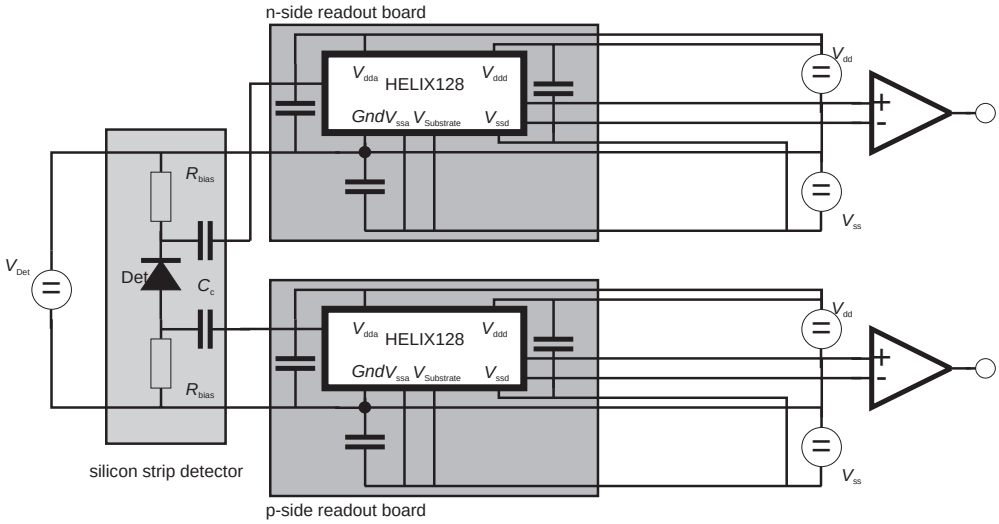

Figure D.1: Recommended grounding schema for HELIX128.

D.1 Preamplifier Bias Current I_{pre}

An undershoot-free pulse can be obtained by matching I_{pre} to the parallel capacitance at the preamplifier input. From the pulse shapes shown in figs. A.1...A.5 it was concluded, that to achieve this

$$I_{\mathrm{pre}} \approx \sqrt{C_p + 0.75\mathrm{pF}} \cdot 65.24 \frac{\mu\mathrm{A}}{\sqrt{\mathrm{pF}}} \tag{D.1}$$

is required. This is shown in fig. D.2.

Since the pulse shapes for $I_{\mathrm{pre}} \gtrsim 200\mu\mathrm{A}$ and $C_{\mathrm{p}} \lesssim 30\mathrm{pF}$ do not change with irradiation (cf. figs. 5.10 and A.15...A.24), there is no reason to change them, especially in a high-rate environment. In noise-critical low-occupancy environments however, a linear increase of I_{pre} with the accumulated dose can be advisable.

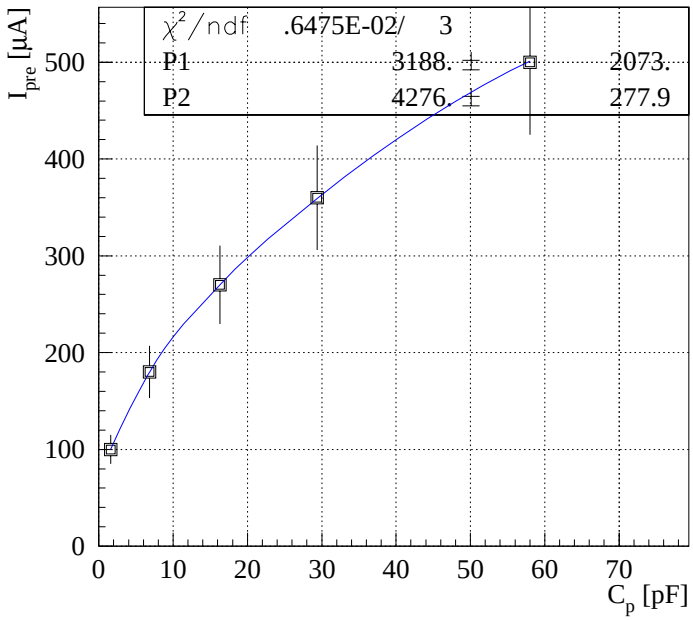

Figure D.2: I_{pre} values for zero undershoot of the pulse as a function of the parallel capacitance C_{p}.

D.2 Preamplifier Feedback Control Voltage V_{fp}

As shown in fig. D.3 the measured values for the cut-off value of V_{fp} nicely run in parallel. Therefore the recommended value can be easily extracted by shifting one of the curves up or down to the (measured) cut-off value of $\mathrm{V_{fp}}$ for the unirradiated chip. However, for doses exceeding approx. 3kGy

this method does no longer work, since parasitic currents in the feedback transistor gain an important role. For these doses the cut-off value can only be determined by sweeping V_{fp}. It should be denoted, that $V_{\mathrm{fp}} = -2\mathrm{V}$ means that the preamplifier can no longer be cut off and that the resulting low parallel resistance R_{p} will contribute some excess noise.

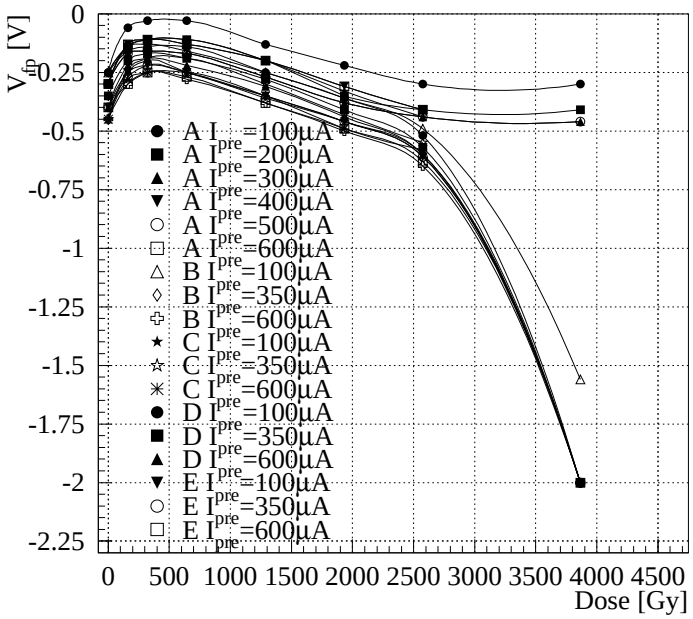

Figure D.3: $\mathrm{V_{fp}}$ values for all irradiated chips and $\mathrm{I_{pre}}$ settings. The -2V measured at 3.9kGy are due to parasitic currents in the feedback transistor (cf. section 4.3.1).

D.3 Shaper Bias Current I_{sha}

For parallel capacitances $C_{\mathrm{p}} > 0$ the effect of $I_{\mathrm{sha}} > 100\mu\mathrm{A}$ on the pulse shape is neglectable. Therefore I_{sha} should be kept constant under irradiation.

D.4 Shaper Feedback Control Voltage V_{fs}

For a certain pulse shape, V_{fs} can be calculated from one of the equations 5.4 to 5.6 or taken from figs. A.1 to A.8. For $I_{\mathrm{pre}} \geq 200\mu\mathrm{A}$ and $C_{\mathrm{p}} \lesssim 30\mathrm{pF}$ pulse shapes do not change under irradiation and thus V_{fs} should not be changed.

D.5 Buffer Bias Current I_{buf}

I_{buf} should be kept constant under irradiation. The decrease of the gain with irradiation is dependent on the pulse height and most noticeable for pulses with slow rise time. Thus a degradation of the buffer's g_{m} can not account for it.

D.6 Pipeamp Bias Current I_{pipe}

The pipeamp bias I_{pipe} was kept constant (at 40µA) during irradiations. On HELIX128-2.1 it was neccesary to lower I_{pipe} in order to move the required V_{dcl} below the V_{dd} power supply voltage of +2V.

D.7 *Pipeamp* Reset Voltage V_{d}

As already pointed out in sect. 3.6, V_{d} should match the frontend's offset voltage. This voltage is available at the `TestOut` pad or can be taken from fig. 5.14.

D.8 *Pipeamp* Drain Voltage V_{dcl}

V_{dcl} was adjusted as proposed in the manual (appendix C), i.e. such that the baseline of the analogue readout was exactly in the center of the "high" and "low" levels of the pipeline address encoded in the readout. The increase found on daughter cards '*A*' and '*D*' at 3.9kG is supposed to be dose rate dependent and should vanish at lower dose rates, as the curve for '*D*' shows. The slope of this curve is about 6mV/kGy.

D.9 Multiplexer Bias Current I_{sf}

$I_{\mathrm{sf}} = 100\mu\mathrm{A}$ was kept constant during irradiation, since no degradation of the MUX's speed was observed.

D.10 Current Buffer Bias Current I_{driver}

$I_{\mathrm{driver}} = 90\mu\mathrm{A}$ was kept constant during irradiation for the same reasons as I_{sf}.

D.11 Current Buffer Offset Voltage V_{offset}

To exploit the dynamic range of HELIX128 V_{offset} has to be adjusted such, that the offset output current (during readout) has to be about 3.3mA. Using the receiver circuit depicted in fig. 5.6, this corresponds to $\approx$ 1V

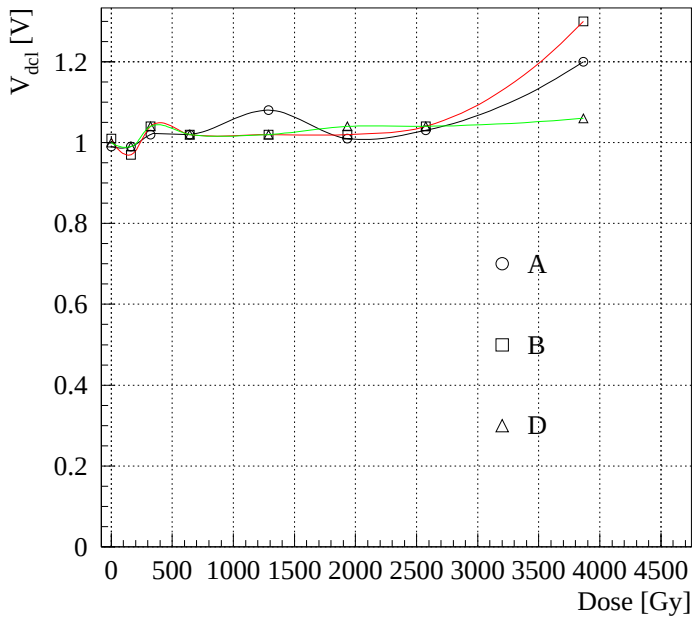

Figure D.4: Change of V_{dcl} with irradiation.

on the output of the transimpedance amplifiers. The values shown in fig. D.5 were measured by disconnecting `AnalogOutDummy` and measuring the voltage on the output of the circuit. Thus the results might be spoiled by the (e.g. temperature dependent) offset voltage of the unconnected transimpedance amplifier.

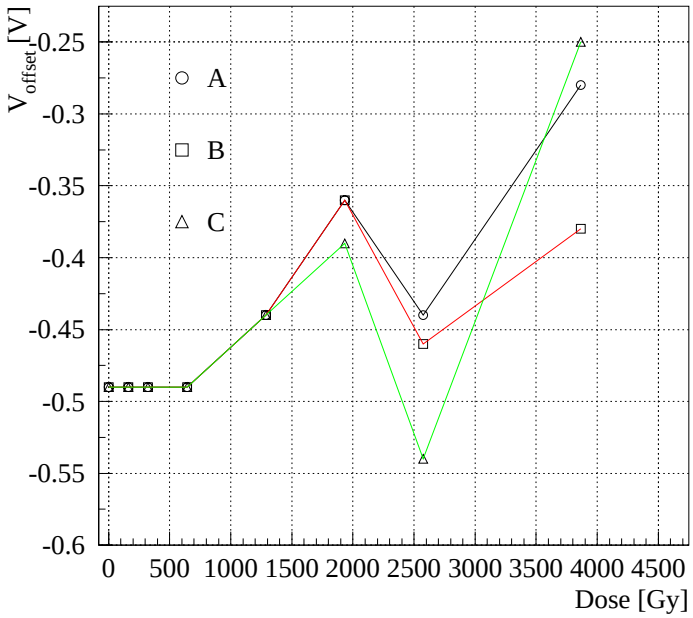

Figure D.5: Change of V_{offset} with irradiation.

Appendix E

HELIX128-2 known Bugs and Limitations

This section provides some in-depth explanation for the known bugs and limitations of HELIX128 listed in appendix C. The items in the following list are categorized by their severity:
Bugs (indicated by BUG) are severe errors that are supposed to be fixed in a later version. Limitations (LIM) put up minor restrictions for chip operation or performance. They will be only fixed in case of a known origin of the problem. Specification updates (SPU) are minor discrepancies between the expected and real behaviour of the chip and will not be fixed. The affected HELIX128 versions are also indicated.

BUG	2.0	*Multi-Event Buffer non functional* Unfavorable routing of `SClk` caused this failure. The *inhWrite* flag is not cleared and the readout pointer is not incremented (cf. fig. 3.37). Thus the data of the first triggered event is read out over and over without further triggers and the chip has to be reset after the first readout.
BUG	2.0 2.1 2.2	*Stall of operation* (1) A certain trigger sequence can stall the chip's operation. Discarding an entry in the Multi-Event Buffer coincident with a trigger causes a lockup condition in the readout controller.
BUG	2.0	*VcompRef adjustment* Adjustment of *VcompRef* in $\approx$ 31mV steps corresponds to $\gtrsim 1/3MIP$. This is much too coarse for a sensitive adjustment. Reason is the missing 1 : 10 voltage divider.

BUG	2.0	*Crosstalk from* `SClk` *and* `Rclk`
	2.1	`SClk` and `Rclk` are unipolar signals with CMOS levels (i.e. ±2V swing). These signals can cause excess noise on the chip, especially at high `Rclk` frequencies.
SPU	2.0	*Timing of* `SerClk` *and* `RClk`
	2.1	The interface converts data from serial to parallel with `SerClk`, while the actual programming of the registers is done synchronous with `RClk`. Since there is no handshake in between them, data might be lost if `RClk` is slower than `SerClk`.
LIM	2.0	*Jitter of* `DataValid` *wrt. the analog readout*
	2.1	`AnalogOut` and `AnalogOutDummy` jitter with respect to `DataValid`. The jitter can be up to n `Rclk` cycles, (where n is the ratio of `RClk` and `SClk`). The problem arises from not synchronising the multiplexer (using `RClk`) with `SClk`, which is done for the `DataValid` signal.
BUG	2.0	*Offset of* `AnalogOut` *and* `AnalogOutDummy`
	2.1	Due to the missing level shifter in the pipeamp, the operating point of the pipeamp forced by its reset is not stable under open loop conditions. The caused transition when opening the pipeamps reset switch causes an `SClk`-dependent change of the analogue signals' offset, which limits the dynamic range, and causes common mode noise.
BUG	2.0	*Radiation softness of Pipeline readout amplifier*
	2.1	This issue is related to the preceeding one. Threshold voltage shifts and the missing voltage divider require $V_{\mathrm{dcl}} > +2\mathrm{V}$ for a stable operation of the Pipeamp. Due to the limitation of $V_{\mathrm{dcl}} \leq +2\mathrm{V}$ by the chips power supply, the transition's amplitude increases. Decreasing I_{pipe} moves V_{dcl} back into the dynamic range of the DACs, but requires `SClk` frequencies $< 10\mathrm{MHz}$.
BUG	2.0	*Crosstalk of a switching comparator to all channels*
	2.1	Feedthrough of the comparator's switching from the
	(2.2)	open-collector discriminator outputs at the chip's bottom side via scribeline, guardrings and substrate to the amplifier power supply or inputs was found.
LIM	all	Pairwise crosstalk between channels $(2n, 2n+1)$ Crosstalk between channels $(2n, 2n+1)$ of $\approx 8\%$ has been observed. The pattern follows an asymmetry in the pipeline layout, the origin is not yet clear.

BUG 2.0 *Drift of the pipeline amplfier*
2.1 The pipeamp's reset is not closed when the stage
2.2 is idle. Thus leakage and photocurrents (e.g. in at the diffusion areas of the feedback transistor) cause a charge up of the feedback capacitor, altering the amplifiers operating point. This can drive the amplifier into saturation, from which it can not recover within one reset cycle. As a result, the dynamic range is limited. The phenomenon only occours at low trigger rates (less than 100Hz). Higher trigger rates keep the amplifier operable. Solved by different sequencer pattern. Reset switch is now closed all the time the Pipeamp is idle.

BUG 2.1 *Startup of the internal bias current source*
2.2 The current source relies on a certain leakage current to '*bootstrap*' its error amplifier bias. Improvements in the process' technology reduced these leakage currents, causing some current sources not start operation when powered. The necessary currents can be enforced by shining light on the circuit. Sloved by a small diode connected transistor providing the necessary current.

BUG 2.1 *Oscillation of the internal current source*
2.2 The internal current source shows oscillation, which
3.0 increases common mode noise and limits the com-
3.1 parator threshold. Reason for this bug is an increase of the transistors' f_T, rendering the error amplifier instable at unity gain. To reproduce the behaviour in a parasitc simulation, a large (few pF) capacitor had to be connected between the error amplifiers' inputs. The effect of the nearly sine-shaped oscillation of approx. 10MHz can be eliminated completely at by blocking the reference current (i.e. the `IrefOut` pad).

BUG 2.0 *Stall of operation*
2.1 At maximum Latency, the chips internal operation
2.2 can be stalled by a rare trigger sequence: Trigger-
3.0 ing the sample preceding 7 topologically consecutive triggered pipeline columns causes an underrun of a FIFO in the pipeline controll circuit. The problem is addressed in sect. 3.9.1 and visualized in fig. 3.36.2. It can be cirumvented by reducing the latency to 127 (3.0: 122) clock cycles.

BUG 3.0 *Reduced Latency*
The pipeline control circuit of HELIX128-3.0 can only address $128+8 = 136$ pipeline columns. This reduces the usable latency to 123`SClk` cycles. Reason is a bug introduced by porting the design to a new release of the *Cadence* '*Synergy*' tool used for ciruit synthesis.

BUG 3.0 *Different readout timing*
The readout sequencer of HELIX128-3.0 uses an inverted RClk signal. Furthermore the readout sequencer lacks the 200ns of the pipeamp's reset phase (cf. fig. 3.23). Thus the time between `trigIn` and the begin of the rising edge of `DataValid` is different.

BUG 2.0 *HELIX128 can loose Latency*
2.1 The FifoFull signal of these chips is defined as a logic
2.2 AND of all *inhTrig* bits in the Derandomiser Buffer.
2.3 Its entries may be discarded in a different order than they were written to it. Thus the trigger pointer might point to a slot still occupied while Fifo Full is no longer active. In case of a trigger, the entry in this slot is overwritten. While the write incrementer usually has skiped the old entry, the trigger incrementer might not (since it is no longer in the derandomiser buffer). This causes the chip to loose its latency. On HELIX128-31 it was fixed by defining `FifoFull` as the *inhTrig* bit referenced by the trigger pointer.

LIM 3.1 *Excess Token*
3.1a On power up each HELIX128-3.1 has a readout token, which is not removed by pulling `low notReset`. This is due to the missing reset of the corresponding "gotToken" latch. Thus all chips in a readout daisychain will start sending data in parallel, regardless of their programming. These excess tokens can be removed by pulling low `notReset` **during** this first readout, since the reset inside the multiplexer itself works.

Appendix F

Verilog Source of HELIX128-2's Interface and Control Circuit

The *Verilog* code describing the "SUFIX" control circuits was broken down in rather small modules to

- obtain human readable schematics and
- enforce the synthesis of certain schematic structures.

"**sufixDigitalModule.v**" is the functional description of the complete circuit.

```
// "SUFIX"-the control circuit of the HELIX chip - top module
// "SUFIX"-the control circuit of the HELIX chip
// Written by Ulrich Trunk (c) 1996
// Changed 06.10.97 by U.T.: Decoder now clocked with SerClk i.e. loading of
//                           regs now only needs SerClk
//                           FailSafe Token schema
// Changed 10.10.97 by U.T.: removed firstToken, added comments
`include "sufixIF.v"
`include "sufixDEC.v"
`include "latchEight.v"
`include "starter.v"
`include "sufixTPG.v"
`include "syncMon.v"
`include "sufixSCLK.v"
`include "sufixTRG.v"
`include "sufixToken.v"

module sufixDigitalModule_FST (sdata,clock,load,trigIn,rclk,sclkIn,sclk,
                           sufixReset,ID,notResetIn,syncIn,write0,trig0,
                           dataValid,fcsTP,notReset, notTReset,trigOut,TP,err,
                           syncOut,data,notSEL,HTI,HTO_last,FHTI,RTI,FRTI,RTO,
                           disable_HTO,HelixToken);

input         sdata,     //serial mode data input line
              clock,     //serial mode data clock line
              load,      //serial mode data enable line
```

```
              trigIn,    //L1 trigger input line
              rclk,      //readout clock
              sclkIn,    //additional input for ext. SCLK
              sufixReset,//Sufix internal reset (not used)
              HTI,HTO_last,RTI,FRTI,FHTI; //(Fail safe and return)Token inputs

input [5:0]   ID;        //adress of sufix instance
input         notResetIn;//Helix notReset
input [5:0]   syncIn;    //Sync monitor daisychain input
input         write0,    //Helix writeMon signal input
              trig0,     //Helix trigMon signal input
              dataValid, //Helix dataValid signal input
              fcsTP;     //TP signal from FCS
output        notReset,  //Helix write pointer notReset
              notTReset, //Helix trigger pointer notReset
              sclk,      //Helix sampling clock
              trigOut,   //L1 trigger output line
              TP,        //Testpulse output
              err,       //error output line
              RTO,       //output of the HELIX's mux token
              disable_HTO,HelixToken; //tokens

output [5:0]  syncOut;   //Sync monitor daisychain output
output [7:0]  data;      //Interface data output
output [16:0] notSEL;    //notSelect decoder outputs

wire          sdata,
              clock,
              load,
              trigIn,
              rclk,
              sclk,
              sufixReset,
              RTO,disable_HTO,HelixToken;
wire [5:0]    ID;
wire          notReset;
wire [5:0]    syncIn;
wire          write0,
              trig0,
              dataValid;
wire          notTReset,
              trigOut,
              TP,
              err;
wire [5:0]    syncOut;
wire [7:0]    data,div_clk_reg;
wire [16:0]   notSEL;

// Internal connections:
wire          TPGtrig,
              notLE;
wire [7:0]    SLatency,clk_div_reg,
              TLatency,
              TBX;
wire [11:0]   adr;

SufixIf IF(sdata,clock,load,adr,data,notLE,sufixReset);
```

```
SufixDEC DEC(adr,ID,notLE,rclk,notSEL,sufixReset);
latchEight StarterTrigL(data,notSEL[13],SLatency);
starter LetsGo(sclk,notResetIn,notReset,notTReset,SLatency);
SufixTPG Pulser(fcsTP,TP,sufixReset,rclk);
SyncMon Syncro(syncIn,dataValid,write0,trig0,sclk,rclk,data,notSEL[14],syncOut,
              err);
SufixSCLK SCLK_FST(rclk,data,sclk,notResetIn,notSEL[15],sclkIn,clk_div_reg);
sufixTRG trigger(trigIn,sclk,trigOut);
sufixToken sufixToken_FST(RTI, FRTI, HTI, FHTI, HTO_last, RTO, HelixToken,
                          disable_HTO, div_clk_reg[7:4], rclk, data, notSEL[16],
                          notReset, notTReset);
endmodule
```

"**sufixIF.v**" contains the serial to parallel conversion part of the programming interface.

```
// Interface
// "SUFIX"-the control circuit of the HELIX chip
// Written by Ulrich Trunk (c) 1996

module SufixIf (
        data,     //serial IF data input
        clk,      //serial IF data clock
        load,     //serial IF serial to paralell enable
        adr,      //adress output (to decoder)
        val,      //data output
        EN,       //LatchEnable for Sufix' adr. decoder
        reset);   //SUFIX internal reset

input   data,
        clk,
        load,
        reset;
output  EN;

output [11:0] adr;
output [7:0]  val;

reg [11:0] adr;
reg [7:0]  val;
reg [19:0] sr;

reg [1:0]IEN;

wire load,
     data,
     clk,
     EN;

// Just a simple shift register

assign EN = (reset == 1) ? 1:IEN[1];

               always @(posedge clk)
          begin
              IEN[1:0] = {IEN[0],load};   //delay EN by 1 RCLK respective to
                                          //load
```

```
            if (load == 1)
              begin
                {adr,val} = sr;           //convert ser to par
              end
            else
              if (reset == 0)             //if there is no SUFIX reset condition
                begin
                 sr = {sr[18:0],data};    //clock in data
                end
              else
                begin                     //otherwise reset everything to 0
                  sr = 0;
                  {adr,val} = 0;
                end
          end
endmodule
```

"**sufixDEC.v**" is the address decoding and register programming part.

```
//Address decoder
// "SUFIX"-the control circuit of the HELIX chip
// Written by Ulrich Trunk (c) 1996

module SufixDEC (
        adr,      //adress from shift reg
        ID,       //chip adress input pin (hw adr)
        EN,       //field bus serial to paralell enable
        clock,    //clock
        notSEL,   //module (register) select output (active low)
        reset);

input [11:0] adr;
input [5:0]   ID;
input      EN,
           clock,
           reset;

output [16:0] notSEL;

reg [33:0] dec;
reg [1:0] iEN;
wire [16:0] inotSEL;

//only if chip address matches ID or in broadcast mode apply decoded signal
//to the module select bus.
      assign inotSEL = ((adr[11] ==1) | (adr [10:5] == ID)) ?
                       ~dec[33:17]:17'b11111111111111111;
//if the SUFIX is reseted, pull all lines to reset the regs....
      assign notSEL = (reset == 1) ? 17'h00:inotSEL;

        always @(posedge clock)
//delay decoder outputs 3/2 RCLK respective to the IF's EN signal
//(i.e. asserted @negedge RCLK), since the Data is assertyed @posedge
//this one gives 1/2 RCLK of delay
         if (EN == 1)
           iEN = 1;
         else
           if (iEN > 0)
```

```
            iEN = iEN -1;

        always @(negedge clock)
//THE DECODER
          if (iEN >0)
            begin
              if (adr[4:0] == 5'h01)         // Ipre
                dec[16:0] = 17'b00000000000000001;
              else if (adr[4:0] == 5'h02)    // Isha
                dec[16:0] = 17'b00000000000000010;
              else if (adr[4:0] == 5'h03)    // Ibuf
                dec[16:0] = 17'b00000000000000100;
              else if (adr[4:0] == 5'h04)    // Icomp
                dec[16:0] = 17'b00000000000001000;
              else if (adr[4:0] == 5'h05)    // IpipeL
                dec[16:0] = 17'b00000000000010000;
              else if (adr[4:0] == 5'h06)    // Isf
                dec[16:0] = 17'b00000000000100000;
              else if (adr[4:0] == 5'h07)    // Idriver
                dec[16:0] = 17'b00000000001000000;
              else if (adr[4:0] == 5'h08)    // Vfp
                dec[16:0] = 17'b00000000010000000;
              else if (adr[4:0] == 5'h09)    // Vfs
                dec[16:0] = 17'b00000000100000000;
              else if (adr[4:0] == 5'h0A)    // VcompRef
                dec[16:0] = 17'b0000001000000000;
              else if (adr[4:0] == 5'h0B)    // Vd
                dec[16:0] = 17'b00000010000000000;
              else if (adr[4:0] == 5'h0C)    // Vdcl
                dec[16:0] = 17'b00000100000000000;
              else if (adr[4:0] == 5'h0D)    // Voffset
                dec[16:0] = 17'b00001000000000000;
              else if (adr[4:0] == 5'h11)    // starter L1 latency
                dec[16:0] = 17'b00010000000000000;
              else if (adr[4:0] == 5'h12)    // SyncMonCtrl
                dec[16:0] = 17'b00100000000000000;
              else if (adr[4:0] == 5'h13)    // RCLK divider
                dec[16:0] = 17'b01000000000000000;
              else if (adr[4:0] == 5'h14)    // token delay
                dec[16:0] = 17'b10000000000000000;
              else
                dec[16:0] = 0;
            end
             else
//and this one another RCLK cycle of delay
              dec = {dec[16:0],17'b00000000000000000};



endmodule
```

"**latchEight.v**" is a simple 8bit latch with the same behaviour as those included in the DACs.

```
// Simple 8-bit latch
// "SUFIX"-the control circuit of the HELIX chip
// Written by Ulrich Trunk (c) 1996
```

```
module latchEight (in,notEN,out);

input [7:0] in;
input notEN;
output [7:0] out;
reg [7:0] out;
// like AMS's latches it's triggered on the neg edge
always @(negedge notEN)
   out = in;
endmodule
```

"**starter.v**" is the functional for the chip's latency adjustment, i.e. a simple counter.

```
// Latency initializer
// "SUFIX"-the control circuit of the HELIX chip
// Written by Ulrich Trunk (c) 1996

module starter (fBX,notResetIn,notReset,notTReset,latency);

input fBX,
      notResetIn;
input [7:0]latency;

output notReset,
       notTReset;

reg [7:0] counter;
reg       notReset;
wire      notTReset;

// Simple counter to adjust the distance between the write- and trigger
// pointer, circulating through the pipeline...

     assign notTReset = (counter == 0) ? 1:0;

        always @(posedge fBX)
         begin
          notReset = notResetIn;
          if (notReset == 0)
             counter = latency+1;
          else
            if (counter != 0)
              counter = counter-1;
            else
              counter = 0;
         end


endmodule
```

"**sufixTPG.v**" is the digital part of the test pulse circuit.

```
// Test-pulse circuit
// "SUFIX"-the control circuit of the HELIX chip
// Written by Ulrich Trunk (c) 1996
//        16-9-98 RK;Reset becomes notreset, reset now comes from NotResetIn which
//                is easier with testing. fcsTP starts now in defined position
//                --
```

```
module SufixTPG (
        fcsTP ,   //test oulse signal from FCS
        TPout,    //Test pulse ouTPoutut
        reset,    // this will hopefully never be used
        clock);

input   fcsTP,
        reset,
        clock;
output  TPout;

reg     TPout;
wire    itp,
        notreset;

assign notreset = !reset;
assign itp = (reset == 1) ? clock:fcsTP;
          always @(posedge itp)
            if (reset == 1)
              TPout = 0;
            else
              TPout = TPout +1;
endmodule
```

"**syncMon.v**" is the synchronicity monitoring circuit.

```
// Synchronicity monitor
// "SUFIX"-the control circuit of the HELIX chip
// Written by Ulrich Trunk (c) 1996
`include "syncDET.v"
`include "dreiOr.v"

module SyncMon (in, dv, wm, tm, sclk, rclk, data, notEN, out, err);
    output err;
    output [5:0] out;
    input sclk,
          rclk,
          notEN;
    input [5:0] in;
    input [7:0] data;
    input dv;
    input wm;
    input tm;
    wire [3:0] ierr;
    wire [5:0] iout;
    reg [7:0] creg;
    wire [2:0] mon;
    reg  latchErr;
    wire err;

// The syncOut[2i:2i+1] signals are choosen in a way that they behave like
// differential signals during synchronous operation, to minimize their effect
// on analogue signals

// syncOut[0] is something like !(trigMon||!syncIn[0], i.e. an active low wired
// or of the preceeding chips' trigmon
// syncOut[1] is trigMon&syncIn[1], i.e. a wired-and of all preceeding chips'
// trigMon signals
```

```
// monitoring=syncOut signals can toggle err

    assign mon[2] = (creg[1] == 1) ? in[5]:dv;  //disable dataValid monitoring
    assign out[5:4] = (creg[1] == 1) ? in[5:4]:iout[5:4];
    assign mon[1] = (creg[2] == 1) ? in[3]:wm;  //disable writeMon monitoring
    assign out[3:2] = (creg[2] == 1) ? in[3:2]:iout[3:2];
    assign mon[0] = (creg[3] == 1) ? in[1]:tm;  //disable trigMon monitoring
    assign out[1:0] = (creg[3] == 1) ? in[1:0]:iout[1:0];
    assign err = (creg[7] == 1) ? ierr[3]:latchErr;

// error evaluation=signal (dataValid, writeMon, trigMon) contributes to
// syncOut's

    syncDET sync1(in[5],in[4],dv,rclk,iout[5],iout[4],ierr[2]);
    syncDET sync2(in[3],in[2],wm,sclk,iout[3],iout[2],ierr[1]);
    syncDET sync3(in[1],in[0],tm,sclk,iout[1],iout[0],ierr[0]);
    dreiOr  sum((ierr[0] && (!creg[6])),        //disable trigMon evaluation
                (ierr[1] && (!creg[5])),        //disable writeMon evaluation
                (ierr[2] && (!creg[4])),        //disable dataValid evaluation
                ierr[3]);

    always @ (negedge notEN or posedge ierr[3])
      begin
        if (notEN == 0)
          begin
            creg = data;
            latchErr  = data[0];
          end
        else
          latchErr = 1;
      end

endmodule
```

"**syncDET.v**" synchronicity detection module used by "syncMon.v".

```
// Synchronicity detector (static)
// "SUFIX"-the control circuit of the HELIX chip
// Written by Ulrich Trunk (c) 1996

module syncDET(
       and_in,
       or_in,
       sig_in,
       clk,
       and_out,
       or_out,
       err);

input and_in,
      or_in,
      clk,
      sig_in;
output and_out,
       or_out,
       err;
reg    err;
```

```
// and_out=and_in&sig_in (wired-and)
// or_out=!(!or_in||sig_in) (active-low wired-or)
assign and_out = (sig_in ==1) ? and_in:0;
assign  or_out = (sig_in ==0) ? or_in:0;

always @(posedge clk)
   if (or_out == and_out)
     err = 1;
   else
     err = 0;

endmodule
```

"**dreiOr.v**" is a simple OR with three inputs. It is used by "syncMon.v".

```
// OR with 3 inputs
// "SUFIX"-the control circuit of the HELIX chip
// Written by Ulrich Trunk (c) 1996

module dreiOr (in1,in2,in3,out);

input  in1,
       in2,
       in3;
output out;

assign out = ((in1 == 1) || (in2 == 1)) ? 1:in3;

endmodule
```

"**sufixSCLK.v**" circuit generates *SClk* from `RClk`.

```
//SCLK divider
// "SUFIX"-the control circuit of the HELIX chip
// Written by Ulrich Trunk (c) 1996
// Changed 10.10.97 by U.T.: loading of clk_div_reg asynchronous from rclk

module SufixSCLK_FST(
         RCLK,     //RCLK input
         clk_div,  //clock divider register (only the lower 4 bits are used)
         SCLK,     //SCLK output
         notReset, //notReset from FCS
         notEN,    //not ENable of clk_div latch
         SCLKin,   //additional SCLK input
         clk_div_reg); // output for FST programming 18-2-98 RK^

input [7:0] clk_div;
input RCLK,
      notReset,
      notEN,
      SCLKin;

output SCLK;
output [7:0] clk_div_reg;

wire RCLK2,
     RCLK,
     SCLK2,
```

```
     SCLK,
     SCLKin,
     notReset,
     notEN;
wire [7:0] clk_div;

reg  CLK1,
     CLK2;
reg [7:0] clk_div_reg;
reg [3:0] counter1,
          counter2;
reg [3:0] start_counter;
reg [2:0] sync;

// How it works:
// divide clock and delayed clock (for even dividers) or delayed !clock (odd
// deviders) by 2*clock_div_reg and XOR these signals
// _   _   _   _   _   _   _   _   _   _
//  |_| |_| |_| |_| |_| |_| |_| |_| |_|       clock
// _             -----------
//  |___________|           |___________      clock/6
//         -----------             -----
// _______|           |___________|           t+!clock/6
// _       -----       -----       -----
//  |_____|     |_____|     |_____|           clock/3

     assign RCLK2 = ((clk_div_reg[0]) == 0) ? RCLK:!RCLK;   //use inv. RCLK for
                                                            //odd clk_div
     assign SCLK2 = ((CLK2) == (CLK1)) ? 0:1;               //XOR CLK1 and CLK2
     assign SCLK  = (clk_div_reg[3:0] == 0) ? SCLKin:SCLK2; //use ext. RCLK for
                                                            //clk_div=0

//     always @ (negedge notEN)                           //latch-in of clk_div
//       clk_div_reg = clk_div;
// due to merging of serClk and RClk clk_div_reg loading synchronous again

//-----------------------------------------------------------------------------

//counter, which divides RCLK by 2*clk_div

     always @ (posedge RCLK)
       begin
         sync = {sync[1:0],notReset};
         if (notEN == 0)
           clk_div_reg = clk_div;
         if ((sync[2] == 1) && (sync[0] == 0))
           begin
             CLK1 = 0;
             counter1 = 0;
           end
         else
           begin
             if (counter1 == 0)
               begin
                 counter1 = clk_div_reg[3:0]-1;
                 CLK1 = CLK1 + 1;
               end
```

```
            else
              counter1 = counter1 - 1;
          end
      end



//-------------------------------------------------------------------------
//counter, which divides RCLK by 2*clk_div.
//This one starts only if start_counter
//has expired. This ensures a 50% duty cycle

    always @ (posedge RCLK2)
      begin
        if ((sync[2] == 1) && (sync[0] == 0))
          begin
            CLK2 = 0;
            counter2 = 0;
          end
        else
          begin
            if (start_counter == 0)
              begin
                if (counter2 == 0)
                  begin
                    counter2 = clk_div_reg[3:0]-1;
                    CLK2 = CLK2 + 1;
                  end
                else
                  counter2 = counter2 - 1;
              end
            else;
          end
      end


//-------------------------------------------------------------------------
//delay timer for counter2. Counts  0.5*clk_div counts on
//the "wrong" edge of RCLK

    always @ (negedge RCLK2)
      if ((sync[2] == 1) && (sync[0] == 0))
          start_counter = {1'b0,clk_div_reg[3:1]}+clk_div_reg[0];
        else
          begin
            if (start_counter > 0)
              start_counter = start_counter - 1;
            else;
          end


endmodule
```

"**sufixTRG.v**" synchronises the `trigIn` signal with *SClk*.

```
// Trigger-synchronizer
// "SUFIX"-the control circuit of the HELIX chip
// Written by Ulrich Trunk (c) 1996
```

```
module sufixTRG(trigIn,SCLK,trigOut);

input  trigIn,
       SCLK;
output trigOut;

wire     trigIn,
         SCLK;
reg      trigOut;

always @ (posedge SCLK)
  trigOut = trigIn;

endmodule
```

"**sufixToken.v**" implements the fail-safe token schema and generates an initial readout token.

```
// Token-Handler Selects various token inputs and generates
//delayed/initial token for the first chip
// "SUFIX"-the control circuit of the HELIX chip
// Written by Ulrich Trunk (c) 1996
// Changed 06.10.97 by U.T.: FailSafe Token schema
// Changed 10.10.97 by U.T.: Removed "FirstTokenIn", added a few comments

module sufixToken_FST(
       RTI,        //from the last chip in the chain (inPad)
       FRTI,       //Token from the pre-last chip in the chain (inPad)
       HTI,        //Token from the preceeding HELIX (inPad)
       FHTI,       //Token from the pre-preceeding HELIX (inPad)
       HTO_last,   //Token input from HELIXPart for last ReturnToken generation
       RTO,        //Return Token to free a pipeline column (=> PipeCtrl)
       HelixToken, //propagating token (initiates readout of 2nd and following
                   //chips in chain, latched in 1st chip,=>MuxCtrl)
       disable_HTO,//stop HelixTokenOut to next chip
       TokenStatus,//Status of Token handling (norm/failsafe), FirstInChain(MSB)
                   //connected to the upper 4 bits of ClkDiv reg (<=sufixSclk)
       RCLK,       //clock for the delay
       data,       //inputs of delay register
       notEN,      //delay registe notEnable
       notReset,   //HELIX's notReset and notTReset are
       notTReset); //required to generate an initial token upon startup

input       RTI,FRTI,HTI,FHTI,HTO_last,
            RCLK,
            notEN,
            notReset,
            notTReset;
input [7:0] data;
input [3:0] TokenStatus;
output      RTO,HelixToken,disable_HTO ;

wire        RTI,FRTI,HTI,FHTI,HTO_last,disable_HTO,
            firstToken,HT,
            RTO,RT,
            RCLK,
            notEN,
```

```
            notReset,
            notTReset;
wire [3:0]  TokenStatus;
reg [7:0]   delay;
reg [8:0]   counter;

// Switches to programm FS-operation:
// TokenStatus[3]: 1= First chip in the chain, 0= all other chips
// TokenStatus[1]: 0= ReturnToken from last chip,
//                 1= ReturnToken from pre-last chip
// TokenStatus[0]: 0= normal operation, 1= preceeding chip disabled
// Switches are mapped to ClkDiv[8:4] register!!!!!

// Generate a first token upon reset, which is only sent to the first chip
assign firstToken = (((notReset ==1) && (notTReset == 0))||(counter == 1)) ?
                    1:0;

assign HT = (TokenStatus[0] == 0) ? HTI:FHTI;              //bypass HelixToken
assign RT = (TokenStatus[1] == 0) ? RTI:FRTI;              //bypass ReturnToken
assign disable_HTO = TokenStatus[1];          //stop HelixTokenOut to next chip
assign RTO = (TokenStatus[2] == 1) ? HTO_last:RT ;         //last chip in chain
assign HelixToken = (TokenStatus[3] == 1) ? firstToken:HT; //first in chain


// Delay Token for the first chip by (TokenDelay)# of Rclk cycles
//(i.e. pause between readout bursts)
always @(negedge notEN)
  delay = data;

always @(posedge RCLK)
    begin
    if (notReset == 0)
      counter = 0;
     else
      if (RTO == 1)
          counter = delay+1;
      else
        if (counter > 0)
          counter = counter - 1;
        else
          counter = 0;
     end

endmodule
```