Originalveröff. in: Proceedings of the Fifth Workshop on Electronics for LHC experiments

DESIGN OF A PROTOTYPE FRONTEND AND BIAS GENERATOR FOR A NEW READOUT CHIP FOR LHCb

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Abstract

This paper presents the design and simulation results of components for a new LHCb readout chip for the silicon vertex detector, the inner tracking system, the pile-up veto trigger and the RICH. It is planned to use the same readout chip for these subdetectors. However, different versions of the analog input stages might be developed depending on the choice of the detector type.

In section 1, the specification of the new readout chip named Beetle with respect to the different subdetector systems is described. Sections 2 and 3 describe the design and the simulation results of two test chips. The first chip contains different types of frontends for the vertex detector and the second chip bias generators. Section 4 gives a brief overview on the future plans for the development towards a readout chip for LHCb.

1 Specification of the readout chip

The Beetle readout chip will contain 128 channels. Each channel consists of a charge sensitive preamplifier, a pulse shaper, an analog pipeline of a programmable maximum latency of 160 stages with an integrated derandomizing buffer of 16 stages and a serial readout for up to 40 MHz readout speed. In case of using the chip in the binary pipeline mode, the discriminated output of the shaper is stored into the pipeline and a fast binary multiplexer is used to read out the chip at a speed of 80 MHz. Readout multiplexing can be done in several modes: for fastest readout speed of analog data, four ports can be used at 40 MHz, each multiplexing 32 channels. Two ports multiplexing 64 channels running at 80 MHz can be used for readout of binary data. For applications which do not demand a fast readout, a single port multiplexing 128 channels can be used and several chips

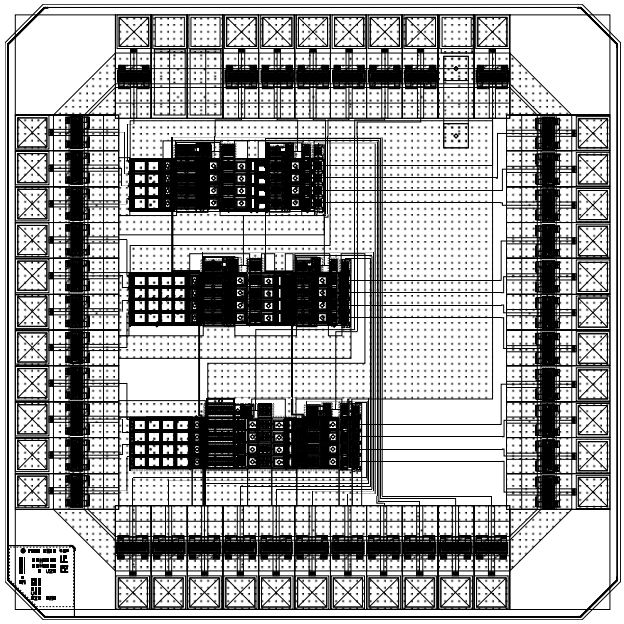

Figure 1: Layout of the BeetleFE-1.0

can be connected to build up a readout daisy chain, sharing a single readout line. In addition to the pipelined data path the combined signals of four neighbouring discriminators, that are located behind the shaper, are routed off the chip. All digital control and data signals are realized as low voltage differential signals (LVDS). The chip is programmable via the standard I^2C interface and by another serial interface, yet to be defined [1].

The requirement on the radiation tolerance is driven by the application of the chip in the silicon vertex detector. A radiation level of 2 MRad per year is expected for the frontend chips. With an expected usage time of 5 years, this leads to a total accumulated dose of 10 MRad [4]. In order

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	silicon vertex detector	pile-up veto trigger	RICH	inner tracker
sampling frequency	40 MHz			
L0 trigger rate	1 MHz			
readout speed	max. 900 ns per event			
max. latency	$160 \cdot 25$ ns			
multi event buffers	16			
consecutive L0 triggers	yes			
slow control interface	I^2C			
number of channels	220,000		400,000	220,000
overall readout pitch	50 µm	50 µm	60 µm	
max. power consumption	4 mW per channel	4 mW per channel	2 mW per channnel	
irradiation dose per year	2 MRad	2 MRad	few 100 kRad	1 MRad
detector capacitance	10 pF		4 pF / few pF	
required S/N	>14		>8 / >20	>10
dynamic range [electrons]	$\pm$110,000		45,000 / $6 \cdot 10^6$	

Table 1: Summary of the requirements on the LHCb readout chip. Empty or multiple entries depend on the detector type decision

to withstand this demanding dose, several measures have been taken. A standard 0.25 µm CMOS process has been chosen, since recent experience of the RD 49 collaboration shows only minimum threshold voltage shift under irradiation. Edgeless layout for NMOS transistors has been used to prevent an increase in leakage current under irradiation. Guardrings have been used in a systematic way to minimize the rate of single event effects [2]. The concept of using forced bias currents in the analog stages instead of fixing node voltages has been applied, as it has been proven to be successful for example in [3].

A summary of the requirements on the LHCb readout chip is shown in table 1.

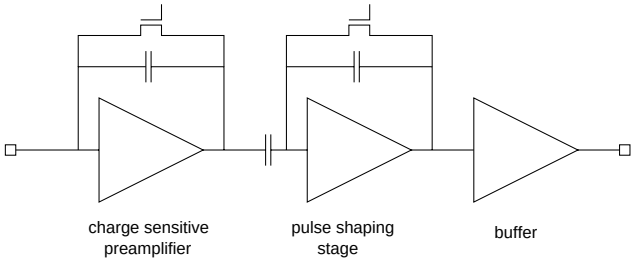

Figure 2: Principle schematic of the input stage with a charge sensitive preamplifier followed by an active CR-RC pulse shaping stage and a buffer

2 Design and simulation of the BeetleFE-1.0 frontend chip

The BeetleFE-1.0 chip contains three different sets of a prototype input stage, one of which is intended to be used in the Beetle readout chip for the silicon vertex detector and the pile-up veto trigger. Each of the three sets consists of four identical channels to allow studies of channel to channel crosstalk. Two of the sets use a PMOS device as input transistor, whereas the third set uses an NMOS transistor. All numerical values given below refer to the third set, since it is expected to most closely match the requirements. Figure 1 shows a layout view of the chip. The size is 2×2 mm^2. The input pads are located on the left side, the output pads on the right side. The remaining pads are used for probing purposes and for the power supply.

Each of the amplifier channels consists of a charge sensitive preamplifier, an active CR-RC shaper and a subsequent buffer. A schematic drawing of this configuration can be seen in Fig. 2. The transistors in the feedback of both stages are used as adjustable resistors. The buffer is realized with a standard source follower. The opamp cell of the preamplifier and the shaper use the well established folded cascode configuration. To a good approximation the noise of this amplifier circuit is determined by the input transistor of the preamplifier and its biasing. The power consumption is restricted by the silicon vertex detector specification to 4 mW per channel, for which the preamplifier has been optimized. The thermal noise as a function of the input capacitance C_{input} can be calculated by

$$\frac{ENC_{thermal}}{C_{input}} = e\sqrt{\frac{(1+\eta)\cdot kT}{3\cdot T_{peak}\cdot g_m}}$$

where T_{peak} is the peaking time, g_m the transconductance of the input transistor and η the bulk-source transconductance of the input transistor. The $1/f$ noise can be neglected in this application, since the band pass characteristic of the shaping stage attenuates the low frequencies. In principle, the designer can choose the shaping time and the g_m, which is defined by the transistor geometry and the bias current. The pulse shape is constrained by the LHC bunch crossing

frequency, since any shaped signal needs to return to zero 25 ns after its maximum to avoid a possible pile-up. The geometry can be optimized for minimum noise, since g_m rises proportional to W/L whereas the gate capacitance (which contributes to the load capacitance of the amplifying stage) rises with $W \cdot L$. The value of η rises with decreasing L. However, for this first submission, a set of values has been

power consumption	slope of the noise function
0.88 mW	46.5 e^-/pF
1.13 mW	41.4 e^-/pF
1.38 mW	37.5 e^-/pF
1.63 mW	35.5 e^-/pF
1.88 mW	33.6 e^-/pF

Table 2: Slope of the calculated noise function for different values of power consumption

chosen that distribute around the optimum set of values to make a comparison between the calculated noise values and the measurements. Table 2 lists calculated values of the slope of the noise function for different bias settings as a function of the total power consumption for one frontend channel of the third set. The offset of the noise function is not calculated, since the final layout of the input protection diodes and the input pads, that contribute a considerable amount of the input capacitance, is not yet defined.

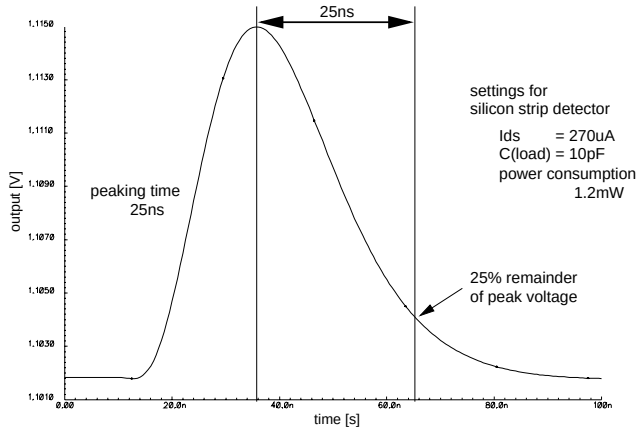

Figure 3: Transient response on a delta-shaped signal of 11,000 electrons

The pulse shape of the frontend depends on the bias settings of the preamplifier as well as on the time constants of the shaping stage. Figure 3 shows an example of a simulated pulse shape from a signal of 11,000 electrons (which corresponds to a minimum ionizing particle in the silicon strip detector) with optimized settings for the silicon strip detector. The falling edge of the shaped pulse leads to an acceptable remainder of 25% of the peak voltage at 25 ns after the peaking time.

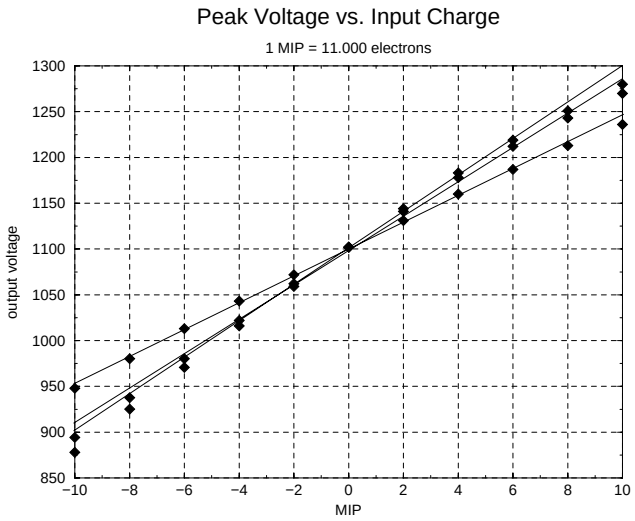

Figure 4: Peak voltage at the output of the frontend as a function of the input charge (1 MIP = 11,000 electrons) for a load capacitance of 0 pF (upper curve), 4 pF and 10 pF (lower curve)

The frontend has been designed to have a dynamic range between –10 MIP and +10 MIP, as demanded by the specifications of the subdetectors. A deviation from linearity of 5% is accepted. Figure 4 shows the simulated peak voltage as a function of the input charge for three different values of the load capacitance. The gain of the complete frontend is simulated to be 20.4 mV/MIP, 19.0 mV/MIP and 14.5 mV/MIP for a load capacitance of 0 pF, 4 pF and 10 pF, respectively.

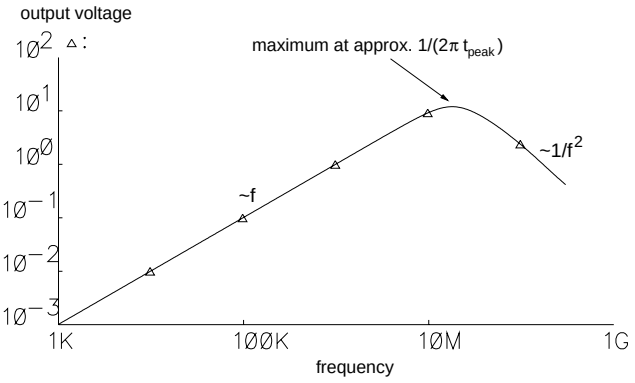

Figure 5: Frequency response of the pulse shaping stage

The frequency response of the pulse shaping stage is plotted in Fig. 5. As expected for a semigaussian pulse shape, the frequency sweep shows a maximum at f_{max}=$1/(2\pi t_{peak})$. This closely resembles the value for t_{peak}=20 ns obtained from the transient simulation.

	type of current source	maximum load (ΔI = 1%)	small signal resistance	power consumption	size [μm^2]
(1)	opamp feedback	1.06 V	4 MΩ	2.35 mW	164 x 61
(2)	opamp feedback and regular cascode output	1.94 V	14 MΩ	2.5 mW	189 x 61
(3)	regular cascode	1.93 V	17 MΩ	599 μW	84 x 23

Table 3: Specifications for the three different current source options

3 Design and simulation of the BeetleBG-1.0 bias generator chip

The bias generator chip BeetleBG-1.0 contains 3 different types of current sources, a voltage digital-to-analog converter (DAC), a current DAC and test structures that will be used to study the change of transistor parameters under irradiation. Figure 6 shows a layout view of the chip. The size of the chip is 2×2 mm^2 and the components are laid out in such a way that the chip can be directly bonded to the BeetleFE chip to allow for frontend biasing and coupled testing.

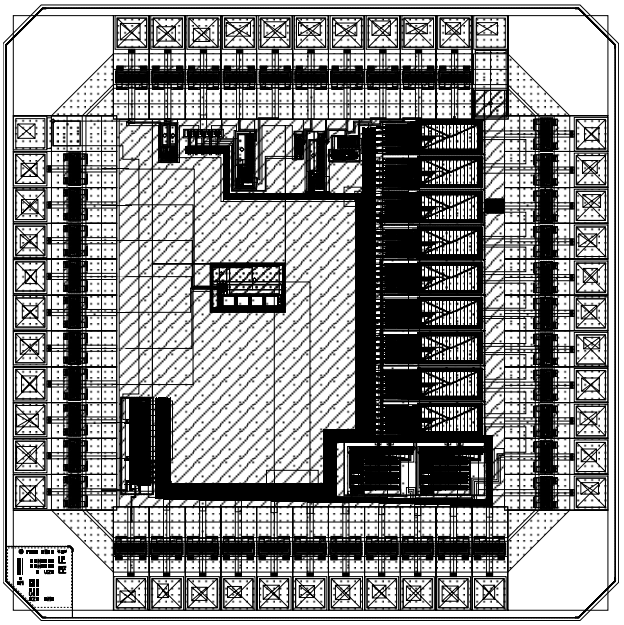

Figure 6: Layout of the BeetleBG-1.0

The three different current sources vary with complexity and performance. Table 3 lists the three different types with their simulated values. The current source (1) uses an opamp feedback. The second also uses an opamp feedback system but improves the small signal resistance by using a regular cascode at the output. The third choice uses only a regular cascode and relies on the fact that the chosen process has minimum threshold voltage shift and will not need compensation for radiation damage. The nominal current of the opamp feedback with a regular cascode output is 300 μA, whereas the others are 100 μA.

The voltage DAC uses an R-2R-ladder configuration with

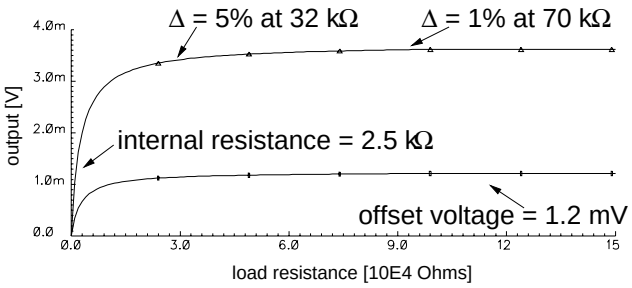

Figure 7: Output voltage of the voltage DAC (LSB is set in the upper curve) and offset voltage versus the load resistance

a resolution of 10 bit and an output range from rail to rail, that is from 0 V to 2.5 V. The 3.0 kΩ resistors are of the n^+ diffusion type. The power consumption of the DAC is 690 μW. Figure 7 shows a plot of the output voltage for the least significant bit set as a function of the load resistance. A change in the output voltage of 1% is simulated at a load resistance of 70 kΩ. The lower curve in this plot shows the offset voltage, which has an acceptable value of 1.2 mV. The differential non-linearity caused by the resistance of the switches simulates to be 8 mV. The resolution of the DAC will be lowered for the final version, the high resolution of this prototype version has been chosen to learn about mismatch of devices in this technology.

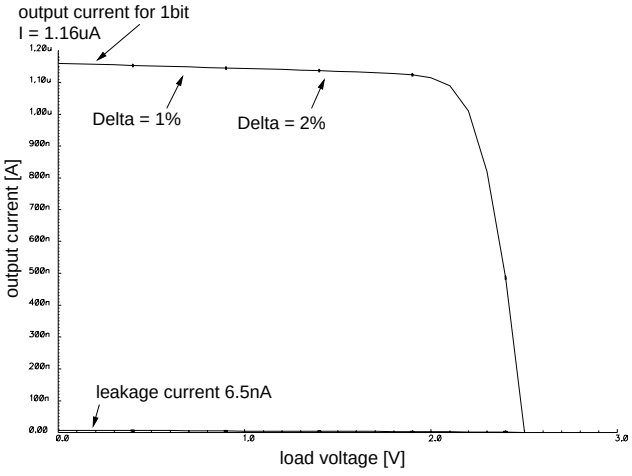

Figure 8: Output current of the current DAC (LSB is set) versus load voltage (upper curve) and simulated leakage current (lower curve)

The current DAC consists of 1024 conventional PMOS transistors with a W/L ratio of 0.6µm/3µm to optimize the current source to the LSB. Each bit switches on 2^n parallel transistors, acting as a current source. Figure 8 shows the simulated output current for the LSB set as a function of the load voltage. A change of 2% occurs at a load of 1.5 V. The lower curve in the plot shows the simulated leakage current of 6.5 nA, which can be neglected in this application. As for the voltage DAC, it is foreseen to go to a smaller resolution in the final version of the current DAC. The study of leakage current and the transistor mismatch will be performed on this prototype version.

The test structures contain minimum size conventional PMOS and NMOS transistors, PMOS and NMOS transistor with an edgeless layout and conventional transistors with the same effective geometric values as the edgeless transistors. In addition, the sizeable NMOS input transistor, used in the third set on the BeetleFE-1.0, has been added. The behaviour on irradiation will be studied on these devices and compared to results, obtained from other processes.

4 Future milestones

It is intended to submit further components by the end of 1999, which include

- an iteration of the frontend,
- a calibration pulse generator,
- a comparator stage,
- a pipeline capacitor array including a pipeline control logic
- a multiplexer with an output buffer.

We plan to submit the first version of a complete readout chip in October 2000. A final version that can be used in the LHCb experiment, should be submitted by the end of 2001. Status reports will be available in [1].

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